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A Background Correlation-Based Timing Skew Estimation Method for Time-Interleaved ADCs

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ABSTRACT This paper presents a correlation-based all-digital background estimation method for timing skew mismatches in time-interleaved analog-to-digital converters (TI-ADCs). Exploiting the first-order approximation of an autocorrelation function of the digital output of each Sub-ADC, the timing skew mismatch between adjacent channels is identified, which can be used for analog or digital correction methods. The proposed estimation method has a low computation complexity and a simple implementation structure, because it basically only requires multiply-accumulate and average operations. In addition, the proposed method is not limited in the number of channels, does not need any pilot injection, is basically suitable for any bandlimited analog input signal, possess a large estimation range of mismatches and is immune against gain and offset mismatches to a certain extent. Simulation results of a four-channel TI-ADC behavioral model and measurement results from a commercial 12-bit 3.6-GS/s TI-ADC show the effectiveness and superiority of the proposed estimation method.

INDEX TERMS Time-interleaved, ADC, timing skew, background calibration, correlation-based, estimation.

I. INTRODUCTION

Since the performance of a monolithic ADC in any IC process is limited by factors such as the regeneration time of the comparator and settling time of the amplifier [1], time-interleaved analog-to-digital converters (TI-ADCs) have been proposed and widely used to meet the increasing operating rate of modern wideband communication systems (e.g., broadband satellites, radars and optical communication systems) [2]–[4]. As shown in Fig. 1, a TI-ADC uses multiple identical sub-ADCs for parallel sampling to achieve higher sampling rates. Every sub-ADC, driven by equally phase-shifted clocks, has a sampling rate of f_s/M, where f_s and M are the overall sampling rate and the interleaving factor of TI-ADCs, respectively. Ideally, the parameters among the channels should be identical. However, due to some inherent defects (leading to offset, gain and timing-skew mismatches) in the system, the performance of TI-ADC is deteriorated seriously [5]. The solutions for correcting offset and gain mismatches are fairly straightforward, but the timing-skew still presents a challenge [6], [7]. It is more difficult to estimate as it depends on the input frequency. Although the timing-skew can be alleviated by a careful layout design, timing-skew mismatch cause a strong effect in high-frequency applications. For instance, for a B-bit TI-ADC with a sinusoidal input, the tolerable standard deviation of timing skew mismatch Δ is about [8]

$$\Delta = \sqrt{\frac{M}{M-1} \cdot \frac{2}{3 \cdot 2^{2B} \cdot (2\pi f_{in})^2}} \tag{1}$$

where f_{in} is the frequency of input sinusoidal and M is the interleaving factor. For example, for a 12-bit four-channel TIADC, when the input sinusoidal signal frequency is 1GHz, the skew mismatch it can tolerate is only about tens of femtoseconds. However, in the context of high-speed and high-resolution design, even with a reasonable layout and a careful manufacturing process, it is difficult to meet this requirement. Therefore, in highspeed and high-resolution application scenarios, the timing skew mismatch Δ between sub-ADCs must be reduced by some means until it meets (1) at least. There is straightforward solution that adopts the architecture of two-rank sample and hold (S/H) circuit to mitigate timing skew mismatch. The first-rank S/H circuit, however, restricts the whole operating rate of the TI-ADC system [9].

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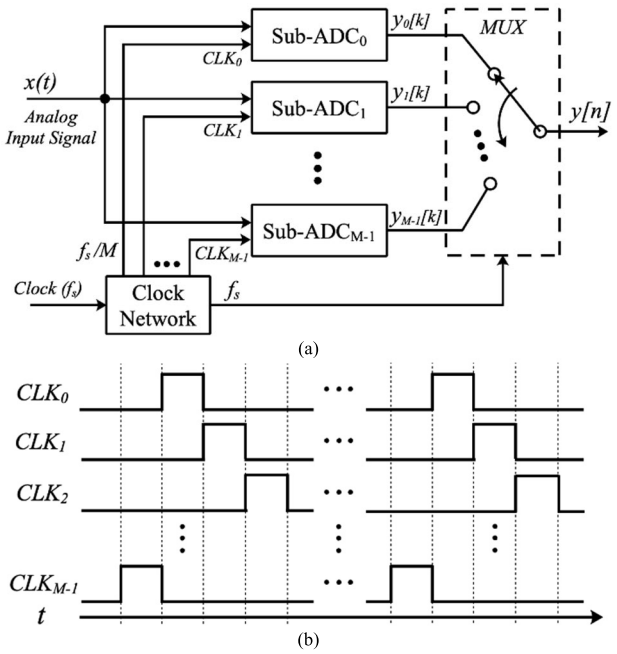

FIGURE 1. Block diagram of the TI-ADC system.

Therefore, post-calibration is essential in the design of high-performance TI-ADCs. The process for timing skew mismatch calibration can be divided into two steps: estimation and correction. In relative terms, the estimation is more important since it is a prerequisite for the correction. For the correction of timing skew mismatches many useful solutions have already been found, such as setting variable delay lines (VDLs) or voltage adjustment circuits in the analog domain [10]–[18], or digital correction filters in the digital domain [22]–[24] [30], [31].

To extract timing skew mismatches, various estimation techniques have been reported. In [10]–[12], several foreground timing-skew calibration methods are presented. The timing skew mismatches can be extracted by injecting a test signal to the TI-ADC, but these techniques are unsuitable for real-time system since the ADC system cannot resume normal operation until the calibration is complete. To cope with the shortcoming of the foreground estimation techniques, the timing skew mismatches estimation methods for operating in the background, i.e., without interrupting the normal conversion, have been reported [13]–[36]. There are several background estimation techniques presented in [13]–[16], that use an auxiliary ADC as a timing reference. Two auxiliary ADCs are used in [13], for extracting derivative information and as ideal reference channel, respectively. In [14], the correlation between the output signal of sub-ADCs and the reference ADC can be used to estimate the timing skew mismatch. In [15], a sign-equality-based timing skew estimation scheme is proposed with a dedicated ADC as a virtual-timing-reference. Despite the effectiveness of this type of approach, additional auxiliary ADCs can increase hardware overhead and power consumption significantly. In view of the drawback, a timing skew estimation method without separate timing reference ADC is proposed in [16]. According to the structural characteristic of the Flash TISAR ADC, the Flash ADC in its structure is used as a reference to estimate the timing skew error. However, this method only works for specific architectures and the first-level Flash ADC limits the sampling rate of the overall TI-ADC. In order to avoid the use of auxiliary ADCs, some simplified analog-assisted-based timing skew estimation techniques are introduced in [19]–[21]. In [19], a phase detection-based timing skew estimation scheme is proposed which uses a comparator to determine the phase relationship between the sampling clock of sub-ADCs and the master clock to estimate the timing skew. In [20] and [21], zero-crossing detection-based estimation techniques are reported to address the timing skew errors. By utilizing a comparator-based zero-crossing window detection (WD) circuit and combining the variance and mean absolute deviation (MAD) of sub-ADC's outputs in the digital domain, the timing skew mismatch is estimated. In fact, for the methods based on a comparator in the analog domain, its own non-ideal factors will reduce the accuracy of the timing skew mismatch estimation. Additionally, the estimation method with analog-assisted circuits is difficult to track process, voltage and temperature (PVT) variations continuously. Therefore, dedicated circuits need to be designed to resist the negative impact of caused by PVT. In addition, due to the slew rate of the comparator, this method is not suitable for ultra-high-rate TI-ADCs.

In the end, all-digital background timing skew estimation techniques seems to be the most ideal approach [26]–[35]. It can compatible with various given processes and adapt to changes in temperature and voltage, avoiding many potential defects of the analog-assisted estimation method. Correlation-based error estimation algorithms are one of the most effective methods to solve the timing skew mismatch problem [26]–[30]. In [26], a cross-correlation based method is proposed to detect the timing skew mismatch, but this method is only suitable for the case of two channels. In [27], the authors utilized the similarity between frequency response mismatch (FRM) and in-phase/quadrature-phase (IQ) imbalance to calibrate the mismatch errors in a four-channel TI-ADC. An estimation design for FRM adapting a multitap version of a circularity-based algorithm for IQ signal processing is proposed. However, for compliance with the IQ method working on the complex baseband signal, have to transform the real signal from the TIADC output into an IQ type one, using Hilbert filtering and fs/2-modulation. In addition, this method is only applicable to four-channel TIADC. In view of the shortcomings of the limited number of applicable channels, the cross-correlation-based estimation techniques have been further developed for an arbitrary number of channels in [28]– [32]. In [28], it obtains the transfer function of each channel by injecting a series of sinusoidal signals with a priori information, and uses WLS theory to design FIR correction filters to eliminate various mismatch errors, thereby greatly improving the SFDR of TIADC. But this method needs to work under certain prior information,

and the filter bank needs to be designed. In [29], it regards the TI-ADC output with channel mismatch as a linear periodic time-varying (LPTV) model, and obtains two sets of LPTV systems based on autocorrelation method to estimate the parameters that cause the frequency response mismatch in the model. However, its normal work needs to be established under certain prerequisites, that is, the mismatch spurious and effective signal must meet a specific frequency relationship. For [30]–[32], all of those techniques involve complex matrix calculations, which means many computational expensive operations are required. In addition, a derivative filter is needed to obtain the first-order derivative of the digital outputs, which further increases the hardware overhead. In [33], timing-skew is estimated by a technique directly operates on the probability density function (PDF). The timing skew error can be extracted according to the difference between the probability distribution of adjacent channels. Although it is innovative and effective, the implementation structure is relatively complicated and has a certain degree of sensitivity on the probability distribution of the input signal. There is also a pseudo-aliasing-generation-based algorithm, by means of generated basis aliasing functions from the output of TI-ADC intentionally, the timing skew mismatch can be adaptively cancelled [34], [35]. However, in the work of [34], the Hadamard transform is employed to generate the pseudo aliasing signal, which limits the algorithm to be valid only for TI-ADC systems with a specific number of channels (e.g., 2, 4, 8,...). This limitation is addressed in [35] and achieved significant effects. But it is invalid when the frequency of input single-tone at $0.25f_s$ and requires additional design of Hilbert filters. Moreover, the implementation architecture of such methods is complex and occupies hardware resources severely. In summary, compared to the developed timing skew mismatch correction methods the estimation methods still have shortcoming to resolve.

In order to avoid the above limitations in the prior techniques, this paper proposed an all-digital correlation-based background timing skew estimation technique for TI-ADCs. Compared with previous methods, its advantages are as follows:

- Suitable for TI-ADCs with any number of channels.
- No need to inject any auxiliary pilot signals.
- No need to use any analog-assisted circuits or reference ADC channels.
- No need to use any digital filters for the estimation process.
- Wide range estimation of timing skew.
- Simple structure and low hardware resources.
- For convergence only a few samples are needed.

The remainder of this paper is organized as follows. In Section II, the TI-ADC model with timing-skew mismatch is described to facilitate understanding the proposed method, which introduced in detail in Section III. Simulation and experimental results are given in Section IV. The impact of offset and gain mismatches on the estimation is investigated in Section V, followed by the conclusion in Section VI.

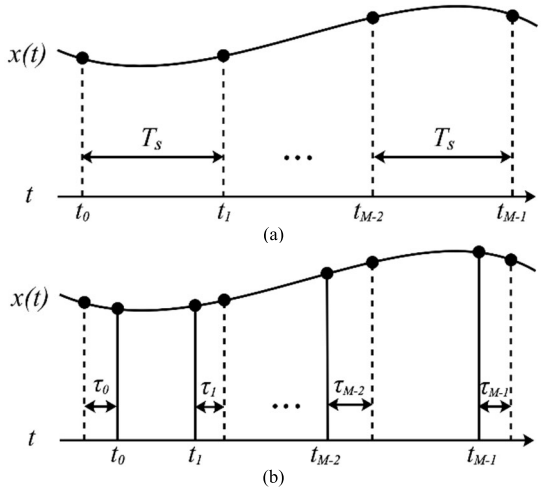

FIGURE 2. Schematic diagram of time signal with (a) ideal sampling and (b) timing skewed sampling.

II. MISMATCH MODEL OF TI-ADCs

In order to facilitate the understanding of the proposed calibration algorithm in this paper, the mismatch model of TI-ADC needs to be analyzed first. The schematic diagram of TIADC sampling ideally for continuous time signal x(t) is shown in Fig. 2 (a). The adjacent sampling instants are kept at the same interval, i.e., the sampling period Ts. Fig. 2 (b) demonstrates the sampling diagram of TIADC when there are timing skew mismatches, where τ_i is defined as the timing skew of the corresponding Sub-ADC. Therefore, timing skew mismatch indicates that there is a difference in timing skew between Sub-ADCs. In this paper, we define the timing skew mismatch between adjacent Sub-ADCs as follows

$$\Delta\tau_i = \tau_{mod(i+M-1,M)} - \tau_i \tag{2}$$

where $i = 0, 1, 2, \ldots, M-1$.

Fig. 3 shows a mismatch model of an M-channel TIADC with a sampling rate of $f_s = 1/T_s$. For an ideal TI-ADC, the offsets (os_i) and the gains (g_i) of each sub-ADC are identical, i.e., $os_i = 0$ and $g_i = 1$, where $i = 0, 1, 2, \ldots, M-1$. Moreover, as shown in Fig. 2(a), the sampling instants t_i of each sub-ADC is

$$t_i = (kM + i) \cdot T_s \tag{3}$$

Therefore, the digital output of i-th sub-ADC can be expressed as

$$y_i[k] = x\left((kM + i) \cdot T_s\right) \tag{4}$$

The output of the TI-ADC is obtained by multiplexing the output of each sub-ADC, such that

$$y[n] = y_{mod(n,M)}\left[\frac{n}{M}\right] \tag{5}$$

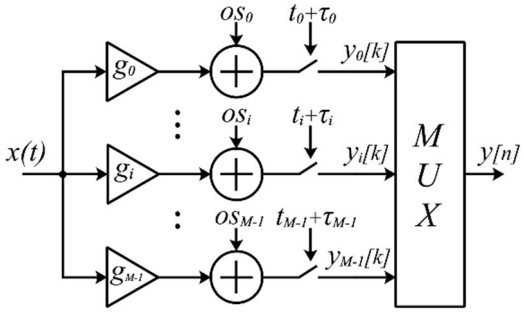

FIGURE 3. Mismatch model of TI-ADC systems.

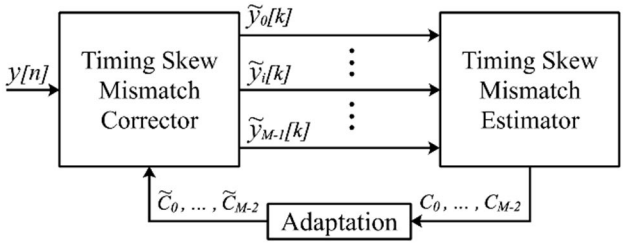

FIGURE 4. System architecture of proposed calibration technique.

where $\lceil\cdot\rceil$ indicate ceiling operation. Unfortunately, each sub-ADC is affected by different offset os_i, gain g_i, and timing-skew τ_i, as shown in Fig. 3. Hence, $y_i[k]$ in equation (4) can be rewritten as

$$y_i[k] = g_i \cdot x\left((kM+i)\cdot T_s + \tau_i\right) + os_i \tag{6}$$

III. PROPOSED CALIBRATION METHOD

A. SYSTEM-LEVEL OVERVIEW

The calibration proposed in this paper belongs to an all-digital background technique. The system-level architecture of the proposed calibration method is depicted in Fig. 4. It is assumed that there are no offset and gain mismatches. The impact of offset and gain mismatches on the estimation is investigated in the Section V. The entire calibration framework is mainly composed of a corrector and an estimator, which both work in the digital domain. The digital output of the TI-ADC with timing skew mismatch $y[n]$ is corrected by the corrector to obtain a calibrated signal with reduced timing skew mismatches $\tilde{y}_i[k]$. The correction parameters $\tilde{C}_i$ required by the corrector are provided by the estimator. The adaptation algorithm adaptively adjusts the estimated timing skew mismatch information so that it gradually converges to the difference of timing skew between adjacent channels, and finally eliminates the mismatches by the corrector to make the timing skew value of each channel identical. The adaptive update equation for the timing skew mismatch calibration can be expressed as

$$\tilde{C}_i[k+1] = \tilde{C}_i[k] - \mu \cdot C_i[k] \tag{7}$$

where $k = 0, 1, 2, 3, \ldots$, and μ is the iteration step factor which usually between 0 and 1.

Once the correction parameters $\tilde{C}_i$ is known, a corrector is needed to eliminate errors caused by timing skew mismatch. Since this paper focuses on the estimation method, for the corrector, we adopt a differentiator-multiplier-cascade (DMC) based correction method [24]. However, this estimation method can be adapted to many correction or compensation methods. There are several ways to correct the sampled input signal $y[n]$. In the analog domain, usually by setting variable clock delay lines (VDLs) [10]– [17]. In the digital domain, digital filter banks are usually used [22]– [25] [30], [31].

B. DIGITAL ESTIMATION METHOD

1) DERIVATION

For the sake of simplicity, we neglect offset and gain mismatches. Hence, the system model in (6) reduces to

$$y_i[k] = x\left((kM+i)\cdot T_s + \tau_i\right) \tag{8}$$

First, we consider the products of adjacent channels and calculate their expected value

$$\begin{aligned} A_i &= E\left(y_{mod(i+M-1,M)}[k]\cdot y_i[k]\right) \\ &= E\left(x\left((kM+mod(i+M-1,M))\cdot T_s\right.\right. \\ &\quad \left.\left.+\tau_{mod(i+M-1,M)}\right)\cdot x\left((kM+i)\cdot T_s+\tau_i\right)\right) \\ &= R_x\left(T_s+\tau_{mod(i+M-1,M)}-\tau_i\right) \\ &= R_x\left(T_s+\Delta\tau_i\right) \end{aligned} \tag{9}$$

where $i = 0, 1, 2, 3, \ldots, M-1$ and $E(\cdot)$ represents the expectation value. Then we end up with the autocorrelation function R_x. Second, we approximate the autocorrelation function at T_s by the first order derivative, i.e.,

$$\begin{aligned} A_i &\approx R_x\left(T_s\right) + \left(\tau_{mod(i+M-1,M)}-\tau_i\right)\cdot R_x\left(T_s\right) \\ &= R_x\left(T_s\right) + \Delta\tau_i \cdot R_x'\left(T_s\right) \end{aligned} \tag{10}$$

The second term of equation (10) represent the timing skew mismatch information between adjacent channels. By adding up all M expected values A_i, $R_x(T_s)$ can be calculated by, (11)

$$R_x\left(T_s\right) = \frac{1}{M}\sum_{i=0}^{M-1} A_i \tag{11}$$

since the sum of all is zero by the definition (2).

Finally, the correction parameters of timing skew mismatch can be obtained as

$$\begin{aligned} C_i &= A_{i+1} - R_x\left(T_s\right) \\ &= A_{i+1} - \frac{1}{M}\sum_{i=0}^{M-1} A_i \\ &= \left(\tau_i - \tau_{i+1}\right)\cdot R_x'\left(T_s\right) \\ &= \Delta\tau_i \cdot R_x'\left(T_s\right) \end{aligned} \tag{12}$$

where $i = 0, 1, 2, 3, \ldots, M-2$ and $R_x'\left(T_s\right) < 0$ because the autocorrelation function is strictly decreasing for any $(T_s) > 0$. Consequently, the timing skew mismatches between adjacent channels can be detected by observing the sign of (14).

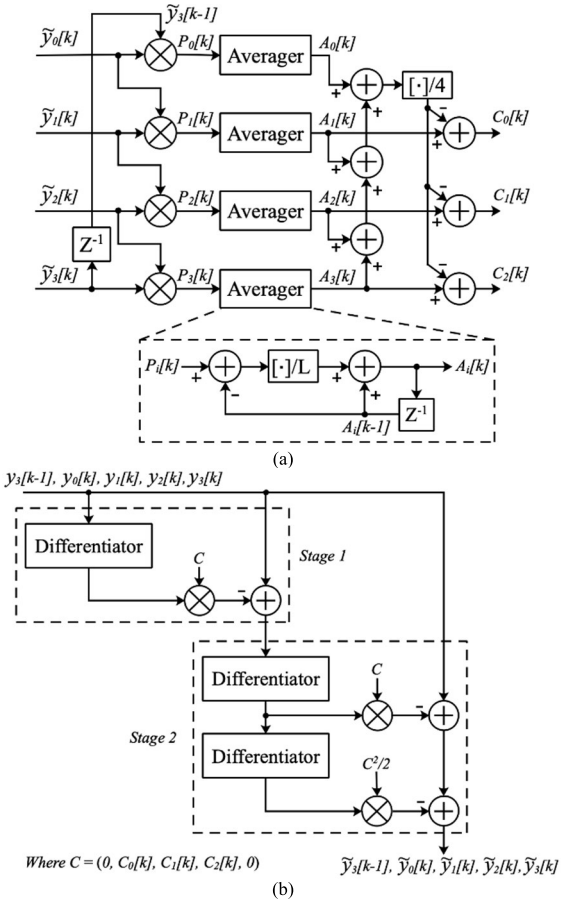

FIGURE 5. Block diagram of (a) The proposed timing skew mismatch estimator and (b) The DMC-based corrector.

If $C_i < 0$, then $\tau_{i+1} < \tau_i$, and if $C_i > 0$, then $\tau_{i+1} > \tau_i$. Therefore, we can use (14) to obtain the sign of the timing skew mismatch for each channel and use this information to adaptively correct all mismatches.

Note that we use only $M-1$ observations ($C_0, C_1, \ldots, C_{M-2}$) here instead of M. The proposed method focuses on the timing skew mismatches between adjacent channels, and accordingly $M-1$ observations reflect the entire mismatch information between all M channels. For example, for a 4-channel TI-ADC, only three observations need to be observed i.e.,

$$C_0 = (\tau_0 - \tau_1) \cdot R'_x(T_s) \tag{13}$$
$$C_1 = (\tau_1 - \tau_2) \cdot R'_x(T_s) \tag{14}$$
$$C_2 = (\tau_2 - \tau_3) \cdot R'_x(T_s) \tag{15}$$

2) IMPLEMENTATION

First, we assume that the output sequence of TIADC is a wide-sense weakly stationary process [37]. The module-level implementation of the proposed method applied to a four-channel TI-ADC is shown in Fig. 5(a). It can be designed through several multipliers, adders and averagers. The calculation of the expected value A_i is implemented as an average

TABLE 1. Parameters setting for TI-ADC model.

Model parameters	Value
Sampling rate (f_s)	2 GS/s
Sampling period (T_s)	$1/f_s$
ADC resolution	12 Bit
Number of channels	4
Timing skew	$[0, 0.01, -0.025, 0.015] \cdot T_s$
Type of input signal	Single-tone, Multi-tone, Random Signal
L	64
Iteration step size (μ)	2^{-8}

of L values of the time series

$$A_i \approx \frac{1}{L}\sum_{l=1}^{L} y_{mod(i+3,4)}[l] \cdot y_i[l] \tag{16}$$

where L is the number of samples for each calculation of the average. Therefore, a moving average can be employed to obtain the expected value A_i. However, the conventional moving average implementation requires dedicated memory. In this paper, we use a more advanced moving average implementation instead, as shown in Fig. 5(a). The output of the averagers can be expressed as

$$A_i[k] = A_i[k-1] + \frac{(P_i[k] - A_i[k-1])}{L} \tag{17}$$

where $P_i[k]$ is the product between the outputs of adjacent channels.

The advantage of this way is that previous samples need not be stored. Furthermore, due to L is an integer-power of two number normally, the division can be achieved by a simple shift operation, rendering avoiding the use of a divider. Fig. 5(b) shows the DMC-based corrector we used, which uses Taylor approximation to eliminate the high-order error of the mismatch signal. The corrector consists of discrete-time differentiators and time-varying multipliers. After the correction parameters $C_i[k]$ are obtained by the estimator, they will be sent to time-varying multipliers of the corrector for signal reconstruction. A detailed description of this corrector can be found in [24].

IV. EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

To verify the effectiveness of the proposed estimation method, a four-channel TI-ADC behavioral model described in Table 1 has been performed and simulated in MATLAB. Moreover, thermal noise is introduced into the simulated TI-ADC, and its variance is the same as the quantization noise. The differentiator-multiplier-cascade (DMC) based correction method (with two stages) in [24] is employed to correct the timing skew mismatch.

For a single-tone signal input at $0.347 \cdot f_s$, the output spectra of the TI-ADC before and after calibration is shown in Fig. 6.

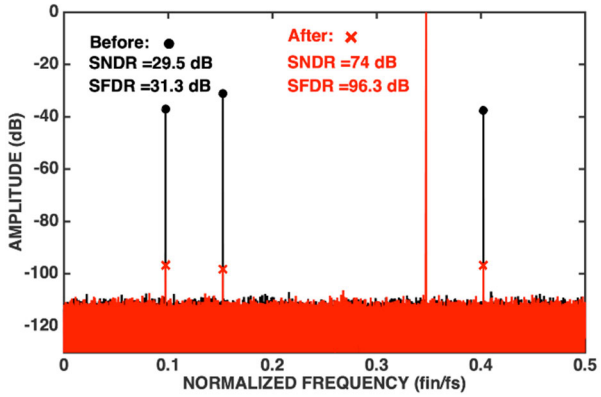

FIGURE 6. Spectra of TI-ADC output before/after calibration for a single tone input at $0.347f_S$.

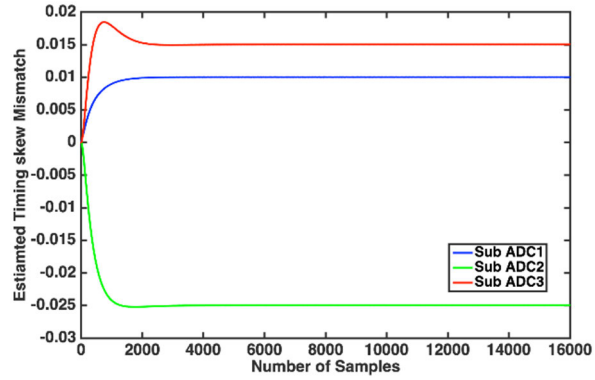

FIGURE 7. Convergence curves of estimated timing skew coefficients.

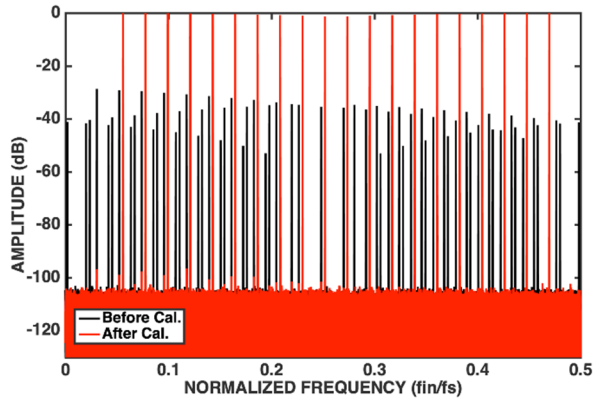

FIGURE 8. Spectra of TI-ADC output before/after calibration for a multitone input.

All timing skew induced spurs are well suppressed and the SNDR and SFDR are improved from 29.5 dB and 31.3 dB to 74.0 dB and 96.3 dB, respectively. The estimated timing skew convergence curve corresponding to Fig. 6 is shown in Fig. 7. Compared with the preset value, the proposed estimation method can accurately extract the timing mismatch error, and the required number of samples is only about 4000. Fig. 8 and Fig. 9 show the comparison of the spectrum of TIADC output before and after calibration in the case of multi-tone and random signal input, respectively. All spurs caused by timing skew mismatch are well suppressed after calibration.

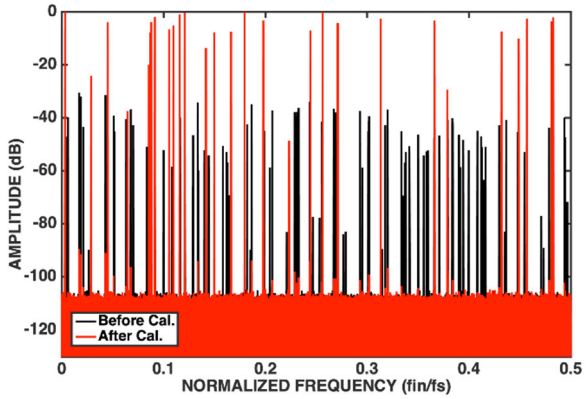

FIGURE 9. Spectra of TI-ADC output before/after calibration for a random signal input.

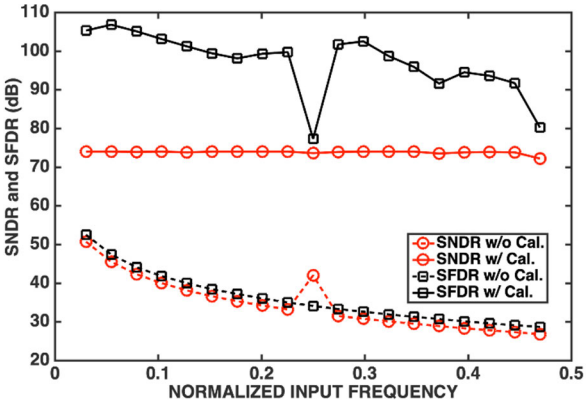

FIGURE 10. SNDR and SFDR versus different input sinusoidal frequencies without and with calibration.

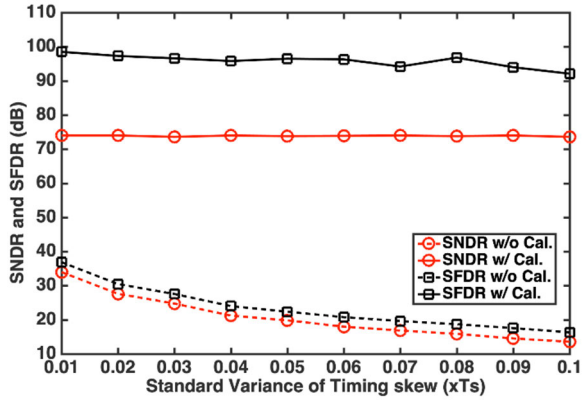

FIGURE 11. SNDR and SFDR versus different timing skew mismatches without and with calibration.

Fig. 10 demonstrates the SNDR and SFDR of TIADC versus different input sinusoidal frequencies. For almost the entire Nyquist domain, the proposed algorithm can maintain an improvement of at least 20 dB. The attenuation at the near Nyquist input is caused by the frequency response of the filter in corrector [24]. The relationship between SNDR and SFDR and different timing skew mismatches is illustrated in Fig. 11. The proposed calibration method can achieve

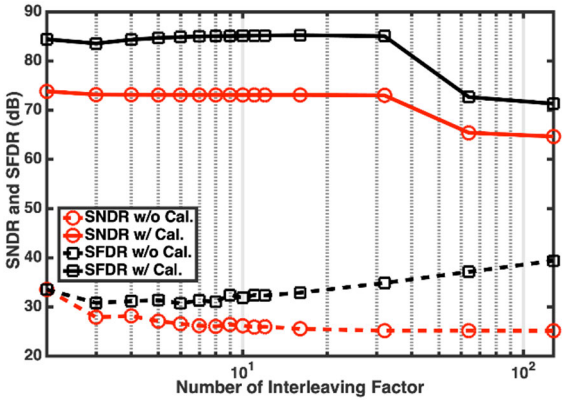

FIGURE 12. SNDR and SFDR versus different interleaving factors M without and with calibration.

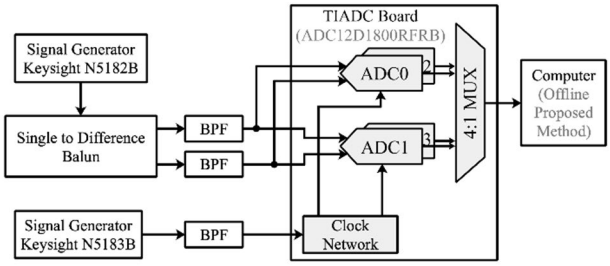

FIGURE 13. Block diagram of the measurement setup.

an improvement of 30dB for SNDR and 50dB for SFDR, even in the case of serious timing skew mismatch. We also simulated the proposed method under different number of interleaving factor (M = 2, 3,..., 12, 16, 32, 64, 128) when input frequency at $0.457 \cdot f_s$, as shown in Fig. 12, and the results show that the dynamic performances of TIADC in each case has been greatly improved.

B. MEASUREMENT RESULTS

The proposed timing skew mismatch calibration method is verified by employing a commercial 12-bit 3.6 GSPS TI-ADC evaluation board (ADC12D1800RFRB), which produced by Texas Instruments [38]. The data sheet of this evaluation board claims that it is a two-channel TIADC. In fact, each channel consists of two Sub-ADCs, so it is actually a four-channel TI-ADC. It has a Double Edge Sampling (DES) mode, which can realize interleaved sampling of the entire converter. Manual analog timing skew adjustment can be performed on chip via a 7-bit control register. Our experiment uses the DES-I mode and sets the timing skew to the maximum mismatch (i.e., 7b'1111111). In addition, the offset and gain mismatch are all completed by on-chip calibration. The block diagram of the entire measurement system is shown in Fig. 13, and Fig. 14 is a photograph of the actual measurement environment. The input signal and sampling clock signal are generated by Keysight's N5182B and N5183B, respectively, and their frequencies are 1.442GHz and 3.6GHz. The TI-ADC chip is set to timing skew mismatch mode through the control register in the

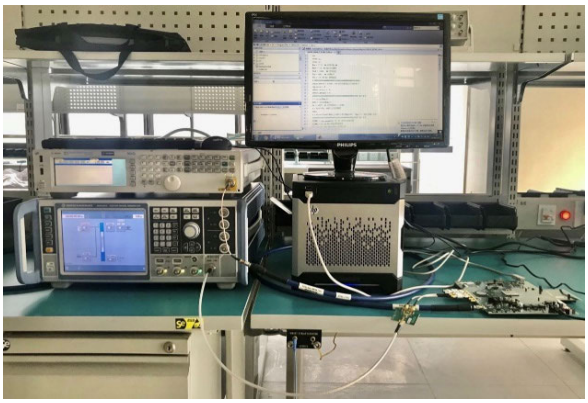

FIGURE 14. Laboratory measurement environment.

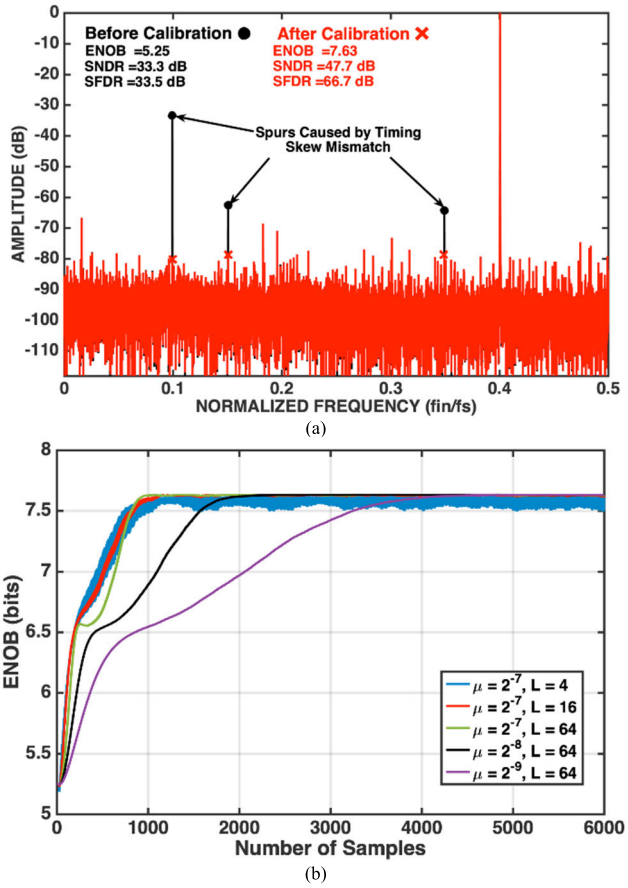

FIGURE 15. (a) Spectra of TI-ADC output before/after calibration for real samples. (b) Convergence curves of TI-ADC's ENOB.

control software. In this way, the digital outputs with timing skew mismatch are sent to the computer for processing by the proposed calibration method.

For the real sampling outputs of the TI-ADC evaluation board, Fig. 15(a) and Fig. 15(b) show the comparison of the output spectrum with and without calibration and the improvement of the TI-ADC chip ENOB during calibration process, respectively. After calibration, both SNDR and SFDR have been significantly improved. The effective number of bits (ENOB) has also been increased from 5.2 to around

7.6 when $L = 64$, slightly lower than the 8 bits described in the data sheet [38] due to the performance limitation of the bandpass filters. Table 2 illustrates the performance comparison between the proposed method and the other state-of-the-art correlation-based estimation methods. The proposed method shows better superiority in comprehensive performance.

V. ASSESSMENT: EFFECTS OF OFFSET AND GAIN MISMATCHES

The above is described on the premise of no offset and gain mismatches. This subsection discusses their impact on the proposed method separately. According to the equations (8)-(12) in the section II, C_i in Fig. 5(a), when there are offset (o_i) and gain (Δg_i) mismatches, can be expressed as

$$\begin{aligned} C_{i,o} &= A_{i+1} - \frac{1}{M}\sum_{i=0}^{M-1} A_i \\ &\approx R_x(T_s) + \Delta\tau_i \cdot R_x'(T_s) + o_{mod(i+M-1,M)} \cdot o_i \\ &\quad - R_x(T_s) - \frac{1}{M}\sum_{i=0}^{M-1} o_{mod(i+M-1,M)} \cdot o_i \\ &= \Delta\tau_i \cdot R_x'(T_s) + o_{mod(i+M-1,M)} \cdot o_i \\ &\quad - \frac{1}{M}\sum_{i=0}^{M-1} o_{mod(i+M-1,M)} \cdot o_i \end{aligned} \tag{18}$$

and

$$\begin{aligned} C_{i,g} &= A_{i+1} - \frac{1}{M}\sum_{i=0}^{M-1} A_i \\ &\approx (1+\Delta G)\cdot\left(R_x(T_s) + \Delta\tau_i \cdot R_x'(T_s)\right) - R_x(T_s) \\ &\quad - \frac{1}{M}\sum_{i=0}^{M-1} \Delta G \cdot \left(R_x(T_s) + \Delta\tau_i \cdot R_x'(T_s)\right) \\ &= \Delta\tau_i \cdot R_x'(T_s) + \Delta G \cdot \left(R_x(T_s) + \Delta\tau_i \cdot R_x'(T_s)\right) \\ &\quad - \frac{1}{M}\sum_{i=0}^{M-1} \Delta G \cdot \left(R_x(T_s) + \Delta\tau_i \cdot R_x'(T_s)\right) \end{aligned} \tag{19}$$

respectively, where

$$\Delta G = \Delta g_i + \Delta g_{mod(i+M-1,M)} + \Delta g_i \cdot \Delta g_{mod(i+M-1,M)} \tag{20}$$

$i = 0, 1, \ldots, M-2$ and $\Delta g_i = g_i - 1$. By comparing with (12), both the offset and gain mismatch will introduce some interference terms into the estimation process. However, we want to know whether the estimation method can still maintain good results under different degrees of offset and gain mismatches. In this regard, we simulate the proposed calibration method in the presence of offset and gain mismatches, respectively. Offset mismatch is set to obey a normal distribution with a mean value of zero, and the standard deviation of the mismatch varies from 0.01 to 0.1. The gain mismatch is set to follow a normal distribution with a mean value of one, and the standard deviation of the mismatch varies from 0.005 to 0.05. The residual difference between the estimated and actual timing skew values of each channel is used to characterize the performance of the proposed technique, and each difference is an average value

TABLE 2. Comparison of the state-of-the-art correlation-based estimation methods.

	[26]	[30]	[31]	[36]	This work
Background	Yes	Yes	Yes	Yes	Yes
Auxiliary Channel	No	No	No	Yes	No
ADC resolution	2	Arb.	Arb.	Arb.	Arb.
Applicable Channels*					
Pilot Injection	No	No	No	No	No
Number of FIR Filter**	0	1	1	0	0
Number of Adder***	1	5	2	1	4
Number of Multiplier***	2	2	1	1	1
Matrix Operation	No	Yes	Yes	No	No
Convergence Samples**	100K	5K	240K	N/A	4K

* Arb. means arbitrary.

** For per Sub-ADC channel.

*** For per Sub-ADC channel and not include the part used in the filter

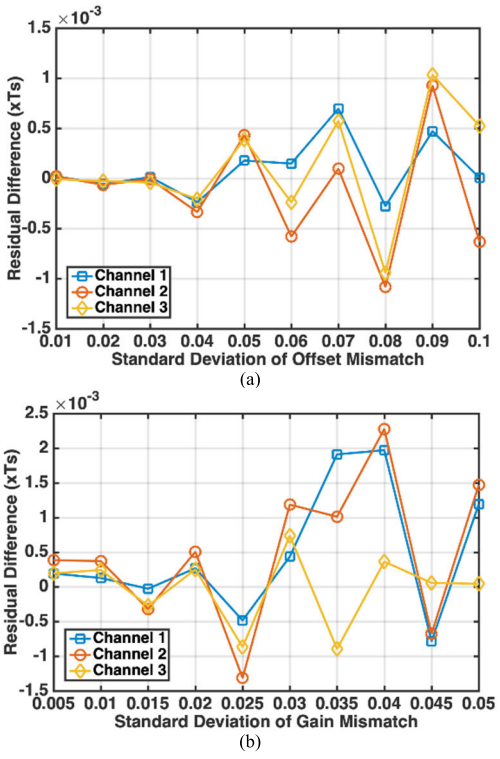

FIGURE 16. (a) Offset and (b) gain mismatch versus the effect of the proposed method.

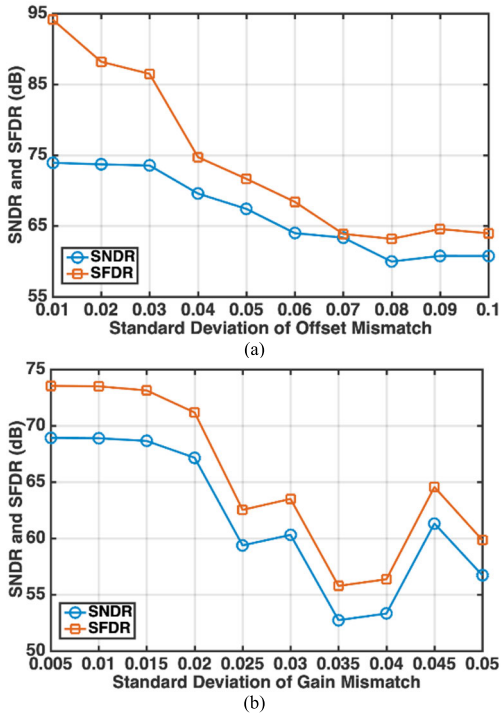

FIGURE 17. (a) Offset and (b) gain mismatch versus the effect of the proposed method.

of 100 simulation results ($L = 64$). The simulation result is shown in Fig. 16, which shows the effect of the proposed estimation method under different degrees of offset and gain mismatch. It can be found that the estimated values of timing skew still maintain high accuracy until the mismatch standard deviations of offset and gain are greater than 0.03 and 0.01, respectively. Unlike Offset, the gain mismatch directly affects the correlation function itself, as shown in equation (19), so the proposed estimation method is less tolerant to it than the offset mismatch. This is also verified in Fig. 17, which shows the SNDR and SFDR corresponding to Fig. 16. In the case of slight mismatch, the impact of offset on SNDR and SFDR is less than gain mismatch.

VI. CONCLUSION

In this paper, an all-digital background calibration method for timing skew mismatch in TI-ADCs has been presented. Correlation-based digital timing skew mismatch estimation and differentiator-multiplier-cascade based correction are combined to achieve accurate timing skew mismatch identification and effective distortion tones suppression. It is suitable for the case of any interleaved channels, and neither requires pilot input signals nor additional auxiliary ADC channels. Compared with the other correlation-based methods, it has a simpler implementation framework and less hardware consumption. The simulation results show that the proposed method can effectively improve the performance of TI-ADC for various types of input signals and various degrees of timing skew mismatch. The SFDR and SNDR are improved by more than 40 dB and 20 dB at least, respectively. In addition, even in the case where there is a certain degree of offset and gain mismatch, the proposed method still maintains a high estimation accuracy. The measurement results based on a commercial TI-ADC evaluation board demonstrate that the proposed method is also effective on real samples with timing skew mismatch.

REFERENCES

[1] M. El-Chammas, X. Li, S. Kimura, K. Maclean, J. Hu, M. Weaver, M. Gindlesperger, S. Kaylor, R. Payne, C. K. Sestok, and W. Bright, "A 12 bit 1.6 GS/s BiCMOS 2×2 hierarchical time-interleaved pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 1876–1885, Sep. 2014.

[2] W. Wei, P. Ye, J. Song, H. Zeng, J. Gao, and Y. Zhao, "A behavioral dynamic nonlinear model for time-interleaved ADC based on volterra series," *IEEE Access*, vol. 7, pp. 41860–41873, 2019.

[3] M. Guo, J. Mao, S.-W. Sin, H. Wei, and R. P. Martins, "A 5 GS/s 29 mW interleaved SAR ADC with 48.5 dB SNDR using digital-mixing background timing-skew calibration for direct sampling applications," *IEEE Access*, vol. 8, pp. 138944–138954, 2020.

[4] A. Buchwald, "High-speed time interleaved ADCs," *IEEE Commun. Mag.*, vol. 54, no. 4, pp. 71–77, Apr. 2016.

[5] C. Vogel, "The impact of combined channel mismatch effects in time-interleaved ADCs," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 1, pp. 415–427, Feb. 2005.

[6] C. Vogel and H. Johansson, "Time-interleaved analog-to-digital converters: Status and future directions," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2006, pp. 3386–3389.

[7] C. Vogel, M. Hotz, S. Saleem, K. Hausmair, and M. Soudan, "A review on low-complexity structures and algorithms for the correction of mismatch errors in time-interleaved ADCs," in *Proc. 10th IEEE Int. NEWCAS Conf.*, Jun. 2012, pp. 349–352.

[8] M. El-Chammas and B. Murmann, "General analysis on the impact of phase-skew in time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 902–910, May 2009.

[9] Z.-M. Lee, C.-Y. Wang, and J.-T. Wu, "A CMOS 15-bit 125-MS/s time-interleaved ADC with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2149–2160, Oct. 2007.

[10] T. Miki, T. Ozeki, and J.-I. Naka, "A 2-GS/s 8-bit time-interleaved SAR ADC for millimeter-wave pulsed radar baseband SoC," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2712–2720, Oct. 2017.

[11] J. Fang, S. Thirunakkarasu, X. Yu, F. Silva-Rivas, C. Zhang, F. Singor, and J. Abraham, "A 5-GS/s 10-b 76-mW time-interleaved SAR ADC in 28 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 7, pp. 1673–1683, Jul. 2017.

[12] Y. Park, J. Kim, and C. Kim, "A scalable bandwidth mismatch calibration technique for time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 11, pp. 1889–1897, Nov. 2016.

[13] D. Stepanovic and B. Nikolic, "A 2.8 GS/s 44.6 mW time-interleaved ADC achieving 50.9 dB SNDR and 3 dB effective resolution bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 971–982, Apr. 2013.

[14] M. El-Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 838–847, Apr. 2011.

[15] H.-W. Kang, H.-K. Hong, W. Kim, and S.-T. Ryu, "A time-interleaved 12-b 270-MS/s SAR ADC with virtual-timing-reference timing-skew calibration scheme," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2584–2594, Sep. 2018.

[16] S. Lee, A. P. Chandrakasan, and H.-S. Lee, "A 1 GS/s 10b 18.9 mW time-interleaved SAR ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2846–2856, Dec. 2014.

[17] P. K. Venkatachala, A. ElShater, Y. Xu, M. El-Chammas, and U.-K. Moon, "Voltage domain correction technique for timing skew errors in time interleaved ADCs," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4.

[18] C. Vogel, D. Draxelmayr, and F. Kuttner, "Compensation of timing mismatches in time-interleaved analog-to-digital converters through transfer characteristics tuning," in *Proc. 47th Midwest Symp. Circuits Syst. (MWSCAS)* vol. 1, 2004, pp. 341–344.

[19] B.-R.-S. Sung, D.-S. Jo, I.-H. Jang, D.-S. Lee, Y.-S. You, Y.-H. Lee, H.-J. Park, and S.-T. Ryu, "A 21fJ/conv-step 9 ENOB 1.6 GS/S 2× time-interleaved FATI SAR ADC with background offset and timing-skew calibration in 45 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
[20] J. Song, K. Ragab, X. Tang, and N. Sun, "A 10-b 800-MS/s time-interleaved SAR ADC with fast variance-based timing-skew calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2563–2575, Oct. 2017.
[21] J. Song and N. Sun, "A 10-b 600-MS/s 2-way time-interleaved SAR ADC with mean absolute deviation based background timing-skew calibration," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.
[22] H. Johansson and P. Lowenborg, "Reconstruction of nonuniformly sampled bandlimited signals by means of digital fractional delay filters," *IEEE Trans. Signal Process.*, vol. 50, no. 11, pp. 2757–2767, Nov. 2002.
[23] C. Vogel and S. Mendel, "A flexible and scalable structure to compensate frequency response mismatches in time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 11, pp. 2463–2475, Nov. 2009.
[24] S. Tertinek and C. Vogel, "Reconstruction of nonuniformly sampled bandlimited signals using a Differentiator–multiplier cascade," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 8, pp. 2273–2286, Sep. 2008.
[25] M. Hotz and C. Vogel, "Block processing with iterative correction filters for time-interleaved ADCs," in *Proc. IEEE Int. Conf. Acoust., Speech Signal Process. (ICASSP)*, May 2014, pp. 4923–4932.
[26] B. Razavi, "Design considerations for interleaved ADCs," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1806–1817, Aug. 2013.
[27] S. Singh, L. Anttila, M. Epp, W. Schlecker, and M. Valkama, "Frequency response mismatches in 4-channel time-interleaved ADCs: Analysis, blind identification, and correction," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2268–2279, Sep. 2015.
[28] M. Seo, M. J. W. Rodwell, and U. Madhow, "Comprehensive digital correction of mismatch errors for a 400-msamples/s 80-dB SFDR time-interleaved analog-to-digital converter," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 3, pp. 1072–1082, Mar. 2005.
[29] A. Bonnetat, J.-M. Hode, G. Ferre, and D. Dallet, "Correlation-based frequency-response mismatch compensation of quad-TIADC using real samples," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 8, pp. 746–750, Aug. 2015.
[30] H. Le Duc, D. M. Nguyen, C. Jabbour, P. Desgreys, O. Jamin, and V. T. Nguyen, "Fully digital feedforward background calibration of clock skews for sub-sampling TIADCs using the polyphase decomposition," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 6, pp. 1515–1528, Jun. 2017.
[31] A. Salib, M. F. Flanagan, and B. Cardiff, "A high-precision time skew estimation and correction technique for time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 10, pp. 3747–3760, Oct. 2019.
[32] A. Leuciuc, "Sampling time calibration method for multi-channel interleaved ADCs," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4.
[33] H. Mafi, M. Yargholi, and M. Yavari, "Digital blind background calibration of imperfections in time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 6, pp. 1504–1514, Jun. 2017.
[34] J. Matsuno, T. Yamaji, M. Furuta, and T. Itakura, "All-digital background calibration technique for time-interleaved ADC using pseudo aliasing signal," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1113–1121, May 2013.
[35] Y. Qiu, Y.-J. Liu, J. Zhou, G. Zhang, D. Chen, and N. Du, "All-digital blind background calibration technique for any channel time-interleaved ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 8, pp. 2503–2514, Aug. 2018.
[36] S. Azizian and M. Ehsanian, "Generalized method for extraction of offset, gain, and timing skew errors in time-interleaved ADCs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 7, pp. 1214–1218, Jul. 2020.
[37] I. Florescu, *Probability and Stochastic Processes*. Hoboken, NJ, USA: Wiley, 2014.
[38] Texas Instruments. (2016). *ADC12D1800RF, 12-Bit, Single 3.6 GSPS RF Sampling ADC (Rev. H)*. [Online]. Available: http://www.ti.com

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