IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received January 25, 2021, accepted March 7, 2021, date of publication March 17, 2021, date of current version March 26, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3066261

Cascaded- and Modular-Multilevel Converter Laboratory Test System Options: A Review

THEODOR HEATH[1], MIKE BARNES[1], (Senior Member, IEEE), PAUL D. JUDGE[2], (Member, IEEE), GERAINT CHAFFEY[3], PHIL CLEMOW[4], TIM C. GREEN[4], (Fellow, IEEE), PETER R. GREEN[1], (Member, IEEE), JAMES WYLIE[4], GEORGIOS KONSTANTINOU[5], (Senior Member, IEEE), SALVADOR CEBALLOS[6], JOSEP POU[7], (Fellow, IEEE), MOHAMED MOEZ BELHAOUANE[8], HAIBO ZHANG[8], XAVIER GUILLAUD[8], (Member, IEEE), AND JACK ANDREWS[1]

[1]Department of Electrical Engineering and Electronics, The University of Manchester, Manchester M13 9PL, U.K.
[2]School of Engineering, Institute for Energy Systems, The University of Edinburgh, Edinburgh EH9 3FB, U.K.
[3]Department of Electrical Engineering (ESAT), KU Leuven, 3001 Leuven, Belgium
[4]Energy Futures Lab, Department of Electrical Engineering, Imperial College London, London SW7 2BU, U.K.
[5]School of Electrical Engineering and Telecommunications, UNSW Sydney, Sydney, NSW 2052, Australia
[6]Basque Research and Technology Alliance (BRTA), Tecnalia, 48160 Derio, Spain
[7]School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798
[8]ULR 2697–L2EP, Centrale Lille, Yncrea Hauts-de-France, Arts et Metiers Institute of Technology, University of Lille, 59000 Lille, France

Corresponding author: Mike Barnes (mike.barnes@manchester.ac.uk)

This work was supported in part by The University of Manchester supported by the National Innovation Allowance project "VSC-HVDC Model Validation and Improvement" and Dr. Heath's iCASE Ph.D. studentship supported through Engineering and Physical Sciences Research Council (EPSRC) and National Grid, in part by the Imperial College London supported by EPSRC through the HubNet Extension under Grant EP/N030028/1, in part by an iCASE Ph.D. Studentship supported by EPSRC and EDF Energy and the CDT in Future Power Networks under Grant EP/L015471/1, in part by University of New South Wales (UNSW) supported by the Solar Flagships Program through the Education Infrastructure Fund (EIF), in part by the Australian Research Council through the Discovery Early Career Research Award under Grant DECRA–DE170100370, in part by the Basque Government through the project HVDC-LINK3 under Grant ELKARTEK KK-2017/00083, in part by the L2EP research group at the University of Lille supported by the French TSO (RTE), and in part by the Hauts-de-France region of France with the European Regional Development Fund under Grant FEDER 17007725.

ABSTRACT The increasing importance of cascaded multilevel converters (CMCs), and the sub-category of modular multilevel converters (MMCs), is illustrated by their wide use in high voltage DC connections and in static compensators. Research is being undertaken into the use of these complex pieces of hardware and software for a variety of grid support services, on top of fundamental frequency power injection, requiring improved control for non-traditional duties. To validate these results, small-scale laboratory hardware prototypes are often required. Such systems have been built by many research teams around the globe and are also increasingly commercially available. Few publications go into detail on the construction options for prototype CMCs, and there is a lack of information on both design considerations and lessons learned from the build process, which will hinder research and the best application of these important units. This paper reviews options, gives key examples from leading research teams, and summarizes knowledge gained in the development of test rigs to clarify design considerations when constructing laboratory-scale CMCs.

INDEX TERMS AC-DC power converters, HVDC transmission, modular multilevel converters.

I. INTRODUCTION

Cascaded multilevel converters (CMCs) are poised to become a major power electronic technology. In the UK, 15 GW of voltage source converter high-voltage DC transmission (VSC-HVDC) are operational or planned for the next 5 years to connect the UK with mainland Europe [1] using CMC technology. Of the more than 40 GW of offshore wind planned in the UK [2] a large fraction will be interfaced through CMC HVDC. Similar developments are occurring elsewhere internationally. Currently all major HVDC vendors offer a form of CMC. CMCs are also widely used in modern static compensators (STATCOMs) and even medium voltage DC systems. In the future, CMC applications, such

The associate editor coordinating the review of this manuscript and approving it for publication was Hiu Yung Wong.

as VSC-HVDC, will be expected to take on grid support functions (ancillary services) providing frequency support, power system damping and other functions. The complete understanding of the capability envelope of these circuits, their control and system limitations is necessary. Much excellent work can be, and has been, done in simulation, including both hardware-in-the-loop (HIL) real-time simulation, and software-in-the-loop. However, modelling requires knowledge of the system physics and parameters, and often hard-to-model parasitic effects like stray inductance and capacitance can play a significant role; hardware to validate research results therefore becomes invaluable. Industry is capable of producing multi-megawatt scale demonstrators, sometimes in partnership with universities [3], but for most organisations this is impractical – small-scale laboratory demonstrators thus become a necessary component of CMC research. However, the design and construction of a CMC, even at laboratory scale, is non-trivial and limited information is available in the public domain to support the process. There is a trade-off between many variables, and a compromise is required to make a scaled converter. Power, voltage and component ratings need to be reduced to make the design practical and cost-effective, whilst at the same time ensuring that key dynamics and complexities are represented.

A CMC uses a string of sub-modules (SMs) to synthesize an AC waveform in steps from a DC voltage [4]. The CMC family of topologies include cascaded two-level converters (CTLCs) [5]–[7], modular multilevel converters (MMCs) [8], [9] and alternate arm converters (AACs) [10], [11]. CMCs typically comprise a number of series connected SMs of half-bridge (HB), full-bridge (FB) or more complex SM designs, and potentially other circuits like director switches (DS). The SMs are typically stacked into three phases (legs) each split into two arms with a series connected reactor (L_{arm}) for DC fault current limitation and current control purposes [12]. Each phase is typically connected in parallel across the DC bus [4], [8], as shown in Fig. 1.

HB-SMs are two-level designs comprising two switches, which are either individual power electronic devices for MMCs [12], or series-connected devices for CTLCs [5]–[7], with diodes connected in antiparallel, and with a capacitor for energy storage, Fig. 1. The power electronic devices are typically Insulated Gate Bipolar Transistors (IGBTs). In normal operation, the output at the terminals of the HB-SM can either be the voltage stored on the SM capacitor or zero. DS units typically found in AAC topologies are formed of series connected IGBTs and antiparallel diodes. They are used to direct the current into only one arm for portions of each cycle by controlled blocking or conduction. Numerous other SM topologies have also been described in the literature [13]–[15], typically designed with the aim of reducing conduction loss or the number of semiconductor devices required to achieve DC fault tolerance.

Each CMC SM can switch independently, allowing SM capacitors to be connected or bypassed in the arm, effectively

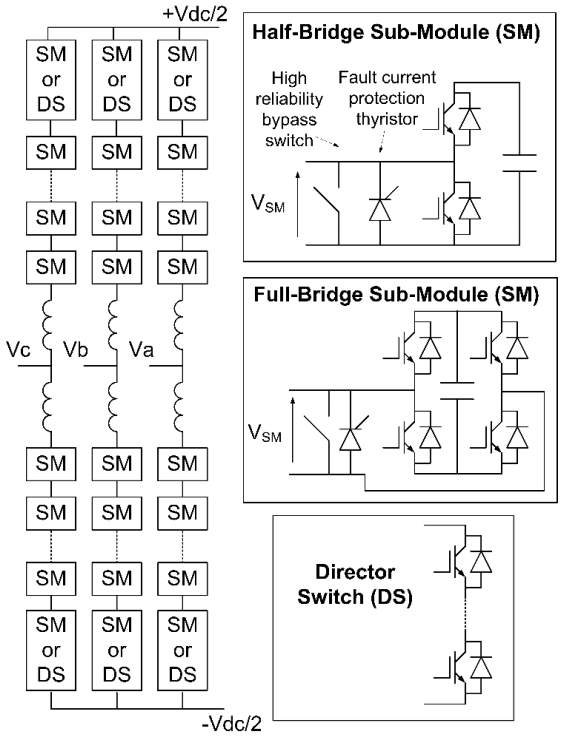


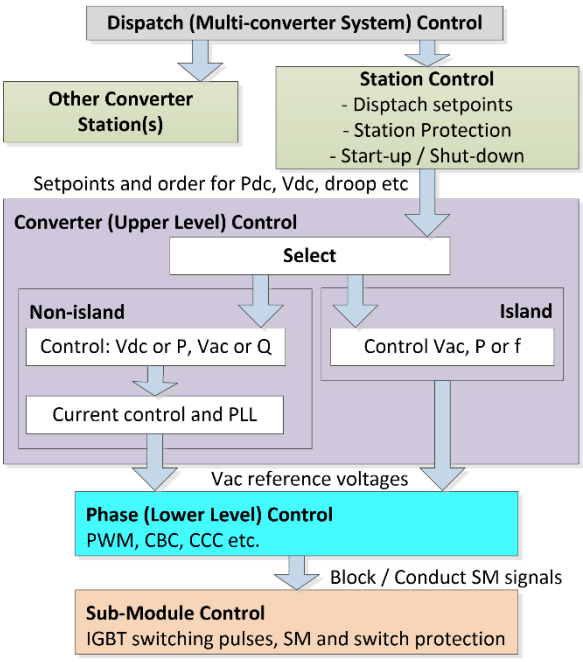
FIGURE 1. Cascaded multilevel converter – generalized structure and typical sub-module designs.

creating two controllable voltage sources (the upper arm and the lower arm) in each phase. Through appropriate switching, the voltage measured at the mid-point of the arms in each phase can be controlled; these are the AC connection points of the converter. For more detailed discussion around the theoretical operation of CMCs, see [7], [8], [16].

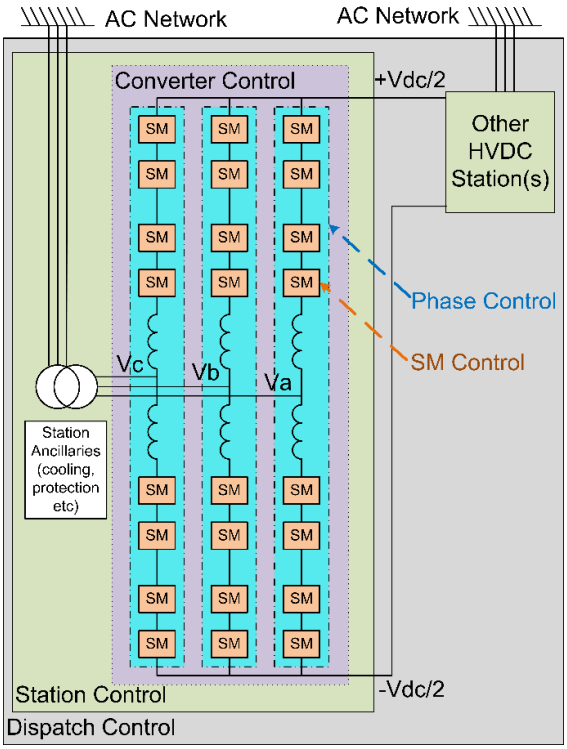
II. CMC CONTROL STRUCTURE

The general 'classic' control structure for CMC has been outlined by Cigré [17] and is widely discussed in the literature, for example [18]. It is shown in simplified form in Fig. 2a. This structure follows a cascaded control with each outer (lower bandwidth) level providing set-points to inner (higher bandwidth) levels. These levels in turn map on to hardware, Fig. 2b. Dispatch control communicates by telecommunications to the station control level, which tells the converter and other station units what set-points to use. The converter control communicates with each phase, which perform functions like capacitor balancing control (CBC) and current control, before sending detailed signals to a local control level which provides IGBT switch pulses and local protection. Here current control includes both output current control and circulating current control (CCC).

In a scale model, not all of the complex factors which affect control in a full-scale system will typically be implemented; for example, the effect of the hardware communication between the different control layers (as shown by the arrows in Fig. 2a). In practice, many laboratory systems centralise all control level functions in one set of powerful hardware (so called centralized control). SMs then receive



(a) Control structure



(b) Approximate mapping of control levels to hardware

FIGURE 2. Generalized CMC Control.

gate drive signals from this centralised control scheme and all SM signals (such as capacitor SM voltages) are fed back to the centralized controller. This simplifies certain functions such as capacitor sorting and practical aspects like reprogramming of the system. A real-world converter system typically does not have this kind of centralized control and telecommunication for a variety of reasons (see Section V). There is also a need for various levels of protection at lower levels. There exists a hierarchy of controllers, and levels of control are distributed among these (so-called distributed control). This adds extra complexity, which may be emulated by laboratory hardware or, if sufficient processing power is available, in software.

III. GENERAL CONVERTER DESIGN

A general overview of industrial converter design is provided in [4], which also identifies the challenges faced by manufacturers. However, the design of an industrial converter is very different to that of a research tool. Customer needs, voltage and current ratings, efficiency requirements, reliability levels and limitations in state-of-the-art technologies constrain industrial designs to very strict performance expectations. In application, these converters have footprints in the thousands of square meters [19] at a cost often exceeding £ 100 million [14], [15], [20], well beyond the affordability of research institutions.

Replicating a system to meet all of the performance criteria of an industrial converter within a research environment is clearly challenging, and also not usually a requirement. Therefore, alternative strategies are adopted. By choosing a sub-set of performance requirements, suitable for the phenomena that is to be investigated with the demonstrator, a specification for a reduced-scale converter can be developed. This process inherently lowers the cost of construction and system size, making it more suitable to academic and other research. Even with reduced requirements, designing and constructing a bespoke laboratory scale converter is not a simple task. In the case of Imperial College London (ICL), three researchers worked for two years (with two full design iterations) to reach the stage of research output. At the University of Manchester (UoM), with time-saving suggestions from the ICL team, this was reduced to one researcher working for three-and-a-half years. In both cases, the converter build process was supported by additional researchers and academics; a large undertaking for any research group. Commercial hardware solutions to CMC research have recently been developed and offer research institutions fast access to multilevel converter prototyping hardware. For example two such systems are offered by Imperix Ltd. [21] and Opal-RT [22]. In some cases, these systems will provide an ideal platform for research. However, research by definition involves doing something 'non-standard': in some cases therefore commercial solutions may not give sufficient flexibility, observability and configurability.

IV. REDUCED-SCALE CONVERTER DESIGN

A. BRIEF AND SPECIFICATION

Based on a review of existing lab-scale test systems, Table 1, and the knowledge gained by the authors developing their CMC systems, the specification for test rigs can be roughly divided into five 'types' according to their intended purpose. An implementation can obviously include more than one category but this is a trade-off. Including more functionality typically increases expense, complexity and

TABLE 1. Examples of test systems (∗denotes estimated value).

Host	Power Rating	SMs / Arm	Type	Reference
Smaller Scale Laboratory Systems				
Tsinghua University	620 W	6	C/D	[24]
Zhejiang University	830 VA	44	C	[25]
Universities of Edinburgh & Strathclyde	900 VA	8	D	[26]
University of Applied Science of Western Switzerland	1kW	5	A	[27]
Georgia Institute of Technology	~1kVA*	4	B	[28]
University of Manchester	1 kW	8	C	[29]
Huazhong University of Science and Technology	2kVA	4	C/D	[30]
Seoul National University	2.5 kVA	6	B	[31]
KTH Sweden	3 kVA	5	D	[32]
Tsinghua University	3 kW	4	D	[33]
GEIRI	4 kW	216	C	[34]
University of Lille	5 kW	20	B	[35]
Zhejiang University	2 to 6 kVA	6-12	B/D	[23][36]
RWTH Aachen University	6 kW	10	A	[37]
Aalborg University	10 kVA	8	C	[38]
Tokyo Institute of Technology	10 kW	8	B	[39]
Tsinghua University	10 kVA	4	B	[40]
University of Nottingham	11 kVA	10	D	[41]
University of Tennessee	15 kVA	10	D	[42]
Imperial College	15 kW	10	B/D	[43]
Harbin Institute of Technology	20 kW	3	B	[44]
UNSW Sydney / Tecnalia	20kVA	8	B/C	[45]
Alcala University	25 kW	5	B	[46]
Pusan National University	50 kW	30	B/C	[47]
Sintef/NTNU (multi-terminal)	50 kW	6/12/18	A/B/E	[48]
Demonstrator Scale Systems				
EPFL	500 kVA	16	B	[49]
Florida State University / ABB	1.35 MW	6	B	[3]
University of the Bundeswehr Munich	2 MW	16	D	[50]
Institute of Electrical Engineering, Chinese Academy of Sciences	15 MVA	14	B	[51]

footprint – particularly as power and voltage requirements increase. In the early days of CMC development, test systems that fulfilled multiple functions were not uncommon – as more experience is gained, targeted solutions are becoming evident: e.g. Tsinghua and Zhejiang Universities both have multiple entries in Table 1. Ultimately it is the project requirements that set the specification. The five types are:

1) TYPE A - POWER SYSTEM AND MULTI-TERMINAL NETWORK STUDIES (PS&MTN)

In this system the primary focus is converter performance and operation within a wider network. The study is of the operation of known architectures – new SM designs are of less interest. A variety of different control studies and applications (scenarios) of the converter are typically the target. The ability to quickly reconfigure control, a fast learning curve, good documentation, and electrically well protected hardware are desirable. Ideally control system programs would be developed using well-known tools such as MATLAB or LabVIEW; internal dynamics are abstracted away from the user, to simplify development, so this system should require minimal converter expertise. This classification typically represents commercial products for laboratory hardware and software development. Much of the desired test results are likely to consist of power, voltage and current flows measured by the actual converter system and fed back via the user interface – such systems are therefore also characterised by minimal extra measurement equipment. However some extra equipment will be necessary, for example AC (typically bi-directional) power supplies, to emulate the AC systems.

2) TYPE B - POWER AND CONTROL SYSTEM STUDIES (P&CS)

This system is focused in much greater detail on researching the hardware dynamics of the converter. Since the focus is primarily on the SM and converter hardware, it should be easy to reprogram and control, enabling good continuity of knowledge between researchers. Topology flexibility can be built into the design but making changes after construction may be challenging. The focus is on the detailed behaviour of the hardware, so supplementary, high-bandwidth voltage and current measurement equipment will probably be required, as will bidirectional AC and DC power supplies.

3) TYPE C - COMMUNICATIONS AND CONTROL ARCHITECTURE STUDIES (C&C)

Industrially representative internal control is distributed rather than centralized – thus some test systems may focus on the difference in these dynamics. Such a system needs to be built around a distributed control architecture. This allows for investigations into internal controls, CBC and modulation strategies and communication delays. Like Type B, topology flexibility can be built into the design, however, it may be difficult to adapt in the future. Due to the complex

internal structure this system requires significant levels of expertise, leading to more challenging knowledge dissemination between hardware users. Since the focus is on the controller hardware, the SM converter may also be somewhat simplified compared with industrial systems. Test equipment will need to include equipment capable of assessing telecommunication features like signal delay on multiple channels simultaneously. Full bidirectional AC and DC power supplies may not be necessary.

4) TYPE D - FUTURE CONVERTER TOPOLOGY AND SM CONFIGURATION STUDIES (FCT)

This represents systems which are designed to investigate novel topologies. As such they need a flexible hardware design that is easily reconfigurable and scalable, typically with low power ratings. They should be easy to adapt and reconfigure for new topologies during the design, and post construction, future proofing the hardware for continued research. Type D systems are therefore typically built around a centralized control architecture. Test equipment similar to Type B studies is needed to investigate the converter's dynamic performance.

5) TYPE E - FAULT AND PROTECTION STUDIES (F&P)

Such units are designed to examine fault behaviour of the converter, SMs and the design of protection and post-fault recovery systems. Type E differs from Type D, in that in Type E the focus is on the protection circuits and controls – these may not always be present in Type D. Representative normal dynamic behaviour may be sacrificed in Type E in order to simplify protection studies. For example Type E SMs may be over-designed in order to enable more flexibility and robustness when performing repeated fault studies. Also reconfigurability of the SMs will typically be sacrificed in favour of robustness – though protection circuits in contrast may be designed to be highly reconfigurable. Test equipment will also be sized differently – fault currents will need to be provided and measured. This category does not feature explicitly among examples in Table 1, since this focuses on the original CMC design goals. However the literature shows some Type B systems starting to be reconfigured for Type E studies (e.g. [23]).

In addition to choosing which of these five types are the target of the design brief, hardware configurability of the converter should be considered before any design process begins, specifically:

- How easy should the converter be to adapt?
- Can any SM be swapped into any location?
- Should SM changes be made in software or physically?
- Is spare physical space or I/O capacity required?

It is also important to consider the level of observation required in the early stages of specification selection. Design decisions are invariably a trade-off between factors:

- Are system-wide measurements required?
- How easy does data access need to be?
- Do all system control lines require observation?
- How easy does control system debugging need to be?
- What feedback is provided to the users and how?

How the hardware and software will be managed over its lifetime also needs considering. This includes repair, version control during development and knowledge transfer between successive researchers.

In practice a key design factor is reducing undue complexity. This led to all SMs in the UoM hardware being identical and being reconfigured by a physical bypass connector from HB to FB. This is also true of the ICL converter except for the AAC where one position in each arm is reserved for the director switch. It also means carefully choosing the 'types' of study to design the test system for, and how the power- and control-electronics need to interact.

Typically, a centralized control architecture offers a much simpler route to data collection and considerably easier control system development. In addition, a centralized control architecture will make the converter more accessible to other researchers, even those without prior hardware knowledge. Converter limits can be easily set in software to 'fool-proof' the equipment and ensure its longevity. CMCs with distributed control architectures require a more detailed understanding of the operation and limitations of the internal converter control and communication structure. A control system change may require months of software redevelopment and certain portions of measurement data may be stored locally, making it more difficult to access and analyse in real-time or for post-test analysis.

A summary of design considerations is provided in Table 2 for each of the type specifications defined in this section. Each type has been awarded a rating for each design element (in comparison to other specifications). System Type A is defined for comparison but will not be discussed in any further detail in this paper, as it represents a system which can be bought commercially, and there is information on the specifications of these systems in the public domain.

B. SIZE AND RATING

Once the specification for the CMC has been selected, an appropriate size and rating can be chosen; examples are shown in Table 1.

1) CONVERTER VOLTAGE AND POWER

Small-scale laboratory system design, including selection of the voltage and power ratings of the converter, is a compromise between the application type, the limitations that are set by the available facilities, other hardware available in the lab and total budget. For Type B studies (power and control studies), a higher voltage and power rating may be expected to offer more representative power system behaviour. Care should be taken however to select a DC voltage and power rating that are compatible with other pieces of equipment (commercial or otherwise) that may be used with the CMC (i.e. other converters, grid emulators, DC power supplies and loads).

TABLE 2. Comparison chart for system specifications and design considerations.

Type	A - PS&MTN	B - P&CS	C - C&C	D - FCT	E - F&P
Power System Study	Good	Good	Fair	Poor	Poor
Internal Control Study	Software only	Software only	Good	Software only	Software only
Multi-terminal Network Study	Good	Fair	Poor	Poor	Poor
Hardware Flexibility	Limited	Fair	Fair	Good	Protection only
System Observability	Fair	Good	Poor	Good	Good
Expertise Required	Low	Medium	High	Medium	High
Ease of Use	High	High	Low	Medium	Low
Protection Study	Limited	Limited	Unsuitable	Limited	Good

At higher voltages the converter will have increased converter losses (in absolute terms as heat) and have more stringent isolation requirements. However at higher voltages it is easier to make the converter more efficient, have a less damped response and thus be more representative of a full scale system. It will also enable the use of SMs that derive their power from the SM capacitor (discussed further in Section IV.D). The Type B converter built by ICL has a power rating of 15 kW with a DC-side voltage of $\pm$750 V, leading to a nominal SM voltage of 150 V (10 SMs per arm). It uses a 90 kVA AC/AC programmable converter for the AC network. The decision to use a $\pm$750 V DC bus resulted in significant additional capital cost as it required the use of non-standard AC and DC contactors, as well as requiring two series-connected 15 kW AC/DC programmable converters for the DC network.

Type C systems can be constructed at much lower voltages as the area of interest for the research is on internal control and communication, rather than power system studies. Low voltage/power systems are generally cheaper to construct and more forgiving in design constraints. Keeping SM ratings low simplifies bench-top prototyping. At 50 V DC and above, additional precautions should be taken when working with the equipment, which may slow down development. At lower powers, heat extraction also becomes easier. The Type C converter built by UoM has a power rating of 1 kW with a DC link voltage of $\pm$100 V, leading to a nominal SM voltage of 25 V (eight SMs per arm). It uses a resistive load for the AC side and a 5.1 kW AC/DC programmable converter for the DC network.

The design specifications for the UNSW system were a balance between functionality, flexibility and hardware availability. Two three-phase converter configurations are possible from within the one cabinet with the maximum rated power for the system, when operating as a single converter set to 20 kW based on the power ratings of the two DC power supplies and the four-quadrant grid emulator that were available and in use in the lab. The DC-link voltage is set at 800 V for a nominal SM voltage of 100 V per SM (eight SMs per arm) although the system can operate with a maximum DC-link voltage of 1150 V. Each SM is rated for operation up to 200 V as a provision for testing different arm energy control methods. The converter can be used connected to the grid (up to 400 V), connected to passive RL loads, digital AC loads as well as a rectifier using 3 $\times$ 5 kW digital DC loads on its DC terminals.

If Type D converters (future converter topology and SM configuration studies) are designed with fewer SMs, this enables fast reconfiguration and reduced costs when considering SM redesign. The choice of voltage rating for a converter of this design is largely dependent on research interests. However, it is important to consider that components with higher ratings are often more expensive, potentially increasing the cost of SM construction.

Type E (protection) study ratings will be driven to a large extent by the protection equipment and test equipment available.

2) SUB-MODULE SWITCHES AND RATING

For industry, the selection of components at high voltage is very limited and so much of the design process centres on equipment ratings. This also drives the number of SMs used. For example, the number of SMs selected for a converter is determined by the DC-side voltage of the CMC, power rating, state-of-the-art IGBT operational voltages and the number of IGBTs in series per SM 'switch' (i.e. the DC voltage rating of the SMs).

As the rating of the system drops, the range of components increases, and the design process becomes less restricted. Oversizing as a means of indirect protection also becomes readily possible. The number of levels for the converter is a greater matter of choice, which could be influenced by the desired nominal SM voltage, resulting cost of construction, physical size of converter, required harmonic performance, or the available I/O on controllers. However, care must be taken if system dynamics are to be replicated. For a full-scale 2 kV industrial SM, the IGBT voltage drop is about 3 V. For a test-rig, the DC link capacitor may be 200 V or less – the conduction power loss in similar switches (and hence the inherent system damping) will be larger. The use of MOSFETs instead may be appropriate, since conduction losses can be lower, and gate drive design is straightforward. However the MOSFET equivalent circuit during conduction is a resistance only (rather than the IGBT's voltage source in series with a resistance), resulting in slightly different dynamics. For example, UNSW's system uses 300 V/210 A discrete IXFB210N30P3 MOSFETs.

3) SUB-MODULE CAPACITORS

Capacitor sizing, another major design consideration, is typically based around permissible voltage ripple in the SM capacitor. Example design equations for an MMC [29], [52], [53] are:

$$\Delta W_{arm} = \frac{P_d}{3\omega} m \left(1 - \frac{1}{m^2}\right)^{3/2} \tag{1}$$

$$m = \frac{3\hat{I_{ac}}}{2I_{dc}} \tag{2}$$

$$C_{sm} = \frac{\Delta W_{arm}}{2N\varepsilon V_{cap}^2} \tag{3}$$

where ΔW_{arm} is the change in energy stored in an arm of one phase, P_d is the power rating of the converter, ω is the AC frequency in rad/s, $\hat{I}_{ac}$ is the peak AC current, I_{dc} is the DC current, C_{sm} is the SM capacitance, N is the number of SMs in an arm, ε is the ripple voltage factor ($0 < \varepsilon < 1$) and V_{cap} is the nominal capacitor voltage. This also assumes that the output voltage and current are sinusoidal, that the converter is symmetrical, circulating currents are zero, and the DC voltage is smooth and split equally between the SMs. Based on this analysis,

$$C_{sm} \propto \frac{P_d}{NV_{cap}^2} \tag{4}$$

This ratio will vary considerably from, say an industrial system rated at 1000 MW with 500 SMs per arm each with a 2 kV DC link, to a 10 kW test rig with 10 SMs each at 100 V. It is evident that systems which aim to closely replicate full-scale converter dynamics (Type B) need careful design, see for example [35]. This design is further complicated for applications which aim to operate at low fundamental frequencies or if substantial reactive power is required. If the CMC is designed to emulate several different topologies, each with different potential energy storage requirements, it may be desirable to design the SM capacitor as a selectable bank that allows the SM capacitance to be varied. This was done in the ICL SM as it was designed with the aim of representing both MMC and AAC topologies which have different ΔW_{arm}.

4) ARM INDUCTORS

Arm inductors are typically chosen with a per-unit value (L_{pu}) of between 0.1 and 0.2 [52], [54], [55], i.e.

$$L_{arm} = L_{pu}L_{base} = L_{pu}\frac{V_{base}}{\omega I_{base}} \tag{5}$$

where L_{arm} is the arm inductance in SI units, and V_{base} and I_{base} are the voltage and current base values respectively. This provides a reasonable balance between inductor size, fault current limitation and inductive smoothing at the AC output terminals. In high power applications, the arm and grid side inductors are sized to limit the time-gradient (A/s) of the DC and AC fault currents [35], [56]. With few SMs, this inductance may also play a role in terms of filtering effect. leading to a slight oversizing of the inductance in per unit terms compared to the value used at higher powers.

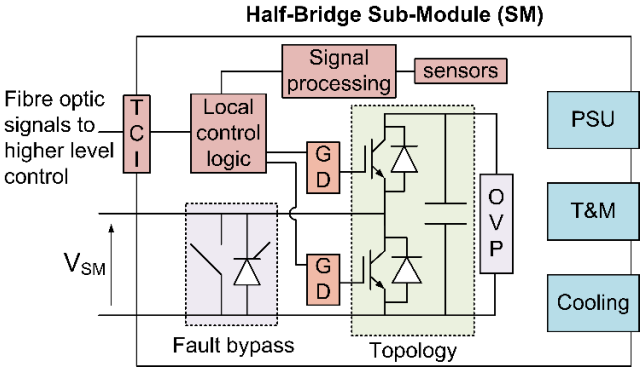


FIGURE 3. Example Sub-module – GD - Gate Drive, OVP - Overvoltage Protection, PSU – Power Supply Unit, TCI - Telecommunications Interface, T&M – Test and Measurement (not all connections shown).

5) ANCILLARY EQUIPMENT

Converters will require additional protection, power supply and measurement equipment to facilitate testing; in general, the higher the voltage, current and power requirements, the higher the cost. In some cases the equipment required for testing can be prohibitively expensive. Other limits on the power rating may be down to the available laboratory grid connection points. A standard 3-phase, 32 A, 400 V line-to-line supply point for example provides a maximum power output of 22 kW. Test and measurement systems will vary depending on the application (please see discussion on application types, Section IV.A).

C. SUB-MODULE DESIGN

1) GENERAL PRINCIPLES

The main components of an example SM are shown in Fig. 3. Along with the rating, the topology, i.e. FB, HB or other, defines much of the space requirement and layout. A fixed layout is simpler and more compact than a reconfigurable solution. Defining this topology and component rating is thus usually a first step. It is tempting to over-rate all components to create a very robust device; the disadvantage of this is that the converter will be unnecessarily large and expensive, and potentially exhibit non-linear behaviour caused by operating devices at well below the desired range.

It is worth considering sizing the printed circuit boards (PCBs) to an industry standard as this will make it easier to find compatible sub-racks and mounts. External interfaces will be required not only for the electrical output voltage (V_{SM}) and the control, but also for heat extraction (cooling) and external test and measurement. These must be accommodated within the dimensions of the unit. Voltage, current and potentially temperature must be measured, and their signals converted to a format usable by the control and monitoring system. Some of this may be local, though much of the system control will be external – the detailed choice of this will be determined by how accessible these signals need to be from an external source, how fast they need to be processed and the cost (complexity) of the telecommunications and telecommunications interfaces needed. All of these need

a power supply – this may need to be externally derived – for the systems with so many SMs this is such a significant issue that it will be dealt with separately (Section IV.D).

The degree of protection needed is also a design choice. Overvoltage protection is generally good practice. Fault bypass may be required depending on the system. Overcurrent protection is typically achieved by a feedback current sensing loop and local control, though a separate fuse may be desirable.

In detailed PCB and layout design, usual power electronic best practice should be followed. The gate driver should be placed as close as possible to the desired IGBT/MOSFET for best performance.Lead and track lengths should be kept short. Due to the capacitive nature of SMs, gate driver turn-on and turn-off circuits may require some tuning to avoid over-voltages and ringing at the output. Plenty of capacitive decoupling should be provided to local power supplies and ICs to reduce high frequency noise and with close attention being paid to return current paths on all PCBs to avoid excessive inductive loops and hence ringing. Similarly, logic circuits on SMs using a ground derived from the high voltage side of the board should be protected from ground bounce through decoupling. Ideally bootstrap drivers for SM switching should be avoided as there should be no restriction on duty cycle.

Fault finding (especially for Type D and E systems) needs to figure prominently in design. Test-points should be included on any PCB design to simplify debugging. This is not only important at the prototype stage, but also for repairs, or to find construction faults. If the design includes isolation on the board itself, close attention should be paid to which ground should be referred to. Basic techniques such as including indicator LEDs to clearly show when power supplies are connected and turned on throughout the converter are also very helpful for fault diagnosis.

2) SPECIFIC EXAMPLES

The approach to implementing a Type B system design taken by ICL [57], has SMs using no local control and a physical bypass switch between topologies, Fig. 4.

A single optical communication fibre is used for each half-bridge. For this design, to avoid shoot-through faults, the dead-time can be handled by an on-board chip (to reduce I/O lines). SM capacitor voltages are returned by means of either an analogue signal or as an encoded digital signal. At higher voltages, protection mechanisms such as a bypass thyristor and mechanical switch would be required across the SM electrical connection. To provide maximum control flexibility separate enable/disable control signals for each SM are recommended [58] and possibly for each sub-circuit in more complex SMs.

The University of Lille (UoL) Type B CMC prototype adopts separated boards for the SM power components and controls, as shown in Fig. 5 b and c. The controller utilises a secondary control board, where the 20 SMs of the same

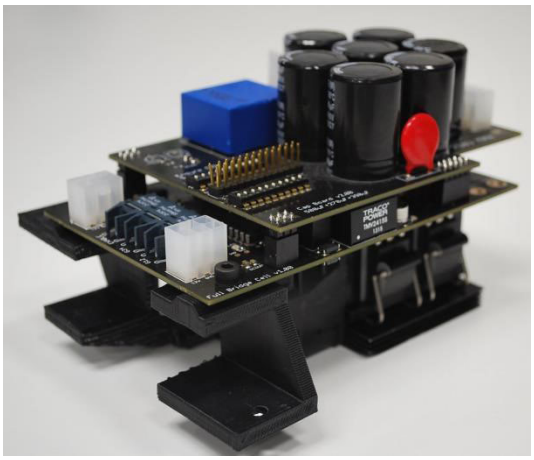


FIGURE 4. Imperial College London SM design [57].

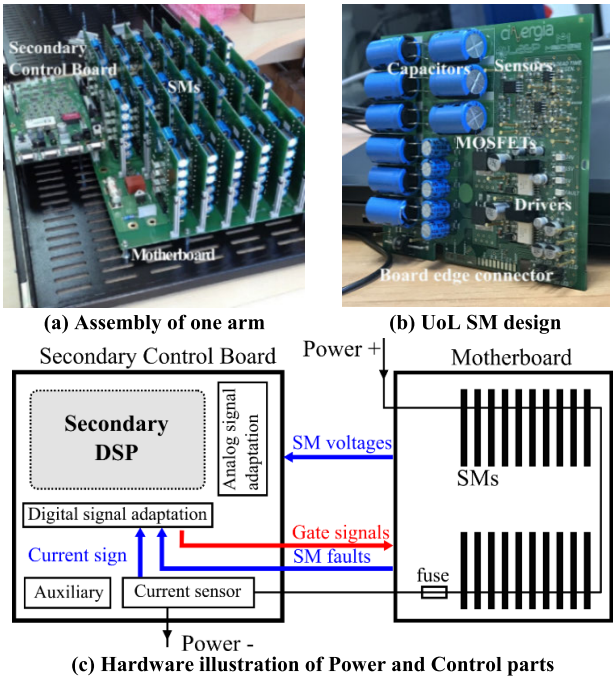


FIGURE 5. UoL System.

arm are vertically mounted to the motherboard (Fig. 5a) using board-to-board card edge power connectors.

The power flows through the motherboards to the accommodated SMs.

This design avoids excessive wire/cable connection and possible human error during maintenance. This is a good option for a larger number of SMs to be connected in the limited space. However, the cooling system needs to be placed at the tray edge due to the high density of switching elements. Each motherboard also accommodates overcurrent protection components like a fuse and a bypass thyristor. The power supply is provided externally and isolated using board mount DC/DC converters. Care must be taken regarding voltage representation of logic levels. Signal adaption circuits were housed in the secondary board as shown in Fig. 5c.

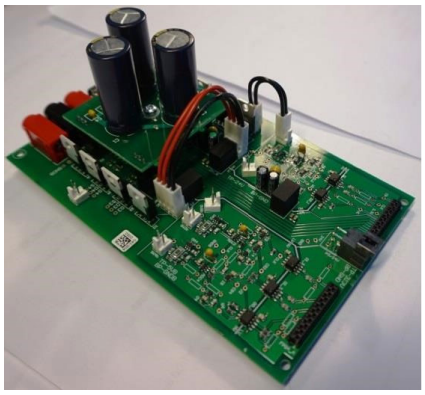


FIGURE 6. University of Manchester SM design [29].

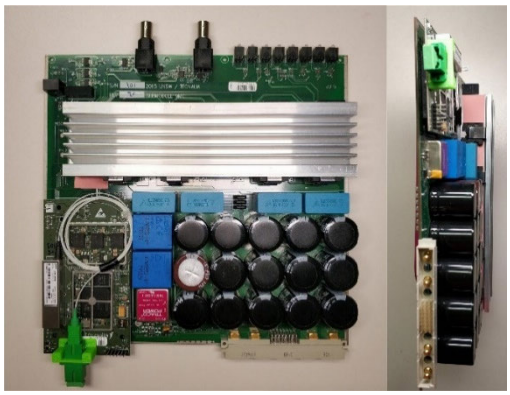


FIGURE 7. UNSW Sydney / Tecnalia SM design.

In the design step, additional digital signal processor (DSP) I/O and adaptation circuits were reserved for possible future development. Correspondingly, the external power supply and on-board DC/DC converters were over-rated.

The Type C design, as implemented in the UoM system, used an SM topology with limited reconfigurability: a physical bypass switch is used to select between HB and FB topologies, Fig. 6. The UoM system SMs are of standard Eurocard size (100 mm x 160 mm), ideal for mounting in a 19-inch server rack. Similar standardisation was undertaken in [35]. In contrast ICL designed compact PCBs and full custom mounting to enable small converter size (a key design limitation for the ICL implementation) but at the expense of considerable design effort.

In UoM's Type C design, secondary local control was used (the SM level Fig. 2a) and switching dead-time is handled by the secondary controller, mimicking industrial designs. This minimises telecommunications traffic and computational burden on higher level controllers.

An on-board analogue-to-digital converter (ADC) driven by the local controller is used for SM capacitor voltage measurement and space was left for additional filtering and measurement systems on the SM as required by the research aim. Ideally, each SM has an independent controller – however the UoM system used one controller for multiple SMs, partitioned in FPGA software to appear as independent units (apart from a common clock), due to research budget constraints.

The UoM SM uses back-to-back Zener diodes rated at just below the maximum voltage rating of the SM capacitors and power electronic switches to clamp the voltage at safe levels. In case of faults, and to ensure safe shutdown, a resistor is placed in parallel with the capacitor and Zener diodes to provide a discharge path.

UNSW's design, Fig. 7 [45], is based on the FB-SM with two legs in each SM which are controlled independently. This allows one arm to operate as a bipolar voltage source and enables DC-fault blocking capabilities for the system. A single connector is used for all power connections to simplify mounting of the SM to the rack. Each SM communicates to the central control board (CCB) through a single dedicated optical fibre cable. Two BNC connectors have been included in the front of each SMs, providing direct measurement of the SM capacitor voltage and the AC output voltage of each SM.

Individual control of the two half-bridges and a range of self-diagnostic and protection functions are performed in a low-power Xilinx Artix XC7A50T FPGA which is located in a separate mezzanine board. Such an approach, of course, comes at a higher cost and design complexity and also leads to a larger footprint per SM in the converter (for instance the UNSW SM size is 220 mm $\times$ 230 mm). However, it maximises the flexibility of the system and enables for simpler and faster troubleshooting.

The local controller provides diagnostics for the SM communication with the CCB, the status of the temperature sensor, the SM power supplies (each SM includes a 5 V and 24 V DC power supply) the ADC and the MOSFET drivers as well as temperature, overvoltage and under voltage alarms. All of these functions are also communicated to the CCB where they can be observed in the HMI as well as the front panel of the converter through LEDs.

In a Type D system, reconfigurable SMs with no local control and an electrical bypass switch between topologies may be beneficial. This allows for reconfiguration of the converter without having to touch the hardware for fast comparison work. Ideally the SM would include the option to separate the power electronics side of the board from the communications side, to allow the SMs to be replaced with a new topology without a complete SM redesign; reducing cost and development time.

D. POWER DISTRIBUTION AND ISOLATION

SMs in industrial scale converters are often rated at above or equal to 1.6 kV. Depending on the capacitor size, this equates to a stored energy of around 10 kJ per SM. This allows industrial converters to power SM control logic with power derived from the SM's DC link. Auxiliary systems on each SM are estimated to require 15 W of power, in this case only 0.003 % of the total energy stored is required per 20 ms cycle [4]. A maximum draw per cycle of 0.5 % of the total energy stored in a SM capacitor would enable auxiliary systems to harvest energy from the SMs without

significantly impacting converter behaviour (equivalent to a required DC voltage of 115 V per SM for the UoM system). The UoM system however has a nominal SM voltage of 25 V with a 3 mF capacitor, storing just less than 1 J. The auxiliary requirements are lower than an industrial converter, at approximately 5 W. However this represents a 10 % draw per cycle, which would significantly impact SM capacitor voltage ripple and subsequently whole-converter behaviour. Additionally, at least one step-down DC-DC voltage regulator will be required on each SM to provide a suitable auxiliary supply rail. SMs powered from their own DC capacitor will be uncontrollable when the converter is not charged and during turn-on cycles: appropriate mechanisms and charging procedures should be considered before proceeding down this route.

For systems with lower stored energy, or those that decide against the industrial design, an additional supply is required to power the auxiliary systems. As SMs are series connected at high voltage, the supply to each SM must be isolated and floating with respect to a reference point on the SM. Board-mount isolated DC-DC converters offer an ideal solution. The voltage and power requirements for these devices will be dependent on the specification chosen. SMs with centralized control will have fewer components in an SM and as such will typically require less power consumption. With an external supply, all auxiliary systems will be controllable prior to, and during, converter charging, enabling simplified turn-on procedures and safe operation during fault tests etc. The UoM, ICL, UoL and UNSW systems use external power supplies for auxiliary systems.

While self-powered SMs may be attractive from a cost and wiring perspective, the impact that this has on potential tests should be considered. For example if the converter was to be used to investigate a controller's response in the event of an SM failure, this would be difficult to emulate using a self-powered SM. The SM would not be capable of continuously bypassing itself (in the absence of bypass hardware), whereas an externally powered SM would.

E. ADDITIONAL COMPONENTS

A number of additional components, connectors and PCBs are required to physically connect together all the SMs, power supplies, measurement devices and control hardware, to produce a final test system, Fig. 8. This may vary somewhat from industrial systems, for example a DC-link capacitor may still be required to ease network stability issues with reduced-scale CMC prototypes, particularly during initial commissioning and testing. Partitioning of components into individual control cabinets (for larger designs), and layout within cabinets also needs careful design – access for measurement and replacement needs to be considered along with electrical functionality and cooling.

To ensure suitable isolation between the main controller hardware and power electronics, it is advisable to make use of fibre optic communication where possible. This will also considerably improve noise immunity for control signals

(a) At Imperial College London [57]

(b) University of Manchester

(c) University of New South Wales

FIGURE 8. Cascaded multilevel converter systems.

travelling in the converter. Any measurement systems should also have some form of shielding from electromagnetic interference (EMI) to ensure the accuracy of sensors. Where possible the use of differential probes and optical isolation is preferred for measurements in order to reduce the chance of damaging sensitive and expensive control equipment. Considerable thought should be given to ensure all the measurements required for appropriate system control are mapped out and catered for in advance i.e. arm currents, phase voltages, AC and DC network voltages and currents, SM capacitor voltages and any other control system-specific signals. Allowing space for subsequent modification of SM

boards should be considered, if possible, in keeping with their nature as research tools.

The interconnection of the different SMs also needs careful design. The range of wire-to-board connectors is vast, offering solutions for almost any conceivable application. It is important to ensure that any connectors used for the high voltage side are rated appropriately and have a solid electrical connection. Lead lengths should also be kept as short as possible to reduce inductance between SMs. At lower voltages it is reasonable to make use of quick connectors, such as banana jacks, to connect devices in the converter. A backplane can be used for connecting the SMs in order to minimize stray inductances and the use of cables. This can be very helpful in compact designs but adds to the cost of the system. It may also reduce its flexibility for future reconfigurations. To allow for controlled charging and discharging of the converter, resistors are often used in series with the input supply. These are typically paralleled with controllable circuit breakers to switch them out when the converter is charged. Separate circuit breakers in series with the resistors are required to isolate the converter.

Additional components such as switches and contactors, together with design modifications, enable reconfigurable converter design at the hardware level and a more flexible, multipurpose experimentation platform. For instance, UNSW's converter is built based on a "half-arm" design approach which allows one 8-SM arm to be split into two 4-SM arms by modifying a single selector switch when the converter is offline. In order to achieve such functionality, a number of additional components have been included. Specifically, one converter requires:

- Arm contractors: A contactor at each arm of the converter splits the first four SMs from the rest.
- AC-side contactors and AC-side terminals. These are normally closed in full converter operation and open when the system is split.
- DC-side contactors and DC-side terminals. As above, these are closed in full converter operation and open when the system is split.
- Additional pre-charging resistors. This allows the two DC systems to operate fully independently also during converter start-up.
- Split arm inductors. Instead of a single arm inductor, two inductors are used in each arm. Electrically these are located one adjacent to the DC-side terminal and the second next to the AC terminals.
- Two current sensors are included in the arm. These are located next to the arm inductors and in normal operation the second sensor is used as a backup to the main measurement.

V. CONTROLLER SELECTION AND SOFTWARE DEVELOPMENT

A. CENTRALIZED CONTROLLER ARCHITECTURE

The control and operation of a converter is handled by a device or set of devices which form the control architecture.

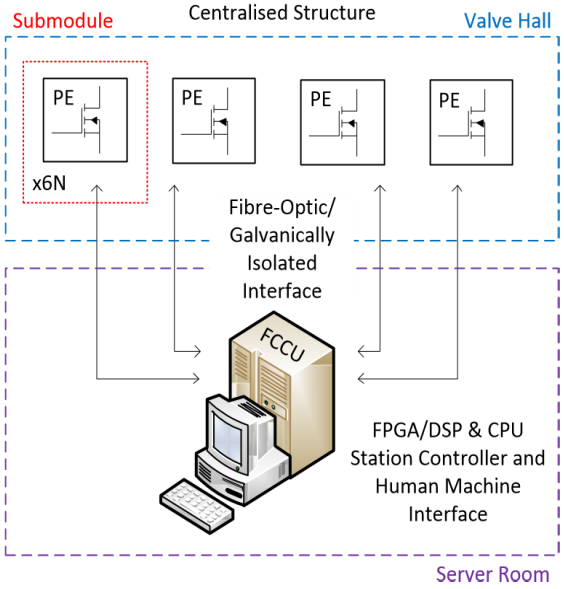


FIGURE 9. Example centralized control architecture. A similar configuration is used in the Imperial College London converter (adapted from [59]).

The simplest method of control is referred to as a centralized control structure where one powerful device is used to control the whole system. In the case of the ICL converter this is a real-time simulator from Opal-RT (OP5600), programmed using MATLAB/Simulink models, and formed of a CPU and an FPGA, as shown in Fig. 9.

A fully centralized control unit (FCCU) requires a large amount of analogue and digital I/O to communicate to the SMs and any auxiliary devices. Using an FCCU enables very fast control system prototyping and development and offers system omniscience for easy access to I/O data for research. The ability to perform rapid control prototyping on the FCCU has benefits for the evaluation of novel control algorithms. Having one centralized control system allows easier switching between testing new control schemes in simulation (with an electrical simulation model of the lab scale converter) and rapidly compiling the control system for testing on the physical lab scale converter. A new control scheme or converter configuration, or converter topology could be tested in a very short period of time given the flexibility provided by the FCCU. Due to the ease with which the entire control system can be reprogrammed and the accessibility to all signals monitored at all levels of the control system, the centralized control structure is characteristic of a typical implementation of Type B, D and E systems.

B. DISTRIBUTED CONTROLLER ARCHITECTURE

In an industrial scale CMC or in laboratory prototypes with many SMs, a distributed control architecture, Fig. 10, is typically more convenient since it features high expansion capability, flexibility and modularity. Consequently, it is relatively straightforward to update the system to make it capable of coping with different numbers of SMs.

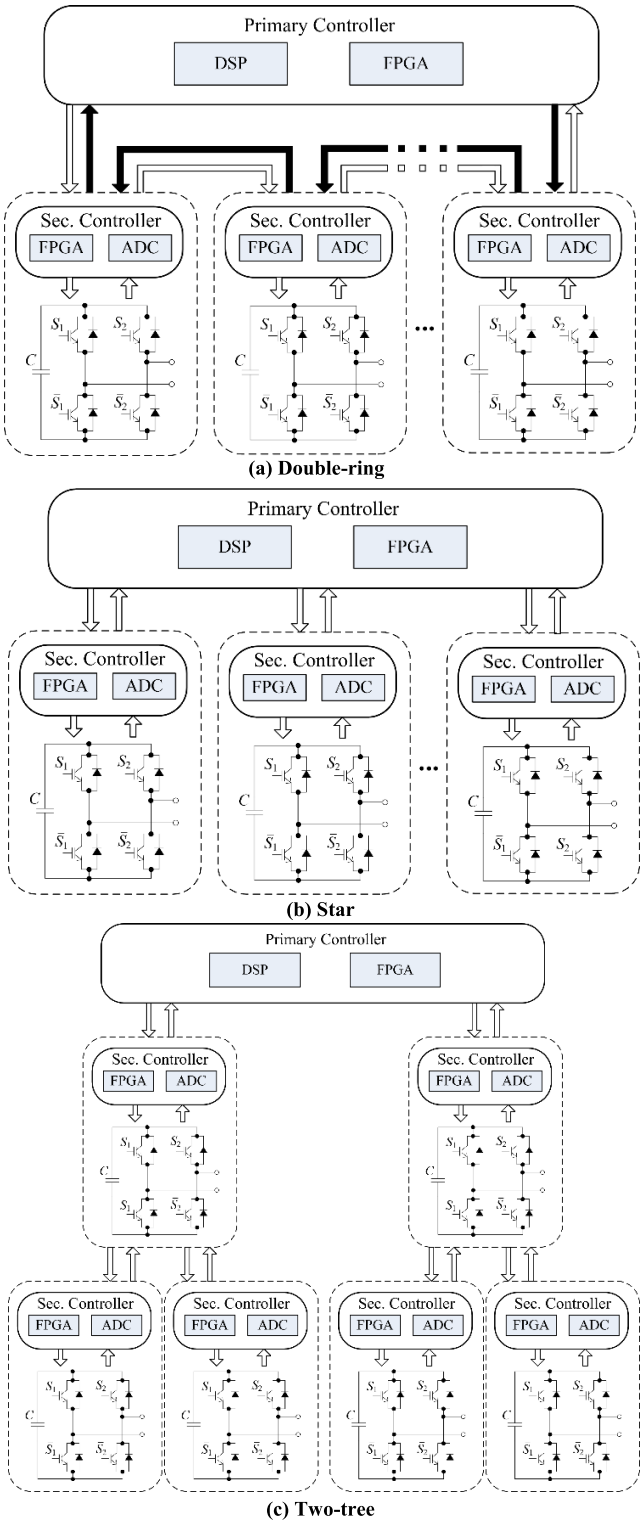


FIGURE 10. Example configurations of distributed control architecture topologies.

The required number of analogue and digital signals/fibre optic cables to control the system are reduced considerably, thus increasing the reliability of the system, enabling a clean design and simplifying the replacement of faulty SMs.

Several distributed control architectures for CMCs have been proposed and tested by universities, research centres and industrial companies. Among them, the most widespread ones make use of ring [38], [60]–[62] (Fig. 10a), star [63]–[66] (Fig. 10b) and tree [67] (Fig. 10c) network communication topologies. Despite the different communication embodiments, all of them share some common features. Generally, a central primary controller is comprised of a processor and FPGA that can be integrated making use of system-on-chip (SoC) technology for compactness. The distribution of tasks between the processor and the FPGA may vary from one implementation to another, but in general terms the processor implements the outer (DC-voltage, active and reactive power, rotational speed) and inner (current) control loops. The FPGA performs the SM voltage balancing and the calculation of the duty cycles of each SM. There are also multiple secondary local controllers that are related to each SM or to a group of several SMs. Local controllers usually comprise a local FPGA and ADC. They are usually in charge of digitalizing the analogue measurements and generate the PWM signals with the corresponding dead-times based on the duty cycles calculated by the central controller. Since the PWM is generated locally, no high bandwidth is required for the communications. Management of fault conditions and protection functions are distributed in both the local secondary and primary central controllers.

Different implementations based on open source real-time Ethernet, such as EtherCAT or PROFINET IRT have been proposed for the ring configuration. To endow the distributed controller with the required reliability a double-ring topology is usually the preferred option [38], [60], [61]. Equivalently, star network implementations using controller area network (CAN), serial communications, and passive optical networks (PON) have also been proposed in [63], [64] and [66] respectively.

Other communication network arrangements such as serial peripheral interface (SPI), EtherCAT driven daisy-chain networks or hybrid configurations mixing CAN with a high-speed bus are also used [25], [62], [68], but less frequently.

Overall, the distributed architecture demonstrates additional limitations and challenges in converter control but opens the opportunity for alternative control structures. However, the complexity means that a simple control system change may require program edits across many different pieces of control hardware, slowing down development considerably. Debugging across multiple devices can also be challenging. When designing a converter using such a control system, the incorporation of coded error signals is strongly advised to more easily identify faults.

C. IMPLEMENTATION EXAMPLES

Type C systems are designed to investigate industrially representative internal control and communication and therefore makes use of distributed control structures. In the case of the UoM converter, Fig. 11a, this includes a star topology

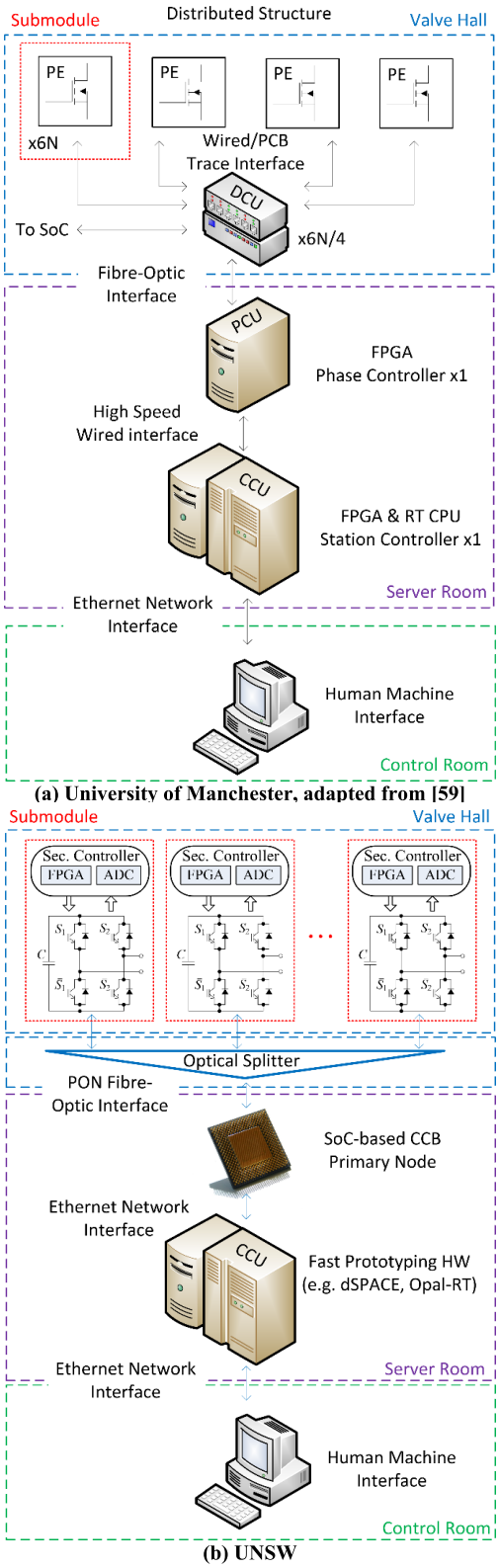


FIGURE 11. Example distributed control architecture.

with a real-time station controller comprising a CPU and an FPGA, an FPGA-based phase/arm controller and twelve further distributed local controllers (one for four SMs) which

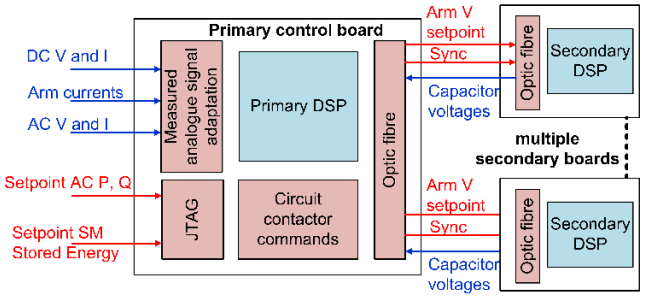


FIGURE 12. Example control system architecture.

use SoC technology formed of an Intel Cyclone V FPGA and an ARM processor.

In the case of the UNSW prototype, a star network topology as in Fig. 11b is used as well. The topology makes use of a PON that provides a point to multipoint communication architecture. It is comprised by a CCB with a Xilinx Zynq SoC as a primary node, and as many secondary nodes as SMs in the converter. The communication between the primary and the secondary nodes follows a point-to-multipoint approach provided through an optical splitter.

This architecture features the following technical characteristics:

- Synchronization accuracy between SMs in the ns range.
- High speed 2.4 Gbps downstream/1.2 Gbps upstream.
- Simple distribution network with passive components.
- High reliability. If one of the secondary nodes crashes the network is not affected.
- All the information send by the primary node is received simultaneously by all the secondary nodes.
- Provides local intelligence at SM level which facilitates the monitoring and feedback from each SM.

Additionally, it is possible to communicate between the CCB and real time fast prototyping hardware such as those supplied by dSPACE, Opal-RT, or National Instruments. The execution of the control algorithms can be split between the CCB and the real time hardware. This allows development of control algorithms using MATLAB/Simulink, which is very convenient for fast prototyping and testing of the developed controllers.

The UoL converter adopts a distributed control architecture made up of seven DSP TMS320F28377D: one primary (global) controller and six secondary (arm) controllers as shown in Fig. 12. The secondary DSP is responsible for regulating voltage balancing among SMs and arm level protection. As the test rig focuses more on the power and control system study, the secondary control, once validated, remains unchanged in most situations. An external JTAG emulator is not necessary from a cost perspective.

The primary DSP is responsible for global control targets, protections and interactions with the human interface. Its control system is changed more frequently. A JTAG emulator with Ethernet communications to host PC could significantly improve the test efficiency. The communication between

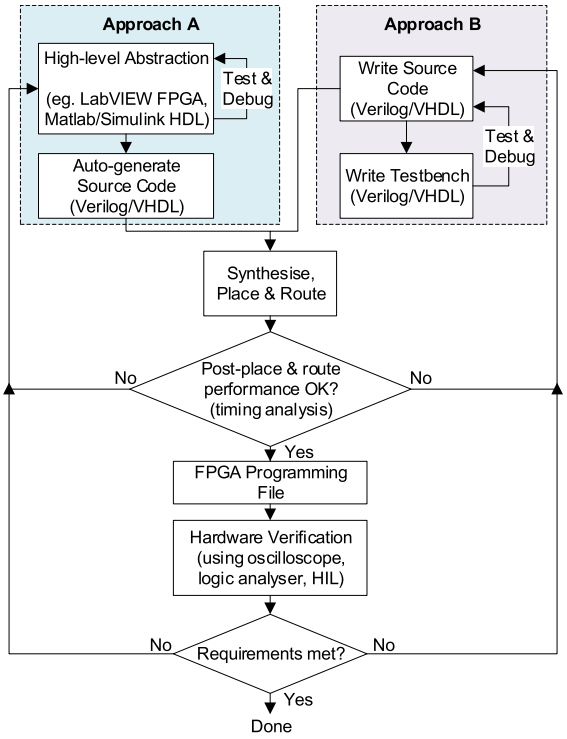


FIGURE 13. CMC control software development approaches.

DSPs is through a fibre optic connection. In the distributed architecture, synchronization of reference and measurement signals in different arm secondary controllers should be considered. In the UoL prototype an optimization process provided by the Texas Instruments Code Composer Studio environment has been applied to the three basic functions (i.e. sorting, limiting and regulating functions) of CBC based in each TMS320F28377D DSP secondary node. The global calculation time is around 5.8 μs, which allows the low-level control to be implemented on a secondary DSP, running properly, over a period of 10 μs.

D. CONTROL SOFTWARE DEVELOPMENT AND OPTIMISATION

Control software development for a CMC is a substantial task, due to the significant processing and I/O demands placed upon the control hardware. Although powerful FPGAs and DSPs are available which could comfortably run almost any desired control scheme with an excess of processing resources, such devices are often prohibitively expensive. As a result, control software development for a CMC is a trade-off between cost, performance (processing speed), resource utilisation (logic cells in the case of FPGAs, memory utilisation or required clock frequency in the case of a microcontroller/DSP), and implementation of the desired control method.

Two general approaches to control software development are possible, as shown in Fig. 13 for the FPGA development process, and are termed 'Approach A' and 'Approach B' respectively. Software development for microcontroller or DSP-based control hardware follows a similar process, apart from the generated source code (typically C language) and the test and debug workflow. When developing software for an FPGA, it is imperative that as much testing as possible is carried out at the design stage, since re-synthesis of code following changes is time-consuming, and debugging FPGA code whilst running is difficult. For microcontroller or DSP software development, re-compilation is quicker and debugging of a running system is easier, therefore test and debug is less front-loaded.

The chosen approach for control software development is dictated by the control architecture of the CMC, the control hardware, and the system study type (A to E). In a converter with a centralized control architecture using a commercial control platform, Approach A is typically the usual approach, such as in the Opal-RT system used in the ICL converter. In a converter with a distributed control architecture using control hardware from different vendors, both Approach A and Approach B may be used, such as in the UoM converter. A combination of Approach A and B on a single hardware platform is also possible by importing user-defined modules written using Approach B into the high-level block diagram.

Approach A facilitates easier translation of a control system design to a discrete time representation for implementation in hardware, and is well-suited to Type A, B, D and E studies. Conversion from continuous to discrete time and source code generation are typically automated, and require minimal user input. Furthermore, early stage debugging can also be carried out in the high-level environment which is familiar to the user.

Approach B has a steeper learning curve, as the user must first gain a detailed understanding of the hardware architecture and programming language to develop even relatively simple control software. Despite this, it is typically easier to enforce direct control over hardware and achieve deterministic timing using Approach B. This is advantageous when developing low-level control functions such as communication protocols and SM switch control. As a result, using Approach B is usually necessary for Type C studies.

Despite its apparent advantages, using Approach A without an understanding of the underlying hardware architecture often results in generation of inefficient code. This may lead to a system which does not meet the performance requirements, or which consumes more than the available FPGA resources. Areas for code optimisation when using Approach A include:

- Do not try to write (or simply transfer) conventional sequential code to FPGAs, which are inherently parallel. Use a finite state machine architecture to control program sequencing.
- Where possible, use low-level, architecture-specific constructs to implement functionality in a high-level block diagram. For example, in LabVIEW FPGA, use registers (fundamental FPGA memory elements) instead of local or global variables.

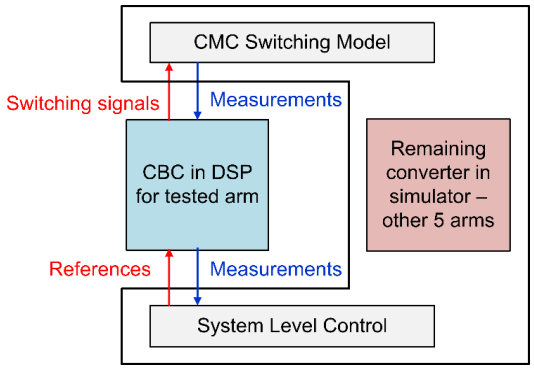


FIGURE 14. Real Time Simulation of CBC.

- Manually specify data types of variables to be the minimum width (number of bits) required to contain the maximum expected value.
- Reduce, or if possible eliminate use of floating-point arithmetic; use integer or fixed point arithmetic instead.
- Ensure that variables (registers) on an FPGA have only a single writer: multiple writers to a single register may cause the synthesis tool to implement resource-intensive arbitration logic.

As the level of optimisation is increased, a detailed understanding of the hardware architecture becomes necessary. As a result, the skills required for Approach A merge with those required for Approach B.

E. CONTROL SYSTEM VALIDATION

Validating the performance of any new control system or tuning before applying the control to the hardware converter is strongly recommended. For centralized Approach A control structures, this may be easiest in software simulation. For distributed control structures and Approach B developments, a simulation only approach may not be possible and the additional complexity of developing a HIL test bench, Fig. 14, may then be required. An initial step is partitioning systems so that they can be feasibly and effectively tested for functionality. In the UoL system, one external CBC among the six was employed as the real-world TMS320F28377D secondary DSP (blue area, left), which interacts with the simulated real-time system (red area, right), running on an OP5142 simulator from Opal-RT. The CMC simulated in the CPU within the OP5142 exchanges signals with the external DSP via a PCIe fibre optic I/O interface. The low-level control receives the reference signals and modulates the switching signals for each IGBT in the SM to balance the capacitor voltages. The results of 20 SM arm capacitor voltages are compared between full real time simulation [56] and HIL simulation. The number of activated SM can be investigated, as can the implemented balancing control algorithm.

The validation of a single arm typically would then be carried through a test protocol of the type shown in Fig. 15. The protocol is designed to operate one single arm in real-world operating modes: with and without power transfer across the arm [56]. This requires, in the red part (left), a source

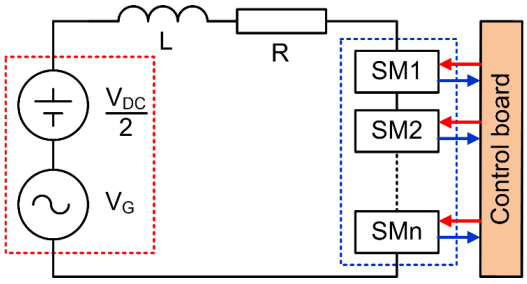


FIGURE 15. Protocol test for full arm validation.

capable of simulating a voltage wave comprising both AC and DC components, emulating the voltage waveform applied to the arm in real conditions. The R-L impedance between the arm and the voltage source corresponds to the arm inductor with its internal resistance. The main idea is to control the blue (right) and red (left) parts synchronously in order to be able to apply a phase shift between both voltage quantities. The current flowing in the R-L arm impedance is a consequence of this phase shift. Initial experimental tests involve fundamentals: displaying arm validation with a non-zero phase shift and therefore non-zero instantaneous arm power. Then a complete arm validation can be carried out based on both operation modes (i.e., with and without power transit in the arm).

VI. THREE-PHASE CMC IMPLEMENTATION AND VALIDATION

A. PROTOTYPE ARCHITECTURE

Even if all hardware is correctly prepared, the implementation of the control system on the test rig is not an easy task. A formalized procedure including start, stop and protection should be carefully designed. For these reasons, contactors and current limiting resistors are inserted in the circuit, typically managed by the primary controller. The use of a HIL test bench increases the equipment budget significantly. However, this is a much safer and more time-saving option than tests directly on the test rig – with consequent manpower time savings.

B. STARTING PROCEDURE OF CMC TEST RIG

Start-up procedures are typically converter-specific, and so as an example the distributed control UoL system will be used. The start-up sequence may be significantly different for other converter structures. The laboratory CMC prototype in UoL is connected to a 400 V DC source and the AC side is connected to a programmable AC power amplifier at 200 V. The nominal SM voltage is 20 V. As control systems are distributed in separated DSPs and the test rig in effect contains three different sources of power, the starting/stop of the test rig requires a formalised procedure that regulates the allowed actions in each step and corresponding controllers to be activated. The test rig starting process is shown in Fig. 16. All steps must be carried out in sequence. The latter command is unlocked only if the previous command executes correctly.

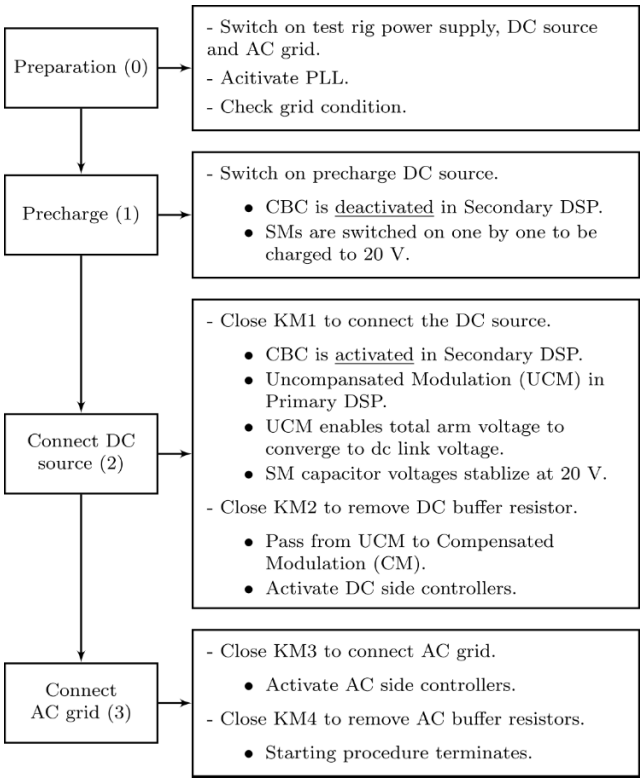


FIGURE 16. Example starting process of a test rig.

In the preparation step, good practice is to activate the phase-locked loop (PLL) as long as the primary DSP is debugged. This is intended to check if the control systems are correctly debugged and also to check the grid condition, in order to determine whether to proceed with the test.

In the pre-charge step, SMs are firstly charged by an external 20 V DC source in open loop. The secondary DSPs need to switch on the SMs one-by-one instead of using CBC. The capacitors do not need to be charged precisely to the nominal value. In practice, a difference always exists, but a big gap will induce an abrupt current flow at the moment of connecting the DC link. It is preferable to eliminate this gap through closed-loop control. For the UoL converter, the asymptotic stability provided by uncompensated modulation (UCM) [35] is used to converge the arm capacitor voltage to the DC link voltage. This is done in the third step, Fig. 16.

Once the pre-charge is terminated, the secondary DSP re-activates CBC to be prepared for connecting the DC-link source. Current limiting resistors are inserted in the arms to prevent surge currents from damaging expensive components. UCM is used to eliminate the gap between arm total capacitor voltage and the DC-link voltage. A CMC with UCM is asymptotically stable and arm voltages will converge to the DC-link voltage value [35]. The convergence time depends on the time constant of the buffer resistor and the total arm capacitor. Controllers for DC and AC sides are activated separately as shown in steps 2 and 3 in Fig 16.

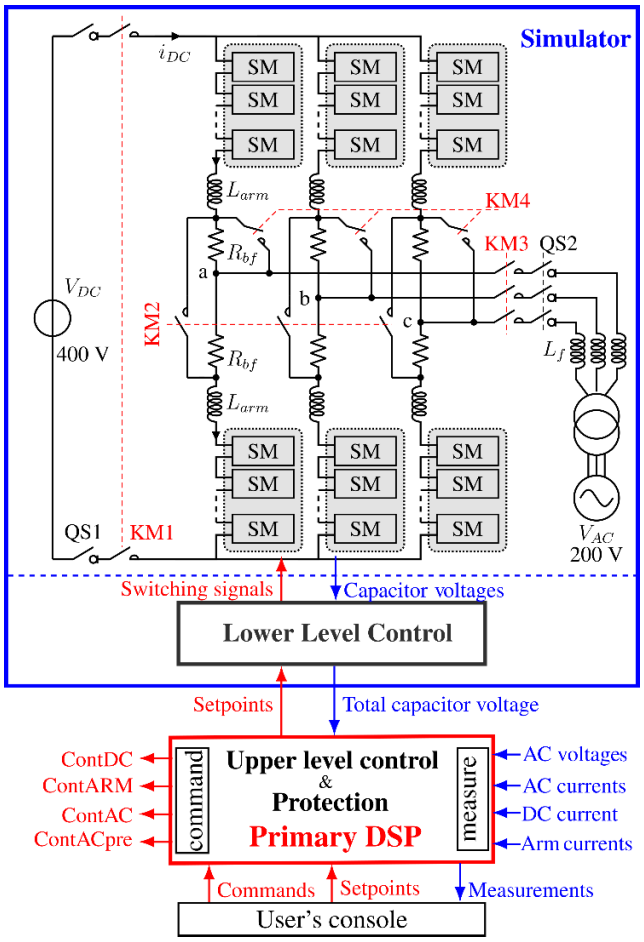


FIGURE 17. HIL simulation structure of the global controller in UoL test system.

C. HIL TEST BENCH AND EXPERIMENTAL TEST RIG

Since the test rig is typically designed for a variety of experiments, the global control will be frequently modified. It is helpful if this can be validated in HIL simulation before implementation on the test rig, e.g. Fig. 17. The CMC model and the arm level controls are emulated in the target OP5142 simulator. The global control is implemented in an external DSP.

The HIL simulation aims to replicate as precisely as possible the behaviour of the CMC test rig. In practice, it is challenging to achieve identical results, due to differences such as communication between equipment, inaccurate models of ICs and the limited accuracy with which auxiliary systems are represented. These elements do not significantly affect the main indices, such as steady-state and transient responses. For example, Fig. 18 shows the DC current responses of an active power step from 0 to 0.5 pu, obtained in the HIL test bench and the test rig.

The test bench further provides functionality for those tests which are too risky to be undertaken on the test rig:

- To simulate faults in any part of the system and verify the functionality of protection systems.

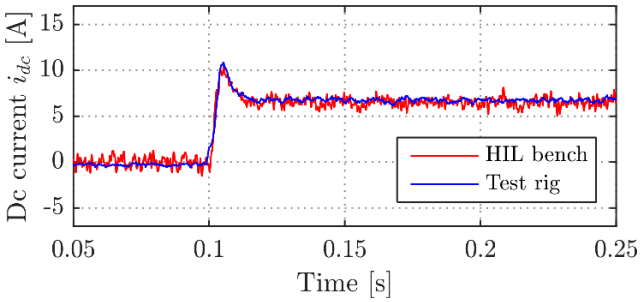


FIGURE 18. HIL simulation and test system response for a DC command step of UoL test system.

TABLE 3. Overview of design considerations when constructing a laboratory scale modular multilevel converter.

Element	Considerations
Study Type	Power systems, internal controls, future topologies, multi-terminal networks or fault and protection
	Combined or specialized
Hardware	Ease of reconfigurability between topologies
	Flexibility in design or purpose built
	Power and voltage rating
	Converter testing platform
	Auxiliary or SM derived power supply
	Number of SMs
	Mounting type and method
	Physical converter size
Control	Centralized or distributed structure
	Traditional or alternative control
	Observability of control signals
	Real-time data access or postprocessing
	Ease of control system redesign
	Ease of debugging
User Group	Hardware design complexity
	Technical expertise requirement
	Fool-proofing and system protection

- Change system parameters to test the robustness of control systems.
- Optimization of codes to minimize DSP calculation times.

VII. CONCLUSION

This paper has reviewed test-rig system layouts and discussed key sub-assembly design. The paper has also identified and addressed some of the key questions faced by ICL, UoM, UNSW and UoL during the design, development and testing process of the four constructed CMC systems. The justification for design decisions and some of the less obvious considerations have been presented and discussed in detail, enabling other organisations an easier path to designing and constructing their own CMC. Table 3 summarizes the key design considerations presented in this paper.

The PCB designs and control system programs for the converter designed and constructed at the UoM are freely available from [70]. A full description of the converter and the control hardware used is provided in [59] and in more detail in the thesis associated with the project [29]. For more detail on the converter designed and constructed by ICL see [57].

REFERENCES

[1] N. Macleod. *HVDC Innovation in Context*. WSP, National HVDC Centre website, Cumbernauld, U.K. Accessed: Jun. 8, 2020. [Online]. Available: https://www.hvdccentre.com/wp-content/uploads/2019/07/Operators_Forum_2019_MacLeod.pdf

[2] S. Renewables. (2020). *Delivering 40 GW of Offshore Wind in the UK by 2030—A High Level Roadmap*. Accessed: Jun. 8, 2020. [Online]. Available: https://sse.com/media/669511/Delivering-40GW-of-offshore-wind-by-2030.pdf

[3] M. M. Steurer, K. Schoder, O. Faruque, D. Soto, M. Bosworth, M. Sloderbeck, F. Bogdan, J. Hauer, M. Winkelnkemper, L. Schwager, and P. Blaszczyk, "Multifunctional megawatt-scale medium voltage DC test bed based on modular multilevel converter technology," *IEEE Trans. Transport. Electrific.*, vol. 2, no. 4, pp. 597–606, Dec. 2016, doi: 10.1109/TTE.2016.2582561.

[4] K. Sharifabadi, L. Harnefors, H. P. Nee, S. Norrga, and R. Teodorescu, *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. Hoboken, NJ, USA: Wiley, 2016.

[5] ABB. (2017). *HVDC Light—It's Time to Connect*. Accessed: Jan. 9, 2021. [Online]. Available: https://library.e.abb.com/public/285c256c03cd4e168eaae9834ad05c90/PRINTPOW0038%20R7%20HR.pdf

[6] Hitachi-ABB. (2020). *HVDC Light—The Original VSC Technology—Reference List*. Accessed: Jan. 9, 2021. [Online]. Available: https://search.abb.com/library/Download.aspx?DocumentID=POW0027&LanguageCode=en&DocumentPartId=&Action=Launch

[7] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, "VSC HVDC transmission with cascaded two-level converters," in *Proc. CIGRE Conf.*, Paris, France, 2010, pp. B4–B110. Accessed: Jan. 9, 2021. [Online]. Available: https://library.e.abb.com/public/422dcbc564d7a3e1c125781c00507e47/B4-110_2010%20-%20VSC-HVDC%20Transmission%20with%20Cascaded%20Two-level%20converters.pdf

[8] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf.*, Bologna, Italy, Jun. 2003, pp. 1–6.

[9] *HVDC/FACTS—Highlights Newsletter*, Siemens, Munich, Germany, 2010, vol. 10, no. 12. Accessed: Jan. 9, 2021. [Online]. Available: www.ptd.siemens.de/artikel1012_high.pdf

[10] D. R. Trainer, C. C. Davidson, C. D. M. Oates, N. M. MacLeod, D. R. Critchley, and R. W. Crookes, "A new hybrid voltage-sourced converter for HVDC power transmission," in *Proc. CIGRE Conf.*, Paris, France, 2010, pp. 1–12, Paper B4-11_2010.

[11] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, D. R. Critchley, and R. W. Crookes, "A new hybrid multi-level voltage-source converter with DC fault blocking capability," in *Proc. 9th IET Int. Conf. AC DC Power Transmiss. (ACDC)*, London, UK, 2010, pp. 1–5.

[12] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications," in *Proc. Int. Power Electron. Conf. (ECCE ASIA)*, Sapporo, Japan, Jun. 2010, pp. 502–507.

[13] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015, doi: 10.1109/TPEL.2014.2310127.

[14] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Trans. Power Del.*, vol. 30, no. 1, pp. 385–394, Feb. 2015, doi: 10.1109/TPWRD.2014.2351794.

[15] L. Huang, X. Yang, P. Xu, F. Zhang, X. Ma, T. Liu, X. Hao, and W. Liu, "The evolution and variation of sub-module topologies with DC-fault current clearing capability in MMC-HVDC," in *Proc. IEEE 3rd Int. Future Energy Electron. Conf. ECCE Asia (IFEEC-ECCE Asia)*, Kaohsiung, Taiwan, Jun. 2017, pp. 1938–1943.

[16] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, and F. Hassan, "The alternate arm converter: A new hybrid multilevel converter with DC-fault blocking capability," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 310–317, Feb. 2014, doi: 10.1109/TPWRD.2013.2282171.

[17] *Guide for the Development of Models for HVDC Converters in a HVDC Grid*, Cigré Working Group, Technol. Brochure, Dec. 2014.

[18] M. Barnes, D. Van Hertem, S. P. Teeuwsen, and M. Callavik, "HVDC systems in smart grids," *Proc. IEEE*, vol. 105, no. 11, pp. 2082–2098, Nov. 2017, doi: 10.1109/JPROC.2017.2672879.

[19] K. Eriksson. (2001). *HVDC Light and Development of Voltage Source Converters*. ABB, Zürich, Switzerland. [Online]. Available: https://library.e.abb.com/public/1f9325bfc027ca6dc1256fda004c8cbb/HVDC%20Light%20and%20development%20of%20VSC.pdf

[20] X. Xiang, M. M. C. Merlin, and T. C. Green, "Cost analysis and comparison of HVAC, LFAC and HVDC for offshore wind power connection," in *Proc. 12th IET Int. Conf. AC DC Power Transmiss. (ACDC)*, Beijing, China, May 2016, pp. 1–6.

[21] *Imperix*. [Online]. Accessed: Apr. 28, 2020. Available: https://imperix.ch/

[22] *Opal-RT—Worldwide Leadership in Modular Multilevel Converter Testing*. Accessed: Apr. 28, 2020. [Online]. Available: https://www.opal-rt.com/modular-multilevel-converter/

[23] W. Zhou, J. Sheng, H. Luo, W. Li, and X. He, "Detection and localization of submodule open-circuit failures for modular multilevel converters with single ring theorem," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3729–3739, Apr. 2019, doi: 10.1109/TPEL.2018.2849441.

[24] S. Lu, L. Yuan, K. Li, and Z. Zhao, "An improved phase-shifted carrier modulation scheme for a hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 81–97, Jan. 2017, doi: 10.1109/TPEL.2016.2532386.

[25] Y. Zhou, D. Jiang, P. Hu, J. Guo, Y. Liang, and Z. Lin, "A prototype of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3267–3278, Jul. 2014, doi: 10.1109/TPEL.2013.2278338.

[26] D. Vozikis, G. P. Adam, P. Rault, O. Despouys, D. Holliday, and S. J. Finney, "Enhanced modular multilevel converter with reduced number of cells and harmonic content," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2954–2965, Sep. 2020, doi: 10.1109/JESTPE.2019.2904205.

[27] D. Siemaszko, E. T. Louokdom, H. Parisod, J. Braun, S. Gavin, L. Eggenschwiler, P. Favre-Perrod, and M. Carpita, "Implementation and experimental set-up of a Modular Multilevel Converter in a Multi Terminal DC/AC transmission network," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, Karlsruhe, Germany, 2016, pp. 1–12.

[28] Q. Yang, M. Saeedifard, and M. A. Perez, "Sliding mode control of the modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 887–897, Feb. 2019, doi: 10.1109/TIE.2018.2818657.

[29] T. Heath, "Modular multilevel converter hardware and simulation comparison," Ph.D. dissertation, Dept. Elect. Eng. Electron., Univ. Manchester, Manchester, U.K., 2019.

[30] Z. Wang, H. Lin, Y. Ma, and T. Wang, "A prototype of modular multilevel converter with integrated battery energy storage," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Tampa, FL, USA, Mar. 2017, pp. 434–439.

[31] J.-H. Lee, J.-J. Jung, and S.-K. Sul, "Analysis and mitigation of AC coupling effects on overhead line of modular multilevel converter (MMC) based HVDC transmission system," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Cincinnati, OH, USA, Oct. 2017, pp. 97–104.

[32] D. Peftitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J.-K. Lim, M. Bakowski, L. Ängquist, and H. Nee, "High-power modular multilevel converters with SiC JFETs," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 28–36, Jan. 2012, doi: 10.1109/TPEL.2011.2155671.

[33] W. Yang, Q. Song, S. Xu, H. Rao, and W. Liu, "An MMC topology based on unidirectional current H-bridge submodule with active circulating current injection," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3870–3883, May 2018, doi: 10.1109/TPEL.2017.2722011.

[34] L. Dong, G. Lu, and K. Longze, "A design method of MMC-HVDC physical simulation system," in *Proc. IEEE Conf. Energy Internet Energy Syst. Integr. (EI2)*, Beijing, China, Nov. 2017, pp. 1–6.

[35] H. Zhang, M. M. Belhaouane, F. Colas, R. Kadri, F. Gruson, and X. Guillaud, "On comprehensive description and analysis of MMC control design: Simulation and experimental study," *IEEE Trans. Power Del.*, vol. 36, no. 1, pp. 244–253, Feb. 2021, doi: 10.1109/TPWRD.2020.2977470.

[36] J. Sheng, H. Yang, C. Li, M. Chen, W. Li, X. He, and X. Gu, "Active thermal control for hybrid modular multilevel converter under overmodulation operation," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4242–4255, Apr. 2020, doi: 10.1109/TPEL.2019.2936010.

[37] P. Ruffing. *MMC Test Bench*. RWTH Aachen University Website, Aachen, Germany. Accessed: Jun. 9, 2020. [Online]. Available: https://www.iaew.rwth-aachen.de/cms/IAEW/Forschung/Infrastruktur-Tools/~dqtqn/MMC-Test-Bench/lidx/1/

[38] R. Teodorescu, E. P. Eni, L. Mathe, and P. Rodriguez, "Modular multilevel converter control strategy with fault tolerance," in *Proc. Int. Conf. Renew. Energies Power Qual. (ICREPQ)*, Bilbao, Spain, 2013, pp. 772–777.

[39] F. Sasongko, K. Sekiguchi, K. Oguma, M. Hagiwara, and H. Akagi, "Theory and experiment on an optimal carrier frequency of a modular multilevel cascade converter with phase-shifted PWM," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3456–3471, May 2016, doi: 10.1109/TPEL.2015.2464694.

[40] X. Li, Q. Song, W. Liu, S. Xu, Z. Zhu, and X. Li, "Performance analysis and optimization of circulating current control for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 716–727, Feb. 2016, doi: 10.1109/TIE.2015.2480748.

[41] O. F. Jasim, F. J. Moreno, D. R. Trainer, R. Feldman, E. M. Farr, and J. C. Clare, "Hybrid experimental setup for alternate arm converter and modular multilevel converter," in *Proc. 13th IET Int. Conf. AC DC Power Transmiss. (ACDC)*, Manchester, U.K., 2017, pp. 1–6.

[42] S. Zhang, S. Wang, N. Praisuwanna, L. Kong, Y. Li, R. B. Martin, F. Wang, and L. M. Tolbert, "Development of a flexible modular multilevel converter test-bed," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Portland, OR, USA, Sep. 2018, pp. 5250–5257.

[43] M. M. C. Merlin, D. Soto-Sanchez, P. D. Judge, G. Chaffey, P. Clemow, T. C. Green, D. R. Trainer, and K. J. Dyke, "The extended overlap alternate arm converter: A voltage-source converter with DC fault ride-through capability and a compact design," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3898–3910, May 2018, doi: 10.1109/TPEL.2017.2723948.

[44] B. Li, D. Xu, D. Xu, and R. Yang, "Prototype design and experimental verification of modular multilevel converter based back-to-back system," in *Proc. IEEE 23rd Int. Symp. Ind. Electron. (ISIE)*, Istanbul, Turkey, Jun. 2014, pp. 626–630.

[45] G. Konstantinou, S. Ceballos, I. Gabiola, J. Pou, B. Karanayil, and V. G. Agelidis, "Flexible prototype of modular multilevel converters for experimental verification of DC transmission and multiterminal systems," in *Proc. Asian Conf. Energy, Power Transp. Electrific. (ACEPT)*, Singapore, Oct. 2017, pp. 1–6.

[46] M. Moranchel, F. M. Sanchez, E. J. Bueno, F. J. Rodriguez, and I. Sanz, "Six-level modular multilevel converter prototype with centralized hardware platform controller," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Yokohama, Japan, Nov. 2015, pp. 003863–003868.

[47] C.-H. Park, B. B. Negesse, J.-M. Kim, and C.-K. Kim, "Back-to-back 31 level modular multilevel converter with EtherCAT communication," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Sep. 2019, pp. 1032–1039.

[48] C. E. Ugalde-Loo *et al.*, "Lessons learnt from the BEST PATHS project for the integration of offshore wind power plants using multi-terminal HVDC grids modular multilevel converter control strategy with fault tolerance," in *Proc. CIGRE Conf.*, Paris, France, 2018, pp. 1–10, Paper B4-113_2018.

[49] A. Christe, E. Coulinge, and D. Dujic, "Insulation coordination for a modular multilevel converter prototype," in *Proc. 18th Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Karlsruhe, Germany, Sep. 2016, pp. 1–9.

[50] M. Glinka, "Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, Aachen, Germany, Jun. 2004, pp. 2572–2576.

[51] Y. Luo, Y. Li, Z. Li, P. Wang, C. Zhao, and Z. Sun, "Control and experiment of a modular multilevel converter-based HVDC transmission system," in *Proc. 17th Int. Conf. Electr. Mach. Syst. (ICEMS)*, Oct. 2014, pp. 2435–2439.

[52] A. J. Beddard, "Factors affecting the reliability of VSC-HVDC for the connection of offshore windfarms," Ph.D. dissertation, School Elect. Eng. Electron., Univ. Manchester, Manchester, U.K., 2014.

[53] R. Marquardt, A. Lesnicar, and J. Hildinger, "Modulares Stromrichterkonzept für Netzkupplungs-anwendung bei hohen Spannungen," ETG Fachtagung, Wuppertal, Germany, Tech. Rep., 2002.

[54] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011, doi: 10.1109/TPWRD.2011.2115258.

[55] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009, doi: 10.1109/TPEL.2009.2014236.
[56] T. Ould-Bachir, H. Saad, S. Dennetiere, and J. Mahseredjian, "CPU/FPGA-based real-time simulation of a two-terminal MMC-HVDC system," *IEEE Trans. Power Del.*, vol. 32, no. 2, pp. 647–655, Apr. 2017, doi: 10.1109/TPWRD.2015.2508381.
[57] P. Judge, "Power converter design for HVDC applications," Ph.D. dissertation, Dept. Elect. Electron. Eng., Imperial College London, London, U.K., 2016.
[58] M. M. C. Merlin, P. D. Judge, G. Chaffey, J. Wylie, and T. C. Green, "Soft-switching of the director switch in the alternate arm converter using blocked sub-modules," in *Proc. IEEE 18th Workshop Control Modeling Power Electron. (COMPEL)*, Stanford, CA, USA, Jul. 2017, pp. 1–7.
[59] T. Heath, P. R. Green, M. Barnes, and D. Kong, "Design, construction and testing of a modular multilevel converter with a distributed control architecture," in *Proc. 15th IET Int. Conf. AC DC Power Transmiss.*, Coventry, U.K., Feb. 2019, pp. 1–6.
[60] E. P. Eni, "Fault tolerant distributed control strategy for modular multilevel converter in HVDC applications," M.S. thesis, Dept. Energy Technol., Aalborg Univ., Aalborg, Denmark, 2013.
[61] C. L. Toh and L. E. Norum, "Implementation of high speed control network with fail-safe control and communication cable redundancy in modular multilevel converter," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Lille, France, Sep. 2013, pp. 1–10.
[62] S. Huang, "Distributed modulation and control of modular multilevel converter for HVDC application," M.S. thesis, Dept. Energy Technol., Aalborg Univ., Aalborg, Denmark, 2013.
[63] Y.-M. Park, H.-S. Ryu, H.-W. Lee, M.-G. Jung, and S.-H. Lee, "Design of a cascaded H-bridge multilevel inverter based on power electronics building blocks and control for high performance," *J. Power Electron.*, vol. 10, no. 3, pp. 262–269, May 2010, doi: 10.6113/JPE.2010.10.3.262.
[64] S.-Y. Lee, M.-H. Woo, J.-K. Kim, and S.-P. Ryu, "A novel method to improve output voltage quality of grid-connected cascaded H-bridge multilevel converter with phase-shifted PWM and serial bus communication," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Rayliegh, NC, USA, Sep. 2012, pp. 4513–4518.
[65] W. Liu, "Distributed modular controller architecture for high power converter applications," M.S. thesis, Graduate Fac., North Carolina State Univ., Raleigh, NC, USA, 2005.
[66] C. C. Davidson, A. C. Lancaster, A. J. Totterdell, and C. D. M. Oates, "A 24 MW level voltage source converter demonstrator to evaluate different converter topologies," in *Proc. CIGRE Conf.*, Paris, France, 2012, pp. 1–10, Paper B4-205_2012.
[67] B. Steinmann, G. Fernandez, and N. Cherix, "Tree-shaped networked control system for modular power converters with sub-μs latency and ns-scale synchronization accuracy," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Baltimore, MD, USA, Oct. 2019, pp. 6775–6782.
[68] S. Huang, R. Teodorescu, and L. Mathe, "Analysis of communication based distributed modulation and control of MMC for HVDC," in *Proc. Eur. Conf. Power Electron. Appl.*, Lille, France, 2013, pp. 1–10.
[69] F. Gruson, R. Kadri, F. Colas, X. Guillaud, P. Delarue, M. Bergé, S. Dennetiere, and T. O. Bachir, "Design, implementation and testing of a modular multilevel converter," *EPE J.*, vol. 27, no. 4, pp. 153–166, Dec. 2017, doi: 10.1080/09398368.2017/1417785.
[70] T. Heath, "Supplementary online repository for modular multilevel converter hardware and simulation comparison," 2019, doi: 10.17632/9sgpn5mdzs.1.

THEODOR HEATH received the B.Eng. degree in engineering and the Ph.D. degree from The University of Manchester, Manchester, U.K., in 2015 and 2019, respectively. This article forms part of continued output from his Ph.D. research. He is currently a Lecturer of Power and Energy with The University of Manchester.

MIKE BARNES (Senior Member, IEEE) received the B.Eng. degree in engineering and the Ph.D. degree from the University of Warwick, Warwick, U.K., in 1993 and 1998, respectively. He is currently a Professor with The University of Manchester (formerly University of Manchester Institute of Science and Technology), Manchester, U.K. His research interest includes power electronics applied to power systems. He is also a Fellow of the Institution of Engineering and Technology, U.K., and the Editor of the IEEE TRANSACTIONS ON ENERGY CONVERSION.

PAUL D. JUDGE (Member, IEEE) received the B.Eng. (Hons.) degree in electrical engineering from University College Dublin in 2012 and the Ph.D. degree from the Department of Electrical and Electronic Engineering, Imperial College London, in 2016, for which he received the Eryl Cadwaladr Davies prize for best doctoral thesis. Since May 2020, he has been a Lecturer of Power Electronics & Smart Grids, The University of Edinburgh. His research interests include power converter design and control, as well as power system integration aspects of renewable energy technology. He also received a Best Paper Award for his submission to the IEEE TRANSACTIONS ON POWER DELIVERY special issue on "Frontiers of DC Technology" in 2018.

GERAINT CHAFFEY received the M.Eng. degree in electrical and electronic engineering from Cardiff University, Cardiff, U.K., in 2012, and the Ph.D. degree from Imperial College London, London, U.K., in 2017. He is currently a Postdoctoral Researcher with KU Leuven/EnergyVille, Belgium, where his research interests include the design and demonstration of HVDC protection systems.

PHIL CLEMOW received the M.Eng. degree in electrical and electronic engineering and the Ph.D. degree in wind farm control from Imperial College London, in 2007 and 2011, respectively. His research interests include multilevel HVDC converters, distribution-level power electronics, and digital grids and electric vehicles.

TIM C. GREEN (Fellow, IEEE) received the B.Sc. (Eng.) degree (Hons.) from Imperial College London, U.K., in 1986, and the Ph.D. degree from Heriot-Watt University, Edinburgh, U.K., in 1990. He is currently a Professor of Electrical Power Engineering with Imperial College London, and the Co-Director of the Energy Futures Lab with a role of fostering interdisciplinary energy research across the university. His research uses the flexibility of power electronics to enable electricity networks to operate with very high fractions of low carbon technologies. In HVDC, he has contributed converter designs that strike improved trade-offs between power losses, physical size, and fault handling. In distribution systems, he has pioneered the use of soft open points. He has made important contribution to the study of stability of grid-connected inverters. He is also a Chartered Engineer in the U.K. and a Fellow of the Royal Academy of Engineering.

PETER R. GREEN (Member, IEEE) received the M.A. degree from Cambridge University, Cambridge, U.K., in 1988, and the M.Sc. degree from the University of Manchester Institute of Science and Technology (UMIST), Manchester, U.K., in 1990. He is currently a Professor with the University of Manchester (formerly UMIST). His research interests include the design and evaluation of wireless and network communication systems for deployment in harsh environments.

JAMES WYLIE received the B.Eng. degree in electrical and electronic engineering from the University of Northumbria, Newcastle, U.K., in 2014, and the Ph.D. degree from Imperial College London, U.K., in 2019. His research interests include the reliability of modular converters for high and medium voltage applications. He has recently taken a position with Eirgrid, Dublin, Ireland.

GEORGIOS KONSTANTINOU (Senior Member, IEEE) received the B.Eng. degree in electrical and computer engineering from the Aristotle University of Thessaloniki, Thessaloniki, Greece, in 2007, and the Ph.D. degree in electrical engineering from UNSW Sydney (The University of New South Wales), Australia, in 2012. He is currently a Senior Lecturer with the School of Electrical Engineering and Telecommunications with UNSW Sydney. His research interests include multilevel converters, power electronics in HVDC, renewable energy, and energy storage applications. He is also an Associate Editor of IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and *IET Power Electronics*.

SALVADOR CEBALLOS received the M.S. degree in physics from the University of Cantabria, Santander, Spain, in 2001, and the M.S. and Ph.D. degrees in electronic engineering from the University of the Basque Country, Bilbao, Spain, in 2002 and 2008, respectively. Since 2002, he has been with Tecnalia Research and Innovation, where he is currently a Principal Researcher with the Energy and Environment Division. His research interests include multilevel converters for high and medium voltage applications, fault-tolerant power electronic topologies, renewable energy systems, and power systems with high penetration of power converters.

JOSEP POU (Fellow, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Technical University of Catalonia (UPC)–Barcelona Tech, in 1989, 1996, and 2002, respectively. He is currently a Professor with Nanyang Technological University (NTU), Singapore, where he is currently a Program Director of Power Electronics with the Energy Research Institute, NTU (ERI@N) and the Co-Director of the Rolls-Royce at NTU Corporate Lab. His research interests include power electronics, renewable energy, energy storage, HVDC systems, and more-electrical aircraft and vessels. He received the 2018 IEEE Bimal Bose Award for Industrial Electronics Applications in Energy Systems. He is also an Associate Editor of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was the Co-Editor-in-Chief and an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.

MOHAMED MOEZ BELHAOUANE received the master's degree in automatic control from the Higher School of Science and Technology of Tunisia, in 2005, and the Ph.D. degree in electrical engineering from the Polytechnic School of Tunisia, in 2011. He is currently a Senior Research Engineer with the Laboratory of Electrical Engineering and Power Electronics (L2EP Laboratory), Centrale Lille, France. His research interests include the modeling and control design based on the integration of high voltage power electronic converters, such as VSC and MMC, in HVDC transmission systems. In addition, his research interests also include the implementation of advanced control strategies using Hardware in the Loop (HIL) and Power Hardware in the Loop (PHIL) concepts based on small-scale multi-terminal DC mock-up.

HAIBO ZHANG received the Ph.D. degree in electrical engineering from the Université des Sciences et Technologies de Lille, France, in 2017. He has been a Research Engineer with the Laboratoire d'Electrotechnique et d'Electronique de Puissance of Lille (L2EP), France, since 2018. His research interests include modelling and control of power electronic converters in transmission systems and hardware-in-the loop simulation.

XAVIER GUILLAUD (Member, IEEE) received the Ph.D. degree from the University of Lille, in 1992. He joined the Laboratory of Electrical Engineering and Power Electronic (L2EP) in 1993. He has been a Professor with the Ecole Centrale of Lille since 2002. His research interests include the integration of high voltage power electronic converters in the transmission system. He is involved on several projects about power electronic on the grid within European projects and a large number of projects with French electrical utilities.

JACK ANDREWS received the B.Eng. degree in engineering from The University of Manchester, Manchester, U.K., in 2018, where he is currently pursuing the Ph.D. degree. His research interests include computational and communication architectures for HVDC MMC construction, with a particular focus upon modelling and compensating for control loop delays caused by real-world control and communication hardware.