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Silicon Near-Infrared Sensor Using Trench Photodiode Array

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ABSTRACT In this paper, we report a method of increasing the sensitivity of a silicon near-infrared sensor. The sensor is realized by forming multiple trench-type photodiodes in a silicon chip. The trench photodiodes can be formed using conventional semiconductor fabrication equipment. The device structure allows the depletion layer to be spread over the entire sensor chip even at a bias voltage of 10 V or less. The sensor chip can thereby extend the collection area of photoelectrons to the maximum. At a chip thickness of 540 μm, the conversion efficiency for near-infrared wavelengths between 940 and 1020 nm is more than 80% at room temperature. In addition, the electrical characteristics and response performance of the fabricated 2.4 mm $\times$ 2.4 mm test chips are reported. Since the proposed method can achieve a high conversion efficiency at low voltage without cooling in silicon semiconductors, it is expected to provide a low-cost and compact solution for various near-infrared receiver devices such as these for Internet of Things (IoT) applications.

INDEX TERMS Optical sensors, optical detectors, infrared sensors, photodiodes, silicon, trench.

I. INTRODUCTION

There are various objects and information scattered throughout in our living environment. In the future, various devices will be able to automatically acquire the information necessary to improve safety and comfort, thanks to the development of Internet of Things (IoT) technology. Various optical sensors are being studied to detect various types of information scattered in real space for this advancement [1]–[7]. Future IoT sensors will be embedded in various things, and thus their miniaturization and ease of use are essential.

IoT interface technologies that use radio waves, such as Wi-Fi [8], [9] with a communication distance of 50–100 m and 11 Mbps to 9.6 Gbps (bits per second), and Bluetooth [10], [11] for short-distance communication of several meters with 3–24 Mbps at 1/100th the power consumption of Wi-Fi are currently in widespread use. Near-infrared wavelengths of 850–900 nm have also become widespread, such as IrDA [12], [13] with communication distances of several meters at 16 M–1 Gbps. Such optical communication methods can easily achieve high directivity and are effective in identifying communication targets, preventing signal interference, and saving energy. To take advantage of their effectiveness and expand their applications, there is a need to develop highly sensitive and low-cost near-infrared sensing devices.

For example, when an optical sensor is used as an IoT interface for transportation infrastructure, it is necessary to guarantee stable operation under all outdoor environments. Its operating temperature should be relatively high, and its wavelength is also limited by various natural phenomena. Moreover, it must be compact and inexpensive and easy to use to make it popular. Regarding the wavelengths of the light used for communication, the wavelengths of IrDA signals (850–950 nm) and night vision camera illumination (750–850 nm), 1400 nm and 1900 nm absorbed by H_2O, and less than 240nm absorbed by O_2 must be avoided in order to prevent interference with existing light. Near-infrared light at the wavelength of about 1 μm is the most effective, considering high-temperature heating elements such as car mufflers ($<$ 300 °C) and sunlight. As for the operating temperature, existing semiconductor sensors such as InGaAs have relatively large absorption coefficients and thus have relatively high sensitivity to light of a wavelength of 1 μm even with a thin depletion layer. However, because the band gap energy is relatively low (approximately 0.7 eV), they cannot provide a sufficient signal-to-noise ratio at high temperatures, and cooling is required. Moreover, the production cost of the

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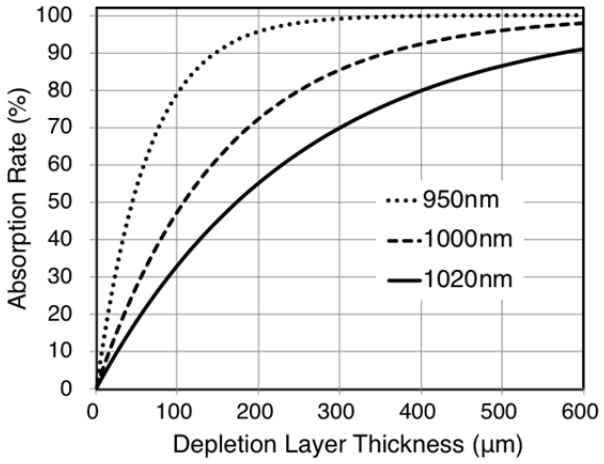

FIGURE 1. Absorption rate of near-infrared light as a function of depletion layer thickness of silicon.

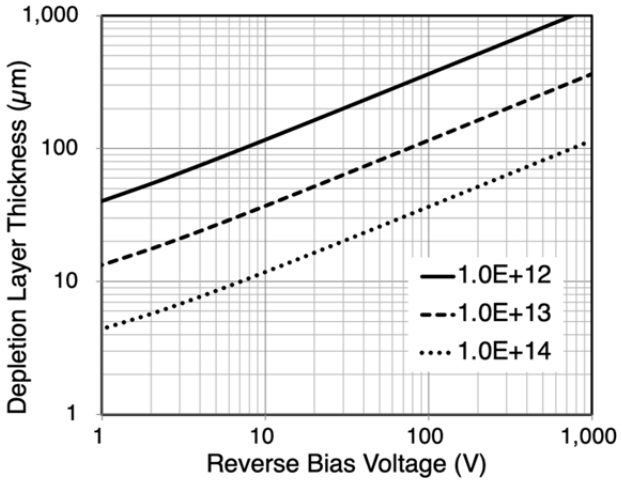

FIGURE 2. Depletion layer thickness of silicon as a function of reverse bias voltage.

substrate is high [14], [15]. On the other hand, the bandgap energy of Si is about 1.12 eV and does not require cooling. Si diodes have already been widely used as photon detectors in the spectral range below 1.1 μm, and they can operate at high temperatures and achieve high signal-to-noise performance and fast response time. In particular, Si devices are also the cheapest microelectronic technology [16]. However, the disadvantage of Si is that its near-infrared penetration depth is greater than that of other materials. To absorb more than 90% of 1 μm near-infrared light, the depletion layer thickness must be about 400 μm (Fig. 1). This requires a high bias voltage of 100 V for a 15kΩcm substrate with an impurity concentration of 1E+12 cm^{-3} and 1,000 V for a 1.5 kΩcm substrate with an impurity concentration of 1E+13 cm^{-3} (Fig. 2). In addition, the response performance of the sensor must be able to communicate with traffic lights, road signs, and other vehicles at a distance of several hundred meters and at a data rate of about 10 Mbps, which is capable of communicating 100 kbit data in 10 ms (moving 28 cm at 100 km/h). Given these limitations, we propose a near-infrared sensor optimized for 1 μm wavelength using a silicon semiconductor with excellent temperature characteristics and low manufacturing cost to solve the problem.

In a related work, a method of increasing the light absorption rate by doubling the optical path length in silicon through reflection, scattering, or diffraction mechanisms on the silicon surface has been reported [17]–[19]. Even with these structures, a depletion layer thickness of about 250 μm is necessary to absorb 95% of 1 μm near-infrared light. Therefore, a high bias voltage of about 40 V is required for a substrate with an impurity concentration of 1E+12 cm^{-3} or an intrinsic semiconductor substrate at about 100°C and about 400 V for a substrate with an impurity concentration of 1E+13 cm^{-3}. A method of making the depletion layer as thick as a chip by injecting light into the side of the chip has also been reported [20], [21]. However, since the aperture size is limited by the depletion layer width, it is necessary to stack multiple chips to increase the photosensitive area. Trench-based photosensors have also been reported: a p-i-n photodetector with a 7-μm-deep trench electrode on a 11–16 Ωcm p-type silicon substrate has been reported [22]. However, it has a shallow trench depth of 7 μm, which results in a depletion layer thickness of about 20 μm and a low 1 μm near-infrared absorption rate of at most 12%. In our previous work, we developed a high-sensitivity silicon X-ray sensor with a method of exposing X-rays from the side of the chip on which the trench photodiode is formed [23]–[27].

This work reveals that by optimizing its trench photodiode array structure for near-infrared wavelengths of 1 μm, a depletion layer as thick as the chip (about 500 μm) with a low bias voltage of less than 10 V is formed and a high optical absorption rate even for 1 μm near-infrared light is achieved.

II. OPTICAL SENSOR WITH TRENCH PHOTODIODE ARRAY STRUCTURE

The photosensitivity of a semiconductor optical sensor is determined by its depletion layer thickness and its absorption coefficient for the incident light. The intensity I of the light transmitted through the material can be expressed using (1) from the Beer–Lambert law [28].

$$I = I_0 e^{\alpha x} \tag{1}$$

Here, Io is the intensity of the incident light, α is the absorption coefficient, which varies with the material and its wavelength and temperature, and x is the distance the light passes through the material. Fig. 1 shows the optical absorption rate for the depletion layer thickness of the silicon optical sensor based on the absorption coefficient at 300 K in silicon [29]. To absorb 80% near-infrared light of 1 μm wavelength in silicon semiconductors, a depletion layer thickness of about 400 μm is required. The depletion layer thickness W can be expressed in (2) by its reverse bias voltage V_R and two types of impurity concentration (N_A and N_D), and if their impurity concentrations differ markedly, it can be approximated by (3)

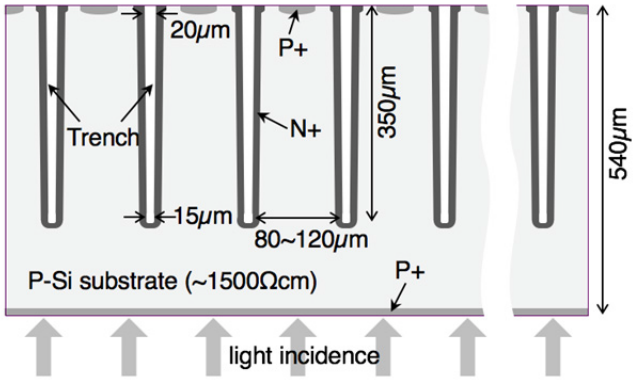

FIGURE 3. Cross-sectional structure of a trench PD array chip. Light is received on the back of the chip (bottom in the figure).

using the smaller impurity concentration $N = \text{Min}\,(N_A, N_D)$ [30].

$$W = \sqrt{\frac{2K_s\varepsilon_0(\emptyset_B + V_R)(N_A + N_D)}{qN_{AN_D}}} \tag{2}$$

$$W \approx \sqrt{\frac{2K_s\varepsilon_0(\emptyset_B + V_R)}{qN}} \tag{3}$$

Here, K_s is the dielectric constant of silicon, ε_0 is the dielectric constant of free space, φ_B is the built-in voltage, q is the electron charge, N_A is the impurity concentration of the p-type semiconductor, and N_D is the impurity concentration of the n-type semiconductor.

Fig. 2 shows the depletion layer thickness versus reverse bias voltage in a silicon semiconductor pn junction diode calculated using (3). For example, by the floating zone (FZ) method [31], a high-resistivity doped silicon wafer with a low impurity concentration of about 1×10^{13} cm^{-3} can be manufactured. When electrodes are placed on the front and back of a sensor chip made from the wafer, a high voltage of more than 1.000 V is required to form a 400 μm depletion layer. This usage condition strongly limits its cost and application.

Therefore, we propose a sensor device structure in which a large number of trench photodiodes are formed in a silicon substrate at appropriate intervals. With the proposed structure, a near-infrared sensor with high conversion efficiency is realized even when the bias voltage is less than 10 V.

A. SENSOR CHIP STRUCTURE

The cross-sectional structure of the proposed trench photodiode (PD) array chip is shown in Fig. 3. A number of trenches with a depth of 350 μm are formed in a silicon semiconductor substrate with intervals of 80 to 120 μm, and pn junction diodes are formed on the sides and bottom of the trenches. The n+ regions were formed by thermal diffusion from the deposited PSG (phosphosilicate glass) films, and the p+ regions were formed by boron ion implantation. The PD arrays are formed by the Bosch process using deep reactive ion etching (Deep RIE) [32]–[34]. Its trench width is 20 μm at the top of the chip and 15 μm at its bottom, and its silicon substrate thickness is 540 μm. In this experiment, three test chips with 80, 100, and 120 μm PD spacings were prepared and their characteristics were compared. The incidence of light is on the back of the chip (lower side in Fig. 3). The two electrodes of the sensor are connected in parallel to the anode and cathode of all the PDs in the sensor chip by aluminum film wiring on the surface of the chip. These test chips did not have electrodes on the back of the chip.

B. TEST CHIP

Although the proposed device structure has the advantage that all trench photodiodes can be formed at once, the anode electrodes formed on the chip surface and the cathode electrodes formed along the trench walls are not facing each other in parallel. This structure causes the depletion layer and electric field in that diode to vary depending on the trench spacing. In addition, the volume of the trench cavity in the nonabsorbing region changes because the number of PDs installed changes with the trench spacing. Therefore, to evaluate the effects of these differences on the conversion efficiency, we fabricated three types of test chip with different trench photodiode spacings.

Fig. 4 shows the micrographs of the three test chips manufactured for performance verification. The FZ silicon wafers used in their fabrication are p-type substrates with a resistivity of about 1,500 Ωcm and a wafer thickness of 550 μm. The size of the test chips is 2.4 mm × 2.4 mm, and the size of the PD trench in each chip is 20 μm wide and 100 μm long. The chip shown in (a) has 80 μm spacing between the PDs and has 200 PDs arranged in an array of 20 columns and 10 rows. The chip in (b) has a PD spacing of 100 μm, and 153 PDs are arranged in an array of 17 columns and 9 rows. The chip in (c) has 120 μm spacing between the PDs, and 120 PDs are arranged in an array of 15 columns and 8 rows. Fig. 5 shows a micrograph of a test chip cross section with a PD spacing of 80 μm. Each boxed area in Fig. 5 also shows a high-magnification micrograph.

III. PERFORMANCE EVALUATION USING TEST CHIPS

The three test chips shown in Fig. 4 were used to evaluate the electrical characteristics, sensitivity, and response performance. To measure the sensitivity (conversion efficiency) and response performance, three types of near-infrared LED were used as light sources. A single LED was placed 20 cm away from the test chip, and each of them was characterized on the basis of the pulse modulation of the LED voltage. The three LEDs used were OSA Opto OCI-440-1020 with a center wavelength of 1020 nm, OSRAM Opto Semiconductors SFH4544 with a center wavelength of 940 nm, and USHIO Opto Semiconductors L810-01AU with a center wavelength of 810 nm. Each was measured at room temperature.

A. ELECTRICAL CHARACTERISTICS

Fig. 6 shows the current characteristics for each test chip with respect to the bias voltage. At a bias voltage of − 10 V, the

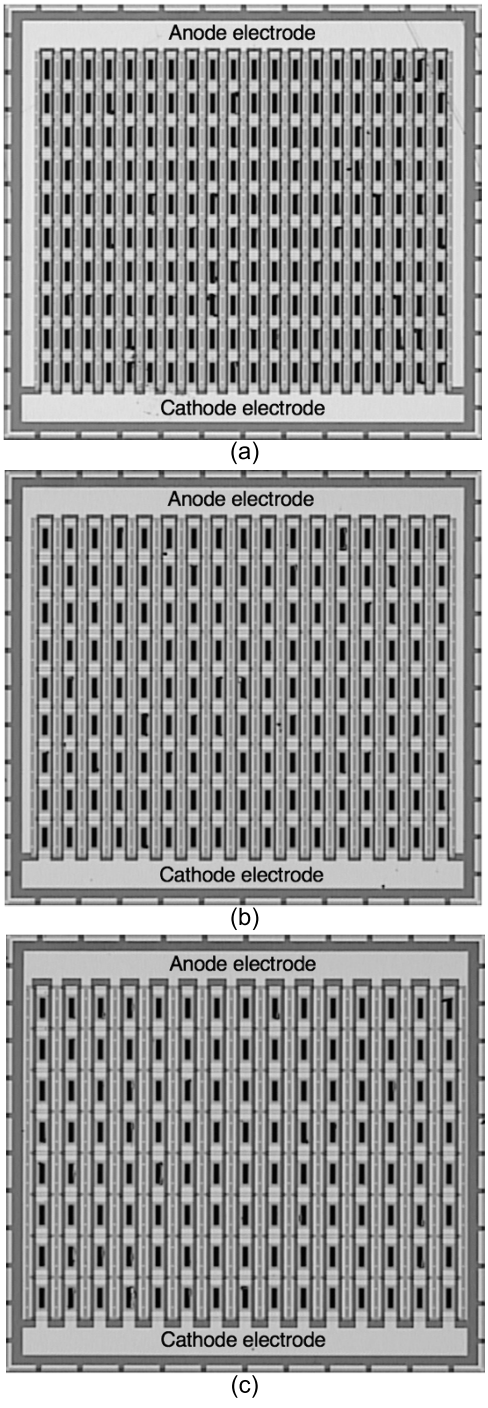

FIGURE 4. Micrographs of the trench PD array chips. (a), (b) and (c) are test chips with PD spacings of 80, 100, and 120 μm, respectively.

leakage current is 6 nA for a test chip with a PD spacing of 80 μm, 5 nA for a test chip with a spacing of 100 μm, and 4 nA for a test chip with a spacing of 120 μm. However, as the voltage is increased, the leakage current increases to 180, 150, and 110 nA at $-$ 20 V respectively. These characteristics seem to be reasonable since the smaller the PD spacing, the lower the voltage at which the whole area is depletion-layered.

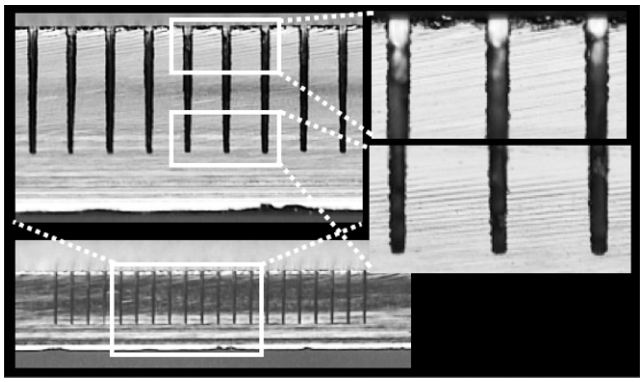

FIGURE 5. Micrograph of a trench PD array chip cross section with a PD spacing of 80 μm. Enlargements of the framed areas are shown.

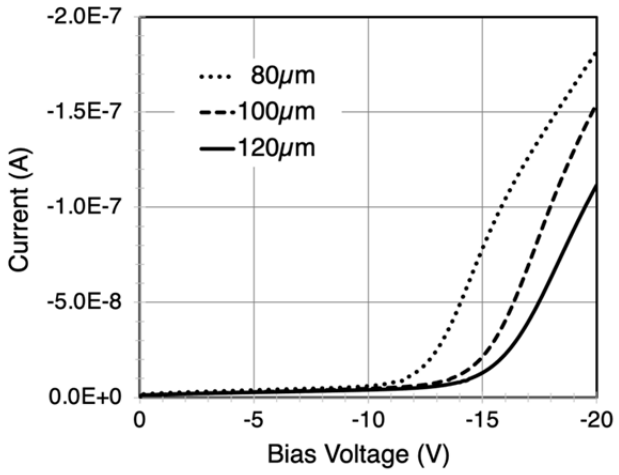

FIGURE 6. Current as a function of bias voltage in a trench PD array chip (the PD spacings of the test chips used for the measurements were 120, 100, and 80 μm).

Fig. 7 shows the capacitance of each test chip with respect to the bias voltage. At a bias voltage of $-$ 10 V, the capacitance is 29 pF for the test chip with a PD spacing of 80 μm, 25 pF with a spacing of 100 μm, and 21 pF with a spacing of 120 μm.

B. SENSITIVITY CHARACTERISTICS

In the test chip used for the measurement, the entire chip was used as the active area of the sensor. The area of the back, which is the light input surface, is 2.4 mm $\times$ 2.4 mm. In this measurement, we observed the sensor current of each LED used as the near-infrared light source when it was emitting and not emitting light and used the difference between these values as the photocurrent. To prevent unnecessary temperature rise of the light source LEDs and the sensor device, the LEDs were intermittently emitted with periodic pulse signals. The light emission ratio to the period is 30%, the light emission time is 30 ms, and the period is 100 ms. The standard deviation of the noise amplitude to the signal amplitude was about 0.1 to 0.5%.

Fig. 8 shows the measurement results of the conversion efficiency for near-infrared light in a test chip with a PD

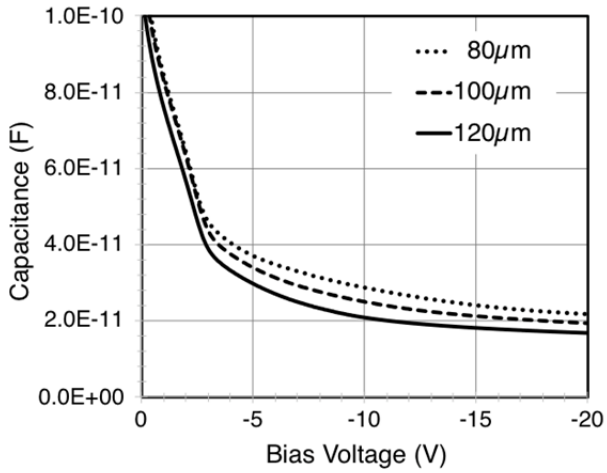

FIGURE 7. Capacitance as a function of bias voltage in a trench PD array chip (PD intervals were 120, 100, and 80μm for the test chips used for measurement).

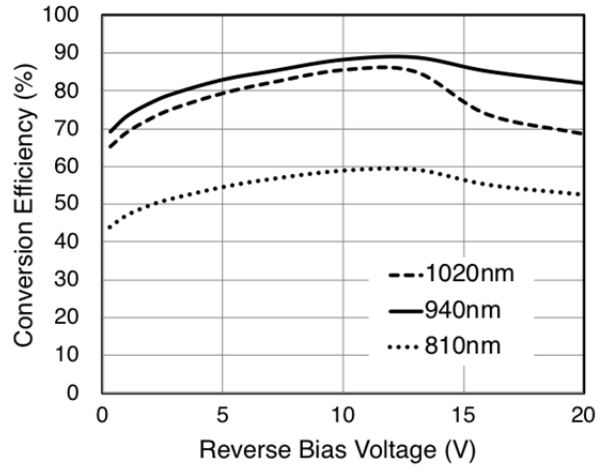

FIGURE 8. Conversion efficiency of near-infrared light as a function of bias voltage in a trench PD array chip with 120 μm PD spacing (the central wavelengths of the light used for the measurements were 1020, 940, and 810 nm).

spacing of 120 μm. The conversion efficiency of the PD to the bias voltage was measured for the center wavelengths of 1020, 940, and 810 nm. The forward current of each LED was set to 100 mA, 20 mA, and 20 mA, respectively, which corresponds to 20% of the maximum rating of each LED. When the bias voltage is − 10 V, the conversion efficiencies are 85% (0.49 A/W for photosensitivity) at 1020 nm, 88% (0.50 A/W) at 940nm, and 59% (0.34 A/W) at 810 nm. At the bias voltage of − 5 V, the conversion efficiencies are 79% (0.45 A/W) at 1020 nm, 83% (0.47 A/W) at 940 nm, and 55% (0.31 A/W) at 810 nm. At the bias voltage of − 0.3V, the values are 65% (0.37 A/W) at 1020 nm, 69% (0.40 A/W) at 940 nm, and 44% (0.25 A/W) at 810 nm. At bias voltages above − 12 V, the leakage current of the PD tends to increase and its conversion efficiency decreases. This phenomenon may be caused by the recombination of the photoelectrons with the minority carriers generated in the depletion layer.

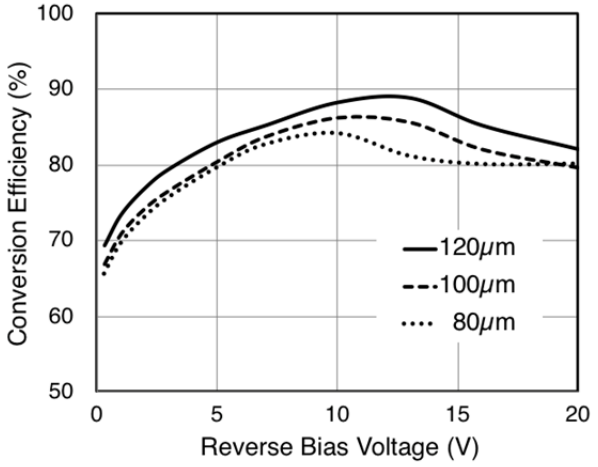

FIGURE 9. Conversion efficiency of near-infrared light at 940 nm as a function of the bias voltage of the trench PD array chips (the PD spacings of the test chips used for the measurements were 120, 100, and 80 μm).

The decrease in the conversion efficiency at the wavelength of 810 nm will be discussed in the next section.

Fig. 9 shows the measured conversion efficiencies for near-infrared at 940 nm for three test chips with different PD spacings. At the bias voltage of − 10 V, the conversion efficiencies at 120, 100, and 80 μm is 88% (0.50 A/W), 86% (0.49 A/W), 84% (0.48 A/W), respectively. At the bias voltage of − 5 V, the conversion efficiencies were 83% (0.47 A/W) at 120 μm, 80% (0.46 A/W) at 100 μm, and 80% (0.46 A/W) at 80 μm. At the bias voltage of − 0.3V, the values were 69% (0.40 A/W) at 120 μm, 67% (0.38 A/W) at 100μm, and 66% (0.38 A/W) at 80 μm. The bias voltages at which the conversion efficiency was maximum are − 12 V for 120 μm, − 11 V for 100 μm, and − 10 V for 80 μm. This phenomenon is consistent with the characteristics of the different bias voltages at which the leakage current starts to increase with increasing PD spacing, as shown in Fig. 6.

These results show that the proposed silicon optical sensor can achieve a high conversion efficiency of more than 80% at room temperature for near-infrared light at 1 μm wavelength even at a low bias voltage.

C. RESPONSE PERFORMANCE

Fig. 10 shows the waveform of the near-infrared detection signal on a test chip with a PD spacing of 120 μm. In this measurement, an LED with a central wavelength of 940 nm was used to provide a cyclic pulse signal with a low level of − 1.1 V and a high level of 1.1 V. The LED was placed 20 cm away from the sensor chip. The bias voltage of the PD was − 10 V. The current detected by the PD was amplified to 1×10^5 V/A by the current–voltage converter amplifier IV-202F4 (NF Corporation). The waveforms in (a), (b), (c), and (d) are for LED modulation periods of 8, 10, 14, and 15 MHz, respectively. Their received signals have a delay of about 50 ns. From these results, it was confirmed that the signal could be detected up to 14 MHz when the emission rate was 40% of the period.

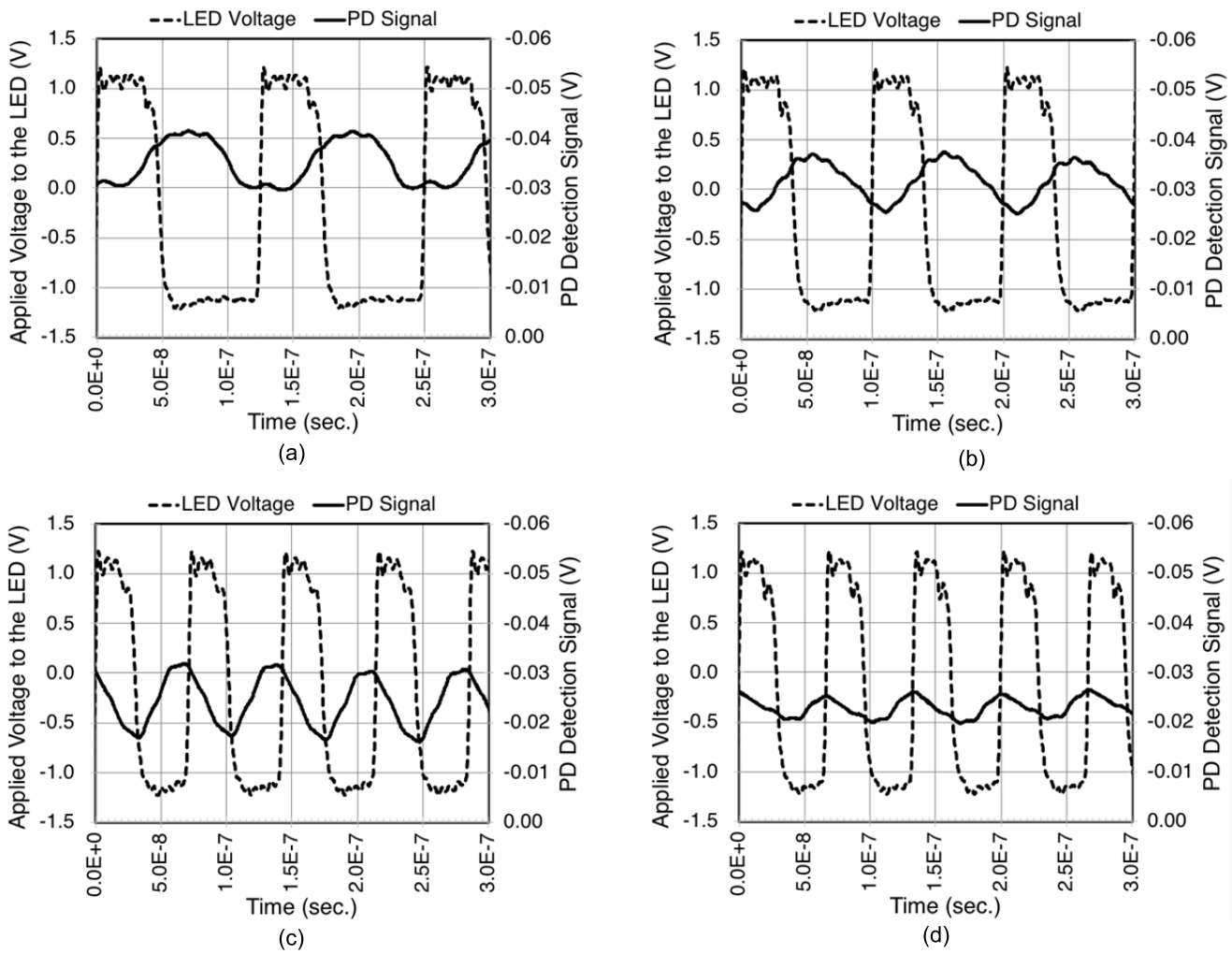

FIGURE 10. Light detection signal in a trench PD array chip with a PD spacing of 120 μm. Near-infrared light of 940 nm wavelength was used for the measurement. The optical intensity modulation periods of 8, 10, 14, and 15 MHz are shown in (a), (b), (c) and (d), respectively.

IV. DISCUSSION

We discuss the measurement results of the decrease in conversion efficiency at the wavelength of 810 nm. Fig. 11 shows the absorption coefficient in silicon for the central wavelength of the LED used in the evaluation experiments with depletion layer thicknesses up to (a) 600 μm and (b) 20 μm. The upper limit of the conversion efficiency, C_{UL}, can be approximated by (4) because there is no trench in the silicon area on the back of the chip where the light enters, and the trench cavity cannot absorb photoelectrons.

$$C_{UL} \approx A(T - D_T) + \{A(T) - A(T - D_T)\} \times \left(1 - \frac{D_T \times W_T \times L_T \times N}{S \times D_T}\right) \quad (4)$$

Here, S is the chip area, T is the chip thickness, D_T is the trench depth, W_T is the trench width, L_T is the trench length, N is the number of trench PDs, and $A(x)$ is the absorption rate in the depletion layer thickness x shown in (5).

$$A(x) = (1 - e^{-\alpha x}) \times (100 - Ref(\lambda)) \quad (5)$$

Here, $Ref(\lambda)$ is the reflectance at its chip surface for light of wavelength λ. The back surface of the test chip has a SiO_2 film of about 200 nm deposited on it, and the reflectance is about 8% for 1020 nm light, 11% for 940 nm, and 20% for 810 nm.

The upper limit of the conversion efficiency, $C_{UL}^{\dagger}$, with no electrodes on the back of the test chip, can be approximated by (6), assuming that the photoelectrons generated in silicon near the back of the chip cannot be absorbed to a depth of X_{BCK}.

$$C_{UL}{}^{\dagger} \approx A(T - D_T) + \{A(T) - A(T - D_T)\} \times \left(1 - \frac{D_T \times W_T \times L_T \times N}{S \times D_T}\right) - A(X_{BCK}) \quad (6)$$

The S of the test chip is 2.4 mm $\times$ 2.4 mm and T is 540 μm. D_T is 350 μm, W_T is 20 μm at top and 15 μm at bottom, L_T is 100 μm, and N is 120. The surface of the test chip has an aluminum film for wiring on about 75% of its area, and since the reflectance of Si-Al is 0.85 for the 1020 nm light

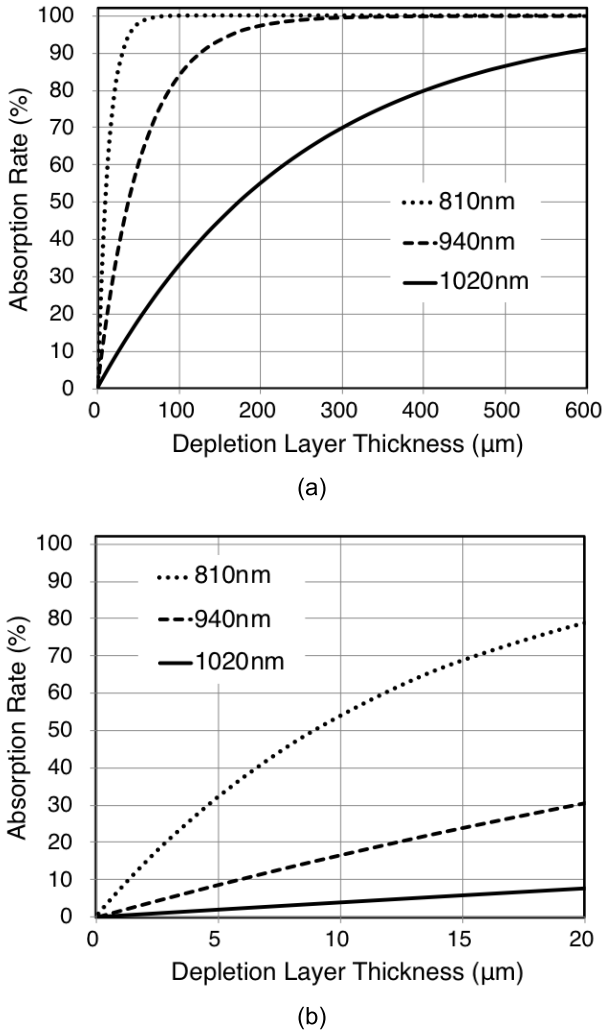

FIGURE 11. Absorption rate of near-infrared light as a function of depletion layer thickness of silicon up to (a) 600 μm and (b) 20 μm.

reaching there, about 64% of it is reflected. Thus, assuming X_{BCK} of 4 μm, its $C_{UL}^{\dagger}$ values are 85% at 1020 nm, 84% at 940 nm, and 59% at 810 nm, which are close to the measured values except for the 940 nm case. It was estimated from the directivity of the 940nm LED that its light intensity would shift by more than 4% even with a misalignment of only a few millimeters. The difference between the measured and estimated values may have been caused by the inaccurate positioning of the LED.

V. CONCLUSION

The proposed trench PD array chip is effective in making the whole area of the chip a depletion layer at low voltage. By changing its PD spacing, the bias voltage in use can be manipulated. The test chips, fabricated using 550-μm-thick silicon wafers, show conversion efficiencies of 79% to 85% at room temperature for near-infrared wavelengths near 1 μm at bias voltages ranging from $-$ 5 to $-$ 10 V. The 2.4 mm $\times$ 2.4 mm test chip was found to be able to detect modulation signals up to 14 MHz. The proposed silicon sensor can cut shorter wavelength light such as visible light by using a long-pass filter. This technology enables the miniaturization of near-infrared sensors that can be used at room temperature and low voltage and is expected to be embedded in a variety of devices such as inexpensive and compact IoT communication sensor devices.

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