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A Physic-Based Explicit Compact Model for Reconfigurable Field-Effect Transistor

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ABSTRACT In this paper, a compact model for the double-gate Reconfigurable Field-Effect Transistor (RFET) is presented. Firstly, the physics-based surface potential model is derived by solving Poisson's equation at different channel regions. Then an explicit expression of drain current is analytically obtained based on the theory of band-to-band tunneling at the Schottky junction. The proposed model shows excellent agreement with TCAD simulations which have been calibrated with experimental data. Finally, the compactible model is implemented in Verilog-A language without convergence problem, and proven by the RFET-based logic circuit.

INDEX TERMS Reconfigurable field-effect transistor, analytical model, surface potential, drain current, Verilog-A.

I. INTRODUCTION

With the rapid development of neuromorphic computing, high-throughput data put forward with substantial requirements for downscaling and power-efficient electronic circuits. However, it becomes increasingly challenging to simply reduce the size of devices based on conventional complementary metal-oxide-semiconductor (CMOS) technology due to their physical limitations. The reconfigurable field-effect transistors (RFET) have emerged as a promising candidate for the single device with tunable polarity [1]–[4]. Instead of conventional physical doping, feature gated Schottky junctions of the RFETs can controllably inject electrons or holes into the channel. In this case, the RFETs can provide both n- and p-FET device patterns by adjusting the bias of the polarity gate [5]–[8]. When one gate injects electrons into the channel, and the other gate stops the holes, then the n-type RFETs are obtained. Similarly, the p-type can also be obtained by reversed bias. By increasing the number of functions per transistor rather than reducing the size of the device [9]–[11], the RFETs are expected to provide reliable and reprogrammable CMOS operation, which are

beneficial to pave the way to silicon circuits that go beyond Moore's law.

Recently, several RFETs have been fabricated based on top-down or bottom-up processes [12]. The experimental results show a high on/off ratio ($\sim 10^9$) and extremely low gate leakage ($\sim 10^{-14}$ A), which make such a device concept desirable for energy-efficient circuit applications. Besides, a high-density synaptic device based on RFET has been proposed to build XNOR binary neural network [13]. Besides, the impact of work-function modulation, gate/spacer-channel underlap have been investigated through numerical simulations [14], [15].

To further understand the mechanism of the RFET, optimize its device characteristics and perform circuit design, it is essential to develop a physics-based compact model. An analytical surface potential and drain current model is reported in [16] by solving drift-diffusion equation in the channel with Schottky tunneling at the source/drain contact. However, the drain current of this model is expressed as an implicit function of quasi-fermi potentials. The complex computational process may cause convergence issues during circuit simulation. Besides, for low drain biases, the model results mentioned in [16] are not in good agreement with the simulations. Thus, the major objective of this paper is to provide a compact model that has no convergence and

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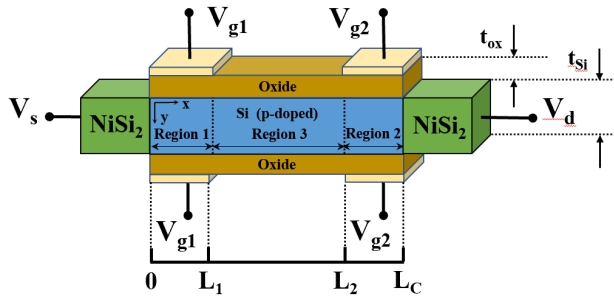


FIGURE 1. The structure of Reconfigurable FET (RFET).

accuracy problem in circuit simulation. Meanwhile, the proposed model is expected to be a SPICE compatible model and universally applicable.

In this paper, a closed-form surface potential-based model for the double-gate RFET is put forward, which is performed in the x and y two-dimensional plane. The silicon channel is divided into three regions to solve the 2D Poisson's equation. To begin with, the surface potential model is developed using several boundary conditions. Then the charge density model is derived from the current continuity equation. Finally, the drain current model for the RFET is given based on the theory of band-to-band tunneling induced by the Schottky junctions. After Taylor expansion and proper approximation, an explicit analytical compact drain current model is developed. The accuracy of the proposed model is validated by numerous TCAD simulations after calibration with the experimental data. Besides, the explicit nature of the model makes it suitable to be a SPICE compatible model, which is beneficial for circuit simulations.

The remainder of this article is organized as follows. Section II describes the device structure and the simulation environment. Section III introduces the derivation of explicit surface potential, charge density and drain current model for the RFET. In Section IV, the implementation of the proposed compact model in Verilog-A is discussed, which is useful for RFET-based circuit simulations. Finally, Section V concludes this article.

II. DEVICE STRUCTURE AND SIMULATION SETUP

Fig. 1 shows the structure of the double-gate RFET. To note that, the source/drain contacts are metallic (typically NiSi_2) to induce lateral Schottky junctions, which is also beneficial to decrease the parasitic capacitance and resistance. In order to modulate the device polarity electrically, the control gate (gate1) and polarity gate (gate2) are applied. Simulations are performed by technology computer-aided design (TCAD) simulations [17]. Based on the experimental data reported in [4], the same structure of RFET is employed to calibrate the simulation setup. Carrier recombination includes Band-to-Band recombination, Shockley-Read-Hall (SRH) recombination and Auger combination. The Wentzel-Kramers-Brillouin (WKB) approximation is employed for the band-to-band tunneling (BTBT) model, with electron and hole tunneling masses as $0.3 m_0$ and $0.2 m_0$ [16]. The

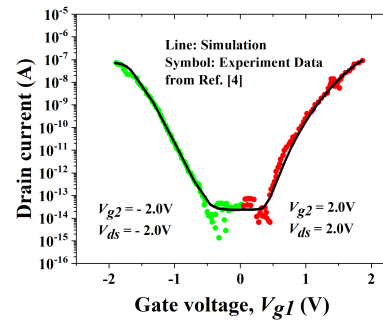


FIGURE 2. The Comparison of transfer curves between simulated and experimental data.

TABLE 1. Parameter table.

Parameters	Values	Unit
Thickness of the oxide layer (t_{ox})	8	nm
Thickness of the silicon layer (t_{si})	12	nm
Total length of the channel (L_c)	230	nm
Length of gate1 or gate 2 (L_l)	50	nm
Work function of S/D contact (W_m)	4.64	eV
Work function of the gate	4.28	eV
Doping concentration (N_c)	10^{15}	cm^{-3}
Permittivity of silicon (ϵ_{Si})	$11.9\epsilon_0$	F/cm
Permittivity of silicon dioxide (ϵ_{ox})	$3.9\epsilon_0$	F/cm

thermionic-field emission model has been applied at the (S/D) Schottky junctions, and the Schottky barriers for electrons and holes are considered to be 0.58 eV and 0.54 eV respectively [18]. Besides, the quantization effects are taken into consideration by introducing electronic quantum potential and hole quantum potential. Besides, high-field Saturation model, Lombardi mobility model, and Philips unified mobility model are included in the Mobility model. It can be observed from Fig. 2 that the transfer characteristic curves plotted with the TCAD simulator agree well with the experimental results, which proves the validity of our simulation environment. In the following studies, the parameters used in this work are presented in Table 1.

The simulated energy band diagrams of both ON-states and OFF-states are shown in Fig. 3. To make the device acts as an n-type FET, the voltages of gate1, gate2 and drain are kept positive. This causes the edge of the conduction band to bend down, which makes it easier for the electrons to tunnel from the source into the channel region. For p-type FET, the voltages of three electrodes mentioned above are kept negative, which makes the conduction band bend upwards. In this case, holes are likely to tunnel into the channel.

III. MODEL DEVELOPMENT

A. SURFACE POTENTIAL MODEL

As shown in Fig. 1, the silicon channel is divided into three regions. Region 1 and Region 2 are Schottky-gated with

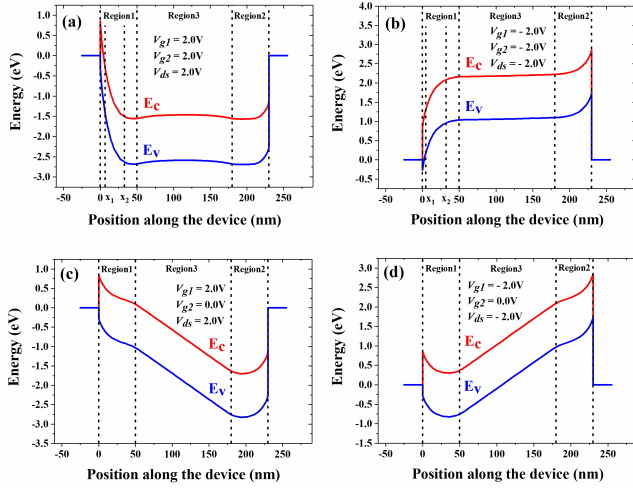


FIGURE 3. (a) ON-state of the n-type device. (b) ON-state of the p-type device. (c) OFF-state of the n-type device. (d) OFF-state of the p-type device.

gate1 and gate2, while Region 3 is not modulated with an external gate. Firstly, the two-dimensional (2D) Poisson's equation can be solved to obtain the surface potentials in Region 1 and Region 2.

$$\frac{\partial^2 \varphi_{1/2}(x, y)}{\partial x^2} + \frac{\partial^2 \varphi_{1/2}(x, y)}{\partial y^2} = \frac{qN_C}{\epsilon_{Si}} \quad (1)$$

where $\varphi_{1/2}(x, y)$ refers to the electrostatic potential of Region 1 or Region 2. ϵ_{ox} and ϵ_{Si} are the permittivities of silicon dioxide and silicon respectively. N_C is the doping concentration of the silicon channel.

The boundary conditions along y -direction (channel thickness) can be given as

$$\left. \frac{\partial \varphi_{1/2}(x, y)}{\partial y} \right|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\varphi_{1/2}(x) - V_{geff}}{t_{ox}} \quad (2a)$$

$$\left. \frac{\partial \varphi_{1/2}(x, y)}{\partial y} \right|_{y=t_{Si}} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{V_{geff} - \varphi_{1/2}(x)}{t_{ox}} \quad (2b)$$

where $V_{geff} = V_{g1/g2} - V_{FB}$, $V_{g1/g2}$ is the voltage applied on gate1 or gate2, and V_{FB} is the flat band voltage.

Using the parabolic approximation [19], the electrostatic potential for Region 1 or Region 2 can be written as

$$\varphi_{1/2}(x, y) = p(x) + q(x)y + r(x)y^2 \quad (3)$$

Assuming $\varphi_{1/2}(x, 0) = \varphi_{1/2}(x, t_{Si}) = \varphi_{1/2}(x)$, the surface potential for Region 1 ($\varphi_1(x)$) and Region 2 ($\varphi_2(x)$) can be solved and expressed as

$$\varphi_1(x) = C_1 \exp\left(\frac{x}{\lambda}\right) + D_1 \exp\left(-\frac{x}{\lambda}\right) + P_1 \quad (4a)$$

$$\varphi_2(x) = C_2 \exp\left(\frac{x}{\lambda}\right) + D_2 \exp\left(-\frac{x}{\lambda}\right) + P_2 \quad (4b)$$

where $\lambda = \sqrt{\frac{\epsilon_{Si} t_{ox} \epsilon_{Si}}{2\epsilon_{ox}}}$, $P_1 = V_{g1} - \frac{qN_C \lambda^2}{\epsilon_{Si}}$, and $P_2 = V_{g2} - \frac{qN_C \lambda^2}{\epsilon_{Si}}$.

The boundary conditions along x -direction (channel length) can be expressed as

$$\varphi_1(0) = V_s + (-1)^k \frac{\chi - W_m}{q} \quad (5a)$$

$$\varphi_2(L_c) = V_d - (-1)^k \frac{\chi - W_m}{q} \quad (5b)$$

where χ is the electronic affinity, W_m is the metal work-function. V_d and V_s are the voltage applied on the drain and source respectively. Besides, k is an even number for the n-program and an odd number for the p-program.

Using the boundary conditions Equations (5a) and (5b), the constants C_1, D_1, C_2, D_2 can be derived.

$$C_1 = \frac{q\varphi_{L1} + M \exp\left(-\frac{L_1}{\lambda}\right)}{2q \sinh\left(\frac{L_1}{\lambda}\right)} \quad (6a)$$

$$D_1 = -\frac{q\varphi_{L1} + M \exp\left(\frac{L_1}{\lambda}\right)}{2q \sinh\left(\frac{L_1}{\lambda}\right)} \quad (6b)$$

$$C_2 = \frac{q\varphi_{L2} \exp\left(-\frac{L_c}{\lambda}\right) + N \exp\left(-\frac{L_2}{\lambda}\right)}{2q \sinh(L_2 - L_c)} \quad (6c)$$

$$D_2 = -\frac{q\varphi_{L2} \exp\left(\frac{L_c}{\lambda}\right) + N \exp\left(\frac{L_2}{\lambda}\right)}{2q \sinh(L_2 - L_c)} \quad (6d)$$

where $\varphi_1(L_1) = \varphi_{L1}$, $\varphi_2(L_c) = \varphi_{L2}$, $M = (-1)^k (W_m - \chi) - qV_s + qP_1$, $N = (-1)^k (-W_m + \chi) - qV_d + qP_2$.

In order to obtain the potential distribution in Region 3, the gradual channel approximation is employed. The surface potential for Region 3 can be expressed as

$$\varphi_3(x) = \frac{\varphi_{L2} - \varphi_{L1}}{L_2 - L_1} (x - L_1) + \varphi_{L1} \quad (7)$$

Because of the continuity of the surface potential and its first derivative, the boundary conditions can be given as

$$\varphi_1(L_1) = \varphi_3(L_2) = \varphi_{L1} \quad (8a)$$

$$\varphi_2(L_2) = \varphi_3(L_2) = \varphi_{L2} \quad (8b)$$

$$\left. \frac{\partial \varphi_1(x)}{\partial x} \right|_{x=L_1} = \left. \frac{\partial \varphi_3(x)}{\partial x} \right|_{x=L_1} \quad (8c)$$

$$\left. \frac{\partial \varphi_2(x)}{\partial x} \right|_{x=L_2} = \left. \frac{\partial \varphi_3(x)}{\partial x} \right|_{x=L_2} \quad (8d)$$

Using the boundary conditions mentioned above, the surface potential φ_{L1} and φ_{L2} are solved for both n- and p-type RFETs, as shown in Fig. 4.

B. CHANNEL CHARGE DENSITY MODEL

Based on the surface potential, the electric field E of the channel surface along the x -direction can be calculated.

$$E_n(x) = -\frac{d}{dx} \varphi_n(x) \quad (9a)$$

$$E_p(x) = -\frac{d}{dx} \varphi_p(x) \quad (9b)$$

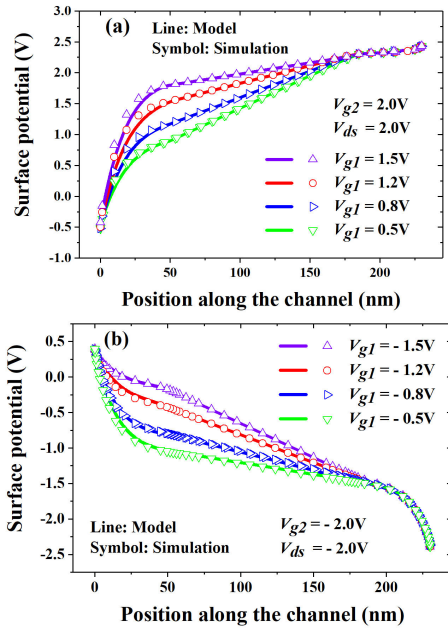


FIGURE 4. (a) Surface potential of the n-type device. (b) Surface potential of the p-type device.

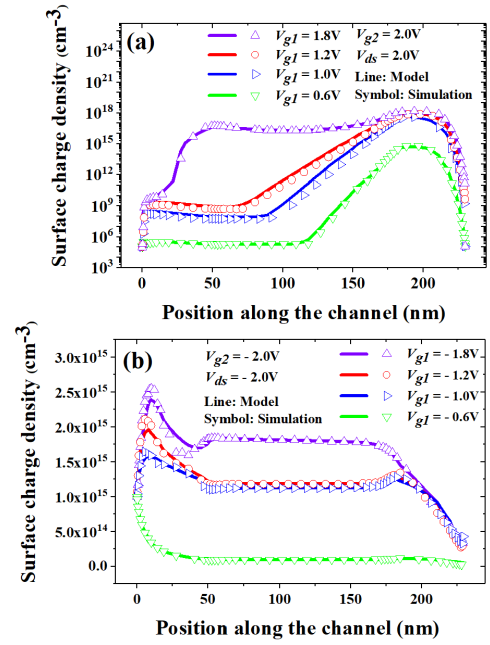


FIGURE 6. (a) Surface charge density of the n-type device. (b) Surface charge density of the p-type device.

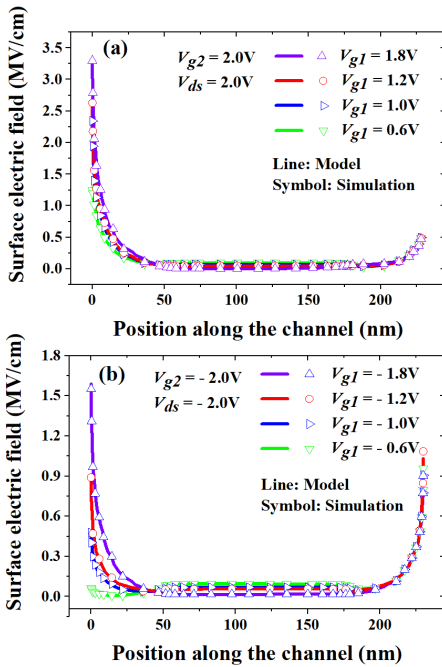


FIGURE 5. (a) Surface electric field of the n-type device. (b) Surface electric field of the p-type device.

The model and simulation results are shown in Fig. 5 for both n- and p-type RFET.

Then the relationship between the carrier mobility (μ) and the surface electric field can be given as

$$\mu_{n/p} \propto \begin{cases} E_{n/p}(x)^{-\frac{1}{2}}, & 10^3 < E < 10^5 \text{ V/cm} \\ E_{n/p}(x)^{-1}, & E > 10^5 \text{ V/cm} \end{cases} \quad (10)$$

A kind of continuity equations which describe charge conservation is shown below

$$\nabla \cdot J_n = qR_{net,n} + q \frac{\partial n}{\partial t} \quad (11a)$$

$$\nabla \cdot J_p = -qR_{net,p} - q \frac{\partial p}{\partial t} \quad (11b)$$

where $R_{net,n}$ and $R_{net,p}$ are the electron and hole net recombination rates, respectively.

In addition, by solving the current continuity equation, the current density in the n-type and p-type channel can be expressed as

$$J_n = q\mu_n n(x)|E_n(x)| \quad (12a)$$

$$J_p = -q\mu_p p(x)|E_p(x)| \quad (12b)$$

When the channel reaches its equilibrium state, the carrier concentration does not change, so $\partial n/\partial t$ and $\partial p/\partial t$ are considered to be zero. By combining Equations (11a) and (12a), (11b) and (12b), the charge densities of both n-type and p-type channels are derived, which are shown in Fig. 6.

C. DRAIN CURRENT MODEL

Using the Kane's model [20], the band-to-band generation rate (G_{BTB}) can be derived as

$$G_{BTB} = A(E_{avg})^{D-1} \exp\left(-\frac{B}{E_{avg}}\right) E \quad (13)$$

The band-to-band tunneling probability is used to calculate the drain current across the Schottky barrier nearby the source.

$$I = q \int G_{BTB} dV = Aq \int (E_{avg})^{D-1} \exp\left(-\frac{B}{E_{avg}}\right) E dV \quad (14)$$

where A , B and D are Kane's tunneling parameters given by [21]. $E_{avg} = E_g/qx$ refers to the electric field on average, E_g is the bandgap of silicon, and x is the tunneling path from x_1 to x_2 shown in Fig. 3(a) and (b). x_1 represents the starting point of the tunneling, and x_2 represents the ending point of the tunneling.

The expressions of x_1 and x_2 can be calculated by [22]

$$x_1 = \lambda \ln \left(\frac{\theta_a + \sqrt{\theta_a^2 - 4C_1D_1}}{2C_1} \right) \quad (15a)$$

$$x_2 = \lambda \ln \left(\frac{\theta_b + \sqrt{\theta_b^2 - 4C_1D_1}}{2C_1} \right) \quad (15b)$$

where $\theta_a = E_g + \frac{\Phi_1}{q} + \frac{\beta}{\alpha}$, $\theta_b = E_g + \frac{\Phi_2}{q} + \frac{\beta}{\alpha}$, $\alpha = \frac{1}{\lambda^2}$, $\beta = -\frac{qN_c}{\epsilon_{Si}} - \frac{V_{g1}}{\lambda^2}$, $\Phi_1 = E_V^{Source} - E_F^{Source}$, and $\Phi_2 = E_V^{Source} - E_V^{Channel}$.

Besides, the electric field is obtained by

$$E = \sqrt{E_x^2 + E_y^2} = \sqrt{\left[-\frac{\partial}{\partial x} \varphi_1(x) \right]^2 + \left[-\frac{\partial}{\partial y} \varphi_{1/2}(x, y) \right]^2} \quad (16)$$

The expression of E_x and E_y can be obtained from (4a) and (3), respectively. The electric field can be given as

$$E = \sqrt{\left[-\frac{1}{\lambda} C_1 \exp\left(\frac{x}{\lambda}\right) + \frac{1}{\lambda} D_1 \exp\left(-\frac{x}{\lambda}\right) \right]^2 + [-q(x) - 2r(x)y]^2} \quad (17)$$

The unary Taylor expansion is applied to the E_x and subsequently binary Taylor expansion is applied to E , the expression can be simplified as

$$E = \eta + \frac{\frac{ab}{\lambda^3}x + 2q(x)r(x)y}{\eta} \quad (18)$$

where $a = C_1 + D_1$, $b = C_1 - D_1$, $\eta = \sqrt{\frac{b^2}{\lambda^2} + q(x)^2}$.

Applying the interval of integration for both x -direction and y -direction, the expression of the drain current is obtained. (here the width of the device is considered to be 1 μm and the parameter D is considered to be 2 for the direct tunneling process).

$$I = Aq \int_0^{t_{Si}} \int_{x_1}^{x_2} \left(\eta + \frac{\frac{ab}{\lambda^3}x + 2q(x)r(x)y}{\eta} \right) \frac{E_g}{qx} \exp\left(-\frac{qB}{E_g}x\right) dx dy \quad (19)$$

After calculating the integration rearranging, the drain current for the RFET is finally obtained

$$I = Aq \left\{ \left[\frac{E_g \eta t_{Si}}{q} + \frac{q(x)r(x)t_{Si}^2}{\eta q} \right] [\xi(x_2) - \xi(x_1)] - \frac{abE_g^2 t_{Si}}{\lambda^3 q^2 \eta B} [\zeta(x_2) - \zeta(x_1)] \right\} \quad (20)$$

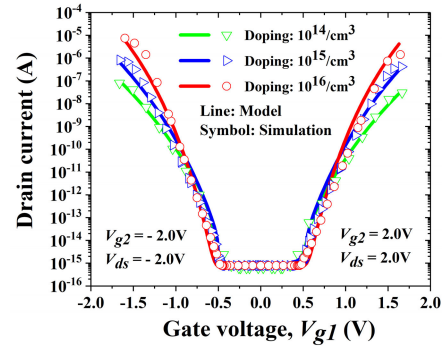


FIGURE 7. Transfer characteristic ($I_d - V_g$) curves with different channel dopings of 10^{14} , 10^{15} and 10^{16} cm^{-3} .

where $\xi(x)$ and $\zeta(x)$ are given by

$$\xi(x) = \ln|x| + \sum_{i=1}^{\infty} \frac{\left(-\frac{qB}{E_g}x\right)^i}{i \cdot i!} \quad (21a)$$

$$\zeta(x) = \exp\left(-\frac{qB}{E_g}x\right) \quad (21b)$$

In equation (20), the parameters a and b explicitly contain the drain voltage V_d , the source voltage V_s , and the gate voltages, which shows the explicit nature of this model.

The transfer characteristic ($I_d - V_g$) characteristics of the RFETs are plotted in Fig. 7 with different channel doping concentrations. For the band to band tunneling, the value of drain current depends on the tunneling probability of carriers. When the applied voltage (V_{g1}) increases, the electric field intensity in the barrier area increases, which shortens the tunnel length. Thus, the carriers are more likely to tunnel. As a result, the current becomes larger. When V_{g1} is small, the electric field in the barrier area under different channel doping concentrations is considered to be approximately equal, which leads to almost the same I_{off} . For a given voltage that is large enough, the RFET with high channel doping concentration has higher electric field intensity in the barrier area, which makes carriers tunnel more easily. As a result, higher channel doping concentration leads to larger saturation current.

From Fig. 8, the transfer characteristic curves of the RFET at different temperatures are depicted. As the temperature rises, the energy of the carrier increases, so the probability of tunneling increases. When V_{g1} is small, the tunneling of carriers largely depends on temperature, and thus the leakage current increases accordingly with temperature.

As the gate voltage goes up, the electric field intensity in the barrier area gradually plays a leading role. When the voltage rises to a certain value, the impact of the evaluated temperature is weakened, and the drain current is mainly determined by gate voltage. In this case, the electric field intensity generated by the voltage (V_{g1}) in the barrier region is the same even at different temperatures, which means that the carriers have almost the same probability to tunnel. Thus, as the gate voltage is high enough, the change

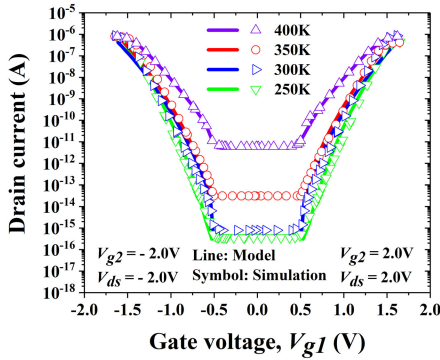


FIGURE 8. Transfer characteristic ($I_d - V_g$) curves at different temperatures of 250K, 300K, 350K and 400K.

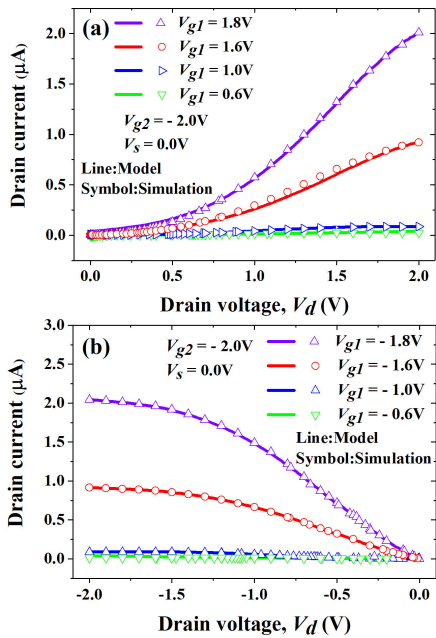


FIGURE 9. (a) Output characteristic ($I_d - V_d$) curves of the n-type device. (b) Output characteristic ($I_d - V_d$) curves of the p-type device.

of drain current at different temperatures tends to be small. In the calculation processes mentioned above, the Fermi level E_F^{Source} strongly depends on the value of temperature, so parameter Φ_1 is influenced by the temperature. As a result, the impact of temperature on the drain current is very significant.

The output characteristics curves of the RFET are shown in Fig. 9. It also shows that the model is in good agreement with TCAD simulations for both n- and p-type RFET.

IV. RFET-BASED LOGIC GATE CIRCUITS

As the polarity gate and control gate are located at two Schottky junctions of the RFETs, it has the potential for high-density integration and low cost, which are suitable for future applications in large-scale integrated circuits.

For circuit validation, the proposed model is implemented in Verilog-A. Here, an RFET-based inverter logic gate circuit is simulated by Cadence Virtuoso. To form an inverter,

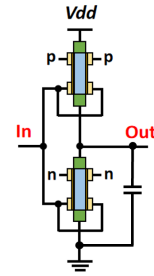


FIGURE 10. INV logic gates with n/p-type RFETs.

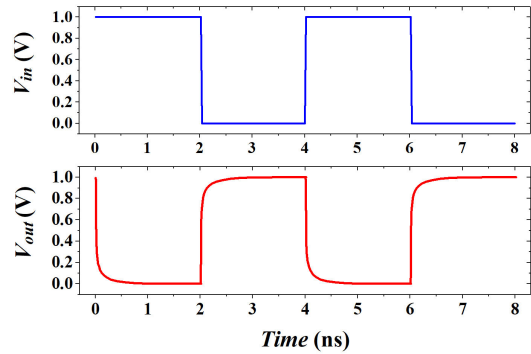


FIGURE 11. The NOT gate binary logic operation characteristic with transient circuit simulations.

two RFETs are connected in series between the supply and ground, and the value of the capacitance is 10 fF, as shown in Fig. 10. One is biased at n-type and the other is biased at p-type. Fig. 11 plots the transient simulation result of an inverter. It can be seen that the proposed INV performs the function successfully. Besides, it shows fast switching speed and full swing output, which performs better performance than conventional CMOS logic operations.

V. CONCLUSION

In this paper, we have presented a compact physics-based model for the surface potential, charge density and drain current of the reconfigurable field-effect transistors (RFETs). The model shows excellent agreement with TCAD simulation data over broad bias. Finally, RFET-based circuit simulation is performed in Verilog-A, which demonstrates that the proposed model is suitable to be a SPICE compatible model.

APPENDIX

For equation (16), the total electric field intensity is equal to the vector sum of the transverse and vertical electric fields, which means $E = \sqrt{E_x^2 + E_y^2}$. The relationship between the electric field and the potential in the tunneling region is obtained as

$$E_x = -\frac{\partial}{\partial x}\varphi_1(x) = -\frac{1}{\lambda}C_1 \exp\left(\frac{x}{\lambda}\right) + \frac{1}{\lambda}D_1 \exp\left(-\frac{x}{\lambda}\right) \quad (S1)$$

$$E_y = -\frac{\partial}{\partial y}\varphi_{1/2}(x, y) = -q(x) - 2r(x)y \quad (S2)$$

where E_x and E_y are the transverse electric field and vertical electric field respectively. Substitute them into equation $E = \sqrt{E_x^2 + E_y^2}$, equation (17) can be obtained.

The Taylor expansion applied to equation (17) is shown below. By applying unary Taylor expansion to the E_x , E_x can be expressed as

$$E_x = -\frac{1}{\lambda}[C_1 - D_1 + \frac{1}{\lambda}(C_1 + D_1)x + \frac{1}{2\lambda^2}(C_1 - D_1)x^2] \quad (S3)$$

Assuming $C_1 - D_1 = b$ and $C_1 + D_1 = a$, the total electric field can be obtained.

$$E = \sqrt{[\frac{1}{\lambda}(b + \frac{a}{\lambda}x + \frac{b}{2\lambda^2}x^2)]^2 + [q(x) + 2r(x)y]^2} \quad (S4)$$

In order to simplify the calculation, the coefficient -1 is ignored here. Next, the computational process of binary Taylor expansion is shown below.

$$E|_{(0,0)} = \sqrt{\frac{b^2}{\lambda^2} + q(x)^2}$$

$$\frac{\partial E}{\partial x}\bigg|_{(0,0)} = \frac{ab}{\lambda^3 \sqrt{\frac{b^2}{\lambda^2} + q(x)^2}} \quad (S5)$$

$$\frac{\partial E}{\partial y}\bigg|_{(0,0)} = \frac{2q(x)r(x)}{\sqrt{\frac{b^2}{\lambda^2} + q(x)^2}}$$

$$E = E|_{(0,0)} + \frac{\partial E}{\partial x}\bigg|_{(0,0)} x + \frac{\partial E}{\partial y}\bigg|_{(0,0)} y$$

$$= \sqrt{\frac{b^2}{\lambda^2} + q(x)^2} + \frac{\frac{ab}{\lambda^3}x + 2q(x)r(x)y}{\sqrt{\frac{b^2}{\lambda^2} + q(x)^2}} \quad (S6)$$

Equation (17) is obtained.

To prove the validity of the integration mentioned in equation (20), we will provide a detailed integral process in this section.

$$I = Aq \int_0^{t_{Si}} \int_{x_1}^{x_2} [\frac{\eta E_g}{qx} \exp(-\frac{qB}{E_g}x) + \frac{abE_g}{\lambda^3 \eta q} \exp(-\frac{qB}{E_g}x) + \frac{2p(x)q(x)E_g y}{\eta qx} \exp(-\frac{qB}{E_g}x)] dx dy \quad (S7)$$

$$I = Aq \int_0^{t_{Si}} \{ (\frac{\eta E_g}{q} + \frac{2p(x)q(x)E_g y}{\eta q}) \cdot \int_{x_1}^{x_2} \frac{1}{x} \exp(-\frac{qB}{E_g}x) dx + \frac{abE_g}{\lambda^3 \eta q} (-\frac{E_g}{qB}) [\exp(-\frac{qB}{E_g}x_2) - \exp(-\frac{qB}{E_g}x_1)] \} dy \quad (S8)$$

After integrating the variable y , the integration can be expressed as

$$I = Aq \left\{ \left[\frac{E_g \eta t_{Si}}{q} + \frac{q(x)r(x)t_{Si}^2}{\eta q} \right] \cdot \int_{x_1}^{x_2} \frac{1}{x} \exp(-\frac{qB}{E_g}x) dx \right.$$

$$\left. - \frac{abE_g^2 t_{Si}}{\lambda^3 q^2 \eta B} [\exp(-\frac{qB}{E_g}x_2) - \exp(-\frac{qB}{E_g}x_1)] \right\} \quad (S9)$$

by using some approximations, it can be calculated that

$$\int_{x_1}^{x_2} \frac{1}{x} \exp(ax) dx = \ln|x_1| + \sum_{i=1}^{\infty} \frac{(ax_1)^i}{i \cdot i!} - \ln|x_2| - \sum_{i=1}^{\infty} \frac{(ax_2)^i}{i \cdot i!} \quad (S10)$$

Now equation (20) can be obtained.

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