IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 14, 2021, accepted February 26, 2021, date of publication March 8, 2021, date of current version March 16, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3064378

A Low Supply Voltage All-Digital Phase-Locked Loop With a Bootstrapped and Forward Interpolation Digitally Controlled Oscillator

JEN-CHIEH LIU AND YU-PING LI
Department of Electrical Engineering, National United University, Miaoli 36063, Taiwan
Corresponding author: Jen-Chieh Liu (jcliu@nuu.edu.tw)

ABSTRACT An all-digital phase-locked loop (ADPLL) with a multiphase digitally controlled oscillator (DCO) incorporating the bootstrapped and interpolated schemes is proposed in this paper. The bootstrapped ring oscillator can boost the output voltage to a higher level than the supply voltage. Thus, the oscillator can be operated in low-supply-voltage applications. MOS varactor is used in the bootstrapped capacitor to reduce the area cost. Circuit analysis and simulated verification were performed for an optimized design. The interpolated DCO has multiphase outputs and a high operating frequency. The test chip was implemented in a 90-nm CMOS process, and the core area was $60 \times 117\ \mu m^2$. The power consumptions at 1160 MHz and 20 MHz were 912.6 μW (at 0.6 V) and 2.94 μW (at 0.2 V), respectively. In the worst-case jitter performance, the root mean square (RMS) jitters were less than 0.42%.

INDEX TERMS Bootstrapped, digitally controlled oscillator (DCO), interpolation, multiphase, phase-locked loop (PLL).

I. INTRODUCTION

Recently, low-supply-voltage phase-locked loops (PLLs) using several digital, analog, and charge pump schemes have been proposed for low-power and high-frequency applications. Fig. 1 depicts the relationship between the power performance and operating frequencies of all-digital PLLs (ADPLLs) [1]–[8], charge-pump PLLs (CPPLLs) [9]–[13] and hybrid digital PLLs (HDPLLs) [14], [15] for low-supply-voltage operations. Operating PLLs at low supply voltage is difficult. Digital schemes do not require analog components, such as operational amplifiers and current sources. The design of digital circuits at low supply voltages is easy. The international technology roadmap for semiconductors (ITRS) was reported in [16]. The current trend of internet of things (IoT) applications suggests a target of less than 0.45 V for ultra-low-supply voltages in the future. Low-voltage and low-power devices are constrained by their battery lives and operating lifetimes. A DC to DC convertor was reported in [17] for an energy harvesting system from solar, thermal, and vibration sources. This convertor can create an output voltage of 0.2 V.

The associate editor coordinating the review of this manuscript and approving it for publication was Teerachot Siriburanon.

Many techniques can be used in digital PLLs to reduce power consumption and achieve a high operating frequency. In [18], the duty-cycled technique was applied to a frequency synthesizer of wireless sensor networks to reduce its average power consumption. A dual-loop configuration was used to achieve a low-frequency error. For the fractional-N clock generators, the multiplying delay-locked loops (MDLLs) were reported in [19], [20]. The digital calibration schemes were adopted to achieve excellent jitter and spur performance. The injection-locked PLLs used the fully-synthesizable fractional-N schemes and had good output phase noise in [21], [22]. The studies [23]–[25] have reported that applying LC oscillators to digital PLLs can result in a superior operating frequency and jitter performance to those achieved by ring-based oscillators. Furthermore, LC oscillators provide low phase noise in wireless communication applications. To satisfy specific requirements in some applications, ring-based oscillators have been used in [26] and [27] for extending the operating frequency range or for operation over a wide supply voltage range. ADPLL designs have high tolerance to process, voltage, and temperature (PVT) variations, as described in [28] and [29]. Start-up calibration and normalization were proposed in [28] to calibrate the digitally controlled oscillator (DCO) period with the

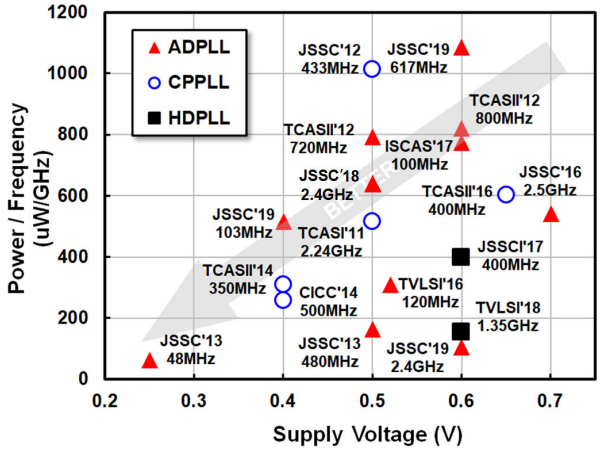


FIGURE 1. Roadmap of low-supply-voltage PLLs.

resolution of a time-to-digital converter (TDC). The technique presented in [29] provided good loop stability and performed independently of PVT variations. Among ADPLL architectures, the TDC-based ADPLL is a popular scheme. However, achieving a high TDC resolution is difficult. The TDC resolution varies with PVT variations, especially at a low supply voltage. Therefore, the jitter performance may be negatively affected by a large TDC resolution at a low supply voltage. The bang-bang phase detector (BBPD)-based ADPLL can achieve low jitter and power consumption because the TDC is replaced by a BBPD in [30].

For low jitter and phase noise applications, the DCO output requires high-quality signals, such as LC tank oscillators. Specific schemes with high PVT tolerance or calibration techniques are designed to increase the stability of ADPLLs. ADPLL loop stability should be considered in ADPLLs with a wide supply voltage range. To achieve an ADPLL with a wide operating frequency range, the operating frequency range of the DCO should be extended. Low-power-consumption and low-supply-voltage applications were considered in this study. Therefore, a low-supply-voltage ADPLL with multiphase outputs was implemented.

In the proposed multiphase DCO, a ring oscillator with the interpolator scheme and bootstrapped techniques were used to extend the maximum operating frequency in the supply voltage range of 0.2–0.6 V. The ADPLL architecture is described in Section II. The experimental and measurement results are presented in Section III. Finally, the conclusion is presented in Section IV.

II. ARCHITECTURE DESCRIPTION

A. MOS VARACTORS OF THE BOOTSTRAPPED DCO

Fig. 2 (a) and (b) illustrate the traditional and proposed bootstrapped inverter cells of the DCO. The traditional bootstrapped inverter can obtain an output voltage that is higher than the supply voltage, as illustrated in Fig. 2 (a). At low supply voltages, transistors operate in a subthreshold region. Thus, the operating frequency and output drive of ring oscillators are limited. Consequently, a bootstrapped technique

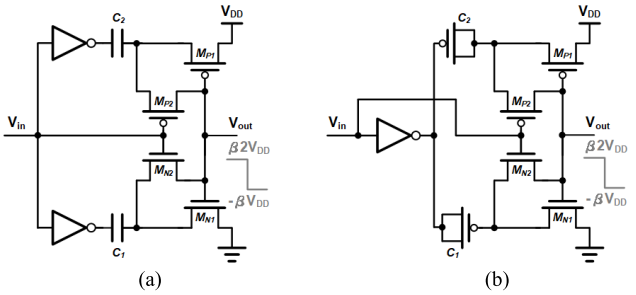


FIGURE 2. Bootstrapped inverter cell of the DCO: (a) traditional scheme and (b) proposed scheme.

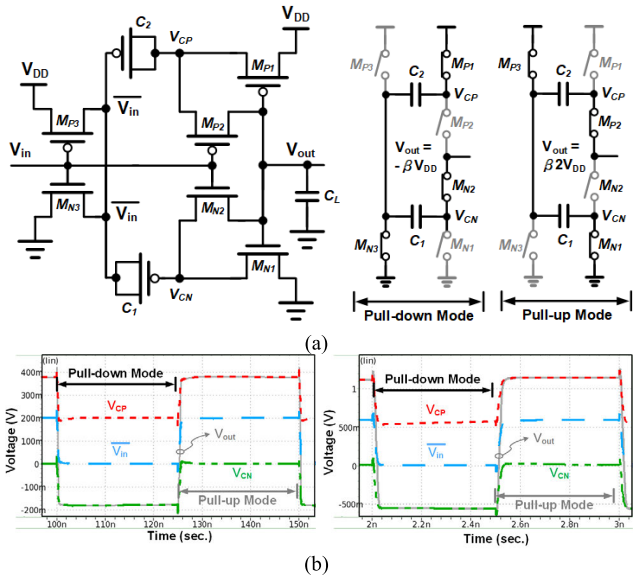


FIGURE 3. Operation of a bootstrapped inverter: (a) pull-down mode and pull-up mode. (b) Simulated results of the operation of the bootstrapped inverter (BT INV) at 0.2 V and 0.6 V.

was proposed in [2], [31], [32] to obtain a high operating frequency and output drive capability. Depending on the capacitor values C_1 and C_2, the voltage swing of the output is from $-\beta V_{DD}$ to $\beta 2V_{DD}$ where β is the boosting factor. In the pull-down mode, β can be defined as $C_1/(C_1+C_L)$, where C_L is the total parasitic capacitance of output (V_{out}). In the pull-up mode, β is equal to $C_2/(C_2+C_L)$ [31]. The output swing can be higher and lower than the supply voltage (V_{DD}) and ground (0 V), respectively. The bootstrapped technique used in this study is depicted in Fig. 2 (b). Metal–insulator–metal (MIM) capacitors are replaced by MOS varactors because MOS varactors have a lower area cost than MIM capacitors do. The proposed bootstrapped inverter is derived from the one frontend inverter, as depicted in Fig. 2 (b).

Fig. 3 (a) presents the operation of the bootstrapped inverter with MOS varactors. When the bootstrapped inverter input varies from 0 V to V_{DD}, the bootstrapped inverter output varies from $\beta 2V_{DD}$ to $-\beta V_{DD}$, as the pull-down mode. M_{N2}, M_{N3} and pull-down capacitor (C_1) pull down the output signal (V_{out}). At the same time, M_{N3} and M_{P1} preset the pull-up capacitor (C_2). Thus, V_{out} can achieve a negative voltage

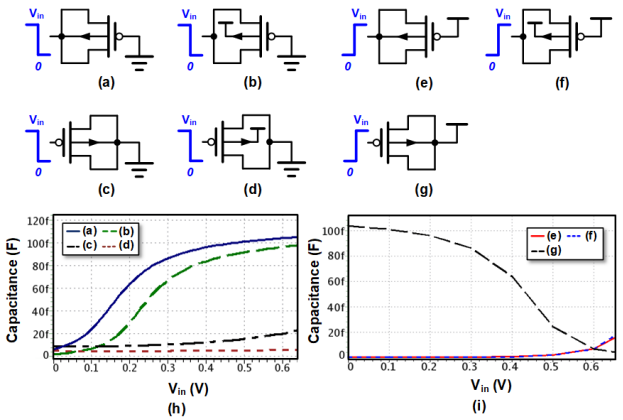


FIGURE 4. MOS varactors for a bootstrapped inverter.

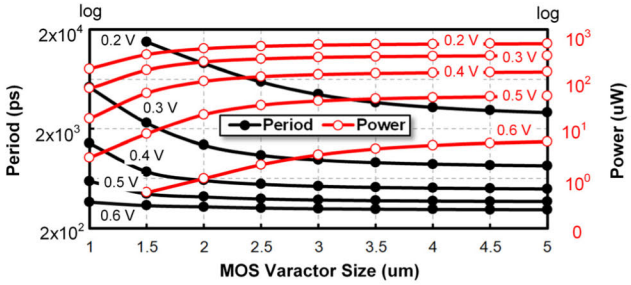


FIGURE 5. Variations of the period and power with the MOS varactor size.

$(-\beta V_{\mathrm{DD}})$. When the bootstrapped inverter input varies from V_{DD} to 0 V, the bootstrapped inverter output varies from $-\beta V_{\mathrm{DD}}$ to $\beta 2V_{\mathrm{DD}}$, as the pull-up mode. M_{P2}, M_{P3} and C_2 pull up the output signal (V_{out}). At the same time, M_{P3} and M_{N1} preset C_1. Thus, V_{out} can achieve an increase in voltage from V_{DD} to $\beta 2V_{\mathrm{DD}}$. The output voltage swing can be from $-\beta V_{\mathrm{DD}}$ to $\beta 2V_{\mathrm{DD}}$, which is useful in low-supply-voltage designs. Fig. 3 (b) displays the simulated results for the operation of the bootstrapped inverter at 0.2 V and 0.6 V. At a supply voltage of 0.2 V, the output voltage range of bootstrapped inverter is form −0.2 V to 0.4 V. At a supply voltage of 0.6 V, the output voltage range of bootstrapped inverter is form −0.5 V to 1.1 V.

The seven connected circuits of PMOS varactors are depicted in Fig. 4 (a)-(g). The four cases (in Fig. 4 (a)-(d)) are dependent on the pull-down mode of the bootstrapped inverter depicted in Fig. 3 (a). For the same PMOS size, the capacitor–voltage (CV) curves are depicted in Fig. 4 (h). The input voltage (V_{in}) is varied from 0 V to V_{DD} through the frontend inverter. The three cases (in Fig. 4 (e)-(g)) are dependent on the pull-up mode of the bootstrapped inverter depicted in Fig. 3 (a). For the same PMOS size, the CV curves are depicted in Fig. 4 (i). As depicted in Fig. 4 (a) and (g), large capacitor values are selected for operations at boosted voltages. For noise rejection, PMOS varactors are superior to NMOS varactors because PMOSs with an n- well process can effectively isolate noise from the substrate.

TABLE 1. Performance comparison between the mim capacitor and pmos varactor.

	MIM Capacitor	PMOS Varactor
Boost Efficiency (%)	72	72
Capacitor Value (fF)	80	80 (Fig. 4)
Layout Area (μm^2)	$(7.08)^2$	$(2.5)^2$
Power (μW)	20.4	21.8
Area Reduction (times)	8.02	

* Boost efficiency = $(V_{\mathrm{OUT}} - V_{\mathrm{DD}}) / V_{\mathrm{DD}}$

Table 1 lists the performances of the MIM capacitors and PMOS varactors. Under the same capacitor value and boost efficiency, the area cost of PMOS varactors can be less than that of MIM capacitors. In the simulation, an inverter with a MIM capacitor or MOS varactor was used at 0.6 V. The boost efficiencies and powers at these two conditions were similar for the MIM capacitor and PMOS varactor. The layout area of the MIM capacitor was 8.02 times the size of the PMOS varactor. Fig. 5 illustrates the variation in the period and power consumption with the MOS capacitor size. In the simulations, a five-stage ring oscillator was used at 0.6 V. When the size of the PMOS varactor increased, the output frequency and power consumption also increased, as depicted in Fig. 5. However, this trend plateaued at a certain PMOS varactor size. When the charge current increased, the output voltage swing and loading capacitance increased. Therefore, the power consumption and output frequency decreased when the PMOS varactor was too large.

Fig. 6 illustrates the leakage currents of the bootstrapped inverter under various processes and temperatures when the operating frequency is 20 MHz. Under the temperature variations, the maximum leakage current is in the FF corner at 120 ° C, and its value is 617 nA. The leakage current ratios between −20°C and 120 °C are 13.4 (in the FF corner), 16.8 (in the TT corner), and 24.4 (in the SS corner) at 0.6 V. However, the worst-case leakage current occurred at a low supply voltage of 0.2 V. The leakage current ratios between −20° C and 120 ° C are 21.8 (in the FF corner), 36.1 (in the TT corner), and 55.3 (in the SS corner). Fig. 7 displays the boost efficiency and power consumption of a five-stage bootstrapped delay chain (five-stage bootstrapped inverters) when the supply voltage was varied from 0.2 V to 0.6 V at 120 °. This bootstrapped delay chain with MOS varactors can obtain the same output voltage swing as that of a traditional scheme operated from 0.3 V to 0.6 V. For the fair condition in the simulation, the operating frequency is defined to illustrate the boost efficiency and power consumption in Fig. 7. Therefore, the leakage current was not the main factor of power consumption. The bootstrapped inverter with MOS varactors consumed almost the same power as a bootstrapped inverter with MIM capacitors. This oscillator was conducted at a high operating frequency. Thus, the dynamic power had

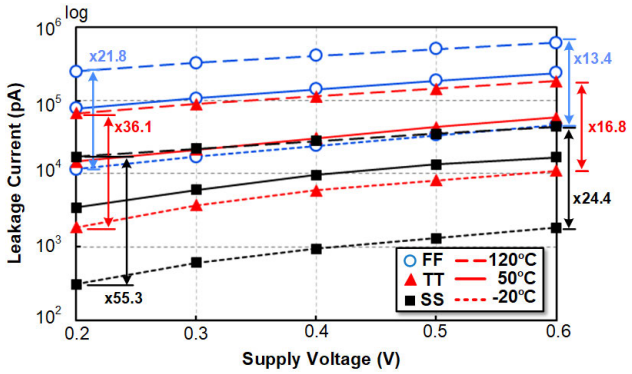


FIGURE 6. Variation of the leakage currents of the bootstrapped inverter under various processes and temperatures.

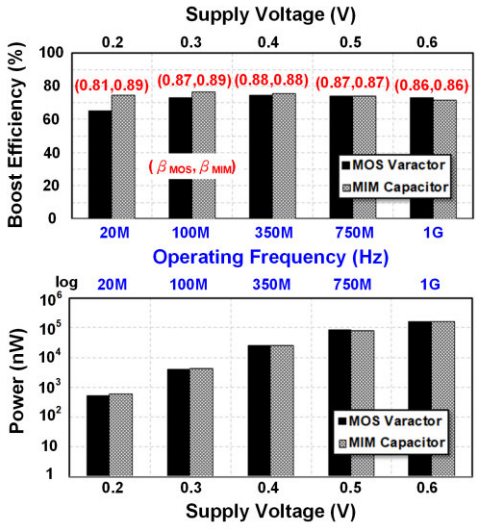


FIGURE 7. Variations in the boost efficiency and power consumption with the supply voltage.

a higher effect than the leakage power did. The boosting factors of traditional and proposed bootstrapped inverters (β_{MIM} and β_{MOS}) are also shown in Fig. 7. MOS varactor has a smaller capacitance value than MIM capacitor at supply voltage of 0.2 V. Thus, β_{MOS} is also smaller than β_{MIM} at the supply voltage of 0.2 V.

Fig. 8 presents the simulated results of the delay time (sum of the rise time and fall time), total current and leakage current of the bootstrapped inverter. According the reported paper in [31], the discharge current in the proposed bootstrapped inverter is

$$\mathrm{I_D} = \mu \mathrm{C_{ox}} \frac{\mathrm{W}}{\mathrm{L}} (\beta 2 V_{DD} - V_{th}) V_{DD} - \frac{1}{2} (\mathrm{V_{DD}})^2 \qquad (1)$$

where μ and C_{OX} are the mobility the depletion capacitance, respectively. W and L are width and length of MOS, respectively. V_{th} denotes the threshold voltage. The fall time of bootstrapped inverter can be defined as $2.2R_{BT}C_L$, where R_{BT} is equal to $\mathrm{V_{DD}/I_D}$ and C_L is the total parasitic capacitance of output. In this study, the parameter of μC_{OX} of NMOS is 337.5 uA/V^2. The ratio of W/L, V_{th} and C_L are 4,

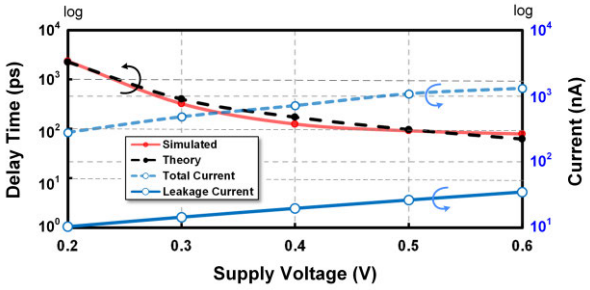
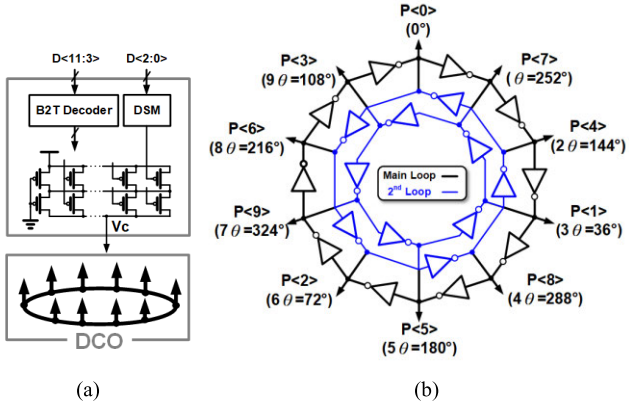


FIGURE 8. Analyses of delay time and current of the bootstrapped inverter.



(a) (b)

FIGURE 9. Proposed multiphase DCO (a) block diagram (b) 10-stage ring oscillator with a 3-stage sub-feedback loop.

0.2 V and 10 fF, respectively. The fall time can be approximate calculated. The rise time also can be calculated via the same way. Therefore, the calculated and simulated delay times are shown in Fig. 8. The simulated results of the total current and leakage current are also presented in Fig. 8. Under the supply voltage range of 0.2–0.6 V, the ratios of total current and leakage current are around 3%. The delay times are dependent on the supply voltage variations.

B. PROPOSED DCO WITH THE BOOTSTRAPPED AND FORWARD INTERPOLATION TECHNIQUES

Fig. 9 (a) illustrates the block diagram of the proposed multiphase DCO. A current-mode scheme was used to tune the operating frequency and a delta-sigma modulator (DSM) was used to increase the resolution of the DCO. For the inverter cell of the DCO, an interpolator scheme with a bootstrapped technique was operated at a low supply voltage. In the forward interpolator scheme, a main loop path was adopted to create multiphase outputs and an aided path (2$^{\mathrm{nd}}$ loop) was adopted to achieve high operating frequency, as depicted in Fig. 9 (b) [13], [33]–[36]. In the stable ring oscillator, the output phase has only one phase value. An N-stage ring oscillator with a 3-stage sub-feedback loop scheme has three conditions for the all possible conditions as reported in [33]. When N is equal to $3p+1$, the relationship between N and the phase angle can be expressed as follows: $\theta=(240°+(120/N))$. In this study, Fig. 9 (b) presents a 10-phase oscillator with a

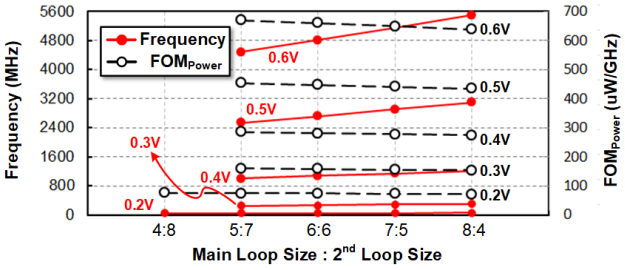


FIGURE 10. Variations in the operating frequency and power-delay product (FOM_{Power}) with the supply voltage.

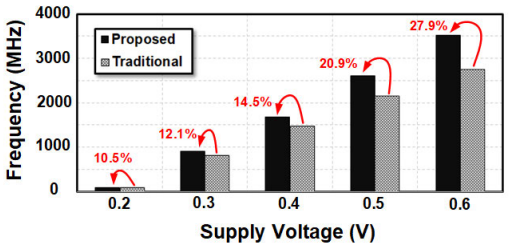


FIGURE 11. Variations in the operating frequencies of the conventional and proposed bootstrapped ring oscillators under the supply voltage.

3-stage sub-feedback loop ($N = 3p + 1$). The equation of the phase position and phase angle can be expressed as follows:

$$\mathrm{P} < \mathrm{i} >= (\mathrm{i} \times \theta) \bmod 360^{\circ} \tag{2}$$

where i is a positive integer. The relationship between the phase (θ) and the phase position (P <9:0>) is defined by Eq. (2) [34]. Fig. 10 shows the simulated results of size ratio of main loop (10-stage ring oscillator) and 2nd loop (3-stage sub-feedback loop). The results indicate that the operating frequency and power-delay product (FOM_{Power}) vary with the supply voltage. This simulation used a traditional inverter to determine the optimized size design. For a fair comparison, the total size of the main loop and 2nd loop (SL) is maintained constant. If the size ratio of the main loop and SL is too large or small, the ring oscillator causes non-oscillation or has the same phases (less than oscillator's output number). Thus, the size ratio of the main loop and SL should be designed carefully. In Fig. 10, the optimized size ratio of the main loop and SL is 2:1 (8:4). This size ratio also exhibits the maximum operating frequency and minimum power-delay product, even at a supply voltage of 0.2 V. Therefore, this 10-phase DCO achieves a maximum operating frequency as high as an operating frequency of a 3-stage ring oscillator and achieves a higher operating frequency [37].

Fig. 11 depicts the operating frequencies of the conventional and proposed bootstrapped ring oscillators under the supply voltage vary. A ten-stage ring oscillator and a ten-stage bootstrapped ring oscillator with a forward interpolation technique were used in the simulation of the traditional and proposed schemes, respectively. The operating frequency of the proposed ring oscillator was 27.9% and 10.5% higher than that of the conventional scheme at 0.6 V and 0.2 V,

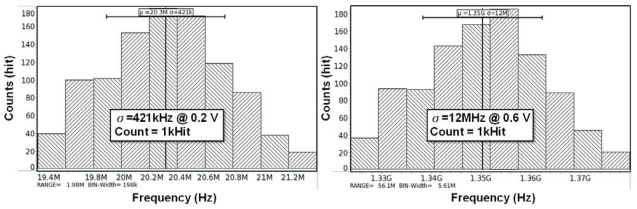


FIGURE 12. Monte Carlo simulations for the proposed DCO at 0.2 V and 0.6 V.

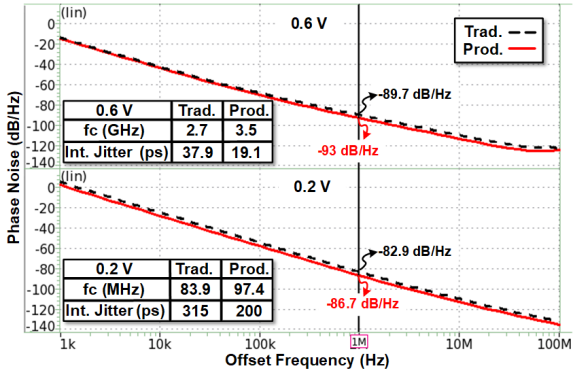


FIGURE 13. Simulated results of phase noise for the traditional and proposed DCOs.

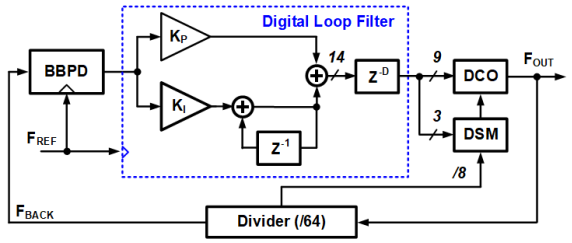


FIGURE 14. Block diagram of the ADPLL.

respectively. Fig. 12 displays the simulated the process variations of the proposed DCO at 0.2 V and 0.6 V. The standard deviations are 421 kHz and 12 MHz, with means of 20.3 MHz (at 0.2 V) and 1.35 GHz (at 0.6 V), respectively, at Monte Carlo simulations of 1000 hits. The mean frequency variations are 2% at 0.2 V and 0.8% at 0.6 V, therefore, the process variation did not considerably affect the operation of the device at a low supply voltage. Fig. 13 presents the simulated results of phase noise of the traditional and proposed DCOs at 0.2 V and 0.6 V. the proposed DCO can achieve the better phase noise and obtain the higher operating frequency. The integrated jitter (Int. jitter) is used to compare their jitter performance. The offset frequency range is from 100 kHz to 10 MHz.

C. ARCHITECTURE OF THE ADPLL

Fig. 14 illustrates the block diagram of the proposed ADPLL, which consists of a BBPD, digital loop filter (DLF), DCO, DSM, and divider (/64). In DLFs, a retiming circuit (Z^{-D}) is used to isolate the glitches resulting from adders to obtain

superior jitter performance. A larger D increases the output jitter, as reported in [38]. Thus, the value of D was selected as 1 in this study. When the ADPLL began its operation, the BBPD created phase and frequency errors. The phase and frequency errors were detected and converted to a digital code and applied to the DLF to align the DCO and reference frequencies. The phase error between F_{REF} and F_{BACK} was determined in the BBPD. The signal *Sign* determined whether the control code of the DLF would increase or decrease. To increase the resolution of the DCO, a three-bit DSM was used. The DSM can improve the resolution of the DCO by eight times. The division ratio should be determined according to the speed of the subcircuits [2]. In this study, the output frequency was divided by 64 and the sample clock of the DLF was used as the reference frequency. Therefore, the clock of the three-bit SDM should be one-eighth the output frequency.

A second-order analog PLL was used to analyze the frequency response of the ADPLL [39]. A proportional–integral scheme was used in the DLF algorithm (Fig. 14), where K_P is a proportional item of DLF parameter and K_I is an integral item of DLF parameter. The loop function of the ADPLL is calculated as follows:

$$G(s) = \frac{2\Pi K_{DCO} K_{PD} F_{REF} KI}{s^2 N}\left(1 + \frac{s}{\omega_z}\right) \tag{3}$$

where K_{DCO} and N denote the gains of the DCO and the divisor of the divider, respectively; ω_z represents the zero frequency, which is equal to $K_I F_{REF}/K_P$; and K_{PD} is the BBPD gain, which can be defined as follows [39]:

$$K_{PD} = \frac{1}{\sigma_j \sqrt{2\pi}} \tag{4}$$

where σ_j is the standard deviation of the Gaussian clock jitter ($\sigma_j = RMS_{jitter}/T_{REF}$). According to the condition $UG(s = j\,\omega_{UGBW})\ U = 1$, the DLF parameter of K_P is calculated as follows:

$$K_p = \frac{\sigma_j N \omega_{UGBW} \sin(PM)}{\sqrt{2\pi K_{DOC}}} \tag{5}$$

where the phase margin of the ADPLL is $\tan^{-1}(\omega_{UGBW}/\omega_z)$ and ω_{UGBW} is the unity gain frequency for this transfer function. Thus, the DLF parameter of K_I can be expressed as follows:

$$K_I = \frac{K_P \omega_{UGBW}}{F_{REF} \tan(PM)} \tag{6}$$

We examined the ADPLL design parameters for a voltage supply range of 0.2 V and 0.6 V. In Table 2, the phase margin and unity gain bandwidth values are defined assuming that the standard deviation of the Gaussian clock jitter (σ_j) is 0.5%. The DCO gains corresponded to the simulated results at 0.2 V and 0.6 V. When the multiplication factor was 64, the output frequencies were 20 MHz and 1 GHz at 0.2 V and 0.6 V, respectively. The DCO ranges at 0.2 V and 0.6 V are from 14.3 to 24.6 MHz and from 933 to 1205 MHz, respectively. Therefore, the phase margin and unity gain bandwidth were 62.64° and 18.8 kHz, respectively, at 0.2 V. The phase margin

TABLE 2. Parameters of the ADPLL.

Parameter	ADPLL	
Supply Voltage (V)	0.6	0.2
Output Frequency (MHz)	1000	20
DCO Gain (kHz/LSB)	83.25	2.14
Reference Frequency (Hz)	15.625M	312.5k
BBPD Gain	79.78 ($\sigma_{\Delta t}$=0.005)	
Divider	64	
DLF Parameters	$K_P=2^0$; $K_I=2^{-5}$	
Phase Margin (deg)	57.68	62.64
Unit Gain Bandwidth (kHz)	770	18.8

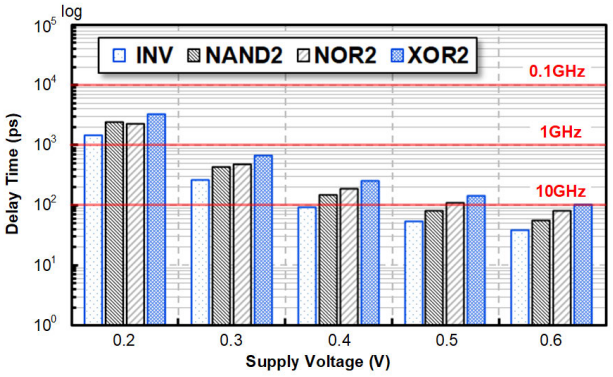


FIGURE 15. Variations in the delay times of the inverter, NAND gate, NOR gate, and XOR gate with the power supply.

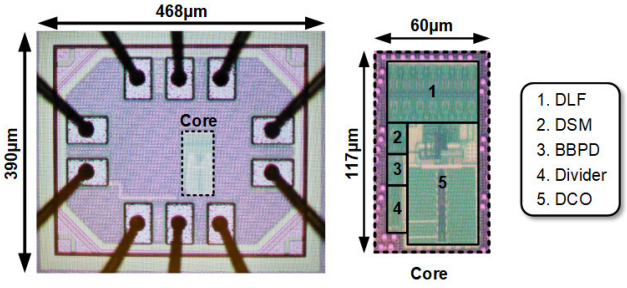


FIGURE 16. Chip photograph of the proposed ADPLL.

and unity gain bandwidth were 57.68° and 770 kHz, respectively, at 0.6 V.

For operating frequency of logic gate designs, the low-threshold voltage devices are used for low supply voltage circuits. The threshold voltages of NMOS and PMOS are both around 200 mV. Under the NMOS and PMOS sizes (L/W) are 0.2um/0.1um and 0.6um/0.1um, respectively. The NMOS and PMOS currents are 30 uA and 25 uA at 0.6 V, respectively. The NMOS and PMOS currents are 500 nA and 300 nA at 0.2 V, respectively. Fig. 15 presents the simulated delay times (sum of the rise time and fall time) of the inverter, NAND, NOR, and XOR gates when the supply voltage range is form 0.2 V to 0.6 V. For this simulation, delay chains

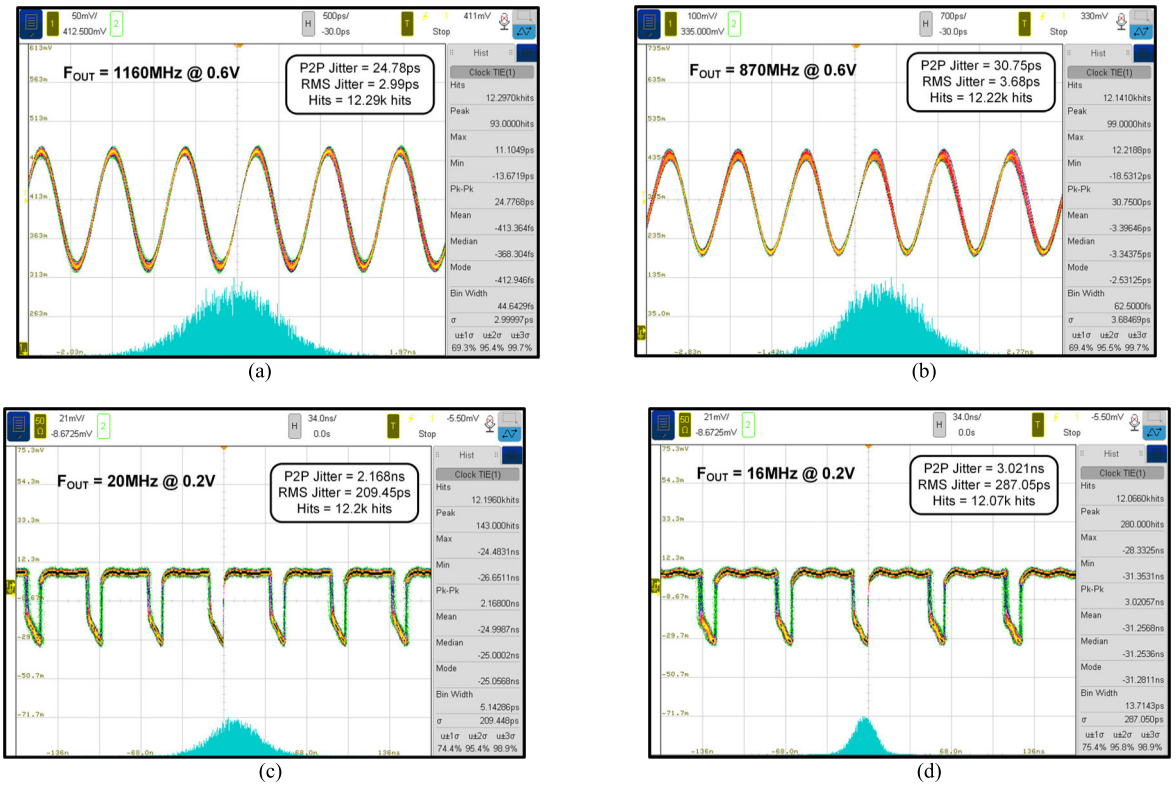


FIGURE 17. Jitter performance: (a) 1160 MHz at 0.6 V, (b) 870 MHz at 0.6 V, (c) 20 MHz at 0.2 V, and (d) 16 MHz at 0.2 V.

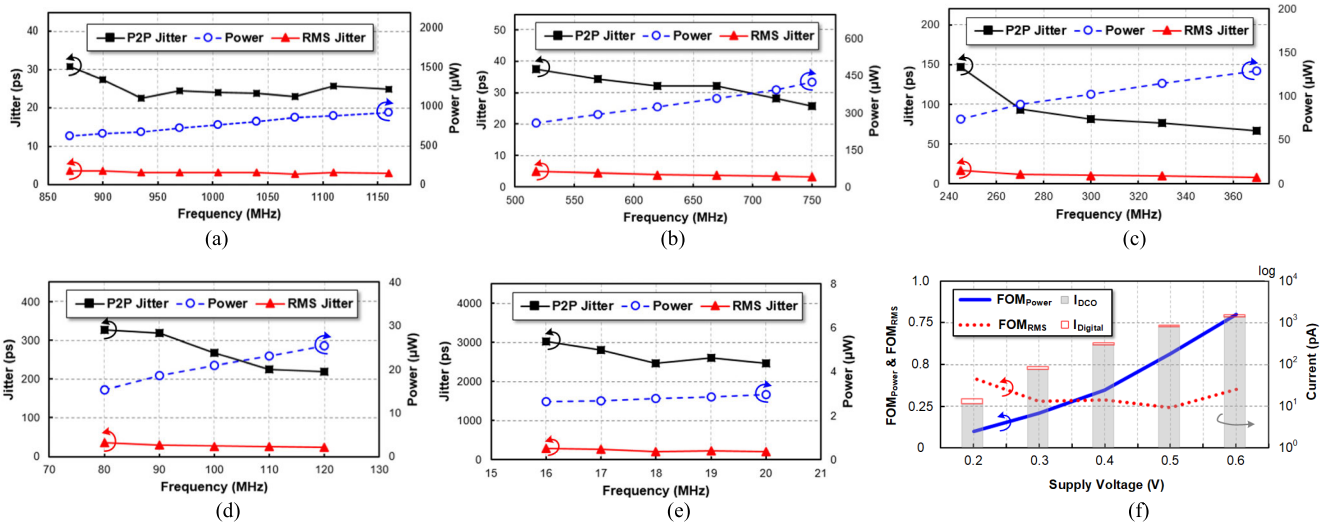


FIGURE 18. Jitter performance and power consumptions at (a) 0.6 V, (b) 0.5 V, (c) 0.4 V, (d) 0.3 V, (e) 0.2 V and (f) the measured performances under supply voltage variations.

are used to measure the rise time and fall time at the input frequency of 20 MHz. The voltage swing can be defined by rise time and fall time. In general, the output voltage of the logic circuit has a full swing, which is a critical factor for digital signals. Therefore, the XOR gate can use operating frequencies of 300 MHz at 0.2 V and 1 GHz at 0.6 V. In this ADPLL, the operating frequencies of the digital part are less than 312.5 kHz at 0.2 V and 18.125 MHz at 0.6 V. However, the delay time increases by a large value when the supply voltage is less than 0.3 V.

III. IMPLEMENTATION OF AND EXPERIMENTAL RESULTS FOR THE PROPOSED ADPLL

Fig. 16 displays the chip photograph of the proposed ADPLL. The chip area and core area of the test chip were 390 × 468 μm^2 and 60 × 117 μm^2, respectively, in a

TABLE 3. Performance comparison between the proposed ADPLL and other ADPLLs.

	This Work		[4]		[1]	[40]	[2]		[36]
Technology (nm)	90		28		90	65	90		90
Supply Voltage (V)	0.6	0.2	0.6	0.3	0.52	0.52/0.58	0.5	0.25	0.6
Phase Number	10		4		8	8	5		8
Operating Frequency (MHz)	1160	20	617	20	120	245	480	48	1600
RMS Jitter (ps)	2.99/48*	209.5	--		26.8	11.9* (0.55V)	7.9	103	3.8
P2P Jitter (ps)	24.78	2168	--		155	--	61.1	--	33.7
RMS Jitter/Period (%)	0.35	0.42	--		0.32	0.15	0.38	0.49	0.61
Area (mm^2)	0.007		0.043		0.065	0.049	0.057		0.036
Power (μW)	912.6	2.94	669	7.74	37	30*	78	3	9100
Int. Jitter (ps) (Range)	48 (10k-10M)	--	9.45 (10k-100M)	--	--	--	23.6 (10k-10M)	894.2 (10k-10M)	--
FOM_{Jitter} (dB)	-206.8	--	-222.2	--	--	-222*	-223.6	-206.2	--
FOM_{Power} (μW/MHz)	0.8	0.1	1.1	0.4	0.3	0.2	0.2	0.1	5.7

* at 130 MHz ; $FOM_{Jitter} = 10\log[(\text{Int. Jitter}/1s)^2(\text{Power}/1mW)]$; FOM_{Power}= Power / Operating Frequency.

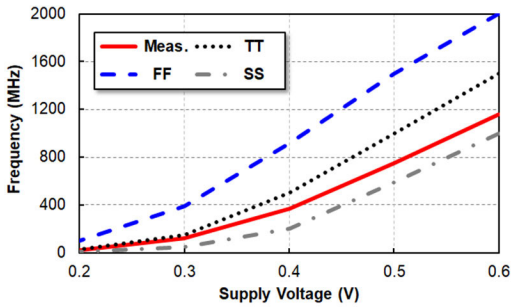


FIGURE 19. Measured and simulated results of ADPLL frequencies under various supply voltages.

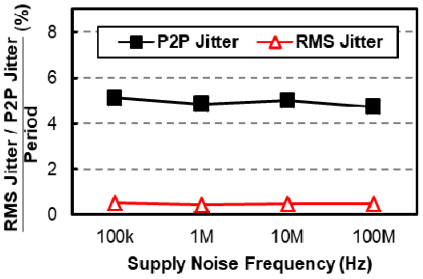


FIGURE 20. Variations in the jitter and period under the supply voltage with the supply noise frequency.

90-nm CMOS. Fig. 17(a) and (b) represents the maximum and minimum operating frequencies and jitter histogram at 0.6 V, respectively. The power consumptions at 1160 MHz and 870 MHz were 912.6 μW and 616.8 μW, respectively. Fig. 17(c) and (d) represents the maximum and minimum operating frequencies and jitter histogram at 0.2 V, respectively. The power consumptions at 20 MHz and 16 MHz were 2.94 μW and 2.62 μW, respectively. Fig. 18 illustrates the jitter performance and power consumptions of the proposed ADPLL in the supply voltage range of 0.2–0.6 V. At the supply voltage of 0.6 V, the maximum percentages of P2P and RMS jitters were 2.9% and 0.35%, respectively. At the supply voltage of 0.2 V, the maximum percentages of P2P and RMS jitters were 4.3% and 0.42%, respectively. Fig. 18 (f) summarizes the jitter and power performance for various supply voltage. The terms FOM_{Power} and FOM_{RMS} are the power-delay product and the ratio of the RMS jitter and period, respectively. The currents of DCO and the digital part are also displayed in Fig. 18 (f). The DCO current was majorly consumed by the ADPLL and accounts for 90% of the chip's total current. Fig. 19 displays the measured and simulated results for the ADPLL frequencies in the supply voltage range of 0.2 V to 0.6 V. In the simulated results, the process variations (the TT, FF and SS corners) for different supply voltages were shown in Fig. 19. When the supply voltage was 0.6 V, the measured ADPLL frequency was 1160 MHz and the ADPLL frequency in the TT corner was 1500 MHz. When the supply voltage was 0.2 V, the measured ADPLL frequency was 20 MHz and the ADPLL frequency in the TT corner was 30 MHz. Thus, the measured results were approximately 0.7 times the frequencies of the TT corner.

Fig. 20 depicts the variations in the measured RMS and P2P jitters with the supply noise frequency. The supply voltage of the ADPLL was mixed with a sinusoidal waveform by using a pulse generator for verifying the performance of supply noise suppression. Under a 900-MHz output, the ADPLL operated at 0.6 V $\pm$ 30 mV (10%) and the additional supply noise frequency varied from 100 kHz to 100 MHz. In the absence of supply noise, the RMS and P2P jitters at 900 MHz

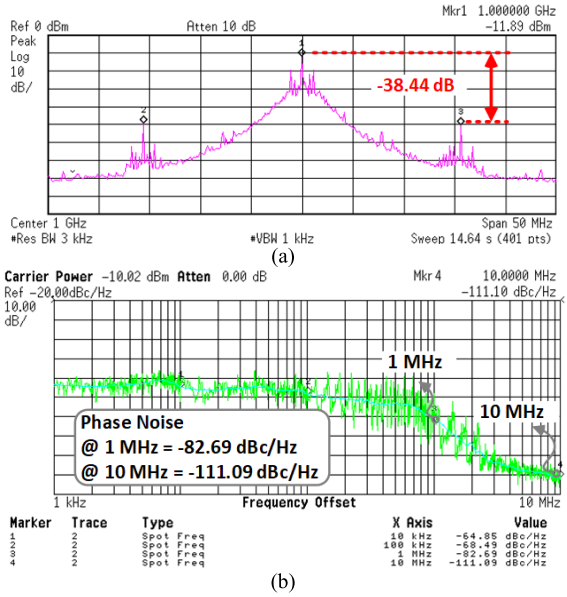


FIGURE 21. Measured results at 1 GHz (a) spectrum (b) phase noise.

were 0.35% and 2.46%, respectively. Under a supply noise of 100 kHz, the RMS and P2P jitters at 900 MHz were 0.51% and 5.13%, respectively. Under a supply noise of 100 MHz, the RMS and P2P jitters at 900 MHz were 0.47% and 4.74%, respectively. Fig. 21 displays the measured spectra of the proposed ADPLL at 1 GHz, and the amplitude difference with the reference spur is 38.44 dB. Fig. 17(b) depicts the measured phase noise at 1 GHz. The phase noise was 82.69 dBc/Hz at a 1 MHz frequency offset. Table 3 lists the performance of the proposed multiphase ADPLL and other ADPLLs presented in the literature. The prior ADPLLs can operate at a lower supply voltage than their process supplied the supply voltage. In addition to multiphase outputs under an ultralow supply voltage, this PLL with the multiphase DCO can achieve higher operating frequency than the previously presented ADPLLs. In [36], an operating frequency of 1.6 GHz with 10 phases was achieved at 0.6 V. However, the power consumption was 9.1mW for the sub-feedback loop scheme. At the operating frequency of 1.1 GHz, the power consumption of the proposed system was eight times lower than that of the design proposed in [36]. For the integrated jitter, the output buffer should be redesigned to archive the stable output signals at an ultra-low supply voltage in our work, such as that [2] adopted the bootstrapped inverters or level shifters as output buffers. The proposed ADPLL implemented in a 90-nm CMOS process can operate at frequencies of 1160 MHz and 20 MHz at 0.6 V and 0.2 V, respectively. The proposed design achieved a higher operating frequency and lower operating voltage than the previously proposed designs.

IV. CONCLUSION

A low-supply-voltage and multiphase ADPLL is proposed in this study. A bootstrapped and interpolated ring oscillator was used in the DCO. MOS varactors were used to save the area cost and replace MIM capacitors in the proposed bootstrapped inverter. The proposed interpolated scheme achieved a high operating frequency at a low supply voltage. The proposed ADPLL can operate at frequencies of 1160 MHz and 20 MHz at 0.6 V and 0.2 V, respectively. A sub-0.6 V 10-phase ADPLL was fabricated in a 90-nm CMOS process. This ADPLL exhibited a good jitter performance, a small area, and low power consumption and required ultralow supply voltage.

ACKNOWLEDGMENT

The authors thank the Ministry of Science and Technology (MOST) and the Taiwan Semiconductor Research Institute (TSRI), Taiwan, for their support in the use of EDA tools and the fabrication of the test chip. They also thank Wen-Yuan Tsai for the support of the simulation and measurement.

REFERENCES

[1] C.-C. Chung, W.-S. Su, and C.-K. Lo, "A 0.52/1 V fast lock-in ADPLL for supporting dynamic voltage and frequency scaling," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 1, pp. 408–412, Jan. 2016.

[2] Y. Ho, Y.-S. Yang, C.-C. Chang, and C. Su, "A near-threshold 480 MHz 78 μW all-digital PLL with a bootstrapped DCO," *IEEE J. Solid State Circuits*, vol. 48, no. 11, pp. 2805–2814, Nov. 2013.

[3] K.-H. Cheng, J.-C. Liu, and H.-Y. Huang, "A 0.6-V 800-MHz all-digital phase-locked loop with a digital supply regulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 12, pp. 888–892, Dec. 2012.

[4] M. Lee, S. Kim, H.-J. Park, and J.-Y. Sim, "A 0.0043-mm^2 0.3–1.2-V frequency-scalable synthesized fractional-N digital PLL with a speculative dual-referenced interpolating TDC," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 99–108, Jan. 2019.

[5] A. Elkholy, S. Saxena, R. K. Nandwana, A. Elshazly, and P. K. Hanumolu, "A 2.0–5.5 GHz wide bandwidth ring-based digital fractional-N PLL with extended range multi-modulus divider," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1771–1784, Aug. 2016.

[6] Y. Zhang, X. Liu, W. Rhee, H. Jiang, and Z. Wang, "A 0.6 V 50-to-145 MHz PVT tolerant digital PLL with DCO-dedicated $\Delta\Sigma$ LDO and temperature compensation circuits in 65 nm CMOS," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 28–31.

[7] N. Pourmousavian, F.-W. Kuo, T. Siriburanon, M. Babaie, and R. B. Staszewski, "A 0.5-V 1.6-mW 2.4-GHz fractional-N all-digital PLL for Bluetooth LE with PVT-insensitive TDC using switched-capacitor doubler in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2572–2583, Sep. 2018.

[8] X. Chen, J. Breiholz, F. B. Yahya, C. J. Lukas, H.-S. Kim, B. H. Calhoun, and D. D. Wentzloff, "Analysis and design of an ultra-low-power Bluetooth low-energy transmitter with ring oscillator-based ADPLL and 4× frequency edge combiner," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1339–1350, May 2019.

[9] W.-H. Chen, W.-F. Loke, and B. Jung, "A 0.5-V, 440-μW frequency synthesizer for implantable medical devices," *IEEE J. Solid State Circuits*, vol. 47, no. 8, pp. 1896–1907, Jul. 2012.

[10] K.-H. Cheng, Y.-C. Tsai, Y.-L. Lo, and J.-S. Huang, "A 0.5-V 0.4–2.24-GHz inductorless phase-locked loop in a system-on-chip," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 5, pp. 849–859, May 2011.

[11] J.-W. Moon, S.-G. Kim, D.-H. Kwon, and W.-Y. Choi, "A 0.4-V, 500-MHz, ultra-low-power phase-locked loop for near-threshold voltage operation," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2014, pp. 15–17.

[12] J.-W. Moon, K.-C. Choi, and W.-Y. Choi, "A 0.4-V, 90-350 MHz PLL with an active loop-filter charge pump," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 319–323, May 2014.

[13] S.-G. Kim, J. Rhim, D.-H. Kwon, M.-H. Kim, and W.-Y. Choi, "A low-voltage PLL with a supply-noise compensated feedforward ring VCO," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 6, pp. 548–552, Jun. 2016.

[14] J. Zhu, R.-K. Nandwana, G. Shu, A. Elkholy, S.-J. Kim, and P.-K. Hanumolu, "A 0.0021 mm^2 1.82 mW 2.2 GHz PLL using time-based integral control in 65 nm CMOS," *IEEE J. Solid State Circuits*, vol. 52, no. 1, pp. 8–20, Jan. 2017.

[15] Z. Zhang, J. Yang, L. Liu, P. Feng, J. Liu, and N. Wu, "A 0.9–2.25-GHz sub-0.2-mW/GHz compact low-voltage low-power hybrid digital PLL with loop bandwidth-tracking technique," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 5, pp. 933–944, May 2018.
[16] *International Technology Roadmap for Semiconductors 2.0-Section 1: System Integration*, Int. Technol. Roadmap Semicond., Semicond. Ind. Assoc., San Jose, CA, USA, Jun. 2015, pp. 15–16.
[17] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, Sep. 2012.
[18] S. Drago, D. M. W. Leenaerts, B. Nauta, F. Sebastiano, K. A. A. Makinwa, and L. J. Breems, "A 200 μA duty-cycled PLL for wireless sensor nodes in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1305–1315, Jul. 2010.
[19] B. Liu, Y. Zhang, J. Qiu, H. C. Ngo, W. Deng, K. Nakata, T. Yoshioka, J. Emmei, J. Pang, A. T. Narayanan, H. Zhang, T. Someya, A. Shirane, and K. Okada, "A fully synthesizable fractional-N MDLL with zero-order interpolation-based DTC nonlinearity calibration and two-step hybrid phase offset calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 2, pp. 603–616, Feb. 2021.
[20] S. Kundu, L. Chai, K. Chandrashekar, S. Pellerano, and B. R. Carlton, "A self-calibrated 2-bit time-period comparator-based synthesized fractional-N MDLL in 22-nm FinFET CMOS," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 43–54, Jan. 2021.
[21] B. Liu, Y. Zhang, J. Qiu, H. Huang, Z. Sun, D. Xu, H. Zhang, Y. Wang, J. Pang, Z. Li, X. Fu, A. Shirane, H. Kurosu, Y. Nakane, S. Masaki, and K. Okada, "A fully-synthesizable fractional-N injection-locked PLL for digital clocking with triangle/sawtooth spread-spectrum modulation capability in 5-nm CMOS," *IEEE Solid-State Circuits Lett.*, vol. 3, no. 1, pp. 34–37, Jan. 2020.
[22] B. Liu, H. C. Ngo, K. Nakata, W. Deng, Y. Zhang, J. Qiu, T. Yoshioka, J. Emmei, H. Zhang, J. Pang, A. T. Narayanan, D. Yang, H. Liu, K. Okada, and A. Matsuzawa, "A 1.2 ps-jitter fully-synthesizable fully-calibrated fractional-N injection-locked PLL using true arbitrary nonlinearity calibration technique," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.
[23] E. Temporiti, C. Weltin-Wu, D. Baldi, R. Tonietto, and F. Svelto, "A 3 GHz fractional all-digital PLL with a 1.8 MHz bandwidth implementing spur reduction techniques," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 824–834, Mar. 2009.
[24] R. B. Staszewski *et al.*, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.
[25] S.-Y. Yang, W.-Z. Chen, and T.-Y. Lu, "A 7.1 mW, 10 GHz all digital frequency synthesizer with dynamically reconfigured digital loop filter in 90 nm COMS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 578–586, Nov. 2010.
[26] J. A. Tierno, A. V. Rylyakov, and D. J. Friedman, "A wide power supply range, wide tuning range, all static CMOS all digital PLL in 65 nm SOI," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 42–51, Jan. 2008.
[27] K.-H. Choi, J.-B. Shin, J.-Y. Sim, and H.-J. Park, "An interpolating digitally controlled oscillator for a wide-range all-digital PLL," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 9, pp. 2055–2063, Sep. 2009.
[28] J. Lin, B. Haroun, T. Foo, J.-S. Wang, B. Helmick, S. Randall, T. Mayhugh, C. Barr, and J. Kirkpatric, "A PVT tolerant 0.18 MHz to 600 MHz self-calibrated digital PLL in 90 nm CMOS process," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2004, pp. 488–489.
[29] W. Liu, W. Li, P. Ren, C. Lin, S. Zhang, and Y. Wang, "A PVT tolerant 10 to 500 MHz all-digital phase-locked loop with coupled TDC and DCO," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 314–321, Feb. 2010.
[30] G. Marucci, S. Levantino, P. Maffezzoni, and C. Samori, "Analysis and design of low-jitter digital bang-bang phase-locked loops," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 1, pp. 26–36, Jan. 2014.
[31] Y. Ho, Y.-S. Yang, and C. Su, "A 0.2–0.6 V ring oscillator design using bootstrap technique," in *Proc. IEEE Asian Solid-state Circuits Conf.*, Nov. 2011, pp. 333–336.
[32] T. Jiang, J. Yin, P.-I. Mak, and R.-P. Martins, "A 0.5-V 0.4-to-1.6-GHz 8-phase bootstrap ring-VCO using inherent non-overlapping clocks achieving a 162.2-dBc/Hz FoM," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 2, pp. 157–164, Mar. 2019.
[33] H.-Y. Huang and F.-C. Tsai, "Analysis and optimization of ring oscillator using sub-feedback scheme," in *Proc. 12th Int. Symp. Design Diag. Electron. Circuits Syst.*, Apr. 2009, pp. 28–29.
[34] Y.-H. Tu, J.-C. Liu, K.-H. Cheng, and C.-Y. Chang, "Low supply voltage and multiphase all-digital crystal-less clock generator," *IET Circuits, Devices Syst.*, vol. 12, no. 6, pp. 720–725, Dec. 2018.
[35] W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada, and A. Matsuzawa, "A fully synthesizable all-digital PLL with interpolative phase coupled oscillator, current-output DAC, and fine-resolution digital varactor using gated edge injection technique," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 68–80, Jan. 2015.
[36] Y.-H. Tu, J.-C. Liu, K.-H. Cheng, H.-Y. Huang, and C.-C. Hu, "A 0.6-V 1.6-GHz 8-phase all digital PLL using multi-phase based TDC," *IEICE Electron. Exp.*, vol. 13, no. 2, pp. 1–12, Jan. 2016.
[37] J. Kim and M. A. Horowitz, "Adaptive supply serial links with sub-1-V operation and per-pin clock recovery," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1403–1413, Nov. 2002.
[38] T.-K. Kuan and S.-I. Liu, "A bang bang phase-locked loop using automatic loop gain control and loop latency reduction techniques," *IEEE J. Solid State Circuits*, vol. 51, no. 4, pp. 821–830, Apr. 2016.
[39] J.-M. Lin and C.-Y. Yang, "A fast-locking all-digital phase-locked loop with dynamic loop bandwidth adjustment," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2411–2422, Oct. 2015.
[40] C.-W. Chang, K.-Y. Chang, Y.-H. Chu, and S.-J. Jou, "Near-threshold all-digital PLL with dynamic voltage scaling power management," *Electron. Lett.*, vol. 52, no. 2, pp. 109–111, Jan. 2016.

JEN-CHIEH LIU received the B.S. and M.S. degrees from the Department of Electronic Engineering, Fu Jen Catholic University, Taipei, Taiwan, in 2004 and 2006, respectively, and the Ph.D. degree from the Department of Electrical Engineering, National Central University, Taoyuan, Taiwan, in 2012.

From 2010 to 2014, he was with the Industrial Technology Research Institute, Zhudong, Taiwan. Since 2014, he has been an Associate Professor with the Department of Electrical Engineering, National United University, Miaoli, Taiwan. His current research interest includes low-power and high-speed clocking systems.

YU-PING LI received the M.S. degree in electrical engineering from the National United University, Miaoli, Taiwan, in 2019. In 2019, she joined M31 Technology Corporation, Zhubei, Taiwan.