A Highly-Integrated Reconfigurable Ka-Band Receiver Supporting Active and Passive Detections in a 90-nm CMOS Technology

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ABSTRACT A highly-integrated reconfigurable Ka-band receiver in a 90-nm CMOS technology is proposed for the applications of satellite wireless communications, remote sensing of atmospheric conditions, and detection of space debris. The proposed receiver can be reconfigured to support active-receiver and passive-receiver modes. At the active-detection mode, it works as a direct-conversion coherent receiver for high-speed and global-coverage satellite communications. Measured conversion gain of 45.2 dB, noise figure of 7.6 dB, and output 1-dB compression point of -6.8 dBm can be acquired at 35 GHz while only consuming 54.4 mW from a 1.2-V supply. As switched to the passive-detection mode, it can potentially operate as a non-coherent radiometer to sense atmospheric conditions which are employed to dynamically compensate the atmospheric attenuation to mitigate the fading effects. This enables the satellite communication systems to establish reliable links. Moreover, the proposed passive receiver can be utilized to detect the space debris. Collisions can be avoided and hence satellite lifetime can be enhanced. Experimental results show that the proposed receiver at the passive-detection mode exhibits voltage responsivity of 1.2 GV/W and noise equivalent power (NEP) of 2.1 aW/Hz$^{0.5}$ at 35 GHz. The power dissipation is only 49.6 mW from a supply voltage of 1.2 V. To the best of the authors' knowledge, the proposed receiver owns the highest responsivity and the lowest NEP at Ka-band reported thus far. It is also the first receiver capable of being reconfigured to support active-detection and passive-detection modes according to different application scenarios.

INDEX TERMS Reconfigurable, Ka-band, CMOS, active receiver, passive receiver, satellite communications, radiometer, effect of fading, space debris.

I. INTRODUCTION

Satellite communications (SATCOM) have drawn great attention in recent years since they are potential candidates to provide a wireless service with low latency and high speed anytime and anywhere [1]–[4]. They are also considered as key enablers for the next sixth-generation (6G) wireless communication systems to supply Gbps communication capability for extreme coverage including sky, sea, and space [5]. A great number of low-earth-orbit (LEO) satellites must be deployed in order to establish a dense wireless network, implying that the reduction of the weight, volume, and cost are extremely desired for these satellites. Obviously, CMOS technologies are attractive candidates to realize the satellite systems because they can provide a low-cost, high-integration, high-yield, and light-weight solution.

The path delay problem is an issue for satellite communications [6]–[8]. The systems must acquire atmospheric conditions at different locations and different times in order to compensate the dynamic atmospheric attenuation to mitigate the fading effects. Traditionally, ground-based radiometric instruments are used to measure temperature, water vapor content, and cloud liquid water [9]–[11]. However, the high cost and bulky volume dramatically limit the availability

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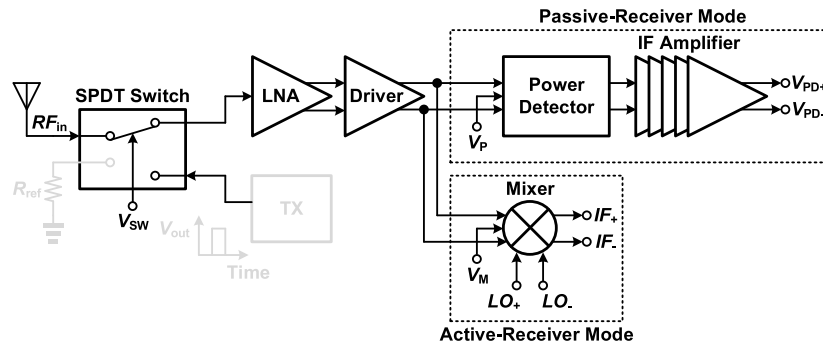
FIGURE 1. Proposed reconfigurable Ka-band receiver architecture.

of measurements, leading to incomplete information for the satellite communication systems to provide a reliable wireless link. On the other hand, space debris is a great concern [12]. Collisions with the debris are detrimental to the satellites. Suitable sensors must be installed to detect the debris and execute the required actions promptly to avoid collisions. This not only can stabilize the satellite wireless network, but it can also increase the satellite lifetime. Apparently, it will be much beneficial to the satellite communication systems if the satellite could equip with a radiometer and a collision-detected sensor simultaneously.

A wireless receiver is a key component of the satellite communication systems. Many Ka-band receivers have been reported in literatures using SiGe BiCMOS, GaN, and CMOS technologies [13]–[26]. Yet these receivers are only for the communication purpose, not supporting a radiometric function capable of dynamically measuring the atmospheric conditions. Certainly some microwave and millimeter-wave radiometers were presented to sense the atmospheric conditions and realize passive imagers [6], [27]–[32]. However, they only provide the radiometric function without any wireless communication capability. To supply radiometric and communication functions simultaneously, two independent bulky modules must be put together, inevitably increasing the system weight, cost and volume, which is particularly undesired for satellite communication systems.

In this paper, we propose a reconfigurable Ka-band receiver realized in a 90-nm CMOS technology which can solve the aforementioned issues. The proposed receiver can support active and passive detections simultaneously in a single chip. This not only reduces the cost, but it can also decrease the system weight and volume, which is greatly desired for satellite communication systems. Moreover, the passive-detection capability can be employed to detect space debris. Prompt actions can be executed in time to avoid collisions and hence increase the satellite lifetime. As the operation frequency is 35 GHz, the proposed receiver can provide conversion gain of 45.2 dB and double-sideband (DSB) noise figure (NF) of 7.6 dB at the active-receiver mode while giving measured voltage responsivity R_V of 1.2 GV/W and noise equivalent power (NEP) of 2.1 aW/Hz$^{0.5}$ at the

passive-receiver mode. To the best of the authors' knowledge, the proposed receiver exhibits the highest R_V and lowest NEP reported thus far. Furthermore, it is also the first Ka-band receiver which can be reconfigured to provide active- and passive-receiver modes simultaneously. Such a Ka-band receiver capable of providing communication capability, atmospheric sensing, and debris detection are very suitable for the next 6G satellite wireless communication systems which require reliable, low-cost, small-volume, and light-weight solutions. This paper is organized as follows. Section II explains the concept of the proposed reconfigurable receive architecture which can be programmed to support active and passive receiver modes. Subblock circuit designs are presented in Section III. Section IV illustrates the experimental results. Finally, Section V concludes this work.

II. KA-BAND RECONFIGURABLE RECEIVER ARCHITECTURE

Fig. 1 shows the proposed reconfigurable Ka-band receiver architecture in a 90-nm CMOS technology which can support active-receiver and passive-receiver modes for satellite communication and radiometer applications. The subblocks shown in grey colors are not included in this work, but they can be easily realized in the future system integration. The receiver integrates a single-pole-double-throw (SPDT) switch, a low-noise amplifier (LNA), a RF driver, a mixer, a power detector (PD), and an IF amplifier into a single chip. As working at the active-receiver mode, the control voltage V_P and V_M are set as 0 and 0.45 V to disable the power detector and enable the mixer, respectively. By doing this, the architecture becomes a time-division duplexing (TDD) direct-conversion transceiver which can be used for satellite communication applications. By contrast, the receiver is switched to the passive-receiver mode as the control voltage V_P and V_M are changed to 0.3 and 0 V to enable the power detector and disable the mixer, respectively. As integrated with a double-pole-double-throw (DPDT) switch shown in grey colors in Fig. 1, not included in this work, the receiver input can be switched between the antenna port and a reference resistor R_{ref} of 50 Ω to form a Dicke radiometer architecture. Hence the atmospheric conditions, such as temperature,
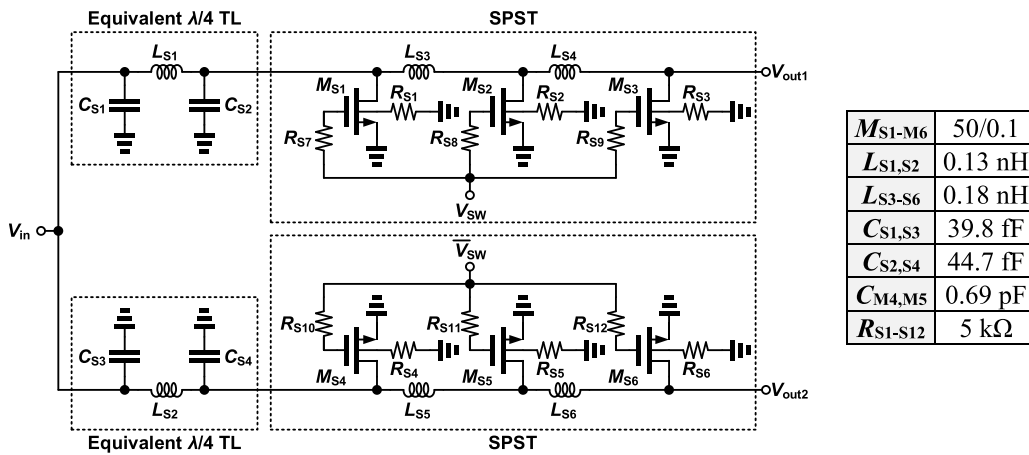
FIGURE 2. Schematic of the proposed SPDT switch.

M_{S1-M6}	50/0.1
$L_{S1,S2}$	0.13 nH
L_{S3-S6}	0.18 nH
$C_{S1,S3}$	39.8 fF
$C_{S2,S4}$	44.7 fF
$C_{M4,M5}$	0.69 pF
R_{S1-S12}	5 kΩ

water vapor content, and cloud liquid water, can be measured at every location and anytime. The collected atmospheric information is then fed back to the satellite systems and stored to dynamically compensate the atmospheric attenuation to mitigate the fading effect for reliable satellite links. Moreover, at the passive-receiver mode, all other subblocks, except the passive receiver, can be turned off to reduce the system power dissipation.

The proposed radiometer architecture can also be used to detect space debris to increase the satellite lifetime. As shown in Fig. 1, the transmitter (TX) can be designed to regularly emit a short pulse to the space by a single-pole-single-throw (SPST) switch. If no space debris exists along the locus of the satellites' orbit, no signals are reflected back and the output of the radiometer will keep quite. On the contrary, if the space debris is unfortunately appeared on the orbit, the transmitted pulse signal will be reflected back by the debris and received by the proposed receiver. The receiver output will have nonzero voltage and can be processed to provide a digital-high warning signal to detour the satellite for collision prevention. Once the crisis is solved, the satellite could then go back to its normal altitude. In order to achieve this goal, the receiver must own high voltage responsivity R_V and sensitivity to detect a weak reflected signal. In this work, our proposed receiver can give measured R_V of 1.2 GV/W at 35 GHz, implying that the receiver will produce 1.2-mV output voltage if it receives a weak power of -90 dBm. Assume that the transmitter output power, the transmitter antenna gain, the receiver antenna gain, and the cross-section area of the debris are 30 dBm, 50 dBi, 50 dBi, and 100 cm^2, respectively. The power of the reflected signal received by the receiver can be calculated to be -88.9 dBm using the radar range equation as the distance between the satellite and the debris is 1.3 km. The LEO satellite travels at a speed of around 7.8 km/s. Hence the satellite has response time of roughly 0.2 second, long enough to detour its path from collisions. The following section will go through the design details of each subblock of the proposed reconfigurable receiver.

III. SUBBLOCK CIRCUIT DESIGNS
A. SPDT SWITCH DESIGN
Fig. 2 illustrates the proposed SPDT switch composed of two quarter-wave transmission lines (TL) and two single-pole-single-throw (SPST) switches. As the SPST switch on the top path is turned off, i.e., $V_{SW} = 1.2$ V, the $\lambda/4$ TL on the top path transforms a short circuit at its output to an open circuit at its input. By doing this, the input signal V_{in} can go smoothly to V_{out2} through the bottom path. The same principle can be applied to direct the input signal to V_{ou1} by setting V_{SW} equal to 0 V. To reduce the chip size, these quarter-wave transmission lines are realized by equivalent π-networks comprised of L_{S1}, C_{S1}, and C_{S2} and L_{S2}, C_{S3}, and C_{S4}, respectively. The SPST switches adopt a two-stage travelling-wave architecture to increase the isolation between the input and output ports. Moreover, 5-kΩ resistors R_{S1-S6} are added to the body nodes of the transistors M_{S1-S6}, which not only reduces the insertion loss, but it can also enhance the isolation. Fig. 3 illustrates the simulated insertion loss (IL) and isolation (ISO) of the SPDT switch. The proposed switch can give insertion loss of 2.2 dB while providing isolation of 43.5 dB without dissipating any dc power.
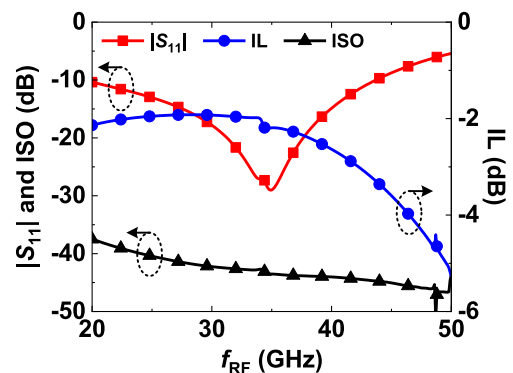

FIGURE 3. Simulated insertion loss and isolation of the proposed SPDT switch.
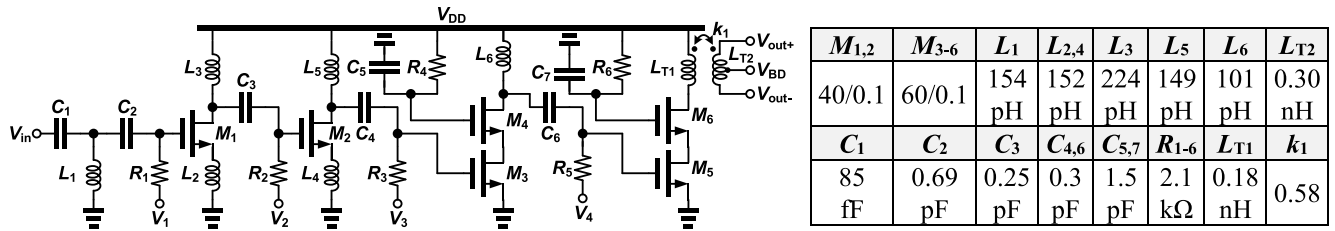
$M_{1,2}$	M_{3-6}	L_1	$L_{2,4}$	L_3	L_5	L_6	L_{T2}
40/0.1	60/0.1	154 pH	152 pH	224 pH	149 pH	101 pH	0.30 nH
C_1	C_2	C_3	$C_{4,6}$	$C_{5,7}$	R_{1-6}	L_{T1}	k_1
85 fF	0.69 pF	0.25 pF	0.3 pF	1.5 pF	2.1 kΩ	0.18 nH	0.58

FIGURE 4. Schematic of the proposed Ka-band LNA.

B. LNA AND RF DRIVER DESIGNS

An LNA needs to have low noise while providing enough gain to suppress the noise contribution from the following stages. Fig. 4 illustrates the proposed 35-GHz LNA schematic. The device parameters are also shown. $R_{1-3,5}$ and $C_{3,4,6}$ are bias resistors and dc blocking capacitors, respectively. The LNA cascades four stages in order to give enough gain at Ka band. The noise from the first stage is critical to the overall noise performance. The number of used active transistors shall be as few as possible. A common-source (CS) topology with a single transistor M_1 is thus chosen to realize the first stage. The transistor size of 40 μm is selected to have minimum noise figure NF_{min} of 2.3 dB while providing maximum available gain of 10.8 dB as biased at the optimal current density of 150 μA/μm. Moreover, in order to achieve simultaneous noise and impedance matching (SNIM), a source degeneration inductor L_2 and an input T-matching network composed of C_1, C_2 and L_1 are utilized to adjust the input impedance Z_{in} and the complex conjugate of the optimal noise impedance Z_{opt}^* to be close to 50 Ω. As depicted in Fig. 5, the LNA NF is equal to NF_{min} and S_{11} circulates around the center of the Smith chart at 35 GHz, i.e., the SNIM condition is reached. The drain inductor L_3 is used to resonate out the parasitic capacitance at the M_1 drain to boost the gain at frequency of interest. Since the priority of the first stage is designed to exhibit NF as low as possible, its gain is not high enough to completely suppress the noise contribution from the second stage. The second stage must adopt the same CS topology to

have low-noise performance. On the contrary, the noise from the third and fourth stages is well suppressed by the gain of the first two stages. The third and fourth stages can thus be realized by a cascode topology for high gain. R_4 and C_5 and R_6 and C_7 form low-pass networks to ac ground the M_4 and M_6 gates for stability consideration.

The LNA needs to provide differential output in order to drive the next RF driver stage. A resonator coupling technique is utilized to give the required single-ended to differential conversion [33], [34]. As shown in Fig. 6(a), a transformer and the parasitic capacitances from the LNA output and the driver input form a resonator coupling network. The turn ratio of the transformer is designed to be around 1.3 to match the impedance transformation ratio between the LNA output and the driver input. The simulated gain and phase imbalance of the balun are 2.1 dB and 3.7° at 35 GHz, respectively. Fig. 7 illustrates the LNA simulation results. The proposed LNA can provide gain of 41.9 dB gain, NF of 4.7 dB, and
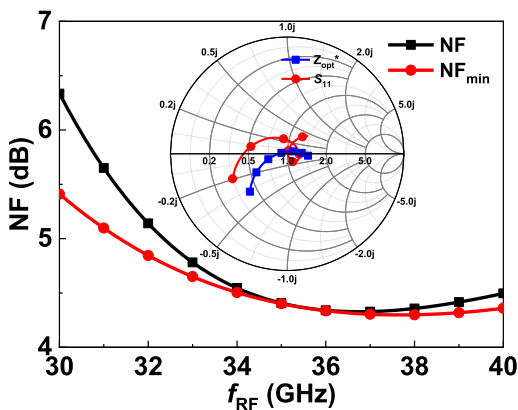

FIGURE 6. (a) Physical structure of the LNA output balun. (b) Schematic of the RF driver.

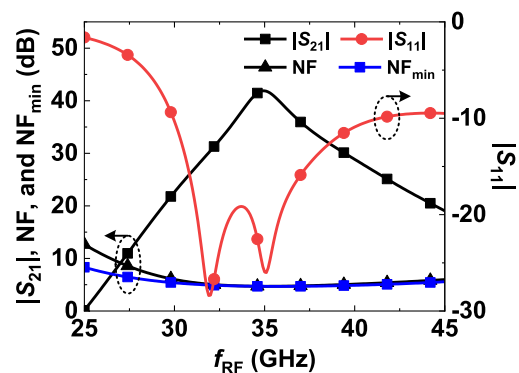**FIGURE 5.** Simulated NF and NF versus the RF frequency.

FIGURE 7. LNA simulation results.

input return loss $|S_{11}|$ of -26 dB at 35 GHz while only consuming 29.9 mW from a 1.2-V supply.

As shown in Fig. 6(b), the driver stage adopts a pseudo-differential amplifier with peaking inductors L_{D1} and L_{D2} at transistor drains. The driver can make sure the LNA output impedance keeps fixed as the mixer and power detector turn on and off and vice versa, respectively. The gate bias V_{BD} of the transistors M_{D1} and M_{D2} is directly applied through the center tap (CT) of the LNA output balun. V_{BD} of 0.5 V is designed to enable the driver to give 2.4 dB gain at 35 GHz and dissipate 14.3 mW from a 1.2-V supply.

C. POWER DETECTOR AND IF AMPLIFIER DESIGNS

A power detector is used to detect the power level of the input signal. It generates an output voltage proportional to the input power value. Fig. 8 shows the proposed power detector which utilizes the even-order nonlinearity of the transistors M_{P1} and M_{P2} to rectify input ac signal to produce corresponding dc output voltage. $C_{P1,P2}$ and $R_{P1,P2}$ are dc blocking capacitors and bias resistors, respectively. The voltage responsivity R_V can be derived as

$$R_V = K_{2,gm}R_P R_{in}, \quad (1)$$

where $K_{2,gm}$, R_P, and R_{in} are the second-order nonlinear coefficient, the load resistor, and the real part of the detector's input impedance, respectively [35]. The noise equivalent power which is mainly contributed by the channel's thermal noise and transistor's flicker noise and the thermal noise from the load resistors can also be derived as

$$NEP = \frac{\sqrt{4kT\gamma g_m}R_P + \sqrt{4kTR_P} + \sqrt{K_{1/f}/(C_{ox}WLf)}g_m R_P}{R_V}. \quad (2)$$

From (1) and (2), higher $K_{2,gm}$ and R_P are desired to provide higher R_V, which also minimizes NEP simultaneously. Higher R_P can give higher R_V, whereas it also reduces the detector's output bandwidth. In this work, the power detector shall be able to process a 1-ns pulse for the debris detection. Hence the load resistor R_P is designed as 8 kΩ to satisfy this requirement. $K_{2,gm}$ can be optimized by choosing appropriate gate bias. Fig. 9(a) shows the simulated R_V versus the gate bias $V_{P1} = V_{P2} = V_P$ under different corner cases of typical-typical (TT), slow-slow (SS), and fast-fast (FF), respectively. At the TT corner case, the optimal gate bias can be determined to be 0.28 V to have the maximal R_V of 12 kV/W. The power
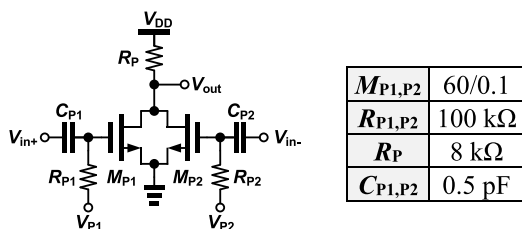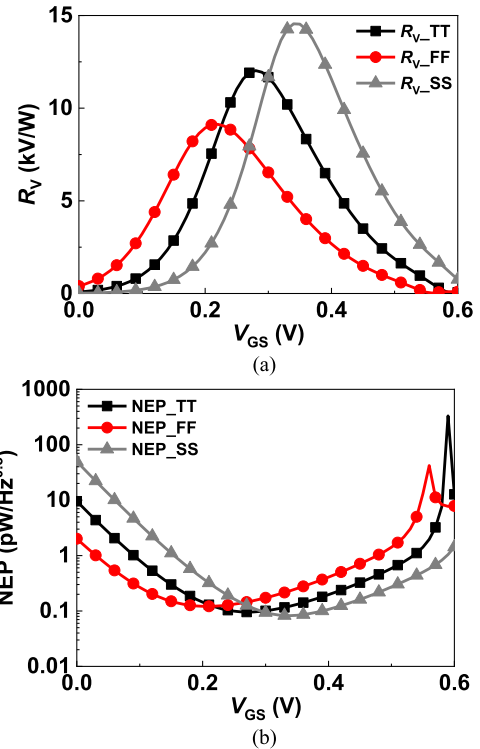

FIGURE 9. Simulated (a) R_V and (b) NEP versus gate bias under different corner cases.

detector also exhibits minimal NEP of 96 fW/Hz$^{0.5}$ at this optimal gate bias as shown in Fig. 9(b). Note that, for practical operations, process variation may occur. The gate bias can be adjusted accordingly to have high R_V and low NEP. The proposed power detector only consumes 0.57 mW from a 1.2-V supply.

To further increase R_V to detect a signal with power level of around -90 dBm, a high-gain IF amplifier is included. As shown in Fig. 1, it cascades five identical amplifier stages. Each stage is a differential amplifier whose schematic is illustrated in Fig. 10. The IF amplifier shall also be able to process a 1-ns pulse for the debris detection. The stage number and the load resistors must be iteratively designed to meet the requirement. The proposed IF amplifier can provide voltage gain of 66 dB with 3-dB bandwidth of 0.7 GHz. It only consumes 7 mW from a 1.2-V supply.
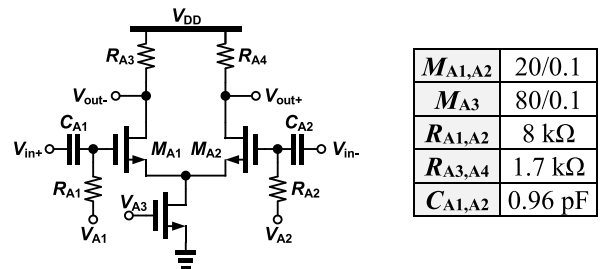

$M_{P1,P2}$	60/0.1
$R_{P1,P2}$	100 kΩ
R_P	8 kΩ
$C_{P1,P2}$	0.5 pF

FIGURE 8. Schematic of the proposed Ka-band power detector.

$M_{A1,A2}$	20/0.1
M_{A3}	80/0.1
$R_{A1,A2}$	8 kΩ
$R_{A3,A4}$	1.7 kΩ
$C_{A1,A2}$	0.96 pF

FIGURE 10. Schematic of the IF amplifier.

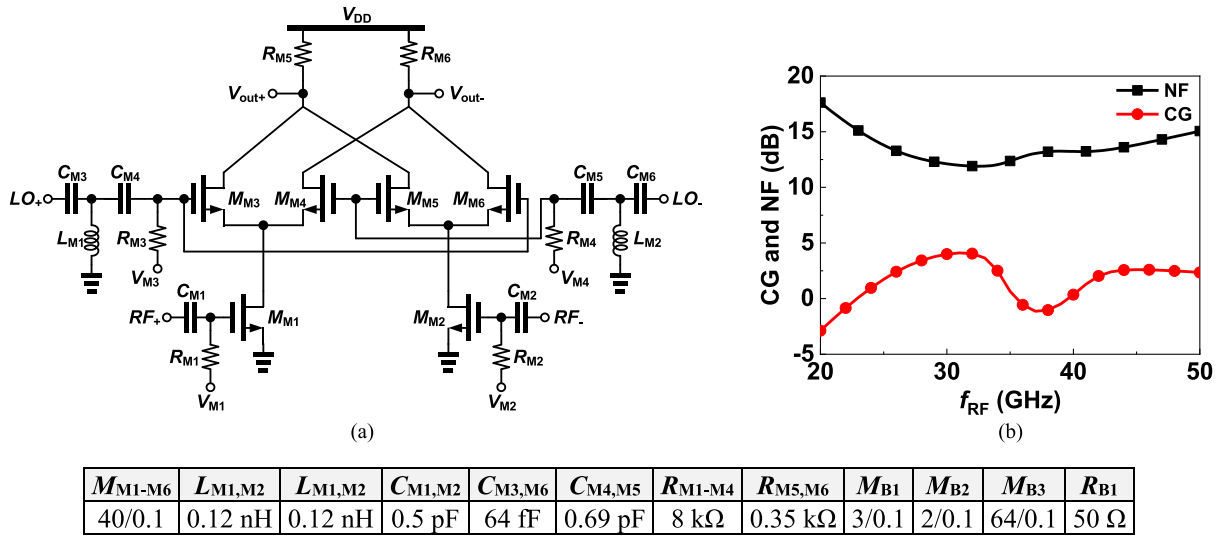| M_{M1-M6}	$L_{M1,M2}$	$L_{M1,M2}$	$C_{M1,M2}$	$C_{M3,M6}$	$C_{M4,M5}$	R_{M1-M4}	$R_{M5,M6}$	M_{B1}	M_{B2}	M_{B3}	R_{B1}
40/0.1	0.12 nH	0.12 nH	0.5 pF	64 fF	0.69 pF	8 kΩ	0.35 kΩ	3/0.1	2/0.1	64/0.1	50 Ω

FIGURE 11. (a) Schematic of the proposed mixer. (b) Mixer simulation results.

D. MIXER DESIGN

Fig. 11(a) shows the proposed mixer which adopts a double-balanced Gilbert architecture. The transconductance stages comprised of transistors M_{M1} and M_{M2} are used to convert input RF voltage to output RF currents. The switching quad formed by transistors M_{M3-M6} downconverts these RF currents to produce IF currents which are subsequently converted back to the voltage domain by the load resistors R_{M5} and R_{M6}. M_{M1} and M_{M2} are biased at 0.45 V, which is at the saturation region while being close to the triode region. This not only reduces the power dissipation, but it also lowers the required LO power for fully switching on and off M_{M3-M6} transistors. The optimal LO power is determined to be −2.5 dBm to maximize the conversion gain (CG). The load resistors R_{M5} and R_{M6} also need to be designed carefully. Higher R_{M5} and R_{M6} can give higher CG. However, it also deteriorates the IF bandwidth. Since the proposed reconfigurable receiver operating at the active-receiver mode is targeted for the next 6G satellite wireless communication systems with Gbps transmission capability, the IF bandwidth shall be wider than 1 GHz. Hence the load resistors R_{M5} and R_{M6} are designed as 0.36 kΩ to have IF bandwidth of 5.5 GHz. Fig. 11(b) depicts the mixer simulation results. The proposed mixer can provide CG of 0.6 dB and double-sideband NF of 13.8 dB at 35 GHz while consuming dc power of 3.6 mW from a 1.2-V supply.

E. SIMULATION RESULTS OF THE PROPOSED RECONFIGURABLE KA-BAND RECEIVER

After explaining the design of each subblock, they are integrated together to form the proposed reconfigurable Ka-band receiver. Fig. 12 shows the simulated CG and NF of the proposed receiver operating at the active-receiver mode. The receiver can give CG of 45.2 dB and NF of 7 dB at 35 GHz. As switched to the passive-receiver mode, the proposed receiver can exhibit simulated R_V of 1.0 GV/W
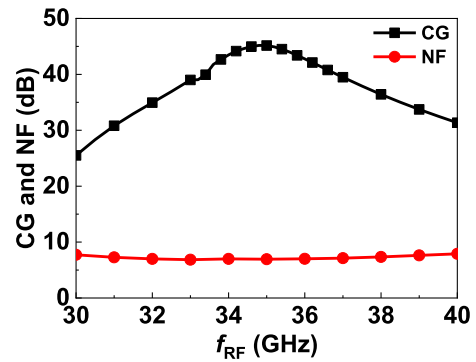

FIGURE 12. Simulated CG and NF of the proposed reconfigurable receiver operating at the active-receiver mode.
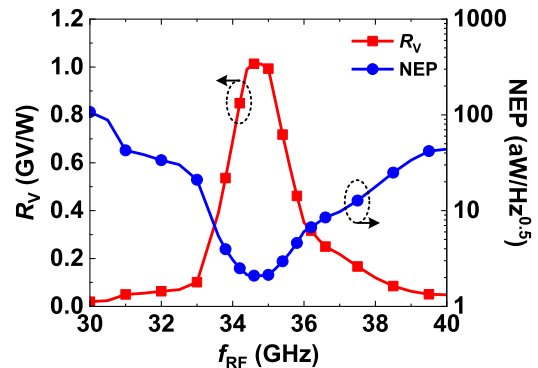

FIGURE 13. Simulated R_V and NEP of the proposed reconfigurable receiver working at the passive-receiver mode.

and NEP of 2.1 aW/Hz$^{0.5}$ at 35 GHz, as illustrated in Fig. 13. The power dissipation is 47.8 and 51.8 mW as working at the active-detection and passive-detection modes, respectively.
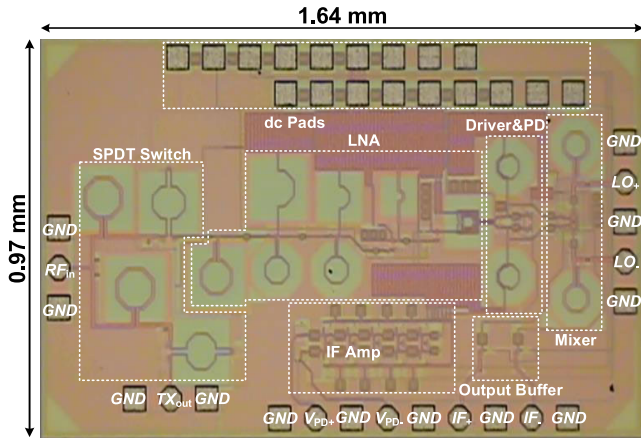
FIGURE 14. Chip photo of the proposed reconfigurable Ka-band receiver.

IV. EXPERIMENTAL RESULTS

The proposed reconfigurable Ka-band receiver is realized in a 90-nm CMOS technology. The chip photo is shown in Fig. 14. The chip size is 0.97 mm × 1.64 mm, including dc and ac probing pads. The measurement is conducted by a chip-on-board setup. The dc pads are bonded to a PCB board while the input RF, LO, IF amplifier output, mixer output, and the signal at the SPDT TX port are applied and acquired by high-frequency ground-signal-ground (GSG) and ground-signal-ground-signal-ground (GSGSG) probes. The proposed receiver consumes dc power of 54.4 and 49.6 mW from a 1.2-V supply as working at the active-receiver mode and the passive-receiver modes, respectively.

Fig. 15(a) shows the measured input return loss of the proposed receiver as V_{SW} is set 0 V, that is, the input signal is directed to the RX port. The measured $|S_{11}|$ is −17.1 dB at 35 GHz while being kept below −10 dB from 26.3 to 53.1 GHz. Under the same setting, the isolation of the SPDT switch can be measured by probing the switch's TX port. The measured isolation can be smaller than −39.6 dB from 20 to 30 GHz as indicated in Fig. 15(b). By contrast, the insertion loss of the switch is measured by setting V_{SW} to 1.2 V and probing the switch's TX port. The measured insertion loss as illustrated in Fig 15(c) is −3.7 dB at 35 GHz, around

1 dB higher than the simulated one. The 3-dB bandwidth can cover from 7.2 to 48.5 GHz. To characterize the receiver performance, the controlled voltage of the SPDT switch V_{SW} is set 0 V for the following measurements.

The active-receiver mode is characterized first. At this mode, the gate bias of the mixer V_M and the power detector V_P are set as 0.45 V and 0 V to enable the mixer and disable the power detector, respectively. Fig. 16(a) shows the measured conversion gain versus the RF frequency as the LO power is −8 dBm and the IF frequency is 100 MHz. The peak conversion is 45.2 dB at 35 GHz, very close to the simulated one. However, the measured RF bandwidth is narrower than the simulated result. This might be caused by the inaccuracy of the device models and some unexpected parasitics not captured by an electromagnetic simulator. As depicted in Fig. 16(b), the measured IF bandwidth is 3.4 GHz, which is wide enough to support Gbps communication capability. The DSB NF is also measured as illustrated in Fig. 16(c). The measured DSB NF is around 7.6 dB over the IF bandwidth, only 0.6 dB higher than the simulated result.

To characterize the receiver working at the passive-receiver mode, the gate bias of the mixer V_M and the power detector V_P are set as 0 V and 0.3 V to disable the mixer and enable the power detector, respectively. A tunable attenuator is included before a signal generator in order to measure R_V with a very low input power level. The attenuator's performance is measured first by a network analyzer, which is then employed to calibrate the RF input power. The measured voltage responsivity R_V versus the RF frequency is shown in Fig. 17(a) as the input power is −76 dBm. The measured trend follows very well with the simulated one. R_V has a maximal value of 1.2 GV/W at 34.8 GHz. Fig. 17(b) illustrates the measured R_V versus the RF input power P_{RF} as the input frequency is fixed at 35 GHz. Since the output voltage is proportional to the input power, the 1-dB compression point for a power detector $IP_{1dB,PD}$ is defined to be the applied power corresponding to R_V dropped by a factor of 1.26. The measured $IP_{1dB,PD}$ is −64 dBm. In the future system integration, a variable-gain function can be added to the receiver chain to improve $IP_{1dB,PD}$.
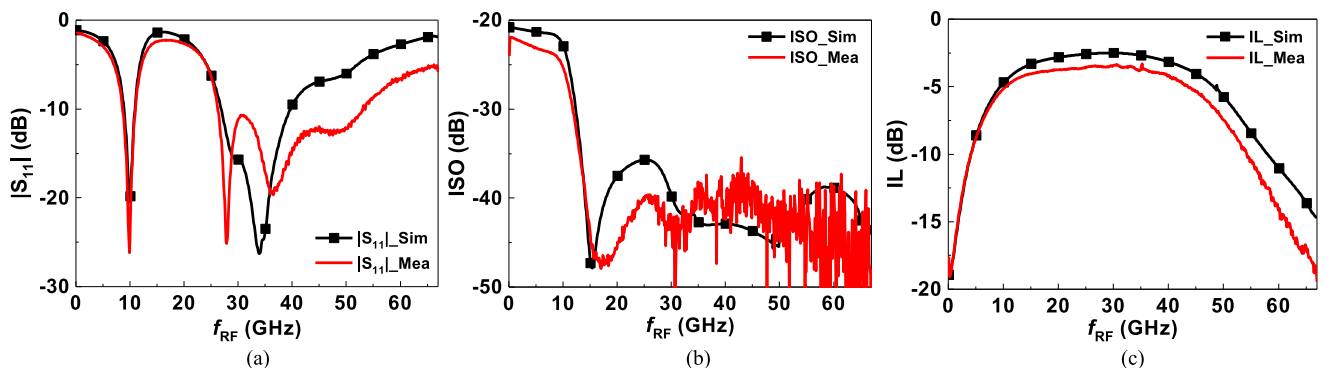

FIGURE 15. Measured (a) input return loss, (b) isolation, and (c) insertion loss of the proposed SPDT switch.
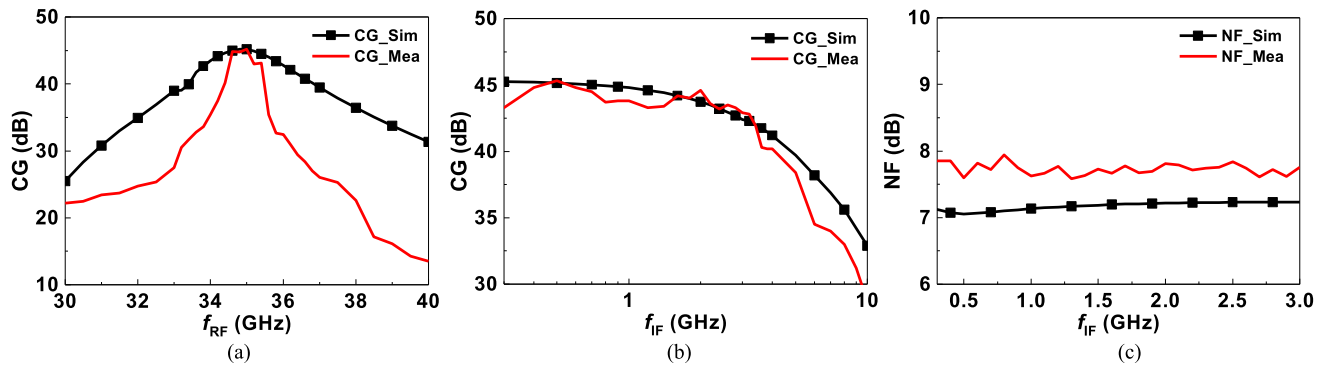
FIGURE 16. Measured (a) CG versus the RF frequency, (b) CG versus the IF frequency, and (c) NF versus the IF frequency of the proposed reconfigurable receiver working at the active-receiver mode.
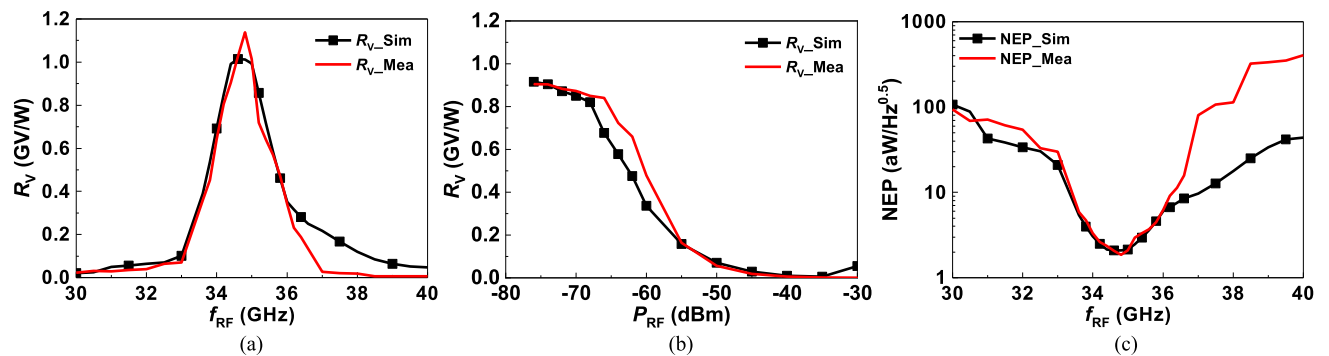

FIGURE 17. Measured (a) R_V versus the RF frequency, (b) R_V versus the RF input power, and (c) NEP versus the RF frequency of the proposed reconfigurable receiver working at the passive-receiver mode.

The noise equivalent power is acquired by firstly measuring the output noise power spectrum density N_0 and secondly dividing the square root of this noise power by the voltage responsivity, that is, NEP $= \sqrt{N_0}/R_V$. Fig. 17(c) shows the measured NEP versus the RF frequency as P_{RF} is -76 dBm. The measured result meets the simulated one very well. Minimum NEP of 2.1 aW/Hz$^{0.5}$ can be obtained at 35 GHz.

As mentioned before, the proposed receiver not only works as a radiometer, but it can also be used to detect the space debris. To verify this, a 35-GHz input signal with power of -50 dBm is amplitude-modulated (AM) by a square-wave signal with a period of 2 ns. This 35-GHz AM signal is then injected to the proposed receiver. Fig. 18 shows the measured time-domain waveform of the power detector output. Clearly, the proposed receiver can successfully demodulate the square-wave signal.

The performance of the proposed receiver is summarized and compared with prior works in Table 1. Clearly, the proposed receiver exhibits the highest voltage responsivity and the lowest noise equivalent power. It is also the only receiver which can be reconfigured to support active-receiver and passive-receiver modes. The proposed receiver not only can be utilized to downconvert the RF signal to the IF band for wireless communication applications, it can also operate as
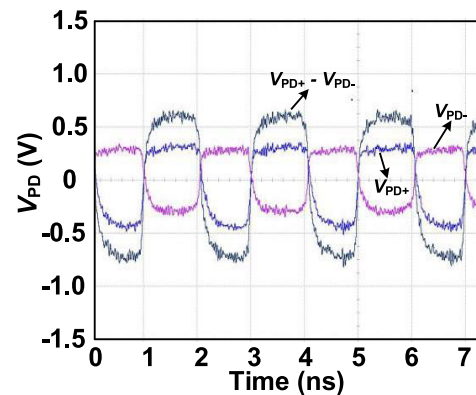

FIGURE 18. Measured time-domain waveform of the power detector output.

a radiometer to sense the atmospheric conditions to dynamically compensate atmospheric attenuation for fading mitigation. Furthermore, its high sensitivity and responsivity is also able to detect the space debris to prolong the satellite lifetime. Consequently, such a reconfigurable Ka-band receiver is very suitable for the next-generation 6G satellite communication systems.

TABLE 1. Performance summary and comparison with prior works.

Reference	JSSC'11 [35]	TCAS-I'17 [6]	RFIC'20[d] [13]	ISSCL'20[e] [14]	Access'20 [36]	JSSC'17 [37]	**This Work**
Support Active- and Passive-Detection Modes?	No	No	No	No	No	No	**Yes**
Type	Passive	Passive	Active	Active	Active	Active	**Active and passive**
V_{DD} (V)	1.2	2.3	1.2	1.0	1.2	2.5	**1.2**
f_{RF} (GHz)	81-91	25.75	17-21	27-31	27.7-35.2	28-32	**35**
CG (dB)	−	−	47	3	4.3	10.5	**45.2**
OIP_{1dB} (dBm)	−	−	NA	NA	-4.3	-2.4	**-6.8**
NF (dB)	−	−	5.0	NA	NA	5.1	**7.6**
R_V (V/W)	16 M	0.76 M	−	−	−	−	**1.2 G**
$IP_{1dB,PD}$ (dBm)	NA	-32[c]	−	−	−	−	**-64**
NEP (fW/Hz$^{0.5}$)	6.1	232	−	−	−	−	**2.1×10^{-3}**
P_{dc} (mW)	101.6	11.7	580	40	15.6	136.5	**54.4[a]/49.6[b]**
Technology	65-nm CMOS	130-nm SiGe BiCMOS	65-nm CMOS	65-nm CMOS	90-nm CMOS	130-nm SiGe BiCMOS	**90-nm CMOS**

(a) Active mode. (b) Passive mode. (c) Estimated. (d) 2 RX. (e) 4-beam phased array.

V. CONCLUSION

A single-chip reconfigurable Ka-band receiver is proposed for the next-generation 6G satellite communication systems and is successfully verified by the experimental results using a 90-nm CMOS technology. The proposed receiver can be electronically reconfigured to support active-receiver mode for wireless communication applications and passive-receiver mode for a radiometric function. At the active mode, the receiver can provide conversion gain of 45.2 dB and DSB NF of 7.6 dB at 35 GHz while only consuming 54.4 mW from a 1.2-V supply. As switched to the passive mode, the proposed receiver can exhibit voltage responsivity of 1.2 GV/W and NEP of 2.1 aW/Hz$^{0.5}$ at 35 GHz. The power dissipation is 49.6 mW from a supply voltage of 1.2 V.

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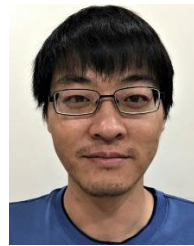
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