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A 74-dB Dynamic-Range 625-kHz Bandwidth Second-Order Noise-Shaping SAR ADC Utilizing a Temperature-Compensated Dynamic Amplifier and a Digital Mismatch Calibration

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ABSTRACT This paper presents the design of a 2nd-order Noise-Shaping (NS) Successive-Approximation-Register (SAR) Analog-to-Digital Converter (ADC) employing a cascade of temperature-compensated dynamic amplifier and a ring amplifier in the feedback path to realize a low-power/low-noise loop filter that is robust to temperature variation. A new mismatch calibration technique optimized for a noise-shaping SAR ADC is also presented to overcome the challenge of finding correct digital bit weights for NS SAR ADCs. Fabricated in 65 nm Complementary Metal-Oxide-Semiconductor (CMOS) process, the prototype ADC demonstrates a peak Signal-to-Noise-and-Distortion Ratio (SNDR) of 71.35 dB and a dynamic range of 74 dB with a signal bandwidth of 625 kHz. Over 80-degree of the temperature range, the ADC exhibits only 2 dB drop in SNDR thanks to the temperature-compensated dynamic amplifier. With a total power consumption of 130 μW, the ADC achieves Walden Figure-of-Merit (FoM) of $\mathrm{FoM_W} = 34.4$ fJ and Schreier FoM of $\mathrm{FoM_{S,DR}} = 171$ dB, respectively.

INDEX TERMS Successive approximation resister (SAR), digital domain calibration, noise shaping (NS), dynamic amplifier, ring amplifier, mismatch calibration, analog to digital converter (ADC).

I. INTRODUCTION

The noise-shaping successive-approximation-register (NS-SAR) analog-to-digital converter (ADC) [1] is an emerging oversampled ADC architecture that has been gaining increasing popularity for high resolution data converter designs. By leveraging the energy efficiency of SAR ADCs in scaled CMOS technology, NS-SAR ADCs have demonstrated excellent power efficiency with target SNDR $>$ 60 dB [1]–[9]. Being a hybrid architecture, however, the NS-SAR ADC also faces several design issues that are commonly found in SAR ADC and $\Delta\Sigma$ ADC designs.

First, the loop filter that processes the residue from the previous quantization step is an essential block in the NS-SAR ADCs, and the transfer function of the loop filter has to be controlled precisely in order to achieve desired noise transfer function (NTF). Traditionally, an opamp-based switched-capacitor circuit has been widely used to realize such a discrete-time analog signal processing block, but using a high-gain opamp drawing constant current in a loop filter leads to power-hungry ADC designs [1]. To overcome this issue, several new ideas have been introduced. Many of previous works [2], [3], [6] have commonly demonstrated that using a dynamic amplifier followed by a passive FIR filter results in a very power-efficient loop filter design while achieving sufficient quantization noise suppression in the signal band. However, the gain variation of the dynamic amplifier over process and temperature has to be addressed. For instance, a common-mode current is injected in [2] to adjust the amplification time to correct the gain. In [6], a 5-bit digitally-controlled degeneration switch is used for gain correction. Both of these correction methods may be allowable for one-time gain adjustment that addresses the manufacturing uncertainties such as process variation.

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However, the gain is not maintained over wide temperature range, limiting its usage for practical applications. A sophisticated digital-domain technique such as digital background calibration can be used to address both process and temperature variation [3], but at the cost of substantial design complexity increase.

Second, the static mismatch in the unit elements in the capacitor DAC (CDAC) inside the NS-SAR ADC appears as an error at the input. The static CDAC mismatch problems in oversampled ADCs are addressed by the dynamic element matching (DEM) such as data-weighted averaging (DWA) that reduces random mismatch errors in a noise-shaped fashion. However, using DWA is challenging in NS-SAR ADCs because the resolution of the SAR quantizer is rather high (typically higher than 7 or 8 bits) in NS-SAR ADCs, and that imposes high design complexity for DEM primarily because the hardware cost of element selection logic (ESL) in DEM grows exponentially with the resolution. Recently, [7] presented a 1st-order mismatch error shaping (MES) technique whose hardware complexity grows only linearly with the DAC resolution at the cost of reduced dynamic range. [10] reported more generalized MES technique that enables higher-order mismatch shaping, but the design complexity has to increase considerably. Alternative technique to deal with the static CDAC mismatch problem in NS-SAR ADCs is to use a foreground bit-weight calibration by measuring the mismatch information based on least-squares optimization [3], [5], [11]. Such a calibration technique has been used for Nyquist ADCs such as SAR ADCs or pipelined ADCs [12], [13]. However, using the algorithm developed for Nyquist ADCs may be sub-optimal when applied to finding optimal bit weights for noise-shaped ADCs.

As an expanded work of the article presented in [14], this paper presents two new approaches that can advance the design of NS-SAR ADCs. First, we report a low-power loop filter topology utilizing a cascade of a temperature-compensated dynamic amplifier and a ring amplifier. Combined with passive FIR filter, this arrangement achieves temperature-tolerant 2nd-order error-feedback (EF) NS-SAR ADC operation without using extra background calibration over wide temperature range. Our prototype chip maintains SNDR>68 dB over $-$ 5 °C to 75 °C with 2 dB SNDR degradation for the worst case. Second, this paper presents a new algorithm that is customized to find optimal bit weights for noise-shaping SAR ADCs. Unlike the traditional calibration algorithm for a standard SAR ADC [11], our calibration algorithm finds optimal bit weights of a NS-SAR ADC under the presence of shaped quantization noise, leading to 10 dB higher SNDR compared to conventional least-squares based calibration algorithm.

This paper is organized as follows. In Section II, we briefly review the design requirement for loop filter to achieve the desired NTF for the 2nd-order EF NS-SAR and present a low-power temperature-compensated loop filter based on the cascade of a dynamic and a ring amplifier. Section III discusses the DAC mismatch issue and presents a new algorithm that finds optimal bit weights for NS-SAR ADCs. Section IV presents overall architecture as well as circuit implementations. Section V presents measurement results of the prototype chip and highlights the improvement by the proposed ideas. Section VI concludes this paper.

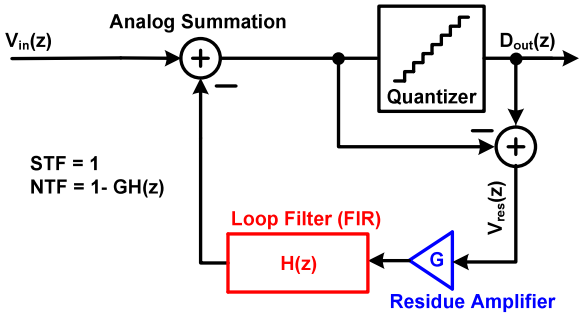


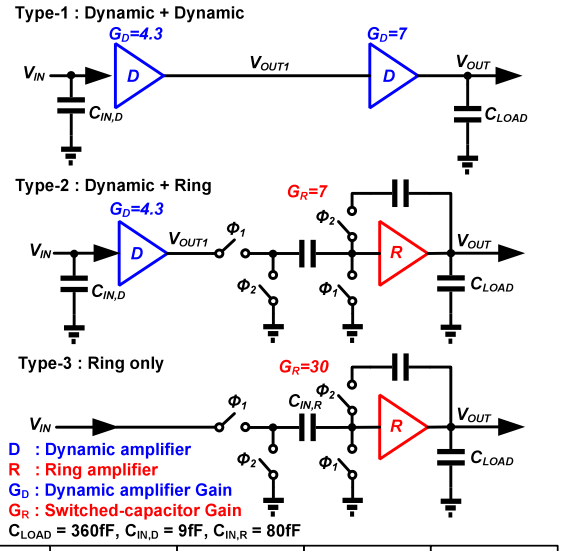
FIGURE 1. Block diagram of 2nd-order error-feedback (EF) NS-SAR ADC.

II. LOOP FILTER DESIGN FOR EF NS-SAR ADC

A. GAIN REQUIREMENT FOR PASSIVE FIR-BASED LOOP FILTER

Fig. 1 shows a generic block diagram of a 2nd-order error-feedback (EF) NS-SAR ADC, in which the loop filter processes unshaped quantization noise and combines the filtered error and input before feeding it to the quantizer. In contrast to traditional CIFF structure where low-loss integrator is required to realize sharp NTF, using simple FIR filter is sufficient to create efficient NTF, which is an attractive feature. [15] first reported a first-order EF NS-SAR ADC with 9.5-dB in-band noise shaping, and subsequently the work by [3] demonstrated a second-order EF NS-SAR with more aggressive noise shaping.

A key design issue in EF NS-SAR ADC is the loop filter implementation. While there can be many different realizations for the analog summation block in the loop filter, a passive charge sharing between the FIR filter and the main CDAC has been the most preferred low-power solution. Being passive, this analog summation inevitably causes signal attenuation with charge sharing gain $A < 1$. Therefore, in this arrangement, the FIR filter needs a preceding amplifier with gain $G > 1$ that compensates the loss in the charge sharing process. Given that the entire loop filter is impacted by gain G, it needs to be rather precisely controlled to maintain the desired NTF. For instance, it was shown that there can be as much as 10 dB SQNR degradation [3] for 10% gain variation. Moreover, while using higher G is advantageous to reduce the impact of the thermal noise from the loop filter, it is also challenging to design a high-gain and low-power amplifier, leading to a tight tradeoff between the design complexity and the noise penalty. For such a reason, a gain of around 30 $[V/V]$ is chosen in [3] as the best compromise. However, such a gain requirement can still be a design bottleneck when one wants to use a low-power dynamic amplifier for EF NS-SAR because achieving gain beyond 4 $\sim$ 6 [V/V] is not easily achievable [6], [16] unless sophisticated techniques such as



Type	Power	Input Capacitance	$V_{OUT,CM}$ Sensitivitiy	PVT-Sensitivity
1	☺	☺	☹	☹
2	☺	☺	☺	☹
3	☹	☹	☺	☺

FIGURE 2. Comparison of various amplification schemes.

using a constant common-mode current [2] or a positive feedback [3] are used.

B. CASCADED DYNAMIC AND RING AMPLIFIER

Fig. 2 shows three possible amplification schemes we consider for a power-efficient high-gain amplifier in the loop filter. First, we can cascade a multitude of dynamic amplifiers, which is shown as Type-1 in Fig. 2 [17]. While this arrangement can certainly boost the signal gain, it is very challenging to regulate the gain over process and temperature variations for the following reasons: 1) The gain of the dynamic amplifier is sensitive to the input common-mode voltage $V_{IN,CM}$. Our simulations, shown in Fig. 3-(a) and Fig. 3-(b), reveal that the gain varies roughly by 7% for the $V_{IN,CM}$ change of $\pm$ 50 mV, and the output common-mode voltage $V_{OUT,CM}$ changes by nearly 100 mV for temperature change from $-$ 40 °C to 85 °C when we adjust the pulsewidth to maintain the amplifier gain constant. 2) The $V_{OUT,CM}$ of the first stage amplifier is simply the $V_{IN,CM}$ of the second dynamic amplifier. So even if we are allowed to set the $V_{IN,CM}$ of the 1st stage amplifier to a desired value, it is difficult to regulate the gain of the entire amplifier because the $V_{OUT,CM}$ of the 1st stage will change over temperature.

To circumvent this problem, we have conceived a hybrid amplifier by cascading a dynamic amplifier and a switched-capacitor amplifier using a ring amplifier [18], which is shown as Type-2 in Fig. 2.[1] In this arrangement, the input signal is first amplified by the dynamic amplifier whose output is further amplified by the switched-capacitor amplifier. The benefit of such a configuration is that the output common-mode variation of the dynamic amplifier does not impact the overall gain because the gain of the ring amplifier in a feedback configuration is determined primarily by the ratio of capacitors. Therefore, this arrangement does not suffer from the common-mode gain sensitivity issue in the cascaded dynamic amplifiers. Also, compared to using a standalone ring amplifier in a feedback configuration shown as Type-3 in Fig. 2, the combination of a dynamic and a ring amplifier is more suitable for achieving both high-gain and high speed. This is because for the gain we target ($\approx$ 30), the standalone ring amplifier is limited by its small feedback factor, which is the inverse of the closed-loop gain, leading to high power dissipation.

To compare the differences quantitatively, we designed three different types of amplifiers in Fig. 2 in 65-nm CMOS process for the same total gain of 30, and the simulated performance is summarized in Fig. 3-(c). Note that the 'Ring-(A)' and the 'Ring-(B)' in Fig. 3-(c) are the ring-amplifier only versions that achieve similar power ($\approx 9\mu W$) and settling time ($\approx$ 2.5 ns) of the hybrid topology, respectively. The comparison reveals that our hybrid topology excels both in power and bandwidth. For instance, when designed for similar total power budget and load capacitance of 360 fF, the hybrid topology is two-times faster. Alternatively, when designed for the same settling time, the standalone ring amplifier consumes 21.8 μW, which is 2.42-times higher than the hybrid topology. Moreover, the input-referred noise of the standalone topology exhibits 60% higher input-refereed noise voltage.[2]

While our numerical comparison is not sufficient to claim that the hybrid topology is better in all possible cases, we can still make observations why our topology is likely to achieve better noise-power-speed tradeoff. Intuitively, the noise output of the hybrid amplifier can be expressed as

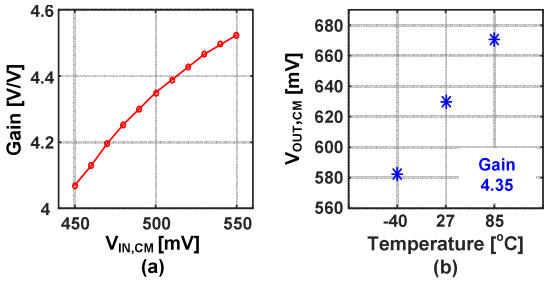
$$v_{n,out}^2 = (G_D \cdot G_R)^2 \cdot v_{n,in,dyn}^2 + G_R^2 \cdot v_{n,in,ring}^2, \qquad (1)$$

where G_D and G_R are the gain of dynamic and ring amplifier, and $v_{n,in,dyn}^2$ and $v_{n,in,ring}^2$ are the input-referred noise power of the dynamic and ring amplifier, respectively. Given $G_D = 4.3$ and $G_R = 7$, the noise performance is dominated by the dynamic amplifier. Although ring amplifiers achieve much improved noise-power tradeoff when compared with conventional OTA-based amplifiers as reported in [19], the bias current of the dynamic amplifier when it is engaged in actual amplification is much higher than the average current due to its dynamic nature, thereby achieving high effective input g_m and low input-referred noise. In comparison, the first stage of the ring amplifier draws constant current, leading to a lower effective input g_m when compared to the dynamic amplifier.

One may be concerned about the input capacitance of the hybrid topology, because large $C_{in,amp}$ reduces the dynamic

[1] We assigned the gain-of-7 to the ring amplifier because the gain of a feedback topology is defined as the ratio of two capacitors, in which case an integer value is the natural choice.

[2] In the comparison table in Fig. 3, we have not included extra power for the on-chip bandgap and LDO shown in Fig. 5 because these blocks are necessary even if we only use a ring amplifier.



Gain=30	Dynamic +Ring	Ring (A)	Ring (B)
99.9% Settling Time [ns]	2.5	5	2.5
Power [μW]	9	9.6	21.8
Input Capaciance [fF]	9	80	80
Input referred noise [μV_{rms}]	154	178	250

(c)

FIGURE 3. Simulation results of dynamic amplifier for (a) input common-mode versus gain and (b) temperature versus output common-mode. (c) simulated performances for the proposed amplifier and the standalone ring amplifier.

range of the ADC and makes the comparator thermal noise more prominent. However, the input capacitance of the hybrid topology is significantly smaller than the CDAC capacitance. For instance, in our case, input capacitance of the dynamic amplifier is only 9 fF and is negligible when compared to 2.56 pF of CDAC total capacitance. By the same reason, the impact of nonlinear capacitance presented by the input transistor of the dynamic amplifier is minimal because the total CDAC capacitance is significantly larger than the nonlinear capacitance and the small voltage-dependent variation of the nonlinear capacitance does not impact the overall performance of the ADC.

C. TEMPERATURE-COMPENSATED DYNAMIC AMPLIFIER

The hybrid amplifier still suffers from the gain sensitivity over environmental change mainly due to the dynamic amplifier. In this article, we focus on developing a technique that maintains the gain over the temperature change. We perform a 1-point gain-adjustment based on a sinewave fitting algorithm at the system startup to correctly set the gain of the dynamic amplifier to fix the impact of the process and voltage uncertainties, leaving our technique to handle the temperature variation.

Shown in Fig. 4, the gain of a dynamic amplifier in the simplest form is expressed as

$$A_v = \frac{g_m}{C_L} \cdot T_P, \tag{2}$$

where the g_m is the input transconductance, C_L is the output capacitance, and T_P is the duration of the activation pulse CK_P. For fixed T_P and C_L, g_m is strongly influenced by the temperature change because both the mobility and drain current are affected, yielding the gain variation.

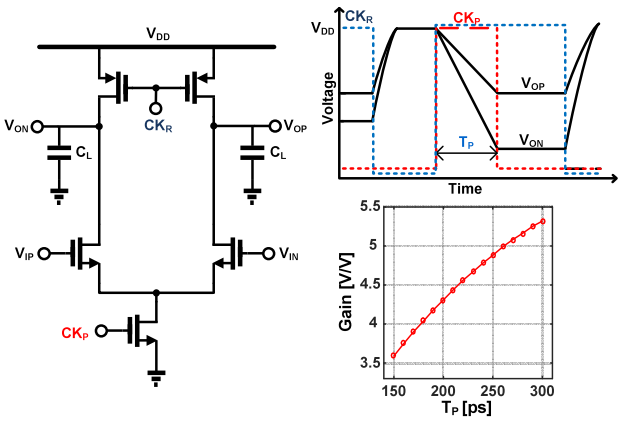


FIGURE 4. Circuit structure of a dynamic amplifier and the simulated amplifier gain versus the pulsewidth T_p.

To regulate the gain over the temperature change, we propose to use the activation pulsewidth T_P as the knob to adjust the gain of a dynamic amplifier. Shown in Fig. 4, the simulated gain of the dynamic amplifier versus T_P shows increasing gain over sufficiently wide range of T_P. Given that the intrinsic gain of a dynamic amplifier is inversely proportional to the temperature rises due to the reduced transconductance, the gain reduction can be compensated by proportionally adjusting T_P with temperature change by utilizing a proportional-to-absolute-temperature (PTAT) current and a local low-dropout (LDO) regulator.

Fig. 5 shows a detailed schematic of such a pulse generator. The PTAT current is generated by an on-chip bandgap reference and is mirrored to generate a voltage that decreases with temperature as

$$V_{REF,BUF} = V_{DD,LDO} - I_{PTAT} \cdot R_{EXT}, \tag{3}$$

where R_{EXT} is an external resistor with low temperature coefficient and $V_{DD,LDO}$ is the supply voltage of the on-chip LDO. Note that $V_{DD,LDO}$ can be tightly controlled over temperature variation since this voltage can be provided by an external off-chip LDO. The on-chip LDO takes the $V_{REF,BUF}$ as a reference of the negative feedback to generate a local buffered supply voltage $V_{DD,BUF}$ such that $V_{DD,BUF} \approx V_{REF,BUF}$. The core of the pulse generator for the dynamic amplifier is powered under this $V_{DD,BUF}$. Specifically, the delay buffers consisting of I_1 and I_2 under $V_{DD,BUF}$ determine the activation pulse-width T_{pulse} for the dynamic amplifier. Therefore, as the temperature rises, so does the I_{PTAT}, which results in the decrease in $V_{DD,BUF}$. Consequently, lower supply voltage for I_1 and I_2 results in longer delay, which is equivalent to the T_{pulse} increase. Therefore, by choosing proper R_{EXT} and PTAT current values, the gain can be maintained reasonably well over a wide temperature range.

To verify the feasibility of temperature robustness, Fig. 6-(a) shows a simulated dynamic amplifier gain over wide range of temperature. Our target range for the gain variation is ±3%, which is required to maintain the SNDR of the ADC. The result indicates that the gain of the amplifier stays

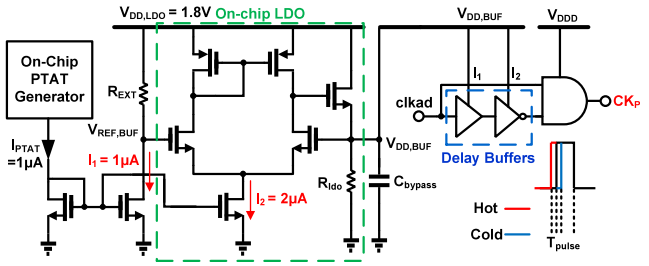


FIGURE 5. Proposed temperature aware pulse generator.

within -0.6% to $+1\%$ error bound over $-45°C \sim +125°C$, while the gain without the proposed technique varies from -4% to $+13\%$. Similarly, Fig. 6-(b) shows a simulated total gain of the hybrid amplifier using both the dynamic and the ring amplifier, indicating that the total gain stays with -0.9% to $+2\%$ error bound over the same temperature range, while the gain without the proposed technique varies from -3.7% to $+13\%$. The LDO output $V_{DD,BUF}$ ranges from 0.9V to 1.1V over the entire temperature range, which is acceptable for a source-follower based LDO output stage with $V_{DD,LDO} = 1.8V$.

Note that there has been a published article [20] that aims to achieve PVT stability of the dynamic amplifier by modulating the pulsewidth. While our work has similarity with [20], the way the pulse is generated is completely different. In [20], the pulse is generated by using a slow single-pole amplifier and dual-path voltage-to-time converters with weakness being the threshold mismatch between the dual-path.[3] On the other hand, our way of generating the pulse depends on the accuracy of the PTAT current and we do not have the path mismatch issue. Since the PTAT current is commonplace in bandgap reference designs, we believe that our approach is relatively easier to design.

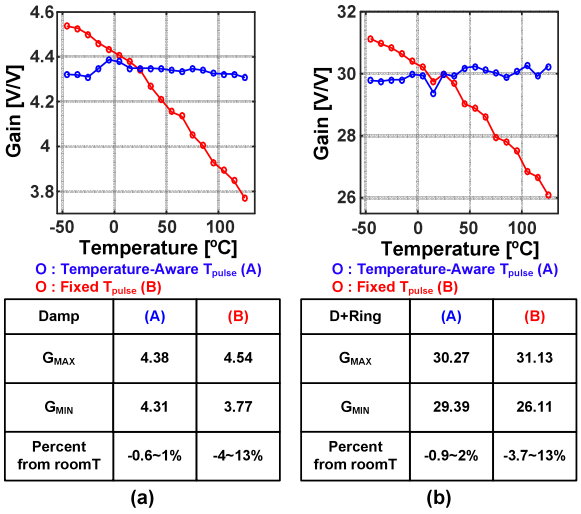
III. MISMATCH CALIBRATION FOR NS-SAR ADCs

A. REVIEW OF PRIOR CALIBRATION METHOD

The CDAC mismatch is one of the primary linearity error sources in noise-shaping SAR ADCs and therefore needs to be corrected to achieve high linearity. Either a dynamic mismatch shaping or a static digital calibration technique can be used to mitigate the CDAC mismatch problem and a comparison between various techniques is reviewed in detail in a recent paper [10]. In this section, we introduce a new algorithm that finds optimal bit weights for noised-shaping SAR ADCs. For the completeness of discussion, we begin by reviewing a conventional method that finds the optimal bit weights via least-squares (LS) minimization.

Let us consider the test setup shown in Fig. 7, where a sinusoid generator applies a full-scale sinewave of a known frequency f_{sig} to the ADC. We assume that the N-bit raw ADC

[3]This weakness is acknowledged by the authors of the paper



Damp	(A)	(B)
G_{MAX}	4.38	4.54
G_{MIN}	4.31	3.77
Percent from roomT	-0.6~1%	-4~13%

(a)

D+Ring	(A)	(B)
G_{MAX}	30.27	31.13
G_{MIN}	29.39	26.11
Percent from roomT	-0.9~2%	-3.7~13%

(b)

FIGURE 6. Simulated amplifier gain versus temperature with and without the proposed temperature compensation technique for (a) dynamic amplifier and (b) dynamic + ring amplifier.

output d_{out} with record length of M is obtained. To be more specific, $d_{out}[k][i]$ is the kth-bit raw ADC output ($k = 0$ for MSB and $k = N-1$ for LSB) that corresponds to the ith input sampled at time instance t_i. The optimal bit weight $w[k]$ for the $d_{out}[k][i]$ for $k = 0, \cdots, N-1$ can be found by solving the following optimization problem

$$\begin{aligned} &\text{minimize } \|err\|_2^2 \\ &\qquad \text{variables } A_s, A_c, w[0], \ldots, w[N-1] \\ &\text{subject to } err[i] = \sum_{k=0}^{N-1} d_{out}[k][i] \cdot w[k] - y_i, \\ &\qquad y_i = A_s \cdot \sin(2\pi f_{sig} t_i) \\ &\qquad\quad + A_c \cdot \cos(2\pi f_{sig} t_i), \quad i = 1, \ldots, M, \end{aligned} \tag{4}$$

where A_s and A_c are the estimation parameter for the sinusoid with an unknown magnitude and phase. Solving the problem (4) by least-squares method or convex optimization [21] yields optimal bit weights $w[0], \ldots, w[N-1]$. Once the optimal bit weights are known, the calibrated ADC output d_{outcal} in a regular conversion mode is generated in the digital calibration logic by computing a linear combination of the bit weights and the raw ADC outputs. Note that the functional model of the calibration logic in Fig. 7 can be implemented by simple adders and multiplexers *without* using digital multipliers [22], and therefore the power and area cost are not substantial.

B. PROPOSED CALIBRATION ALGORITHM

While the traditional LS minimization is still applicable to the NS-SAR ADC calibration, using the same method in NS-SAR ADCs leads to sub-optimal bit weights. This is due to the presence of shaped quantization noise. Specifically, the LS method assumes that the quantization error is white over the entire Nyquist band, and therefore the error term is simply the difference between the best estimate and

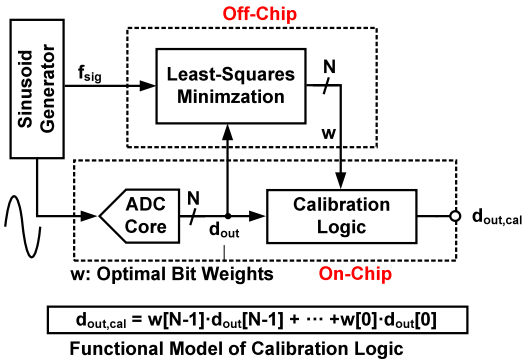


FIGURE 7. Conventional foreground digital domain calibration method.

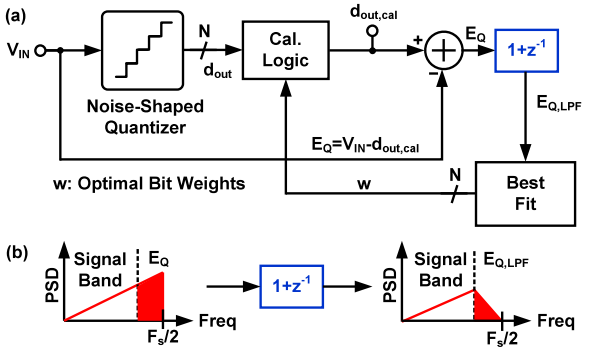


FIGURE 8. Proposed digital domain calibration algorithm optimized for noise-shaping.

the calibrated ADC output using optimal bit weights. However, in noise-shaping SAR ADCs, the quantization noise is enhanced at higher frequency, which hinders finding the truly optimal bit weights for NS-SAR ADCs. In other words, the high-frequency contents of quantization noise, which is in fact *not* critical in oversampled ADCs, is as equally treated as low-frequency noise when evaluating the objective function of the LS minimization in (4).

To exclude the impact of shaped quantization noise in the calibration process, this work uses a modified objective function in the original problem formulation by applying a simple $1 + z^{-1}$ filter to the error calculation, *i.e.*,

$$\begin{aligned} \text{minimize} \quad & \sum (err[i] + err[i+1])^2 \\ & \text{variables } A_s, A_c, w[0], \ldots, w[N-1] \\ \text{subject to} \quad & err[i] = \sum_{k=0}^{N-1} d_{out}[k][i] \cdot w[k] - y_i, \\ & y_i = A_s \cdot \sin(2\pi f_{sig} t_i) \\ & \quad + A_c \cdot \cos(2\pi f_{sig} t_i), \quad i = 1, \ldots, M, \end{aligned} \tag{5}$$

where $err[i]+err[i+1]$ in the objective function is the result of applying the $1 + z^{-1}$ filter. Fig. 8-(a) shows the modified setup for the new calibration, which we call noise-shaped least-squares (NS-LS) method. Since the magnitude response of the $1 + z^{-1}$ filter exhibits low-pass characteristic with

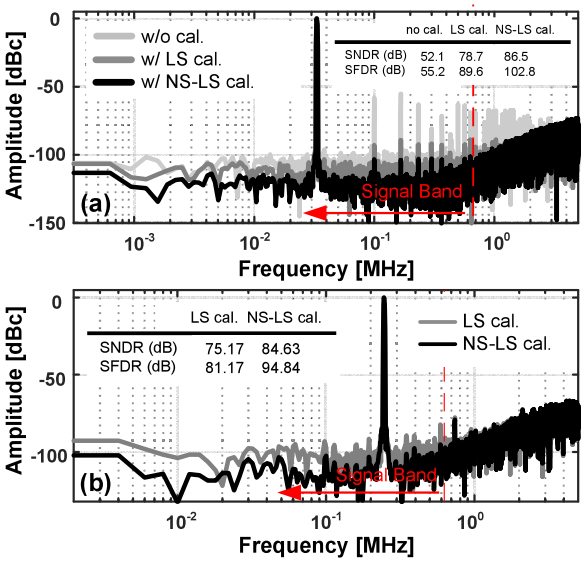


FIGURE 9. (a) Simulated output spectrum with random unit capacitor mismatch of $1\sigma = 5\%$ with and without LS and NS-LS calibration. (b) Simulated output spectrum with LS and NS-LS calibration using a fully-extracted circuit netlist that contains systematic capacitor mismatch in CDAC.

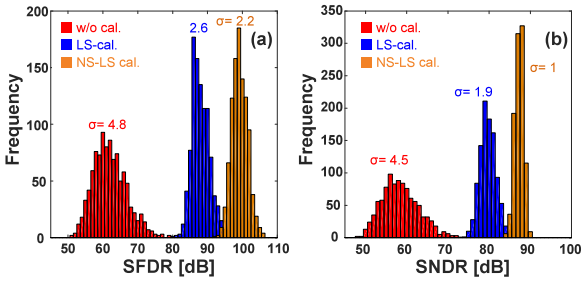


FIGURE 10. Histogram of (a) SFDR and (b) SNDR from 1000 monte carlo simulations, showing the advantage of NS-LS calibration.

a null at Nyquist frequency, this filter can effectively suppress the quantization noise beyond signal band as illustrated in Fig. 8-(b) and the obtained bit weights will result in higher linearity compared to using digital weights obtained from the NS-agnostic LS-minimization. Note that the filtering we introduce is applied only in the process of finding bit weights; this is different from a conventional low-pass decimation filter used in the noise-shaped ADCs in which the filtering is applied to the ADC outputs. The design tradeoff here is the resolution of the bit weights in the calibration logic versus the accuracy of the calibration. In this work, we use 11-bit resolution for the weights, which is high enough for the desired linearity specification. Note that there is little concern on the complexity of the low-pass filter because this filter is not implemented in actual hardware. Also, one may think that similar benefit could be obtained by applying digital low-pass filter *after* performing conventional LS-based calibration. However, the quantization error at the ADC output is already nearly white, and therefore post-filtering the ADC output cannot achieve the same benefit.

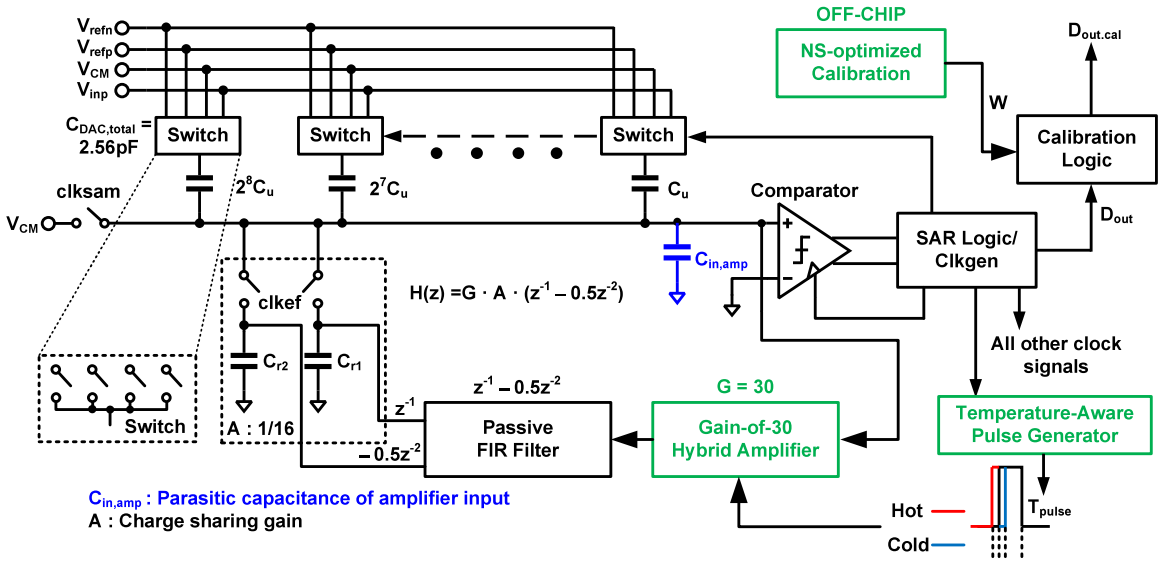


FIGURE 11. Proposed 2nd-order NS-SAR ADC architecture.

To verify the performance improvement, we have tested the new algorithm using both 1) a behavioral 2nd-order NS-SAR ADC model having random CDAC mismatches and 2) a fully-extracted transistor-level ADC circuit simulation that suffers from systematic CDAC mismatch arising from metal wire routing capacitance. First, we added $\sigma = 5\%$ mismatch to all unit capacitors in the CDAC of the 2nd-order NS-SAR ADC behavioral model, and compared the SNDR and SFDR of those from the simulation after applying the LS and NS-LS calibration. Fig. 9-(a) shows the resulting output spectrum, where a noticeable difference between two cases is observed. With NS-LS algorithm, the SNDR improves by 34 dB thanks to the calibration. However, traditional LS calibration achieves only 26 dB SNDR improvement. Second, we used a fully-extracted transistor-level simulations for similar comparison, and Fig. 9-(b) displays the resulting output spectrums. The NS-LS calibrated ADC output achieves SNDR of 84 dB while LS calibration yields SNDR of only 75 dB, verifying the effectiveness of new algorithm. For more exhaustive experiments, we ran 1000 Monte Carlo simulations utilizing the behavioral ADC model, and Fig. 10 shows the histogram of SNDR and SFDR after applying both LS and NS-LS calibrations. As expected, the proposed NS-LS calibration algorithm improves SNDR by around 10 dB more when compared to LS-calibration in addition to having narrower SNDR and SFDR spread.

One last note is that our selection of simple 1-pole $1 + z^{-1}$ filter would not yield optimal performance for all NS-SAR ADCs. Rather, one many need to find proper filter order and the pole frequency considering the order of noise shaping and the oversampling ratio of the ADCs.

IV. CIRCUIT IMPLEMENTATION

Fig. 11 displays overall architecture of the NS-SAR ADC. The core ADC is a 9-bit bottom-plate-sampled asynchronous SAR ADC with a binary-scaled capacitor DAC. With unit capacitance of $C_u = 5$ fF, the total capacitance of the DAC is 2.56 pF. The 2nd-order noise shaping is implemented as the error-feedback topology, which is similar to [3]. The key difference is that this work does not reuse the comparator as a residue amplifier. Instead, the hybrid amplifier described in section II provides an upfront gain of G before driving the amplified residue voltage to the passive FIR filter. The output of entire ADC is digitally calibrated in the calibration logic using the optimal bit weights that are found by the algorithm presented in section III.

The gain of the amplifier is chosen to compensate the signal loss in the passive charge sharing in the error feedback. Specifically, the charge on two reservoir capacitors C_{r1} and C_{r2} is shared with CDAC total capacitance during the SAR conversion, leading to the feedback path gain $H(z) = G \cdot A \cdot (z^{-1} - 0.5z^{-2})$, where A is the signal attenuation factor due to the charge sharing. Choosing $C_r = 180$ fF and $C_{DAC,total} = 2.56$ pF results in attenuation factor $A = C_r/(C_{DAC,total} + 2C_r) = 0.0616$, which requires total gain of the amplifier $G = 30$ in order maximize the SQNR for a target OSR of 8 as previously analyzed in [3].

Fig. 12 shows the details of the feedback path circuit. A two-stage amplifier consisting of a temperature-compensated differential dynamic amplifier and a differential ring amplifier [18] achieves total gain of 30. The transistor-level schematic for the ring amplifier is shown in Fig. 13, where a fully-differential ring amplifier in [18] is re-sized for our design specification. Output common-mode of the ring amplifier is regulated by the switched-capacitor common-mode feedback loop where $V_{CM} = 0.5V$ is used. The temperature-aware pulse generator introduced in Fig. 5 is utilized to maintain the gain over the full temperature range. A low power CMOS bandgap reference [23] is used for the proposed PTAT current generation.

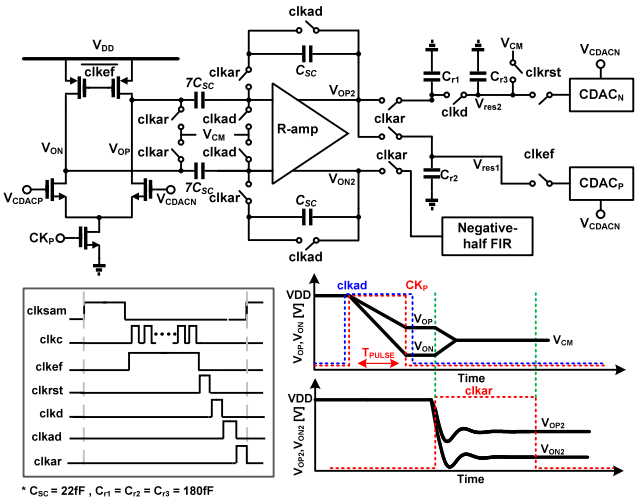


FIGURE 12. Feedback path implementation using the hybrid amplifier and the passive FIR filter.

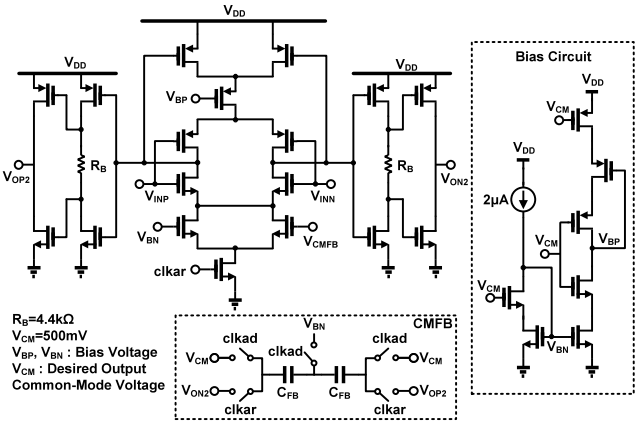


FIGURE 13. Schematic of ring amplifier used in proposed hybrid amplifier.

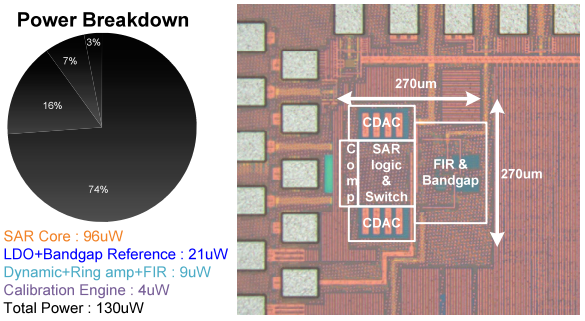


FIGURE 14. Power breakdown and die photograph.

The operation of the passive FIR filter and the amplifier occurs sequentially using multiple clock phases as illustrated in the Fig. 12. Specifically, a short clock pulse *clkrst* after the regular SAR conversion resets the dummy capacitor C_{r3}, and the voltage on C_{r1}, which is the residual quantization error from the previous conversion, is halved and stored on C_{r3} when *clkd* is high. Therefore, V_{res2} corresponds to the $0.5z^{-2}$ path signal. Subsequently, *clkad* activates the temperature-aware pulse generator that triggers the dynamic amplifier with gain of 4.3 while the differential ring amplifier is in the sampling mode. When *clkar* is high, the ring amplifier input is shorted to common-mode voltage in order for the negative feedback loop to realize a gain of 7 amplification. The amplified output is stored on the two memory capacitors C_{r1} and C_{r2}, one of which is used immediately to generate V_{res1} for z^{-1} operation. Finally, combining V_{res1}, V_{res2}, and ADC input signal by charge sharing when *clkef* is high achieves the desired NTF of $1 - H(z)$.

Table 1 shows the noise breakdown of our ADC. The noise calculation is based upon the block diagram in [3], where they find integrated noise voltages after applying a transfer function from the noise injection node to the output. It turns out that the thermal noise of the residue amplifier is the largest noise source with 59.5% of noise contribution. This is in line with a previously reported paper in [3] having a similar error-feedback architecture, where the residue amplifier is reported to contribute 68% of the total noise. In a more noise-optimized design, one can assign more current in the dynamic amplifier and simultaneously scale up the C_{SC} in Fig. 12 to reduce the noise contribution of the residue amplifier while keeping the gain characteristic of the dynamic amplifier.

V. MEASUREMENT RESULT

Fig. 14 shows the die photograph and power breakdown of the prototype ADC chip. The design is fabricated in 65-nm CMOS process and the ADC core occupies an active area of 0.072 mm^2. The sampling rate is 10 MS/s and the effective bandwidth is 625 kHz with an oversampling ratio of 8. The input full scale is $1.8V_{ppdiff}$. The ADC consumes 130 μW from 1V/1.8V supply, where only 9 μW is consumed in the feedback path amplifier and FIR filter. The 1.8V supply is used for bandgap reference and the LDO in the pulse generator, and the rest of the ADC runs under 1V supply. The synthesized digital calibration logic is not fabricated on-chip but its power is included in the total power consumption. The simulated power of the synthesized calibration logic using 11-bit of weight resolution is only 4 μW when running at 10MHz. Moreover, the calibration logic occupies 0.00235 mm^2, which is only 3% of total area. The calibration algorithm in (5) is implemented by utilizing CVX [24], a convex-optimization software package.

Fig. 15-(a) compares the measured spectrum with and without the noise shaping when $f_{sig} = 197$ kHz. The signal frequency is chosen such that 3rd-order harmonic tone is included in the signal bandwidth for proper measurement. Noise shaping improves the SNDR by 11.56 dB and the SFDR improves by 17.06 dB with 2^{nd}-order noise shaping. The SNDR improvement from the noise shaping is limited by the thermal noise. Fig. 15-(b) compares the performance improvement from using traditional LS and the proposed NS-LS algorithm, where NS-LS achieves higher SNDR and SFDR by 2.11 dB and 8.46 dB, respectively, when compared with LS algorithm. Note that the SNDR improvement is less

TABLE 1. Noise breakdown of proposed NS SAR ADC.

	Quantization Noise	kT/C Noise	Residue Amplifier Thermal Noise	Residue Amplifier Supply-Induced Noise	FIR Filter Noise
$V_{noise,rms}[\mu Vrms]$	21	18	53	30	15.6
Percentage	9.3%	6.4%	59.5%	19.5%	5.1%

TABLE 2. Performance summary and comparison table.

	This work	[6]	[1]	[25]	[26]	[27]	[15]	[3]
Process $[nm]$	65	90	65	65	65	28	65	40
Type	EF	CIFF	CIFF	CIFF	CIFF	CIFF	Pseudo-EF	EF
Supply Voltage $[V]$	1	1	1.2	1	0.9	1	0.8	1.1
Sample Rate $[MHz]$	10	25	90	64	80	3.2	50	10
Bandwidth $[kHz]$	625	625	11000	8000	2000	100	6250	625
Power $[\mu W]$	130	630	806	253	870	118	120.7	84
SNDR $[dB]$	71.35	80.4	62	64.9	73.8	69.3	58.03	79
Amplifier Type	Dynamic+Ring	Dynamic	Opamp	Passive	Passive	Passive	Passive	Dynamic
Temperature Tolerance	O	X	O	O	O	O	O	O
DAC Error Correction	NS-optimized	DEM	N/A	N/A	MES	DEM	N/A	Least-Squares
Area $[mm^2]$	0.072	0.08	0.03	0.0129	0.081	0.0575	0.0123	0.024
$\text{FoM}_{\text{Walden}}$ $[fJ/conv-step]$	34.4	58.9	36	10.9	54.3	251	14.8	9
FoM_{S} $[dB]$	168	170	163	170	167	159	165	178

FoM_{Walden} = Power/(2^{ENOB}*Sample rate), FoM_S = SNDR+10log(Bandwidth/Power)

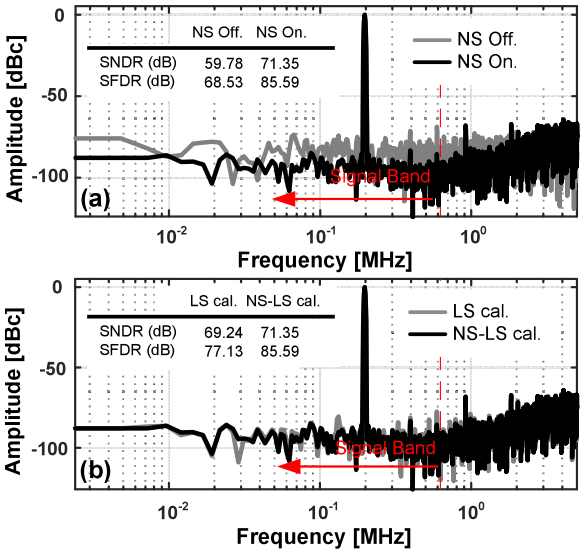


FIGURE 15. Measured output spectrum (a) with and without noise shaping and (b) with NS and NS-LS calibration.

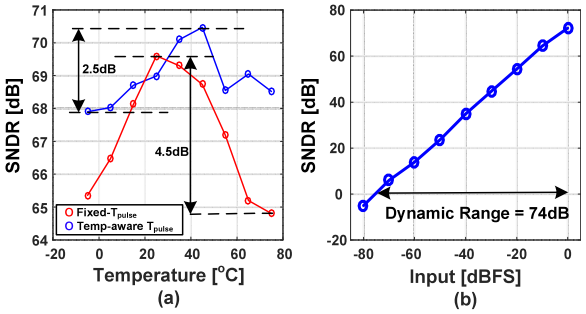


FIGURE 16. (a) Measured SNDR over temperature from −5 °C to 75 °C. (b) Measured SNDR versus input amplitude.

visible than the SFDR because the system thermal noise ultimately limits the achievable SNDR.

To demonstrate the temperature robustness, the entire ADC board is placed inside a temperature-cycling oven while varying the temperature from − 5 °C to 75 °C, and we evaluated the performance of the ADC by enabling and disabling the temperature-aware pulse generator. Fig. 16-(a) shows measured SNDR for this experiment, indicating that the ADC maintains the SNDR within 2.5 dB when the temperature-aware pulse generator is turned on. In contrast, the SNDR drops by as much as 4.5 dB at 75 °C when fixed-width pulse generator is used, demonstrating the effectiveness of our proposed technique. Fig. 16-(b) displays measured SNDR over full input range, which shows the dynamic range (DR) of 74 dB.

Table 2 summarizes the performance of our ADC along with previously published NS-SAR ADCs. This design achieves an FoMs of 168 dB and 171 dB based on SNDR and DR, respectively, and also FoMw of 34.4fJ/conv-step, which are comparable to other state-of-the-art ADCs designed in the same process node. Although our FoM is lower than the ADC such as [3] which is designed in a more advanced process,

the value of this work is successful demonstration of two new design techniques, which are 1) the temperature-tolerant dynamic amplifier *without* background calibration loop and 2) the algorithm that finds optimal bit weights of NS-SAR ADCs. Based upon the noise analysis presented in Table 1, we believe that the FoM can be further improved by 1) substantially reducing the sampling capacitor size (which allows reducing digital gate sizes at the cost of slightly more noise) and 2) assigning more current to the residue amplifier to reduce noise contribution. Given that the core ADC currently consumes 74% of the total power, this strategy will lead to a lower power design while maintaining the noise performance.

VI. CONCLUSION

This paper presented a 2nd-order noise-shaping SAR ADC design in 65-nm CMOS with peak SNDR of 71.35 dB over 625 kHz bandwidth. The SNDR performance is maintained within 2.5 dB from −5 °C to 75 °C even though the design uses a dynamic amplifier in the feedback path, which is enabled by the temperature-aware pulse generator based on PTAT biasing and efficient combination of a dynamic and a ring amplifier. Also, a customized algorithm called NS-LS that finds optimal digital bit weights was presented, and its validity has been extensively verified by both model-based simulations and measured results.

In summary, our measured results demonstrate the effectiveness of two new design techniques, the temperature-tolerant low-power implementation of dynamic amplifier and the NS-aware calibration algorithm. These techniques are highly digital in nature, and therefore are expected to be applicable to many other data converter designs in highly scaled CMOS processes.

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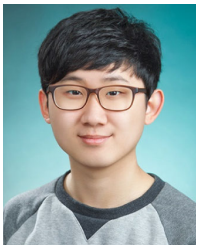

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