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A Simple and Adjustable Technique for Effective Linearization of Power Amplifiers Using Harmonic Injection

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ABSTRACT A simple and effective method for linearization of power amplifiers (PAs) is proposed. The method is based on the second harmonic injection into the input of the PA. The second harmonic is generated in a feedback path by taking the low-power transistors of a pseudo-differential pair amplifier to their nonlinear regime. The amplitude and phase of the second harmonics are controlled by tunable matching networks of the pseudo-differential pair which include trimmer capacitors. Using a theoretical analysis, we show that the proposed method is capable of canceling the third-order intermodulation signal at the PA output. As a proof of concept, a 10-W PA in a frequency band of 1.4 - 1.6 GHz is designed and linearized. By fabricating both the reference and linearized PAs and performing measurements under several conditions, it is experimentally demonstrated that applying the proposed scheme, thanks to its adjustability, highly linearizes the PA in a wide bandwidth and a wide range of output power.

INDEX TERMS Adjacent channel power ratio, intermodulation distortion, power amplifiers, linearization techniques, second harmonic injection, tunable matching network.

I. INTRODUCTION

Power amplifiers (PAs) are an essential part of every communication system whose characteristics greatly impact the system performance. In order to achieve high output power (P_{out}) along with high-efficiency, PAs can be used very close to their saturation region [1]–[3]; however, due to the nonlinear effects at saturation, they would suffer from amplitude and phase distortion and also undesired intermodulation signals. On the other hand, the use of amplitude and phase complex modulated signals with a high peak to average power ratio (PAPR) in modern communication systems calls for high linearity of PAs as well [4]. Although by taking a back-off from saturation, it is possible to have a proper degree of linearity, this would result in a significant drop in efficiency as well as P_{out} [5]–[8]. Therefore, design and implementation of high-efficiency linear PAs, although necessary and important, is complicated and challenging.

To address the problem, linearization methods such as feedback, feedforward, and analog and digital pre-distortion have been developed over the years that each has its own advantages and disadvantages [9]–[16]. For example, the analog pre-distortion (APD), which is one of the widely used linearization techniques, is simple and inexpensive to implement with low power consumption; however, to achieve a high level of linearization, a large number of diodes (or transistors) are required to model the inverse characteristic of the PA accurately which leads to increasing the complexity and the insertion loss of the circuit. Moreover, the diode-based APD linearizers suffer from the temperature sensitivity of their amplitude and phase characteristics circuitry [17], [18]. Harmonic injection (HI) is an effective method for improving the linearity and increasing the efficiency of PAs, which has a number of advantages; such as, good performance on broadband signals, simplicity, low cost, and no dependency on the input signal. In this technique, the second harmonic (SH) of the RF signal is injected into either the output [19], [20] or the input [21]–[26] of the PA. By tuning the amplitude and phase of the injected SH signal, the third-order intermodulation (IMD3) signal can be canceled with the opposite phase, which improves the PA linearity. In a comparison between HI at the input and output of the PA, HI at the output requires a

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higher power level of the SH injection signal, which requires the use of an additional PA or driver working at the SH frequency. In contrast, when injecting the SH to the input, linearization is achievable with a lower power level of the SH signal [21]–[26].

In previous works on the injection of the SH into the PA input, a part of the input signal is sampled, and a SH frequency is generated by using a frequency doubler. An amplifier and a phase-shifter are used to adjust the amplitude and phase of the SH signal, and the signal is injected into the PA input by a diplexer. However, sampling a part of the input signal reduces the gain, and using the frequency doubler, phase-shfiter, and diplexer increases the complexity of the circuit. Furthermore, the amplification and phase-shift of the SH signal requires devices working in the SH frequency which may increase the cost in high-frequency designs.

This paper presents a new implementation of linearization based on the SH injection at the input. In the proposed scheme, a small portion of the P_{out} at the main frequency is sampled in a feedback path, and by using a pseudo differential pair (PDP) amplifier consisting of two low-power transistors operating at the main frequency, a suitable level of the SH is generated and injected to the PA input. Amplitude and phase adjustment of the injected SH signal are easily made by four trimmer capacitors placed in PDP matching circuits. Additionally, in order to prevent the gain reduction, at the main frequency, a weak positive feedback from the output to input of the PA is provided by the PDP. Unlike previous methods, the proposed design does not require amplifiers operating at SH frequency. Also, the need for frequency doubler, phase-shifter, and diplexers has been eliminated, which increases the simplicity and lowers the system price. Moreover, by readjusting the variable capacitors, linearization is achieved in a wide frequency band and for a wider range of P_{out}. We first theoretically show that how applying our proposed linearization technique reduces the IMD3 level at the PA output, and then, as a proof of the concept, this technique is employed to an L-band PA. Our simulations and experimental measurements validate the concept of the proposed method.

II. METHOD DEVELOPMENT AND DESCRIPTION

FIGURE 1 shows the block diagram of the proposed linearization scheme in which, a small portion of the P_{out} at the main frequency is sampled through a feedback path and given to a SH generating (SHG) network, consisting of a PDP of two identical low-power transistors. By taking these low-power transistors to their nonlinear regime, the SH of the main frequency is produced at the output of the SHG which is then injected to the input of the main PA.

A two-tone analysis is performed to show the capability of the proposed scheme to reduce the IMD3 signal. Assuming that the RF input consists of two tones ω_1 and ω_2 with the same amplitudes, the main frequency signals, higher-order harmonics, and intermodulation signals will appear at the output of the PA. If the PA is well-linearized, the intermodulation

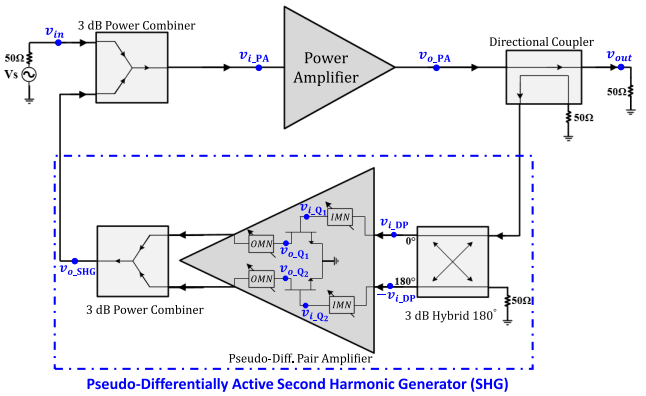


FIGURE 1. Block diagram of the proposed linearization method.

signals' level will be much lower than the level of the main tones. Also, considering that the sampling directional coupler (at the PA output) is designed at the main frequency, by ignoring the higher harmonics, the sampled signal entering the SHG block can be fairly approximated as a summation of the two fundamental tones. The sampled signal enters the differential pair (DP) amplifier through a 180-degree 3-dB hybrid designed in the range of the main frequencies. Notice that for the simplicity of the analysis, here we assume the low-power transistors are in pure differential; however, later we will discuss why in FIGURE 1 a pseudo differential configuration is considered. Therefore, the voltage at the input of one the DP transistors can be written as

$$v_{i\_\text{Q}_1} \approx V_{i\_\text{DP}} G_{\text{IMN}} \left[\cos(\omega_1 t + \Phi_{i\_\text{DP}} - \Phi_{\text{IMN}}) + \cos(\omega_2 t + \Phi_{i\_\text{DP}} - \Phi_{\text{IMN}})\right], \quad (1)$$

where V_{i_DP} and Φ_{i_DP} are the amplitude and phase of the input signal to the DP amplifier, and G_{IMN} and Φ_{IMN} are the voltage gain and phase delay of the DP input matching network (IMN) at the main frequencies, respectively. The voltage at the other DP transistor's input is $v_{i\_\text{Q}_2} = -v_{i\_\text{Q}_1}$.

Considering that the nonlinear characteristic of a transistor can be approximated as a third-order polynomial [27]

$$v_o \approx g_1 v_i + g_2 v_i^2 + g_3 v_i^3, \quad (2)$$

the voltages at the output of the DP transistors are obtained as,

$$v_{o\_\text{Q}_1} \approx g_1^L v_{i\_\text{Q}_1} + g_2^L v_{i\_\text{Q}_1}^2 + g_3^L v_{i\_\text{Q}_1}^3, \quad (3)$$

$$v_{o\_\text{Q}_2} \approx -g_1^L v_{i\_\text{Q}_1} + g_2^L v_{i\_\text{Q}_1}^2 - g_3^L v_{i\_\text{Q}_1}^3, \quad (4)$$

where, the superscript ^{L} indicates the parameters of the DP low-power transistors. These signals after passing output matching networks (OMNs) are combined in-phase, so by adding (3) and (4) (with a factor of $\frac{1}{\sqrt{2}}$) and then substituting (1), the voltage at the SHG output (v_{o_SHG}) is obtained as,

$$v_{o\_\text{SHG}} \approx V_{o\_\text{SHG}} \left[\cos(2\omega_1 t + \Phi_{o\_\text{SHG}}) + \cos(2\omega_2 t + \Phi_{o\_\text{SHG}}) + 2\cos((\omega_1 + \omega_2)t + \Phi_{o\_\text{SHG}})\right], \quad (5)$$

where,

$$V_{o\_\mathrm{SHG}} = \frac{1}{2\sqrt{2}} g_2^L G'_{\mathrm{OMN}} G^2_{\mathrm{IMN}} V^2_{i\_\mathrm{DP}},$$
$$\Phi_{o\_\mathrm{SHG}} = 2\Phi_{i\_\mathrm{DP}} - 2\Phi_{\mathrm{IMN}} - \Phi'_{\mathrm{OMN}} - \Phi'_{\mathrm{C}}, \quad (6)$$

and G'_{OMN} and Φ'_{OMN} are the voltage gain and phase delay of the DP OMN, respectively, and Φ'_{C} is the phase-shift between the input and output ports of the combiner, all at the SH frequency. Eq. (5) shows that the odd harmonics at the output of the SHG are canceled, and only the SHs remain.

The generated SH signal (v_{o_SHG}) is injected to the input of the PA using a wideband power combiner with an operating frequency range covering the main and SH frequencies. Assuming that the input signal of the circuit consists of two tones with the same amplitude V_{in} and phase of zero (as a reference phase), by injecting v_{o_SHG}, the voltage at the input of the PA (v_{i_PA}) is written as,

$$\begin{aligned} v_{i\_\mathrm{PA}} &= cV_{in}[\cos(\omega_1 t - \Phi_{\mathrm{WC}}) + \cos(\omega_2 t - \Phi_{\mathrm{WC}})] \\ &\quad + c' V_{o\_\mathrm{SHG}} \left[\cos(2\omega_1 t + \Phi_{o\_\mathrm{SHG}} - \Phi'_{\mathrm{WC}}) \right. \\ &\quad + \cos(2\omega_2 t + \Phi_{o\_\mathrm{SHG}} - \Phi'_{\mathrm{WC}}) \\ &\quad \left. + 2\cos((\omega_1 + \omega_2)t + \Phi_{o\_\mathrm{SHG}} - \Phi'_{\mathrm{WC}})\right], \end{aligned} \quad (7)$$

where c and c' (Φ_{WC} and Φ'_{WC}) are the attenuation coefficients (transmission phase delays) of the input wideband combiner in the main and SH frequencies, respectively. By substituting (5) in (7) and the outcome in (2), at the PA output, IMD3 component is obtained as,

$$\begin{aligned} v_{o\_\mathrm{PA}}|_{\omega_{\mathrm{IMD3}}} &= cV_{in}[\frac{3}{4} g_3^H (c^2 {V_{in}}^2 + 10 {c'}^2 {V_{o\_\mathrm{SHG}}}^2) \\ &\quad \times \cos(\omega_{\mathrm{IMD3}} t - \Phi_{\mathrm{WC}}) + g_2^H c' V_{o\_\mathrm{SHG}} \\ &\quad \times \cos(\omega_{\mathrm{IMD3}} t + \Phi_{o\_\mathrm{SHG}} + \Phi_{\mathrm{WC}} - \Phi'_{\mathrm{WC}})], \end{aligned} \quad (8)$$

where ω_{IMD3} is the IMD3 angular frequencies, i.e., $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, and superscript ^{H} denotes the parameter of the high-power amplifier (main PA). Assuming that $g_1, g_3 > 0$, and $g_2 < 0$, and recalling (6), fulfilling the following condition, in an ideal case, leads to the cancellation of IMD3 signals:

$$G^2_{\mathrm{IMN}} G'_{\mathrm{OMN}} = k_0 \left(\frac{1}{G^H V^2_{i\_\mathrm{DP}}}\right) \times \left(1 \pm \sqrt{1 - (k_1 G^H V_{in})^2}\right), \quad (9)$$

$$2\Phi_{\mathrm{IMN}} + \Phi'_{\mathrm{OMN}} = 2\Phi_{i\_\mathrm{DP}} - \Phi_0 \pm 180^\circ, \quad (10)$$

where $G^H = g_3^H / g_2^H$, $k_0 = 2\sqrt{2}/\left(15c' g_2^L\right)$, $k_1 = 15c/\sqrt{10}$ and $\Phi_0 = \Phi'_{\mathrm{C}} + \Phi'_{\mathrm{WC}} - 2\Phi_{\mathrm{WC}}$ are constants.

In fact, by adjusting the voltage gain and phase delay of the input and output matching networks of the DP amplifier (G_{IMN}, G'_{OMN}, Φ_{IMN}, and Φ'_{OMN}) so that the conditions of (9) and (10) are fulfilled, it would be possible to cancel the IMD3 signal. To this end, in the proposed linearization scheme as shown in the block diagram of FIGURE 1, tunable matching networks at the input and output of the DP amplifier are employed. It is worth mentioning that by adjusting these gains and phase delays, we merely tune the amplitude and phase of the injected signal.

In our above analysis if the injected signal to the input (v_{o_SHG}) is only the SH, about half of the input power (at the main frequencies) is dissipated in the isolation resistance of the wideband power combiner, which leads to a gain drop of about 3 dB. To prevent this gain reduction, the injected signal can contain the main harmonics (with a level below the input signal level), in addition to the SHs, so that the main harmonics level at the PA input becomes approximately equal to their level at the circuit input. This can be achieved by slightly altering the operating DC bias points of the two low power transistors. In that case, this pair of transistors would have a ''pseudo-differential'' configuration rather than pure differential. It is also worth mentioning that in FIGURE 1, tunning the matching networks of the PDP amplifier affects not only the amplitude and phase of the SH but also those of the main harmonics in the injected signal. Therefore, these matching networks should be adjusted by monitoring the IMD3 level along with the PA gain.

Finally we note that by setting the PDP transistors in two slightly different DC bias points, the third-order polynomial coefficients of the two low power transistors (g_1^L, g_2^L, and g_3^L) will not be identical but slightly different, also the injected signal (v_{o_SHG}) will contain a level of the main harmonics which are not considered in our analysis. Consequently, fulfilling (9) and (10) will not guarantee the cancellation of IMD3 signals in practice. In fact, by providing the theoretical analysis above, we aimed to conceptually show the possibility of IMD3 cancellation using the proposed scheme; however, in a practical design, there is no way to analytically derive conditions guaranteeing IMD3 cancellation, and a practical circuit adjustment is inevitable.

III. CIRCUIT IMPLEMENTATION

According to the block diagram of FIGURE 1 and the description provided in the previous section, for a PA with a specific operating power and frequency range, the circuit implementation of the proposed linearization scheme includes the followings.

1- Designing an SHG network including a PDP of low-power transistors with tunable matching circuit operating at the main frequency, a 180-degree hybrid in the main frequency and a combiner in the SH frequency.

2- Designing a wideband power combiner with a frequency range including both the main and SH frequencies at the input of the circuit.

3- Designing a directional coupler in the operating bandwidth of the PA at the output of the circuit.

4- Connecting the designed blocks according to the topology of FIGURE 1 and adjusting the circuit by tunning the matching networks of the PDP (which adjusts the amplitude and phase of the injected signal) to reduce the IMD3 level while not degrading the gain of the PA.

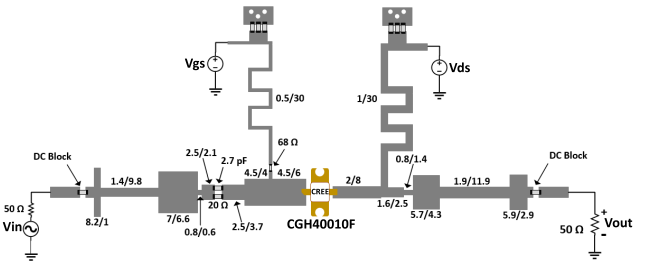


FIGURE 2. Schematic of the 10-W reference PA.

In the following, as proof of concept, we design a 10 W amplifier in the L-band frequency and then implement the proposed technique to linearize it. Notice that the operating frequency and power level of the PA are selected arbitrarily based on the equipment available to us. Rogers RO4003C laminate with a dielectric constant of 3.55, a loss tangent of 0.0027, and a thickness of 0.8 mm was used as substrate in our design. All the simulations were performed in Keysight's Advanced Design System (ADS).

A. DESIGNING THE REFERENCE PA

As shown in FIGURE 2, using a 10-W GaN transistor from Wolfspeed (CGH40010), a class-AB PA with an operating frequency band of 1.4 - 1.6 GHz was designed. According to the device datasheet, the transistor was biased at a drain-source voltage of $V_{DS} = 28$ V and a drain current of $I_{DQ} = 200$ mA. By performing source-pull and load-pull simulations using the nonlinear transistor model, impedance matching networks were designed as shown in FIGURE 2. In order to stabilize the transistor, a parallel RC and a resistor were used at the input matching network and the gate's DC branch, respectively. The gain and power added efficiency (PAE) variation of the designed PA versus (P_{out}) at 1.5 GHz are shown in FIGURE 3, demonstrating a PAE of 57.3 % and a gain of 14 dB at $P_{out} = 40$ dBm which is the output 3-dB compression point (P3dB).

B. DESIGNING THE SHG NETWORK

In order to select suitable transistors for PDP, first in a multi-tone simulation, the designed PA in the previous section was excited by tones ω_1, ω_2, $2\omega_1$, $2\omega_2$ and $\omega_1 + \omega_2$. By changing the level and phase of SHs at the input, their optimum level was obtained about 15 dBm to reduce IMD3 at the output. For satisfying this level and considering the available transistors (and their nonlinear models), ATF511P8 (GaAs-PHEMT from Avago Inc.) with an output P1dB of 30 dBm was used. Our simulations showed that this transistor is able to produce the desired level of the SH by injecting a signal of about 12 dBm to 16 dBm in the main harmonic. Two transistors were biased at the same voltage of 4.8 V but had slightly different currents of 270 mA and 290 mA to form a PDP, (the slight difference between the bias currents was obtained in a trial and error process to achieve the best performance). According to the datasheet recommendation, lumped-element matching circuits for the input and output

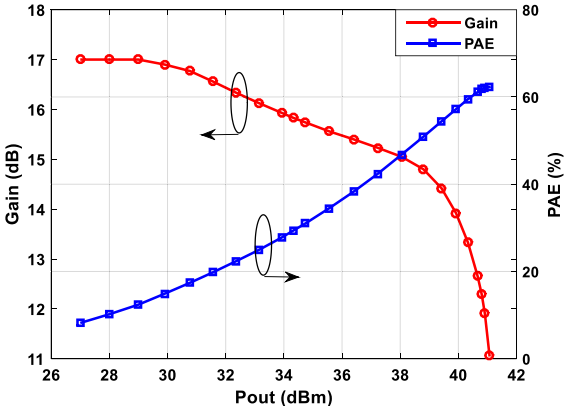


FIGURE 3. Simulated gain and PAE of the reference PA vs P_{out} at 1.5 GHz.

of these transistors at the main harmonic frequency were designed. As shown in FIGURE 4, in each matching circuit, a trimmer capacitor was placed to tune the voltage gain and phase delay of the matching network (as described in Section II) which results in adjustment of the amplitude and phase of the injected signal. It should be noted that by changing the capacitance of the variable capacitors in their tunning range the stability is maintained.

At the input of the SHG network, a 180-degree microstrip rat-race hybrid at the main frequency was used to obtain two signals with a 180-degree phase difference. A symmetric Wilkinson power combiner operating at the SH frequency range (2.8-3.2 GHz) was also designed and placed at the output of the SHG network. A schematic of the designed SHG network is depicted in FIGURE 4.

C. DESIGNING THE INPUT COMBINER AND THE OUTPUT COUPLER

Considering the main harmonic power level at the PA output (40 dBm) and the main harmonic power level required at the SHG input (20 dBm such that each amplifier of PDP has an input power of around 16-17 dBm), a directional coupler with a coupling coefficient of 20 dB and minimum insertion loss at the PA operating frequency was designed and placed at the output of the PA. Also, to combine the power of the input signal and the injection signal (including the SH and the main harmonics) at the input of the circuit, a wideband two-stage Wilkinson combiner covering 1.4 GHz to 3.2 GHz was designed [28].

D. CIRCUIT ADJUSTMENT

The trimmer capacitors in the PDP matching networks (named C_{ti}, C_{to}, C_{bi}, and C_{bo} in FIGURE 4) were tuned to minimize the IMD3 while not degrading the gain of the PA considerably. According to our simulation results, at $P_{out} = 36$ dBm and 1.5 GHz operating frequency, by setting C_{ti}, C_{to}, C_{bi}, and C_{bo} to 1.2 pF, 2.2 pF, 1.6 pF, and 1.8 pF, respectively, the IMD3 at 10 MHz frequency interval between tones is improved by 39 dB with only a 0.1 dB loss of total gain.

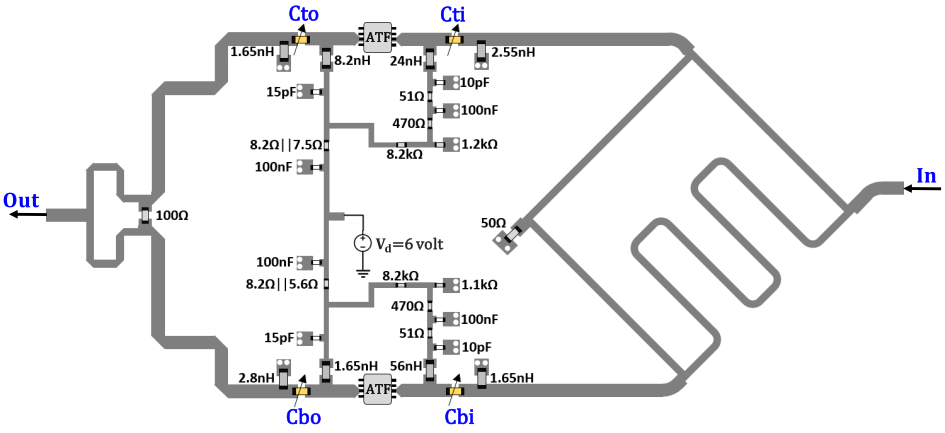


FIGURE 4. A schematic of the SHG network consists of a 180-degree rat race hybrid, a PDP amplifier, and a power combiner.

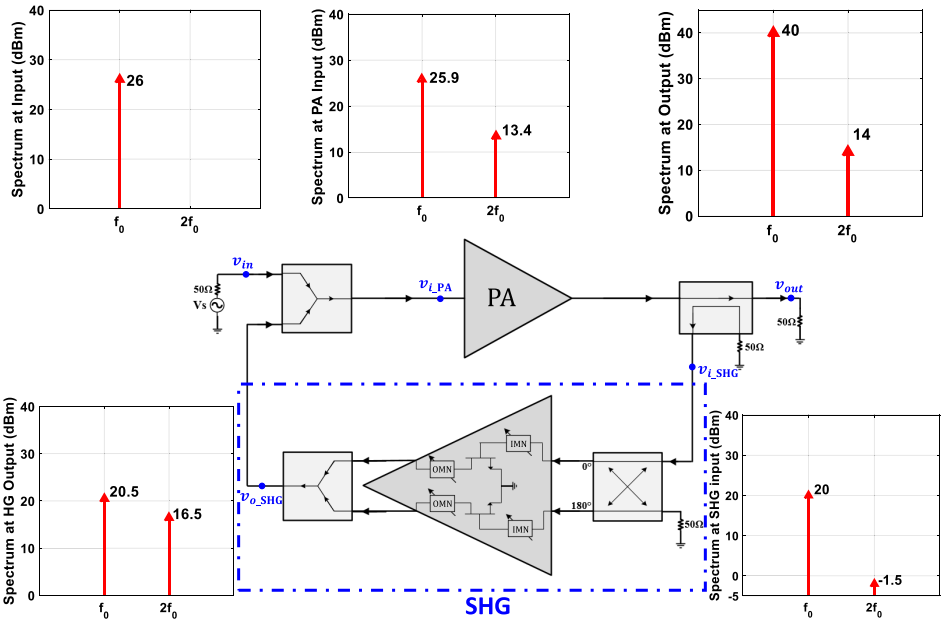


FIGURE 5. Power spectrum at different nodes of the circuit.

E. REMARKS

To ensure the realization of the idea behind the work, we first evaluate the single tone behavior of the circuit by inspecting the main and second harmonics at different nodes, as shown in FIGURE 5. The circuit was excited by a single tone at $f_0 = 1.5$ GHz with a level of 26 dBm. At the output of the PA, the main and the second harmonic levels are equal to 40 dBm and 14 dBm, respectively. After sampling the P_{out} by the directional coupler, at the input of the SHG network, the first and second harmonic levels are reduced to 20 dBm and −1.5 dBm, respectively. At the SHG output, the main harmonic power level is 20.5 dBm (approximately 6 dB lower than the input signal level), and the SH has a level of 16.5 dBm. This level of the SH at the SHG output is due to the nonlinearity of the low-power transistors of the PDP, not due to the amplification of the SH which is available at the SHG input because the PDP amplifier is designed in the main frequency range, therefore, it has quite a low linear gain (S21 of around −1 dB) at the SH frequency. The injection of the SHG output into the PA input leads to having a SH level of 13.5 dBm and a main harmonic level of 25.9 dBm (only 0.1 dB lower than input signal level) at the input of the PA, thus preventing the degradation of the total gain.

It should be noted that the injection of the main harmonic into the input of PA actually provides a weak positive feedback which leads to preventing gain reduction. Due to this weak positive feedback, it is necessary to ensure the stability of the entire circuit (in addition to individual amplifiers). For this purpose, Rollet's stability (K) factor and $|\Delta|$ (where Δ is the determinant of the scattering matrix) of the whole two-port circuit are shown in FIGURE 6, which shows the network is still stable while applying the feedback.

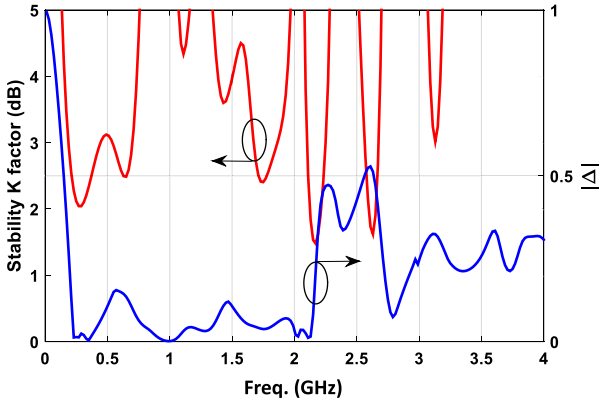
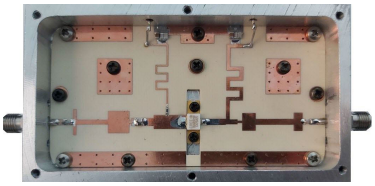
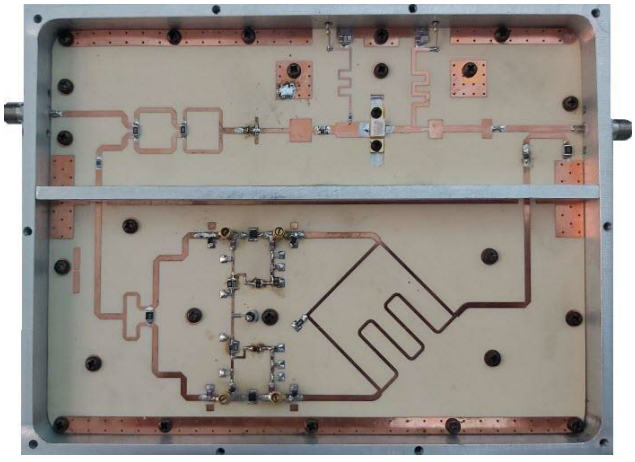


FIGURE 6. Stability factor and |Δ| of the designed circuit.



(a)



(b)

FIGURE 7. Fabricated (a) reference and (b) linearized PAs.

IV. FABRICATION AND MEASUREMENT AND RESULTS

As shown in FIGURE 7, two 10-W PAs were fabricated, one as a reference PA (FIGURE 7a) and one linearized using the proposed scheme (FIGURE 7b). The PAs were measured under two-tone, single-tone, and modulated-signal excitations. The details and results are provided in the following.

A. TWO-TONE TEST

The PAs were excited with two same-level tones with a spacing of 10 MHz at a center frequency between 1.4 GHz and 1.6 GHz. The trimmer capacitors in the PDP matching networks (C_{ti}, C_{to}, C_{bi}, and C_{bo}) were adjusted at different frequencies (1.4, 1.5, and 1.6 GHz) and different output powers to reduce IMD3 at the output of the PA along with preserving the PA gain. TABLE 1 indicates the desired capacitance range

TABLE 1. Desired capacitance range of trimmer capacitors in a 200 MHz bandwidth.

Capacitor (see FIGURE 4)	Desired capacitance range (pF)
C_{ti}	$1.2 - 2.4$
C_{to}	$1.8 - 3$
C_{bi}	$1.2 - 2.1$
C_{bo}	$1.5 - 3$

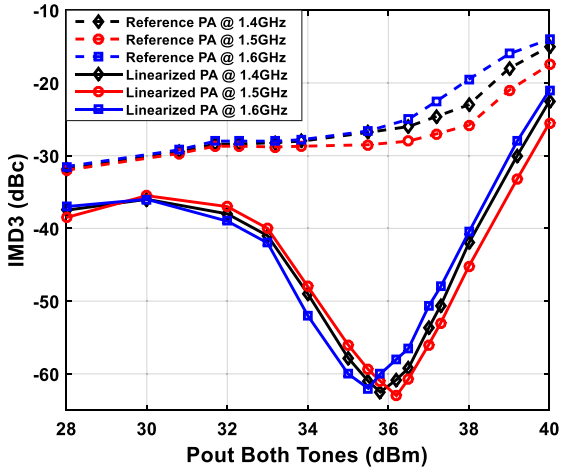


FIGURE 8. Measured IMD3 (10 MHz tone spacing) of the PA at different frequencies with and without proposed linearization.

of these variable capacitors. It is observed that their optimum capacitances vary in a small range from 1.2 pF to 3 pF.

The measured IMD3 of the reference and linearized PAs at 1.4, 1.5, and 1.6 GHz are indicated in FIGURE 8. This figure clearly shows that the level of linearization (IMD3 reduction compared to the reference PA) is almost the same at different frequencies. In addition, owing to the readjustment of variable capacitors at every level of P_{out}, considerable IMD3 improvement in a wide range of output back-off (OBO) is observed, such as an IMD3 reduction of better than 9 dB can be seen from 8-dB OBO ($P_{out} = 32$ dBm) to the saturation point ($P_{out} = 40$ dBm) at every frequency. This demonstrates the ability of the proposed adjustable technique to significantly improve the linearity in a wide bandwidth and a wide range of P_{out}. However, in FIGURE 8, it is seen that the IMD3 improvement is less significant for very low and very high levels of P_{out}. At very high P_{out} levels when the PA is deeply saturated, the drain's voltage and current waveforms are clipped and cannot be reshaped into a sinusoidal waveform by adding a few harmonics. At very low P_{out} levels, the second harmonic injection can linearize the PA; however, in our proposed scheme shown in FIGURE 1, the second harmonics are not sufficiently produced because the PDP transistors do not reach their nonlinear regime, hence less efficient linearization.

In FIGURE 8, it can be also seen that the best IMD3 improvement is around 35 dB occurring at a 4-dB OBO, i.e., an P_{out} of 36 dBm. According to our experiments, for this level of OBO, the optimum value of the variable capacitors (C_{ti}, C_{to}, C_{bi}, and C_{bo}) is 1.4 pF, 2.5 pF, 1.7 pF, and 2 pF,

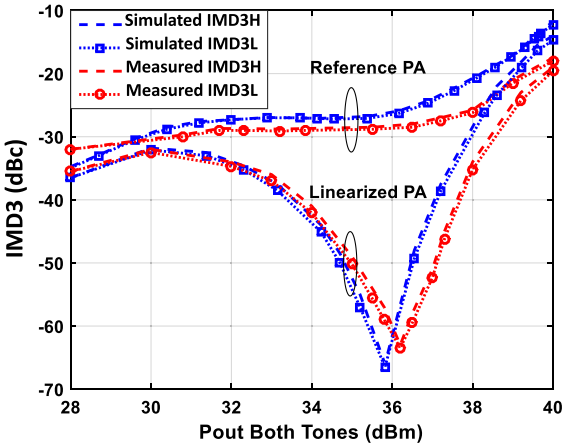


FIGURE 9. Measured and simulated IMD3 of the reference and linearized PAs with 10 MHz tone spacing at 1.5 GHz for a fixed value of trimmer capacitors.

respectively at 1.5 GHz, which is a good match with their optimum values in the simulation (1.2 pF, 2.2 pF, 1.6 pF, and 1.8 pF, respectively). In an additional experiment, the trimmer capacitors were set to these values, and without changing them, the IMD3 was measured at different levels of P_{out}. The result is given in FIGURE 9 and is compared with the reference PA. Notice that in this figure, IMD3L and IMD3H denote the IMD3 at the lower and upper sides of the input signals, respectively, which are almost the same (IMD3L is very slightly lower than IMD3H in both the reference and linearized PAs). Importantly, we can see that, even without readjustment of the variable capacitors, IMD3 is improved compared with the reference PA; however, at output powers far from 36 dBm, this improvement is not as good as the one in FIGURE 8. Besides, the simulation and measurement results are compared in FIGURE 9, demonstrating an excellent agreement between them.

B. SINGLE-TONE TEST

By exciting the linearized and reference PAs by single-tone signals, the gain and PAE were measured at three frequencies, 1.4 GHz, 1.5 GHz, and 1.6 GHz, where the results are reported in FIGURE 10. In these experiments, the variable capacitors were set to their optimal values at 4-dB OBO at every frequency which are provided in the figure. Linearization of the PA gain using the proposed method is evidently observed. Also, it can be seen that at 4-dB OBO, the gain of the linearized and reference PAs are identical. This is because the trimmer capacitors were tunned at this level of P_{out} with the aim of the best IMD3 improvement and preserving the PA gain as well. However, slight decreases in the PAE (around 5 percentage points in the worst case) are observed which are due to the power consumption in the low-power transistors of the PDP.

C. MODULATED SIGNAL TEST

Using an Agilent E4437B signal generator, a 64-QAM signal with a sampling rate of 8-MS/s (the highest rate available by

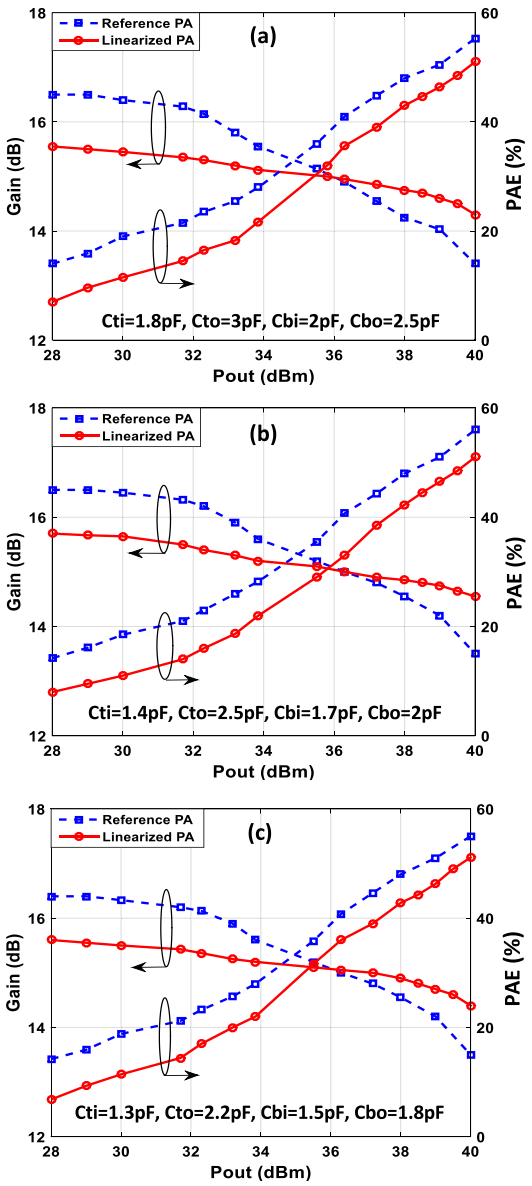


FIGURE 10. Measured gain and PAE of the fabricated reference and linearized PA at: (a) 1.4GHz, (b) 1.5GHz, and (c) 1.6GHz. Note that power consumption in the PDP transistors was considered in the PAE calculation.

this equipment) and a PAPR of 7.5 dB was generated and excited the PAs. The adjacent channel power ratio (ACPR) of the reference and linearized PAs under this modulated signal was measured in three frequency bands (1.4 GHz, 1.5 GHz, and 1.6 GHz) for different levels of P_{out} between 30 dBm and 40 dBm. By monitoring the ACPR as well as the P_{out} (i.e., the PA gain), the trimmer capacitors of the linearized PA were adjusted at every level of P_{out} for each frequency band. The results are given in FIGURE 11. The figure shows a noticeable improvement of between 8 dB (at 3-dB saturation) and 15 dB (at 4-dB OBO) in ACPR at every level of P_{out} in every frequency band due to the application of the proposed linearization method. FIGURE 12 shows the measured PAE of the reference and linearized PAs versus P_{out} under the

TABLE 2. Performance comparison between PAs linearized using a state-of-the-art analog technique.

[Ref.] Year	Linearization Technique	Freq. Band [GHz]	Psat [dBm]	IMD3 Improvement [dB]	Modulated Signal Test		
					Modulated BW [MHz] / PAPR [dB]	ACPR Improvement [dB]	PAE [%] / Pout [dBm] @-45 dBc ACPR
[29] 2016	Linearization Amplifier	0.78 - 0.92	37.8	19 @ 4-dB OBO 26 @ 9-dB OBO	15 / 8.4	13 @ 8.5-dB OBO	16.4 / 29.4
[30] 2018	Doherty	0.7 - 0.9	40.8	7 @ 2-dB OBO 16 @ 6-dB OBO	15 / 8.3	9 @ 8-dB OBO 12 @ 10-dB OBO	27.2 / 32
[31] 2019	APD	3.4 - 3.6	41.5	N/A	5 / 7	11.1 @ 6-dB OBO	28.5 / 36
[32] 2018	APD	2.36 - 2.44	40	8 @ 2-dB OBO 16 @ 6-dB OBO	5 / 10.5	10 @ 6-dB OBO 13 @ 10-dB OBO	8 / 28.5
[33] 2020	APD	5.5	43	12.9 @ 3-dB OBO	N/A	N/A	N/A
[20] 2012	HI*	2.45	37	15 @ Psat 23 @ 4-dB OBO	N/A	N/A	N/A
[19] 2019	HI*	2.3	41.5	10 @ Psat	N/A	N/A	N/A
This Work	HI	1.4 - 1.6	40	9 @ Psat 35 @ 4-dB OBO 10 @ 8-dB OBO	8 / 7.5	8 @ Psat 15 @ 4-dB OBO 13 @ 10-dB OBO	33 / 35.5

* Needs a high level of injected second harmonic, approximately 10 dB below Pout.

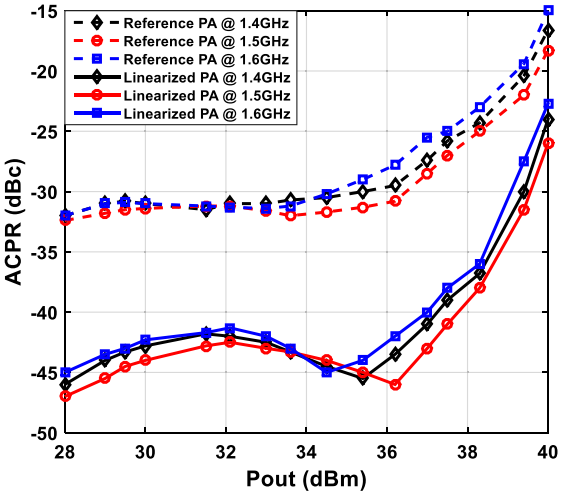


FIGURE 11. Measured ACPR of the reference and linearized PAs driven by 8 MS/s 64-QAM signals at three frequencies.

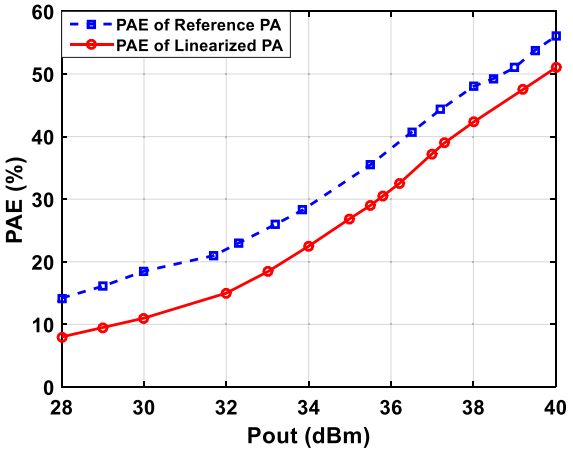


FIGURE 12. Measured PAE of the reference and linearized PAs driven by 8 MS/s 64-QAM signal at 1.5 GHz.

excitation of the signal centered at 1.5 GHz. It is seen that for a similar P_{out}, the linearized PA has a slightly lower PAE due to the power consumption of the PDP transistors. However, in a communication system where a certain level of linearization (ACPR) is required, the linearized PA can work at a higher P_{out} (see FIGURE 11), thus providing significantly higher efficiency. The normalized output spectrum of the reference and linearized PAs at 1.5 GHz and 4-dB OBO ($P_{out} = 36$ dBm), as an example, is plotted in FIGURE 13 showing a 15-dB improvement in ACPR after linearizing the PA. Note that the ACPR on the lower side of the bandwidth is slightly lower than that on the upper side, which is consistent with the slightly lower IMD3L compared to IMD3H in FIGURE 9.

D. PERFORMANCE COMPARISON

Finally, the performance of the linearized PA in this work is compared with some of those with a similar P_{out} linearized using a state-of-the-art analog technique. The comparison is summarized in TABLE 2. It can be observed that the proposed technique is capable of linearizion in a wide operating bandwidth while some techniques work in a very narrow bandwidth. In addition, looking at the IMD3 improvements, it is seen that our method not only has a great linearization performance at 4-dB OBO (35-dB improvement), but it also well linearizes the PA for a wide range of P_{out}, from 8-dB OBO to the saturation. While some linearization techniques show a good performance only for a certain P_{out}. These two important features are due to the adjustability of our method. A detailed comparison between the linearized PAs under modulated signal tests is also provided in the right column of TABLE 2, showing the high performance of this work, i.e. great ACPR improvements in a wide range of OBO and a high PAE and P_{out} when a certain level of ACPR is required.

Also, in comparison with [19], [20] using a HI technique, the required level of the injected second harmonic in our work is significantly lower due to the injection at the PA input.

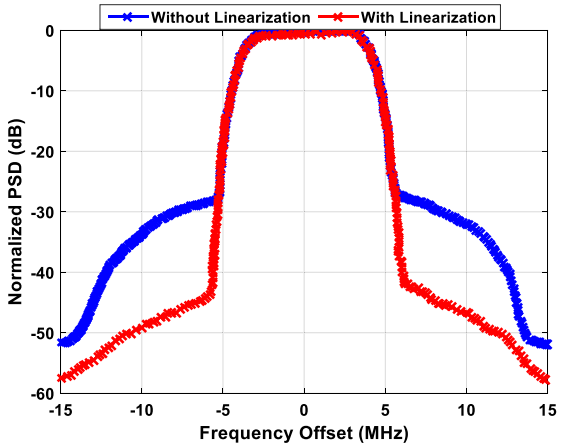


FIGURE 13. Measured output spectrum of the reference and linearized PAs at 1.5 GHz and 36 dBm P_{out} under an 8 MS/s 64-QAM signal excitation.

In those two works, the second harmonic signal with a high level (around 10 dB below the P_{out}) is required to be injected into the PA output, but generating this level of the second harmonic increases the complexity and the expense of the system due the need for a driver amplifier at second harmonic frequency. However, according to FIGURE 5, the level of the injected second harmonic in our design is almost 25 dB below the P_{out}, so we could simply and inexpensively generate it using two low-power transistors. Therefor, an important feature of our proposed design is its simple topology, which can be implemented at a low cost.

V. CONCLUSION

In this paper, a method based on the SH injection was proposed to linearize PAs. This method has a simple topology and a cost-effective implementation. A part of the PA P_{out} (in the main harmonic) is sampled and entered into a pair of low-power transistors in a pseudo-differential configuration. At the output of the PDP, the SH is generated by taking the low-power transistors to their nonlinear regime and then is injected into the PA input. A two-tone analysis showed that the IMD3 can be canceled by providing a suitable voltage gain and phase delay for the input and output matching networks of the PDP amplifier, which is identical to providing a suitable amplitude and phase of the injected SH signal. To this end, trimmer capacitors were employed in the matching networks of the PDP amplifier. Also, the bias currents of the PDP transistors were set slightly differently so that at the output of the SHG network, in addition to the SH, a low level of the main harmonics exists which prevents a drop in the PA gain.

As a proof of concept, a 10-W GaN class-AB PA with an operating frequency band of 1.4 - 1.6 GHz was designed and linearized. Meanwhile, the steps for the implementation of the proposed linearization method were described in detail. The linearized PA and the reference PA (without linearizing network) were fabricated and measured under different conditions. According to our two-tone measurements with a frequency interval of 10 MHz, by adjusting the variable capacitors, the IMD3 could be improved between 9 dB to 35 dB compared to the reference PA for P_{out} ranging from a 8-dB OBO to the saturation. Also, for a 8-MS/s 64-QAM modulated signal, the ACPR was improved between 8 dB to 15 dB for a wide range of P_{out}. The measurements were performed in the entire frequency design band which showed the broadband feature of the proposed linearization technique. The ability for linearization in a wide operating frequency band as well as a wide range of P_{out} is due to the adjustability of the scheme. Finally, it is worth mentioning that although in this work, trimmer capacitors are used for adjusting the circuit, their replacement with varacator diodes is straightforward. By adjusting the DC bias of the varactors based on the frequency, bandwidth, and level of the input signal, we plan to develop an adaptive linearizion method in our future work.

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