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Wideband Variable-Gain Amplifiers Based on a Pseudo-Current-Steering Gain-Tuning Technique

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ABSTRACT This paper reports two variable-gain amplifiers (VGAs) featuring a new pseudo-current-steering gain-tuning technique. In the first VGA (VGA-I), a single-voltage-controlled dual-branch current mirror is developed as a standalone gain control block. In the second VGA (VGA-II), two NMOS transistors, which are biased by a tunable voltage, are integrated into a conventional common-source amplifier to steer away from a part of the total current. Meanwhile, the theoretical analysis is developed to reveal the mechanism of different gain tuning. Fabricated in a 40-nm CMOS process, VGA-I (VGA-II) occupies a tiny area of 0.03 mm^2 (0.024 mm^2) and consumes 22 mW (20 mW). Measured over a gain range of > 64 dB, the -3-dB bandwidth of VGA-I (VGA-II) is 9 GHz (6.6 GHz). For the time-domain tests, VGA-I (VGA-II) exhibits a jitter of 40 ps (30 ps), under a 2^7-1 PRBS input at 12 Gb/s. Their power efficiencies (1.83 and 1.67 pJ/bit) compare favorably with state-of-the-art.

INDEX TERMS CMOS, high-speed transceiver, variable-gain amplifier (VGA), negative capacitance (NC), peak-to-peak jitter, data-dependent jitter (DDJ), pseudo-current steering, wide-tuning gain control, dual-branch current mirror, active inductor.

I. INTRODUCTION

Dynamic range is an important aspect of both wireless and wireline communication systems. It determines the capability of a transceiver to process and handle the signal, or the tolerance on the variation of input power. A wide dynamic range is always desirable since it makes the system insusceptible to interference and versatile for multi-standard applications [1], [2]. Therefore, great efforts have been made to maximize the dynamic range of a certain system. Although gain tuning technique has been implemented with various building blocks, such as low noise amplifier (LNA) [3], power amplifier (PA) [4], trans-impedance amplifier (TIA) [5], [6], etc., incorporating variable gain amplifier (VGA) is still the most efficient way to boost the dynamic range. Based on the control methods, two categories of VGAs are well adopted in the communication systems, namely, digitally-controlled VGA and analog-controlled VGA. The former usually employs an array of switchable resistors [7], [8]. Consequently, the gain changes in a discrete manner, leading to phase discontinuity which may cause problems in the system [9]–[11]. Meanwhile, if a large tuning range and fine gain steps are required, the large number of the control bits will exacerbate the complexity and power consumption of the circuit design. Therefore, continuously-tuned VGA controlled by the analog signal is more preferred.

Due to the rapid increase of data rate, wideband VGA is widely employed in both high-frequency and high-speed communications, such as in the baseband of 60-GHz wireless transceivers [12], and tens-of-Gb/s backplane receivers [13], [14]. To reach a bandwidth (BW) of several gigahertz, many efforts have been made during the last decade. Cherry-Hooper amplifier [15]–[17] is made use to extend the BW of VGA up to 2.2 GHz [18], while the

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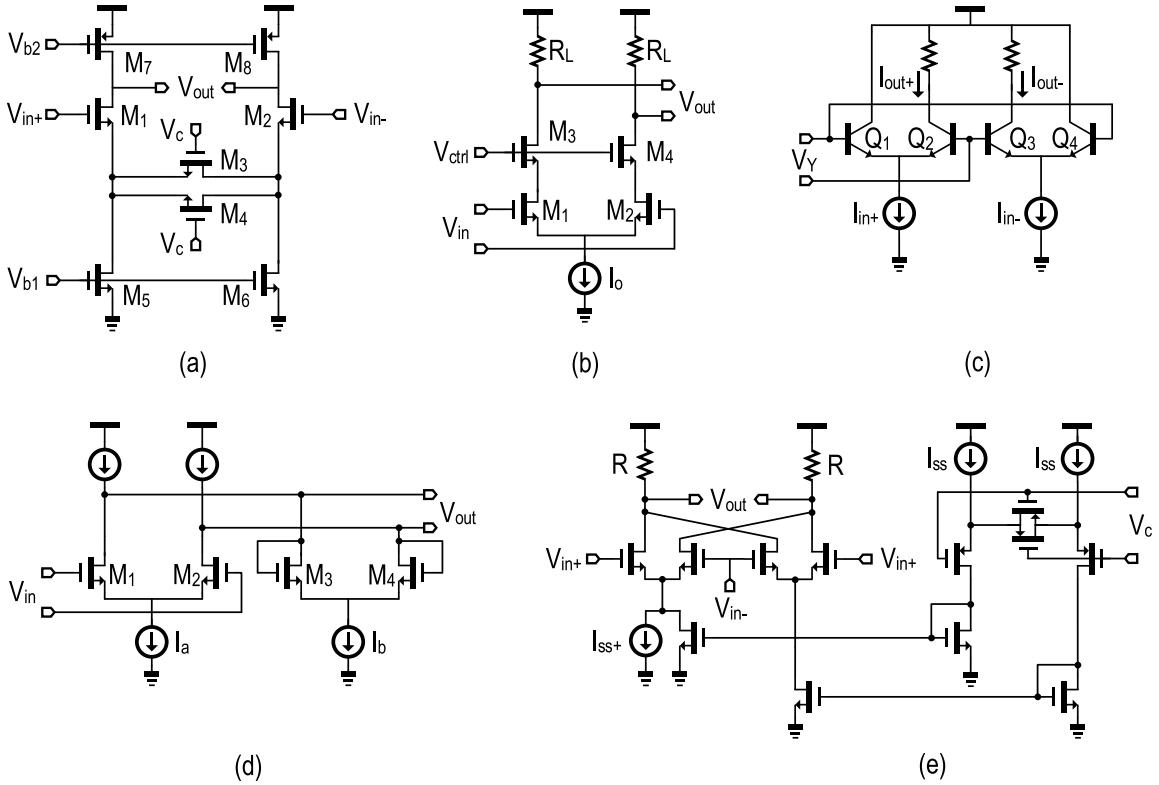

FIGURE 1. Overview of the state-of-the-art gain tuning methods.

grounded or floating active inductors [19]–[27] are used to further extend the BW to 4 GHz [19]. These prior works obtain a wide tuning range as well as low power consumption, but little design room is left for improvements on the BW. To alleviate the stringent requirement on both the gain range and BW, the overall architecture with a post-amplifier (PA) following the variable gain stage is extensively used [28]–[30]. In such a way, the cascading stages can provide an adequate small-signal gain while maintaining broadband feature, whereas the preceding stage only needs to take care of the gain tuning.

This paper reports a pseudo-current-steering gain-tuning method. By incorporating it into two different VGA topologies, both achieve a wide tuning range with a single variable-gain stage [31]. Their BW can be extended beyond 7 GHz, thanks to adopting the PA-embedded scheme. Section II overviews the state-of-art gain tuning methods from two different perspectives. Next, Section III elaborates the proposed gain tuning method and implementations with two variable-gain stages. The complete structures of VGAs are sketched out in Section IV. The measurement results are summarized in Section V, followed by a brief summary in Section VI as the conclusion.

II. REVIEW OF STATE-OF-THE-ART GAIN TUNING METHODS

Based on the control mechanism, the tuning methods can be categorized into voltage-mode and current-mode. The achievable gain tuning range depends strongly on the specific tuning methods and structure of the core amplifier. Next, we will review the state-of-the-art gain control methods and their implementation approaches.

To make use of single-ended voltage control, the signal can be applied to the source degenerative amplifier [32], [33] and cascode amplifier [34], so that their effective trans- conductance is adjustable, as shown in Fig. 1(a). By controlling the gate voltage of the source degenerative transistor, its resistance is increased with decreased biasing, and inversely for the overall gain. However, the transistor will not be turned on until the control voltage is above the sum of its threshold voltage and the drain-to-source voltage across the current tail transistor. Therefore, the useful gain control region, as well as gain variation range, are both limited. As for the cascode structure, as shown in Fig. 1(b), the source voltage of the cascode transistor follows its gate voltage, resulting in a change in the drain-to-source voltage of the input transistors. If the input transistor operates in the triode region, its transconductance varies. Therefore, the gate voltage of the cascode transistor must be high enough to keep the input transistor operating in the triode region. Such limitation prohibits this structure from low power applications. To attain a wide gain variation range with low supply voltage, the single-ended control voltage is applied to both of the feedback resistors and load resistors of the Cherry-Hooper amplifier in [15]–[18]. The two dominant factors of the voltage gain, namely transconductance and load resistance, tune the amplifier simultaneously. Meanwhile, the voltage-control signal can also be applied differentially, as shown in Fig. 1(c).

With the signal-summing VGA [35]–[38], the input signal is applied to the lower transistor pair while the upper-level transistors control the amount of current flowing to the output. Similar to the cascode structure, the range of control voltage also needs to be designed carefully, in order to guarantee a normal operation of the input transistors.

On the contrary, the current-control signal is usually applied differentially, such that the change in the current difference determines the gain of the amplifier. Although it is demonstrated in [39] that single-ended current-control is feasible for tuning the current tail of cascaded amplifiers, the common-mode voltage will be altered in such design, and to avoid problems caused by large variations, the tuning range must be restrained. To implement a differential current-control signal, one popular way is to use the architecture shown in Fig. 1(d), whose load and input transistor share a total current. This structure is efficient in a way that changes the gm and output resistance simultaneously, but the bandwidth keeps changing when the gain is tuned. Another popular choice is the Gilbert cell implementation [28]–[31]. As shown in Fig. 1(e), the lower transistor pair mirrors a differential current-control from the right-hand side circuit. With the input signal applied to the upper transistor pairs, the resultant output is the difference between the two branches of the amplifier.

The desirable feature of gain-tuning characteristics affects the evolution of the VGA's topologies. Generally, the state-of-the-art VGAs can be categorized into two groups: one of which requires a standalone gain-control block, either to convert the linear control voltage to an exponential output [28]–[30] or to enlarge the gain-control range [31], [40], while the other topology possesses the gain-control feature with the amplifier itself [41], [42]. The advantage of standalone topology is that the separate gain-control block is isolated from the signal path. Consequently, the performance of the amplifier, including frequency response, linearity, and power consumption, can be optimized independently. Furthermore, according to different requirements for each application, different exponential generators with desired accuracies and tuning ranges can be chosen, which provides the designers with another degree of freedom. The integrated VGAs, on the other hand, usually have a simpler structure, thereby reducing the size and complexity of the designs. Yet, the architecture is more confined with its corresponding gain-tuning algorithms, exacerbating the trade-off between BW, linearity, and power consumption.

III. PROPOSED GAIN-TUNING METHOD

A. CONCEPTUAL PRINCIPLE

Although the VGA designed in [22] has achieved extremely low complexity, it controls the gain of the amplifier in two steps. First, the negative exponential generator generates a differential control signal in the voltage domain. Then, a pseudo-folded Gilbert cell converts it into the current domain, controlling the two branches of the amplifier.

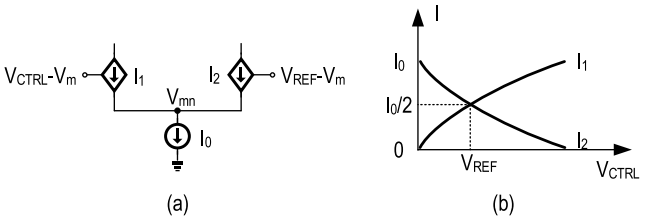

FIGURE 2. (a) Illustration of the proposed pseudo-current-steering gain-tuning technique. (b) Current flow versus gain-control signal (V_{CTRL}) corresponding to (a) when $\alpha_1 = \alpha_2$.

To further simplify the structure, the two-step conversion can be saved if the gain-control signal can be converted to a differential output in the current domain directly. The illustration is shown in Fig. 2(a), in which two voltage-dependent current sources share a constant total current of I_0, and the junction voltage (V_m) is flexible. Assuming one of the current sources is related to a variable voltage, V_{CTRL}, while the other is related to a fixed voltage, V_{REF}, and both of them have a negative voltage-to-current relationship regarding V_m. As a result,

$$I_1 = \alpha_1 (V_{CTRL} - V_m) \tag{1}$$

$$I_2 = \alpha_2 (V_{REF} - V_m) \tag{2}$$

where α_1 and α_2 are the voltage-to-current conversion coefficients of the two voltage-dependent current sources, respectively. Since the sum of I_1 and I_2 is immutable, V_m must change accordingly such that,

$$\alpha_1 (V_{CTRL} - V_m) + \alpha_2 (V_{REF} - V_m) = I_0 \tag{3}$$

The above condition in (3) should always be satisfied, from which the mechanism of current flows in the two branches can be deduced as depicted in Fig. 2(b). As the gain-control voltage increases, I_1 increases from 0 to I_0, while I_2 decreases to maintain a constant total current. If we set $\alpha_1 = \alpha_2$, each of the branch shares the same current, which equals to $I_0/2$, when V_{CTRL} is equal to V_{REF}. As a result, two continuously varying currents can be obtained from one single-ended control voltage, which could be used to adjust the transconductance (g_m) of the transistors and thus the gain of the amplifier. To implement this control method into VGA design, both standalone and integrated gain-control topologies are developed later.

B. IMPLEMENTATION WITH STANDALONE GAIN-TUNING TOPOLOGY

Fig. 3 shows a single stage of our proposed VGA with a standalone gain-control block. The single-ended gain control voltage, V_{CTRL}, is converted to a pseudo-differential current output, thereafter mirrored to the current tail of the gain amplifier on the right-hand side. To guarantee the amplifier's gain increases monotonically across the entire gain-control range, one of the PMOS transistors, M_1, is connected to V_{CTRL}, while the other one, M_2, is tight to the ground, such that the maximum current flowing through M_1 is half of the total current, which happens at $V_{CTRL} = 0$. Under this condition, the drain-to-source voltage of M_1 and M_2 are sustainably large, and the transistors work in the triode region, i.e. zone I

in Fig. 4. Since M_3 works in the saturation region, we have

$$I_1 = I_3 = K_1\left[(V_S - V_C - V_{th1})\,V_{SD} - \frac{1}{2}V_{SD}^2\right] = \frac{1}{2}K_3\,(V_{G3} - V_{th3})^2 \quad (4)$$

where V_S is the source voltage of M_1 and V_{SD} is the source-to-drain voltage of M_1. Then

$$V_{G3} = \sqrt{\frac{2K_1\left[(V_S - V_{CTRL} - V_{th1})\,V_{SD} - \frac{1}{2}V_{SD}^2\right]}{K_3}} + V_{th3} \quad (5)$$

When V_{CTRL} is increased, the overdrive voltage of M_1 becomes smaller than that of M_2, resulting in a larger current flowing through M_2 while less current through M_1. As the current through M_1 and M_3 are reduced, the node voltage at the drain of M_3 is decreased, pushing M_1 to operate in the subthreshold region. With M_3 remained in the saturation region, the current-to-voltage relationship is written as

$$I_1 = I_3 = I_{D0}exp\left(\frac{V_S - V_C - V_{th1}}{nV_T}\right)\left(1 - exp\left(\frac{-V_{SD}}{V_T}\right)\right) = \frac{1}{2}K_3\,(V_{G3} - V_{th3})^2 \quad (6)$$

where I_{D0} is the reverse saturation current and can be obtained from simulation; n is the subthreshold slope factor and can be expressed as $n = 1 + \frac{C_d}{C_{ox}}$, where C_{ox} is the gate oxide capacitance per unit area and C_d is barrier capacitance; V_T is the thermal voltage. Thus, it gives as

$$V_{G3} = \sqrt{\frac{2I_{D0}\frac{W}{L}}{K_3}\exp\left(\frac{V_S - V_C - V_{th1}}{nV_T}\right)\left(1 - \exp\left(\frac{-V_{SD}}{V_T}\right)\right)} + V_{th3} \quad (7)$$

At the same time, the node voltage between M_2 and M_4 keeps increasing to provide a larger current, making the transistor M_2 work in a deep triode region. Consistently in both zone I and II, we have

$$I_4 = I_2 = \frac{1}{2}K_4\,(V_{G4} - V_{th4})^2 = K_2\left[(V_S - V_{th2})\,V_{SD} - \frac{1}{2}V_{SD}^2\right] \quad (8)$$

where V_S is the source voltage of M_2 and V_{SD} is the source-to-drain voltage of M_2. Therefore,

$$V_{G4} = \sqrt{\frac{2K_2\left[(V_S - V_{th2})\,V_{SD} - \frac{1}{2}V_{SD}^2\right]}{K_4}} + V_{th4} \quad (9)$$

While V_{CTRL} keeps increasing, M_1 enters into the subthreshold region with a much smaller I_1 and M_2 maintains in the triode region to flow through most of the current. The difference in current keeps increasing until M_1 is fully turned off and the entire current goes through M_2, at which point the amplifier provides the maximum gain.

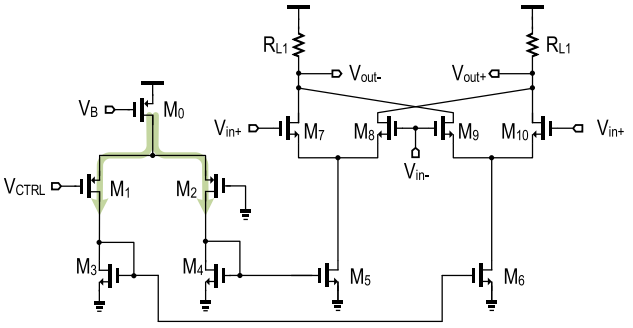

FIGURE 3. Schematic of VGA-I with standalone pseudo-current-steering gain control.

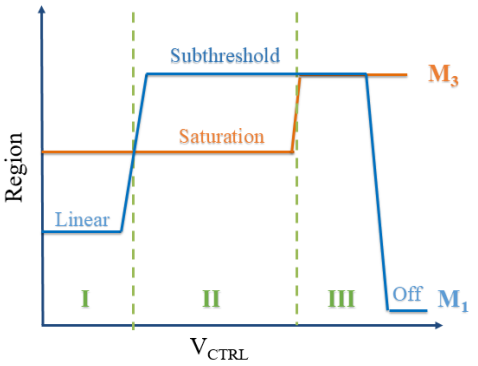

FIGURE 4. Analysis of the operation region of M_1 and M_3 in VGA-I.

Note that, when $V_{CTRL} = 0$, the amplifier's gain will be zero if the effects of the transistors' non-idealities are not considered. In a practical design, the layout routing from M_4 to M_5 is considerably shorter than the one from M_3 to M_6, leading to a relatively larger voltage drop of the latter one and thus a minimum gain close but not equal to zero. Simulation result reveals that one such stage can provide a wide-tuning gain range from -40 to 2 dB, with a BW of 20 GHz.

C. DESIGN WITH INTEGRATED GAIN-TUNING TOPOLOGY

Interestingly, our proposed pseudo-current-steering gain-control method can be integrated with a conventional amplifier as well. As illustrated in Fig. 5, an auxiliary NMOS transistor pair, M_3 and M_4, is placed parallel with the input differential pair, M_1 and M_2, while its gate is connected to V_{CTRL} instead of the input signal. Intuitively, the extra pair manipulates the effective gm by steering away a partial of the total current, thereby controlling the gain of amplifier. When the control voltage is much lower than the common-mode voltage, the control pair, M_3 and M_4, are turned off and the gain of the amplifier is fixed at its maximum level. As V_{CTRL} is gradually increased near to common-mode voltage, M_3 and M_4 start to turn on and work in the subthreshold region. Since the input pair works in the saturation region, only a small amount of current is steered away by the control pair. While V_{CTRL} is increased further beyond the common-mode voltage, the control pair steers away a considerable amount of current and still works in the subthreshold region due to its large transistor size. Meanwhile, the input transistor pair operate from the saturation region to the subthreshold region

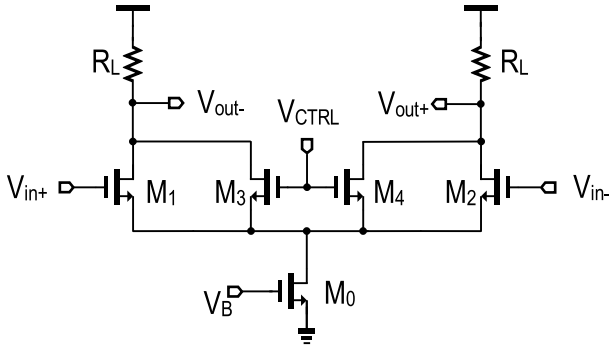

FIGURE 5. Schematic of VGA-II with integrated pseudo-current steering gain control.

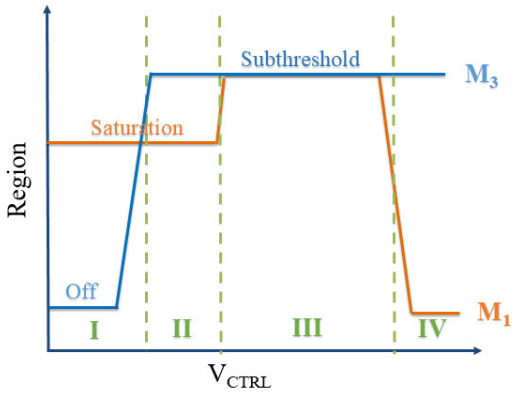

FIGURE 6. Analysis of operation region of M_1 and M_3 in VGA-II.

and even to the cut-off region. Thus, the transconductance of the input transistors shrinks continually, providing a lower and lower gain. The working region of the two pairs is shown in Fig. 6.

When both transistors are working in the subthreshold region, the current through the input and control transistor is given by

$$I_1 = I_{D0}\frac{W}{L}exp\left(\frac{V_G - V_S - V_{th1}}{nV_T}\right)\left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \tag{10}$$

and

$$I_3 = I_{D0}\frac{W}{L}exp\left(\frac{V_C - V_S - V_{th3}}{nV_T}\right)\left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \tag{11}$$

respectively. Since

$$\frac{I_0}{2} = I_1 + I_3 \tag{12}$$

we obtain

$$V_S = nV_T\left[ln\left(e^{\frac{V_G - V_{th1}}{nV_T}} + \frac{(W/L)_3}{(W/L)_1}e^{\frac{V_C - V_{th3}}{nV_T}}\right) - ln\left(\frac{I_0}{2I_{D0}}\left(\frac{L}{W}\right)_1\right)\right] \tag{13}$$

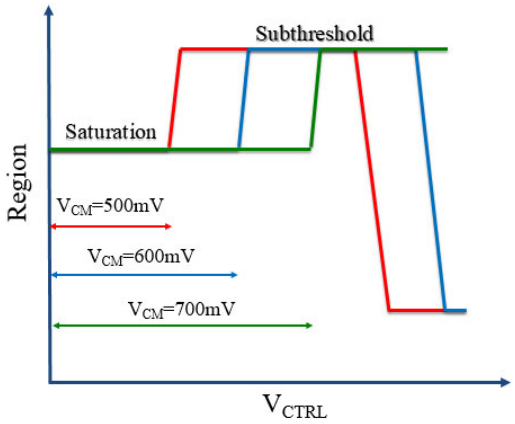

FIGURE 7. The effect of common-mode voltages on the transition point of the operating regions.

Since the effective transconductance of the amplifier (G_m) depends only on the g_m of the input transistor pair, it can be derived as

$$G_m = \frac{I_{D0}\frac{W}{L}\exp\left(\frac{V_G - V_S - V_{th1}}{nV_T}\right)}{nV_T} \tag{14}$$

Additionally, as the operating region of the input differential pair is determined by the difference between the common-mode voltage and control voltage, one can expand or shrink the gain control range by adjusting the common-mode voltage. Fig. 7 illustrates this idea by comparing different common-mode voltages from 500 to 700 mV. The higher the common-mode voltage is set, the later the transition from saturation to subthreshold occurs. To obtain the maximum gain tuning range with a wide gain control range, the common-mode mode of 600 mV is chosen, so that the control transistor is turned off when the control voltage is increased near to the supply voltage, i.e. 800 mV in this design.

Different from the traditional current-steering VGAs, as shown in Fig. 1(c), our proposed design adjusts the transconductance of the input transistors directly, instead of manipulating with the cascode device. In such a way, the number of devices stacked in each branch is reduced, making it suitable for low power applications. Moreover, the current goes through the load resistor does not vary under the different gain setting. Therefore, the common-mode voltage of the output node is constant, and any stage following the VGA can be directly coupled.

Compared to the topology in Fig. 3, this integrated design employs fewer transistors, but the parasitic capacitance accumulated at the output node may bring concerns for high-speed applications. Consequently, a BW of 17 GHz is obtained along with a gain ranging from -30 to 4 dB.

IV. COMPLETE ARCHITECTURE

Plotted in Fig. 8(a) and (b), two completed architectures are implemented with the abovementioned VGA-I/-II, respectively. Both of them comprise two variable gain stages, multiple fixed stages, a DC offset cancellation (DCOC) network, and an output buffer for testing. The broadband technique of

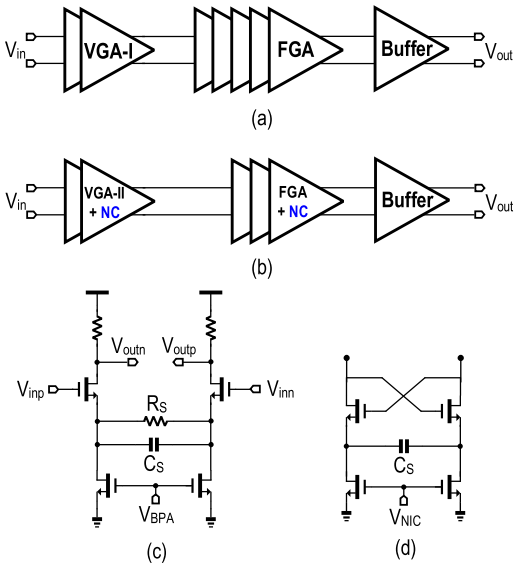

FIGURE 8. (a) Complete design-I for VGA-I with standalone gain control. (b) Complete design-II for VGA-II with integrated gain control. Detailed schematic of (c) fixed gain amplifier and (d) negative capacitance (NC) circuit.

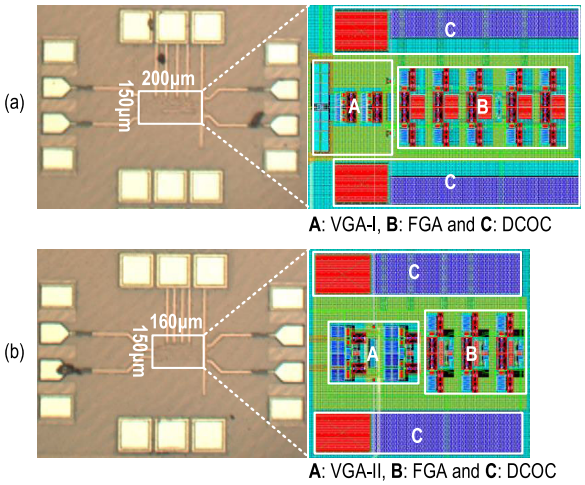

FIGURE 9. Chip photos and their detailed layouts of (a) design-I and (b) design-II.

resistive and capacitive degeneration is adopted in the fixed gain amplifier (FGA), to reduce the effect on bandwidth from cascading multiple stages.

To accommodate different features of the two variable gain stages introduced in the last section, care must be taken when incorporating them into the complete architectures (Fig. 3 and Fig. 5). In design-I, since the pseudo-Gilbert cell in Fig. 3 works in such a way that the gain provided by one input pair is minus from that of another, the resultant maximum gain is lower compared to the integrated design. Thus, five stages of the fixed gain amplifiers [Fig. 8(c)] are required to elevate its maximum gain up to 25 dB, each of which provides a gain of 4 dB with a power consumption of 3.5 mW. On the other hand, to improve the internal BW of design-II, the negative capacitance circuit [43]–[49] [Fig. 8(d)] is inserted between adjacent stages to partially cancel the larger node-to-ground capacitance. With a similar

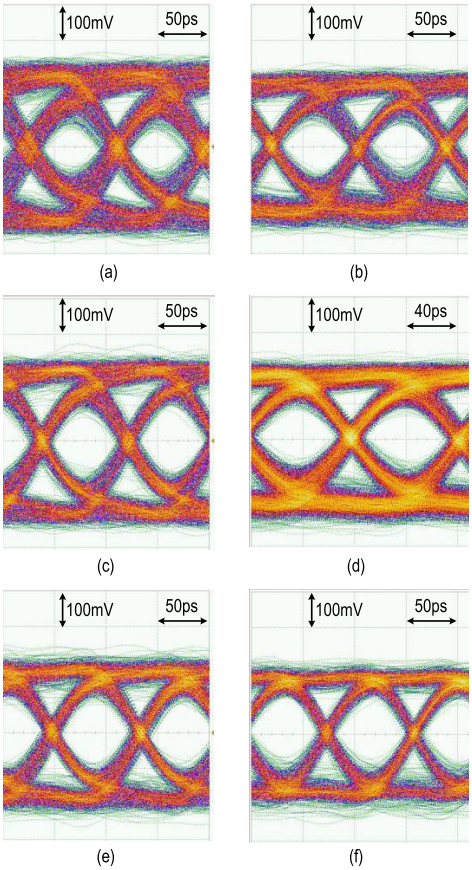

FIGURE 10. Measured eye diagrams at 12Gb/s with different input V_{in}: (a) design-I, V_{in} =75mV, (b) design-II, V_{in} =75mV, (c) design-I, V_{in} =250mV, (d) design-II, V_{in} =250mV, (e) design-I, V_{in} =1V, (f) design-II, V_{in} =1V when the input pattern is 2^7-1 PRBS.

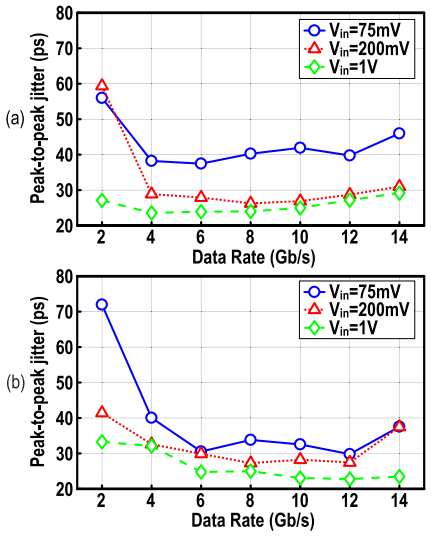

FIGURE 11. Measured peak-to-peak jitter versus data rate: (a) design-I and (b) design-II under different input swing (V_{in}), when the input pattern is a 2^7-1 PRBS.

power budget, three stages of the fixed gain amplifiers are cascaded, such that an overall gain of 23 dB is achieved. The DCOC employs a low pass filter followed by a transconductor cell, while the output buffer adopts the f_T doubler structure [30].

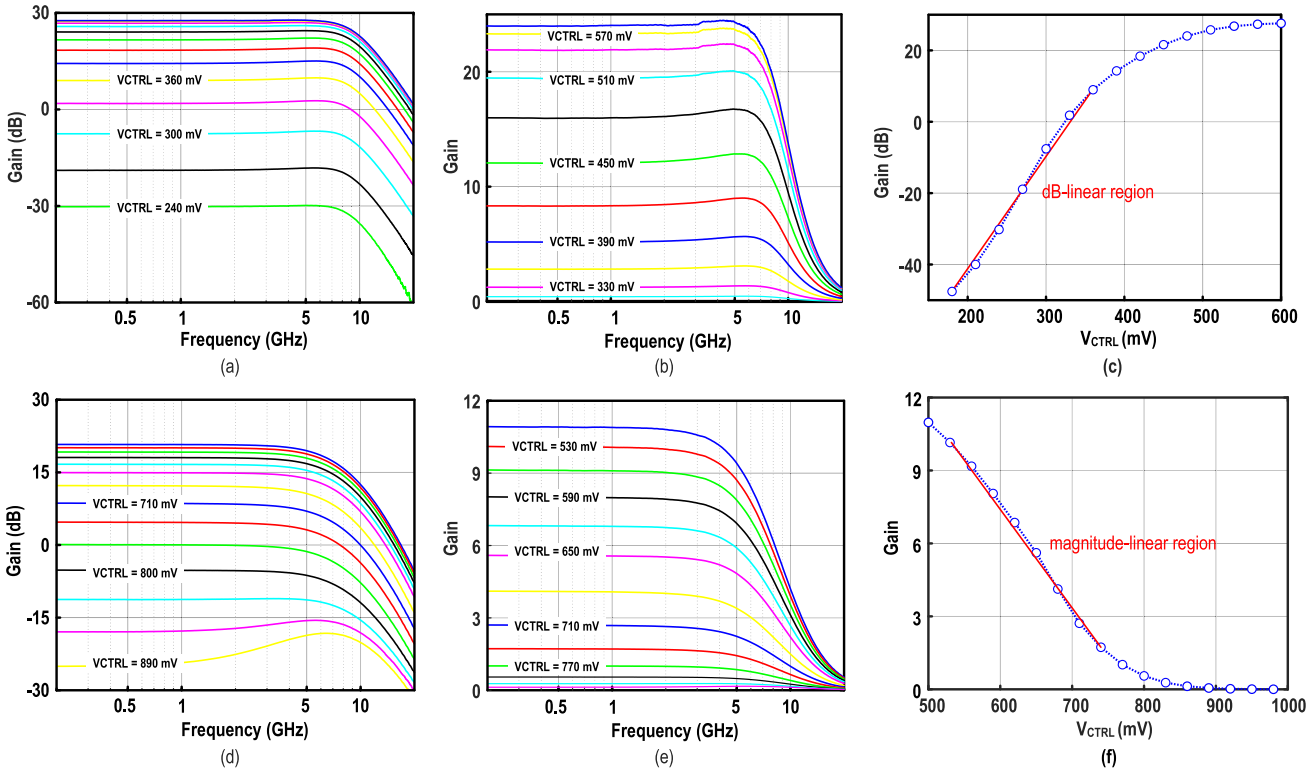

FIGURE 12. Mearsurement results: (a) frequency response of design-I in dB scale, (b) frequency response of design-I in linear scale, (c) gain characteristic of design-I in dB scale, (d) frequency response of design-II in dB sacle, (e) frequency response of design-II in linear scale, and (f) gain characteristic of design-II in linear scale.

TABLE 1. Performance summary and comparison of recent state-of-the-art VGAs.

Parameters	JSSC'12 [28]	JSSC'16 [29]	TCAS-I'18 [30]	TCAS-I'12 [18]	MWCL'15 [39]	ISSCC'04 [40]	This work	
							VGA-I	VGA-II
Technology	130nm BiCMOS	130nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS	180nm CMOS	**40nm CMOS**	
Data rate (Gb/s)	5	10	10	N/A	N/A	3.125	**12**	
Jitter (ps)	< 40	< 44	< 36	N/A	N/A	< 95	**40**	**30**
PRBS	2^{15}-1	2^{31}-1	2^{7}-1	N/A	N/A	2^{31}-1	**2^{7}-1**	
BW (GHz)	0.0002 to 7.5	0.0001 to 5.0	0.0001 to 7.0	0.0002 to 2.2	0.0002 to 4	0.0004 to 2	**0.0001 to 9**	**0.0001 to 6.6**
dB-linear	Yes	Yes	Yes	No	No	No	No	
Gain range (dB)	40 (-10 to 30)	40 (-15 to 25)	57 (-26 to 31)	60 (-10 to 50)	60 (-39.4 to 20.2)	50 (-16 to 34)	**74 (-47 to 27)**	**64 (-44 to 20)**
Power (mW)	72	50	28	2.5	26	40	**22**	**20**
Power eff. (pJ/bit)	14.4	5.0	2.8	N/A	N/A	12.8	**1.83**	**1.67**
Active area (mm^2)	1	0.4	0.045	0.01	0.06	0.7	**0.03**	**0.024**

V. MEASUREMENT RESULTS

Fig. 9 shows the chip photos of the proposed prototypes, both of which were fabricated in standard 40-nm CMOS technology, with an active area of 0.03 and 0.024 mm^2, respectively. Their time-domain performance is verified by the pseudo-random binary sequence (PRBS) with a length of 2^7-1, and the eye diagram is captured by the real-time oscilloscope, as shown in Fig. 10. With different levels of input swing under the weak, moderate, and strong conditions, the measured peak-to-peak jitter is plotted in Fig. 11, covering a data rate from 2 to 14 Gb/s. Under the lower data rate of 2 Gb/s, the jitter is prominent due to the DC wander resulting from the

DCOC network. At the higher data rate beyond 12 Gb/s, high-frequency peaking and its corresponding phase distortion incur data-dependent jitter and inter-symbol interference (ISI), so the time-domain waveform is worsened. In both cases, it is observed that higher input levels can lead to a better jitter performance. Moreover, frequency responses are measured by the network analyzer and are plotted in Fig. 12, both in conventional dB scale and linear magnitude scale. Although incorporating the negative capacitive circuit, design-II rolls off earlier ∼7 GHz, while design-I has a higher BW up to 9 GHz. This may owe to an insufficient compensation of negative capacitance or an underestimation of the parasitic capacitance from the simulation results. By plotting their gain characteristic over the gain-control voltage (V_{CTRL}) in both dB and linear scales, it is interesting to observe that both designs preserve a linear-in-magnitude feature in the high-gain mode whereas a linear-in-dB feature in the low-gain mode.

Table 1 shows the performance summary and comparison with recent state-of-the-art VGAs targeting for similar applications. Both designs show a wider gain range, higher power efficiency as well as a smaller core area.

VI. CONCLUSION

This paper presented a pseudo-current-steering gain-tuning method. Two design examples (Design-I and Design-II) were prototyped in a 40-nm CMOS. Measurement results show that this work obtains a wide gain range (>64 dB) and broad BW (> 6.6 GHz), while occupying a small active area (<0.024 mm^2) and achieving a high power efficiency (<1.83 pJ/bit) up to 12 Gb/s.

REFERENCES

[1] S. D'Amico, A. Baschirotto, M. De Matteis, N. Ghittori, A. Vigna, and P. Malcovati, "A CMOS 5 nV/$\sqrt{}$Hz 74-dB-gain-range 82-dB-DR multistandard baseband chain for Bluetooth, UMTS, and WLAN," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1534–1541, Jul. 2008.

[2] J. C. Fan, C. L. Liu, and L. G. Kazovsky, "Dynamic-range requirements for microcellular personal-communication systems using analog fiber-optic links," *IEEE Trans. Microw. Theory Techn.*, vol. 45, no. 8, pp. 1320–1331, Aug. 1997.

[3] R. Kulkarni, J. Kim, H.-J. Jeon, J. Xiao, and J. Silva-Martinez, "UHF receiver front-end: Implementation and analog baseband design considerations," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 2, pp. 197–210, Feb. 2012.

[4] H.-Y. Shih and C.-W. Wang, "A highly-integrated 3–8 GHz ultra-wideband RF transmitter with digital-assisted carrier leakage calibration and automatic transmit power control," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 8, pp. 1357–1367, Aug. 2012.

[5] W.-Z. Chen, Y.-L. Cheng, and D.-S. Lin, "A 1.8-V 10-Gb/s fully integrated CMOS optical receiver analog front-end," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1388–1396, Jun. 2005.

[6] T. Halvorsrod, O. Birkenes, and C. Eichrodt, "A low-power method adding continuous variable gain to amplifiers," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 1593–1596.

[7] M. A. I. Mostafa, S. H. K. Embabi, and M. Elmala, "A 60-dB 246-MHz CMOS variable gain amplifier for subsampling GSM receivers," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 5, pp. 835–838, Oct. 2003.

[8] P.-I. Mak, U. Seng-Pan, and R. P. Martins, "On the design of a programmable-gain amplifier with built-in compact DC-offset cancellers for very low-voltage WLAN systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 496–509, Mar. 2008.

[9] F. Carrara and G. Palmisano, "High-dynamic-range VGA with temperature compensation and linear-in-dB gain control," *IEEE J. Solid-State Circuits*, vol. 40, no. 10, pp. 2019–2024, Oct. 2005.

[10] H. D. Lee, K. A. Lee, and S. Hong, "A wideband CMOS variable gain amplifier with an exponential gain control," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 6, pp. 1363–1373, Jun. 2007.

[11] Q.-H. Duong, Q. Le, C.-W. Kim, and S.-G. Lee, "A 95-dB linear low-power variable gain amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 8, pp. 1648–1657, Aug. 2006.

[12] S. D'Amico, A. Spagnolo, A. Donno, V. Chironi, P. Wambacq, and A. Baschirotto, "A low-power analog baseband section for 60-GHz receivers in 90-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 8, pp. 1724–1735, Aug. 2014.

[13] K.-L. Fu and S.-I. Liu, "A 56 Gbps PAM-4 optical receiver front-end," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2017, pp. 77–80.

[14] K.-L. Fu and S.-I. Liu, "A 64-Gb/s PAM-4 optical receiver with amplitude/phase correction and threshold voltage/data level calibration," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 7, pp. 1726–1735, Jul. 2020, doi: 10.1109/TVLSI.2020.2991721.

[15] A. Balachandran, Y. Chen, and C. C. Boon, "A 0.013-mm^2 0.53-mW/Gb/s 32-Gb/s hybrid analog equalizer under 21-dB channel loss in 65-nm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 3, pp. 599–603, Mar. 2018.

[16] A. Balachandran, Y. Chen, P. Choi, and C. C. Boon, "0.058 mm^2 13 Gbit/s inductorless analogue equaliser with low-frequency equalisation compensating 15 dB channel loss," *Electron. Lett.*, vol. 54, no. 2, pp. 72–74, Jan. 2018.

[17] A. Balachandran, Y. Chen, and C. C. Boon, "A 32-Gb/s 3.53-mW/Gb/s adaptive receiver AFE employing a hybrid CTLE, edge-DFE and merged data-DFE/CDR in 65-nm CMOS," in *Proc. IEEE Asia–Pacific Conf. Circuits Syst. (APCCAS)*, Nov. 2019, pp. 221–224.

[18] Y. Wang, B. Afshar, L. Ye, V. C. Gaudet, and A. M. Niknejad, "Design of a low power, inductorless wideband variable-gain amplifier for high-speed receiver systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 4, pp. 696–707, Apr. 2012.

[19] L. Kong, H. Liu, X. Zhu, C. C. Boon, C. Li, Z. Liu, and K. S. Yeo, "Design of a wideband variable-gain amplifier with self-compensated transistor for accurate dB-linear characteristic in 65 nm CMOS technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 4187–4198, Dec. 2020.

[20] Y. Chen, P.-I. Mak, and Y. Zhou, "Mixed-integrator biquad for continuous-time filters," *IET Electron. Lett.*, vol. 46, no. 8, pp. 561–563, Apr. 2010.

[21] Y. Chen, P.-I. Mak, and Y. Zhou, "Source-follower-based bi-quad cell for continuous-time zero-pole type filters," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 3629–3632.

[22] Y. Chen, P.-I. Mak, S. D'Amico, L. Zhang, H. Qian, and Y. Wang, "A single-branch third-order pole–zero low-pass filter with 0.014-mm^2 die size and 0.8-kHz (1.25-nW) to 0.94-GHz (3.99-mW) bandwidth–power scalability," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 11, pp. 761–765, Nov. 2013.

[23] Y. Chenl, P.-I. Mak, L. Zhang, H. Qian, and Y. Wang, "0.013 mm^2, kHz-to-GHz-bandwidth, third-order all-pole lowpass filter with 0.52-to-1.11 pW/pole/Hz efficiency," *IET Electron. Lett.*, vol. 23, no. 5, pp. 978–982, May 2013.

[24] Y. Chen, P. Mak, L. Zhang, H. Qian, and Y. Wang, "0.0012 mm^2, 8 mW, single-to-differential converter with < 1.1% data cross error and < 3.4 ps RMS jitter up to 14 Gbit/s data rate," *Electron. Lett.*, vol. 49, no. 11, pp. 692–694, May 2013.

[25] Y. Chen, P.-I. Mak, L. Zhang, H. Qian, and Y. Wang, "A fifth-order 20-MHz transistorized-*LC*-ladder LPF with 58.2-dB SFDR, 68-μW/pole/MHz efficiency, and 0.13-mm^2 die size in 90-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 1, pp. 11–15, Jan. 2013.

[26] Y. Chen, P.-I. Mak, L. Zhang, and Y. Wang, "A 0.07 mm^2, 2 mW, 75 MHz-IF, 4th-order BPF using a source-follower-based resonator in 90 nm CMOS," *IET Electron. Lett.*, vol. 48, no. 10, pp. 552–554, May 2012.

[27] Y. Chen, P.-I. Mak, L. Zhang, and Y. Wang, "A 0.002-mm^2 6.4-mW 10-Gb/s full-rate direct DFE receiver with 59.6% horizontal eye opening under 23.3-dB channel loss at Nyquist frequency," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3107–3117, Dec. 2014.

[28] C. Liu, Y.-P. Yan, W.-L. Goh, Y.-Z. Xiong, L.-J. Zhang, and M. Madihian, "A 5-Gb/s automatic gain control amplifier with temperature compensation," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1323–1333, Jun. 2012.

[29] S. Ray and M. M. Hella, "A 10 Gb/s inductorless AGC amplifier with 40 dB linear variable gain control in 0.13 ?m CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 440–456, Feb. 2016.
[30] L. Kong, Y. Chen, C. C. Boon, P.-I. Mak, and R. P. Martins, "A wideband inductorless dB-linear automatic gain control amplifier using a single-branch negative exponential generator for wireline applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 10, pp. 3196–3206, Oct. 2018.
[31] L. Kong, Y. Chen, H. Yu, Q. Pan, C. C. Boon, P.-I. Mak, and R. P. Martins, "Wideband variable-gain amplifiers based on a pseudo-current-steering gain-tuning technique," in *Proc. IEEE Asia Pacific Conf. Circuits Syst. (APCCAS)*, Nov. 2019, pp. 153–156.
[32] I. Choi, H. Seo, and B. Kim, "Accurate dB-linear variable gain amplifier with gain error compensation," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 456–464, Feb. 2013.
[33] Y. Zheng, J. Yan, and Y. Ping Xu, "A CMOS VGA with DC offset cancellation for direct-conversion receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 1, pp. 103–113, Jan. 2009.
[34] H. Lee, K. Lee, and S. Hong, "Wideband VGAs using a CMOS transconductor in triode region," in *Proc. Eur. Microw. Conf.*, Sep. 2006, pp. 1449–1452.
[35] O. Watanabe, S. Otaka, M. Ashida, and T. Itakura, "A 380-MHz CMOS linear-in-dB signal-summing variable gain amplifier with gain compensation techniques for CDMA systems," in *IEEE Dig. Tech. Papers Symp. VLSI Circuits*, Jun. 2002, pp. 136–139.
[36] S. Otaka, G. Takemura, and H. Tanimoto, "A low-power low-noise accurate linear-in-dB variable-gain amplifier with 500-MHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1942–1948, Dec. 2000.
[37] K.-S. Nah and B.-H. Park, "A 50-MHz dB-linear programmable-gain amplifier with 98-dB dynamic range and 2-dB gain steps for 3 V power supply," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 2, pp. 218–223, Apr. 2003.
[38] C.-C. Kuo, Z.-M. Tsai, J.-H. Tsai, and H. Wang, "A 71–76 GHz CMOS variable gain amplifier using current steering technique," in *IEEE RFIC Symp. Dig.*, Jun. 2008, pp. 609–612.
[39] T. B. Kumar, K. Ma, and K. S. Yeo, "A 4 GHz 60 dB variable gain amplifier with tunable DC offset cancellation in 65 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 1, pp. 37–39, Jan. 2015.
[40] C.-H. Wu, C.-S. Liu, and S.-L. Liu, "A 2 GHz CMOS variable-gain amplifier with 50 dB linear-in-magnitude controlled gain range for 10 GBase-LX4 Ethernet," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2004, pp. 484–485.
[41] I.-H. Wang, W.-S. Chen, and S.-I. Liu, "10 GBase-LX CMOS automatic gain control amplifier design," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2005, pp. 505–508.
[42] H. Liu, C. C. Boon, X. He, X. Zhu, X. Yi, L. Kong, and M. C. Heimlich, "A wideband analog-controlled variable-gain amplifier with dB-linear characteristic for high-frequency applications," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 533–540, Feb. 2016.
[43] Y. Chen, P.-I. Mak, C. C. Boon, and R. P. Martins, "A 27-Gb/s time-interleaved duobinary transmitter achieving 1.44-mW/Gb/s FOM in 65-nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 9, pp. 839–841, Sep. 2017.
[44] Y. Chen, P.-I. Mak, C. C. Boon, and R. P. Martins, "A 36-Gb/s 1.3-mW/Gb/s duobinary-signal transmitter exploiting power-efficient cross-quadrature clocking multiplexers with maximized timing margin," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 9, pp. 3014–3026, Sep. 2018.
[45] Y. Chen, P.-I. Mak, H. Yu, C. C. Boon, and R. P. Martins, "An area-efficient and tunable bandwidth- extension technique for a wideband CMOS amplifier handling 50+ Gb/s signaling," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3107–3117, Dec. 2017.
[46] Y. Chen, P.-I. Mak, C. Chye Boon, and R. P. Martins, "A 0.024-mm^2 45.4-GHz-bandwidth unity-gain output driver with SDD22<-10dB up to 35 GHz," in *Proc. IEEE 63rd Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2020, pp. 687–690.
[47] Y. Chen, P.-I. Mak, and Y. Wang, "A highly-scalable analog equalizer using a tunable and current-reusable for 10-Gb/s I/O links," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 5, pp. 978–982, May 2015.
[48] X. Zhao, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.0018-mm^2 153%-locking-range CML-based divider-by-2 with tunable self-resonant frequency using auxiliary negative-gm cell," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 9, pp. 3014–3026, May 2019.
[49] Y. Chen, P.-I. Mak, Z. Yang, C. C. Boon, and R. P. Martins, "A 0.0071-mm^2 10.8pspp-jitter 4 to 10-Gb/s 5-tap current-mode transmitter using a hybrid delay line for sub-1-UI fractional de-emphasis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 10, pp. 3991–4004, Oct. 2019.

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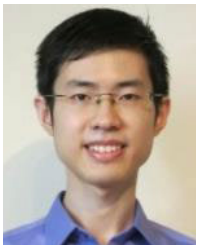

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