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Four-Level Three-Phase Inverter With Reduced Component Count for Low and Medium Voltage Applications

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ABSTRACT This paper proposes a novel three-phase topology with a reduced component count for low- and medium-voltage systems. It requires three bidirectional switches and twelve unidirectional switches for producing four-level voltages without using flying capacitors or clamping diodes, reducing the size, cost, and losses. Removing flying capacitors and clamping diodes allows it to simplify control algorithms and increase the reliability, efficiency, and lifetime. A modified low-frequency modulation (LFM) scheme is developed and implemented on the proposed topology to produce a staircase voltage with four steps. Further, a level-shifted pulse width modulation (LSPWM) is used to reduce the filter size and increase the output voltage controllability. In this study, a voltage balancing control algorithm is executed to balance the DC-link capacitor voltages. The performance of the proposed topology is numerically demonstrated and experimentally validated on an in-house test setup. Within the framework, the power loss distribution in switches and conversion efficiency of the proposed circuit are studied, and its main features are highlighted through a comparative study.

INDEX TERMS DC-AC converters, four-level inverters, low and medium voltage applications, multilevel inverters, three-phase inverters.

I. INTRODUCTION

Multilevel inverters (MLIs) have gained popularity in DC-AC converters, with a wide range of voltage levels, due to their attractive features of low harmonic contents, low dv/dt voltage stress, low filtering requirements, low switching frequency, and using low-rated semiconductor devices. Further, some MLIs have a modularity feature, enabling transformerless operation and increasing the reachable output voltage without increasing the semiconductor device rating [1]–[5]. These unique features make the MLIs remarkable among other DC-AC converters. The cascaded H-bridge MLI (CHB-MLI) [6], neutral-point clamped MLI (NPC-MLI) [7], [8], and flying capacitor MLI (FC-MLI) [9], [10] are considered as the baseline topologies of MLIs. On the other hand, producing a higher count of voltage levels dramatically increases the counts of clamping diodes, flying capacitors, and isolated DC sources in NPC-MLI, FC-MLI, and CHB-MLI, respectively, raising the inverter footprint and cost [11]. Further, in NPC-MLI and FC-MLI, enlarging level count renders extra challenges of balancing the capacitor voltages, increasing switching frequency, sensor count and control complexity, reducing the inverter reliability and lifetime [12]. To address those shortcomings of the conventional MLIs, many MLIs have been intensively introduced with a focus on a high-level count or specific applications [12]–[28]. However, only few publications [20]–[28] aim to develop four-level MLIs for low- and medium-voltage three-phase systems, which are briefly discussed hereafter and detailed in [20]–[28].

The authors in [20] introduced an eighteen-step inverter (EI) topology, generating four voltage levels by using twelve switches, twenty-four diodes, three DC-link capacitors, and one DC source. As compared to most four-level topologies, the EI topology requires fewer active switches and does not need any flying capacitor. However, it suffers from using a high count of clamping diodes and high-voltage rating of the semiconductor devices (e.g. when applying a DC-link

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voltage of $3E$, six switches block $3E$, six switches block $2E$, twelve diodes withstand for $2E$ and twelve diodes subject to E). To mitigate the drawbacks of EI topology, a four-level nested neutral-point-clamped (NNPC) was presented in [21], combining the FC-MLI and NPC-MLI. It consists of eighteen switches, six clamping diodes, six flying capacitors, two DC-link capacitors and one DC source. It reduces the clamping diodes count to only six instead of twenty-four diodes in the EI, but the numbers of the flying capacitors and switches are increased to six capacitors and eighteen switches, respectively. Although the NNPC has a lower count of diodes and DC-link capacitors than the EI circuit, it must use higher flying capacitor and switch counts, increasing the size, cost, and control requirements. However, its salient features include the low total standing voltage of the switches, and using switches of equal rating, attracting more investigations to mitigate its shortcomings [29], [30].

A hybrid π-type topology was reported in [22], eliminating clamping diodes in both EI and NNPC. However, the hybrid π-type requires an addition of twelve switches and three flying capacitors as compared to the EI circuit, or needs six additional switches while saving three flying capacitors as compared to the NNPC. Despite removing clamping diodes, the hybrid π-type topology still has a high count of switches (twenty-four) besides using three flying capacitors, increasing its cost and size. Alternatively, a four-level active neutral-point clamped (4L-ANPC) topology was reported in [23] to eliminate flying capacitors in the hybrid π-type inverter while using the same switch count. It consists of twenty-four switches, three DC-link capacitors, and single DC source. It is worth mentioning that the switch count can be reduced to eighteen instead of twenty-four by replacing twelve switches with only six switches at the double voltage rating.

The authors in [24]–[26] presented a nested T-type (NT-type) MLI, consisting of six switches and two flying capacitors per each inverter leg. The three inverter legs share the same DC-link, which is formed by a single DC source without using DC-link capacitors. The NT-type MLI can be used as a solution to deal with the high switch count of the hybrid π-type topology in [22] while keeping the diode-free feature of the hybrid π-type against EI and NNPC circuits. The switch count is reduced to eighteen instead of twenty-four while the DC-link capacitors are eliminated. These benefits came with the cost of using six flying capacitors instead of three in the hybrid π-type circuit, increasing the control complexity and decreasing the lifetime.

To solve the drawbacks of using flying capacitors in the NT-type inverter while preserving the reduced switch count and removing clamping diodes, the authors in [27], [28] presented the dual T-type (DT-type) and π-type MLIs. The DT-type topology in [27] uses eighteen switches, three DC-link capacitors and one DC source. The eighteen switches are configured in a way to build six T-type legs, being connected back-to-back through three bidirectional switches. Similarly, the π-type inverter in [28] uses the same counts of switches, DC sources, and DC-link capacitors. Both two circuits can eliminate flying capacitors and clamping diodes, being considered as their main merits. However, they still suffer from a high-voltage stress of the full DC-link voltage applied on six switches out of eighteen switches, restricting the reachable output voltage and increasing the switching losses.

To tackle the limitations of the aforementioned MLI topologies, namely high counts of flying capacitors, diodes, switches, and DC sources, this paper proposes a novel three-phase four-level topology with a reduced component count to mitigate those problems in low and medium voltage systems. The proposed topology does not need any clamping diode or flying capacitor and uses only eighteen switches for producing same 4-level voltages, resulting in a compact design, and increasing efficiency and lifetime. Section II introduces the proposed topology, including its circuit description and operation principles. The two switching schemes based on low-frequency and level-shifted pulse width modulations are presented in Section III. Section IV presents a voltage balance control for the DC-link capacitors. Section V provides simulation results and experimental validations. Afterwards, the efficiency of the proposed topology is analysed and highlighted in Section VI. The effectiveness of the proposed topology is proven through a comparative study between the proposed topology and other four-level MLIs in Section VII. Finally, the paper is concluded in Section VIII.

II. PROPOSED TOPOLOGY

Fig. 1 shows the proposed topology, consisting of twelve unidirectional switches (S_1-S_{12}) and three bidirectional switches (B_1-B_3). It does not use any power diode or flying capacitor, reducing control algorithms complexity, power loss and increasing the inverter lifetime. To simplify the gate-drive circuits, the common-emitter structure is adopted to configure the bidirectional switches. Further, the three-phase legs share the same DC-link, reducing the counts of DC sources and DC-link capacitors. Depending on the availability of the DC sources or applications, the DC-link of the proposed topology can be configured in two ways: either using three low-voltage DC sources or single medium-voltage DC source linked to three DC-link capacitors as shown in Figs. 1(a) and (b), respectively. Renewable energy systems based on PVs and fuel cells (FCs) have multiple DC sources, thus the first configuration is recommended to be used in those energy systems. Accordingly, DC-link capacitors and their associated control algorithms can be eliminated. However, power electronic conditioner circuits are needed to control/maximize the raw generated power from those renewable energy sources. On the other hand, the second configuration or single source configuration (SSC) in Fig. 1(b) is recommended for industrial applications, where a single medium-voltage bus is available. Both configurations are detailed in this paper.

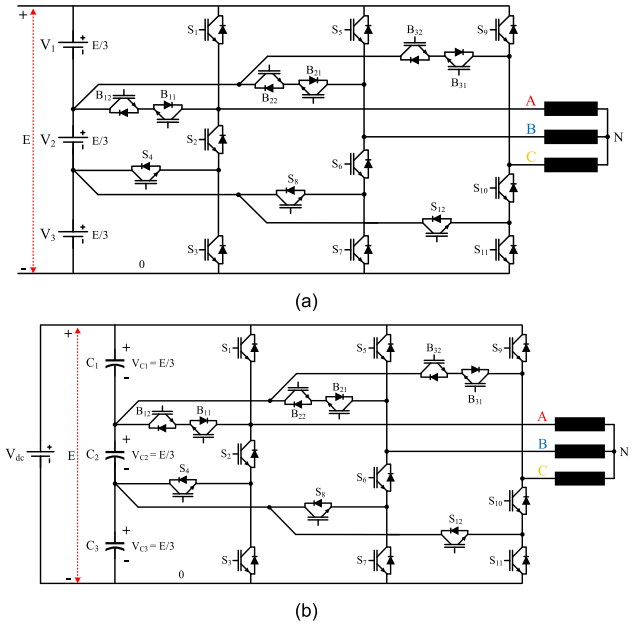

FIGURE 1. The proposed four-level topology. (a) Multiple sources configuration (MSC), recommended for energy systems, (b) Single source configuration (SSC), recommended for industrial applications.

The inverter switches are controlled to produce four unipolar voltage levels of 0, $E/3$, $2E/3$, and E in the pole voltages V_{A0}, V_{B0}, and V_{C0}. Seven-level bipolar voltages can be generated in the line voltages V_{AB}, V_{BC}, and V_{CA} by subtracting the adjacent pole voltages. For example, V_{AB} is synthesized by subtracting V_{A0} from V_{B0}, producing a seven-level voltage of $-E$, $-2E/3$, $-E/3$, 0, $E/3$, $2E/3$, and E. The operating modes of the proposed topology are illustrated in Fig. 2, showing the switching states for producing seven voltage levels in the line voltage V_{AB}. Each state is accompanied by its corresponding paths for the positive and negative currents. For example in Fig. 2(a), the state I shows that the switches S_1, S_6, and S_7 must be in ON-state to obtain the maximum positive voltage of E in the line voltage V_{AB} while switches (S_2-S_4), (S_5, S_8) and (B_1, B_2) are in OFF-state. The positive and negative currents are highlighted in blue and red dash lines, respectively. Similarly, switching states from II to VIII in Fig. 2 explain the different switching modes of the proposed topology for producing the remaining voltage levels. It should be noted that some switching states are removed when forming these switching paths, preventing the short-circuit faults in the inverter. For example, in leg A, the switching combinations of (S_1, S_2, S_4), (S_1, S_2, S_3), (S_3, S_4), (S_1, B_1), and (B_1, S_2, S_4) are marked as unused states in both switching algorithms.

III. MODULATION STRATEGIES

Two modulation strategies are utilized in this section to control the output voltage of the proposed topology. The low-frequency modulation (LFM) is adopted for reducing the switching loss, while the level-shifted pulse width modulation (LSPWM) is implemented for increasing the controllability of the output voltage. Both switching strategies follow the provided switching states in Table 1 to create the switching pulses for the proposed inverter. Table 1 shows the switching pattern of switches (S_1-S_4) and B_1 for producing four levels in the pole voltage V_{A0}.

Fig. 3 shows the LFM switching pattern accompanied by the pole voltage V_{A0}. In the LFM scheme, three sinusoidal reference signals (only SR_A is shown in Fig. 3) and two modulator signals (H^+ and H^-) are used for generating three controlling signals (M_1-M_3). For instance, M_1 and M_2 are produced by comparing the SR_A signal with H^+ and H^-, respectively, while comparing the SR_A signal with zero produces the M_3 controlling signal. Simple logical operators summarized in (1)-(5) are applied on the three controlling signals M_1-M_3 for producing five switching signals of switches S_1-S_4 and B_1 in leg A. Similarly, switching signals for the switches in legs B and C can be generated. Both sinusoidal and modulator signals can be varied in their magnitude from 0 to 1, providing two degrees of freedom for producing voltages at different RMS, level counts, and THDs. For example, selecting a magnitude value of 1 for the three sinusoidal signals and ± 0.35 for H modulators can produce seven-level line voltages with THD of 11. 81%. On the other hand, five-level line voltages with the THD of 34.88% are produced when H modulators are equal to ± 0.9.

$$S_1 = M_1 \tag{1}$$
$$S_2 = \overline{M_3} \tag{2}$$
$$S_3 = M_2 \tag{3}$$
$$S_4 = \overline{M_2} \times \overline{M_3} \tag{4}$$
$$B_1 = \overline{M_1} \times M_3 \tag{5}$$

Although the controllability of the applied LFM is better than the conventional LFM, it is still not as smooth as the other switching schemes based on sinusoidal pulse width modulation. Therefore, the LSPWM scheme is also utilized for producing the switching signals of the proposed topology. The LSPWM requires three carrier signals and three sinusoidal modulation signals to produce the switching pulses for the switches in the proposed inverter. The carrier signals have a fixed amplitude of V_{cr} and are shifted in level by V_{cr} while the three sinusoidal signals are shifted in phase by 120° and their magnitude can be varied from 0 to $1.5V_{cr}$. Fig. 4 shows the generation process of switching pulses for leg A switches, S_1-S_4 and B_1, in which, three carrier signals CR_1, CR_2 and CR_3 are compared with one sinusoidal reference signal SR_A, producing three controlling signals X_1, X_2 and X_3. Equations (6)-(10) describe the logical operation applied on X_1-X_3 signals to produce the required switching pulses. Also, these pre-described operators in (6)-(10) can be applied on X_4-X_9 signals to generate the switching pulses for switches in legs B and C. The X_4-X_9 are the controlling signals, resulting from the comparison process between three carrier signals and other two phase-shifted sinusoidal signals SR_B and SR_C. The last trace in Fig. 4 shows the pole voltage

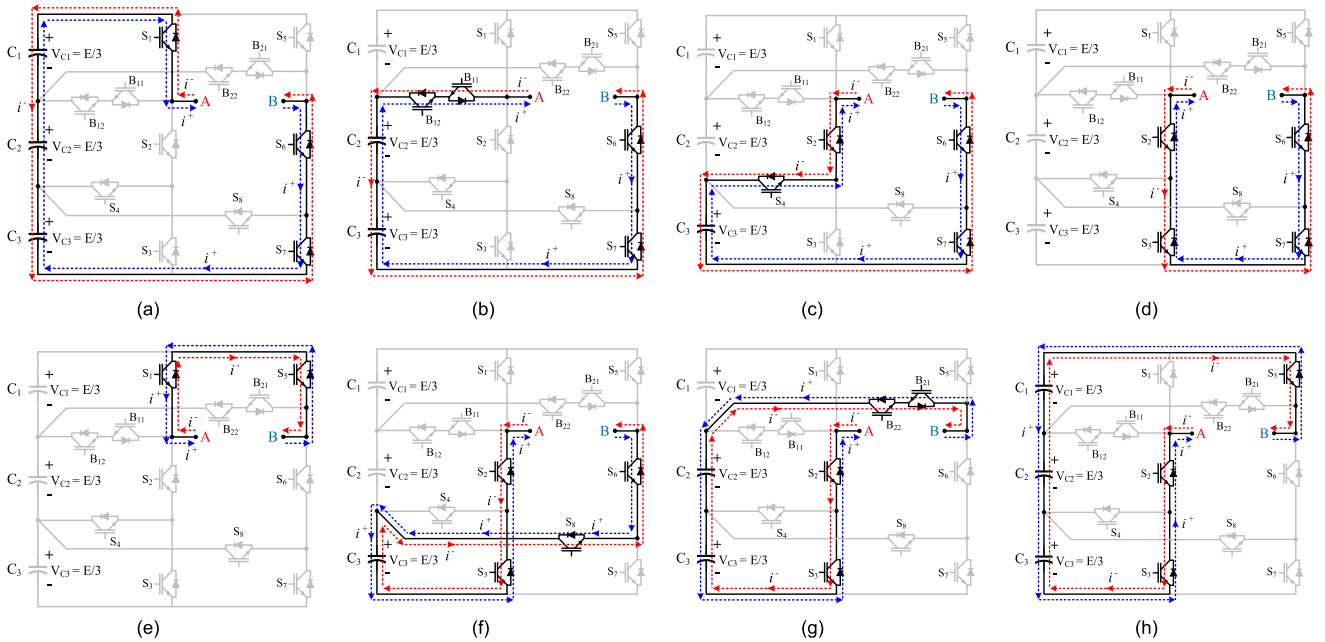

FIGURE 2. Switching states of the proposed topology: (a) State I: $V_{AB} = E$, (b) State II: $V_{AB} = 2E/3$, (c) State III: $V_{AB} = E/3$, (d) State IV: $V_{AB} = 0$, (e) State V: $V_{AB} = 0$, (f) State VI: $V_{AB} = -E/3$, (g) State VII: $V_{AB} = -2E/3$, (h) State VIII: $V_{AB} = -E$.

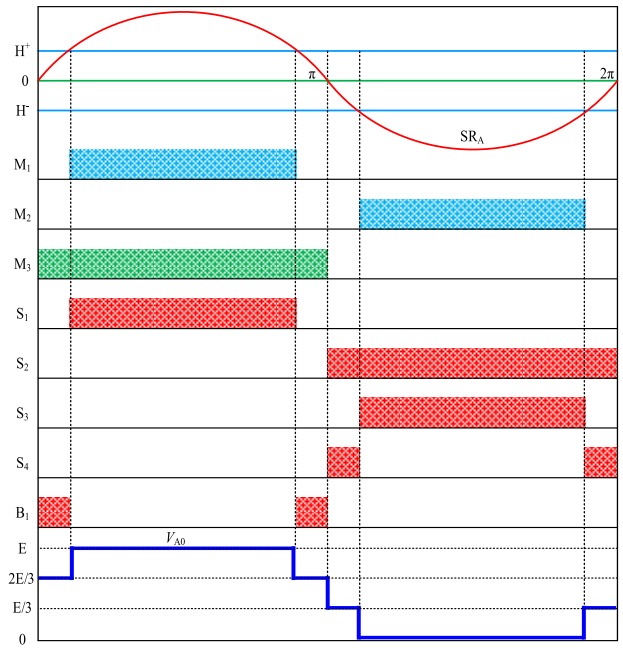

FIGURE 3. Switching pattern and pole voltage under the LFM scheme (leg A).

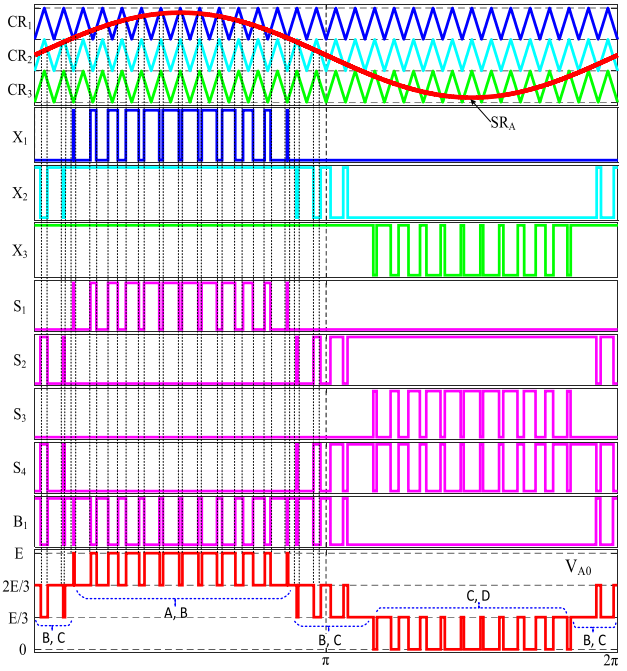

FIGURE 4. Switching pattern and pole voltage under the LSPWM scheme (leg A).

V_{A0} with four voltage levels of 0, $E/3$, $2E/3$, and E, being marked by the switching states in Table 1.

$$S_1 = X_1 \tag{6}$$
$$S_2 = \overline{X_2} \tag{7}$$
$$S_3 = \overline{X_3} \tag{8}$$
$$S_4 = \overline{X_2} \times X_3 \tag{9}$$
$$B_1 = \overline{X_1} \times X_2 \tag{10}$$

IV. VOLTAGE BALANCING CONTROL OF THE DC-LINK CAPACITORS

The capacitor voltage imbalance is common in four-level inverter topologies, where three capacitors are connected in series to divide the DC-link voltage into three equal parts as shown in Fig. 1 (b). A generalized mechanism for investigating the capacitor voltage imbalance in the four-level topologies was provided in [27]. The three capacitor currents

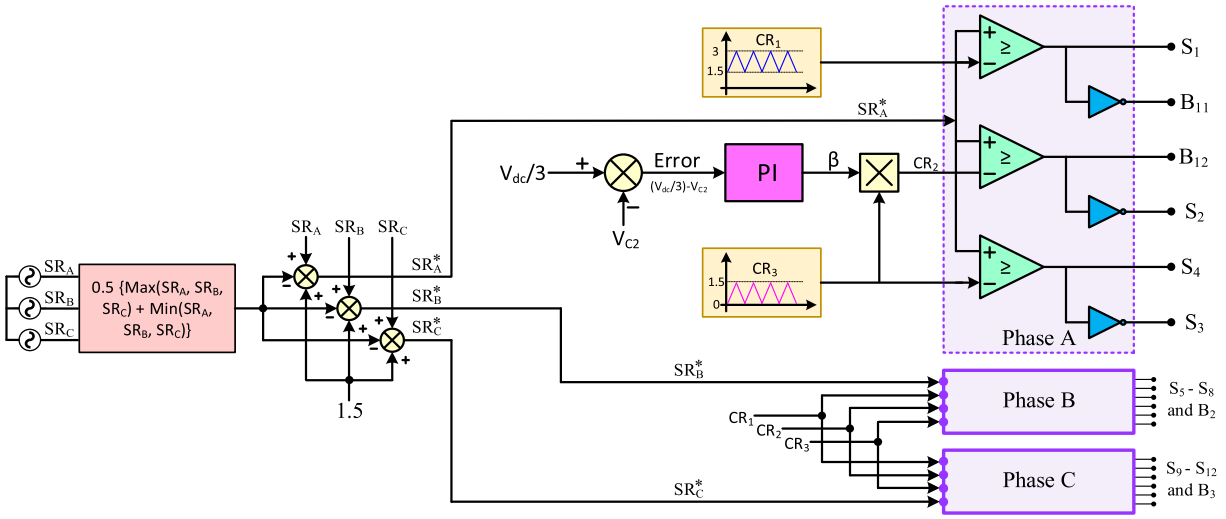

FIGURE 5. Overall voltage-balance control of the DC-link capacitors.

TABLE 1. Switching states for producing four voltage levels in pole voltage V_{A0}.

State	V_{A0}	S_1	S_2	S_3	S_4	B_1
A	E	ON	OFF	OFF	OFF	OFF
B	$2E/3$	OFF	OFF	OFF	OFF	ON
C	$E/3$	OFF	ON	OFF	ON	OFF
D	0	OFF	ON	ON	OFF	OFF

I_{C1}, I_{C2}, and I_{C3} in the single source configuration (SSC) of the proposed topology are not equal, causing a voltage imbalance. The current of the middle capacitor I_{C2} is larger than the currents of other capacitors I_{C1}, and I_{C3}, which are equal. Consequently, the C_1 and C_3 discharge less energy than C_2. Specifically, C_2 discharges faster to zero while the full DC-link voltage V_{dc} is equally shared between C_1 and C_3. The three capacitor currents can be equalized by either applying a voltage-balance control [23], [27], [31]–[34] or using voltage-balance circuitry [35], [36]. The variable-carrier scheme (VCS) can effectively control the voltage balance among the three capacitors [27], [34], thus it is chosen to balance the capacitor voltages in this work.

The capacitor voltages are not balanced because of the over-discharge of C_2. Therefore, by regulating the C_2 voltage V_{C2}, the other capacitors C_1 and C_3 can be balanced at V_{C1} and V_{C3}, where $V_{C1} = V_{C3} = (V_{dc}–V_{C2})/2$. Consequently, the three capacitor voltages V_{C1}, V_{C2}, and V_{C3}, could be equated when V_{C2} is regulated at $V_{dc}/3$. Fig. 5 describes the basic principle of the voltage balance control for the proposed topology, consisting of modulation signal generation block, carrier signal block, and the proportional-integral (PI) controller-based voltage loop. These three parts are used to generate modulation signals with a third-harmonic injection, variable and fixed carrier signals, and regulate the C_2 voltage at $V_{dc}/3$. The three carrier signals, CR_1, CR_2, and CR_3, have the same phase shift and frequency, but are different in the amplitude and level shift. CR_1 and CR_3 have a fixed

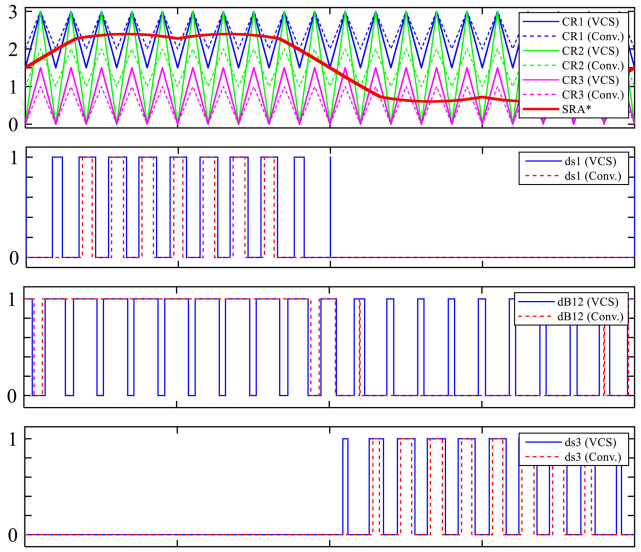

FIGURE 6. Switch duty cycles under the variable-carrier scheme (VCS) and the conventional LSPWM scheme.

amplitude of 1.5, and are shifted in level of 1.5, but the amplitude of CR_2 is variable. It can be any value from 0 to 1.5β, where β is the PI output. Increasing the amplitudes of CR_1 and CR_3 compared to the LSPWM in Fig. 4 raises the duty cycles of S_1 and S_3 (d_{S1} and d_{S3}) as shown in Fig. 6, discharging more energy from (C_1 and C_2) and (C_2 and C_3), respectively. On the other hand, the duty cycles of B_{12} and S_2 (d_{B12} and d_{S2}) are changing through the PI controller, aiming to regulate the middle capacitor voltage V_{C2} at $V_{dc}/3$. Accordingly, the capacitor voltages are effectively balanced.

V. SIMULATION AND EXPERIMENTAL RESULTS

Several simulations and experimental tests were carried out and presented in this section to verify the operating concept of the proposed four-level inverter topology. It is worthy to

TABLE 2. Used component and system specifications.

Description	Value/ Part number	Unit
DC-link voltage (V_{dc})	150	V
Load resistor (R)	40	Ω
Load inductor (L)	100	mH
Switching frequency (F_S)	2	kHz
Modulation frequency (F_o)	50	Hz
Modulation index (MI), LSPWM	0.9	–
Modulator signals (H), LFM	±0.35	–
Sampling time (T_S)	15	µs
DC voltage source	62024P-100-50	–
Switching device	SKM300GA12E4	–
Gate-driver board	SKHI 10/12 R	–

clarify that the included results in this section are for both configurations, SSC and MSC. The MSC is first numerically verified in MATLAB Simulink, and then experimentally validated through the in-house test setup. The SSC results are obtained by using the OPAL-RT real-time simulator OP5707 [37].

Table 2 shows the system specifications of the simulation and experimental validations. Fig. 7 shows the inverter prototype, consisting of three 62024P-100-50 DC voltage sources, eighteen SKM300GA12E4 IGBT modules act as power switches (S_1-S_{12} and B_1-B_3) accompanied by SKHI 10/12 R gate-driver boards, and dSPACE's MicroLabBox digital controller. Further, a low-power DC voltage source for control circuits, and some measurement devices, such as oscilloscope, voltage and current probes, are shown in Fig. 7.

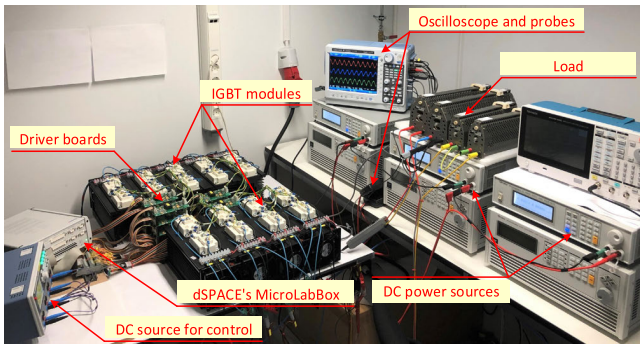

FIGURE 7. The in-house experimental setup.

The switching schemes shown in Figs. 3 and 4 are executed using the digital controller, producing the required switching pulses for the different switches in the proposed topology. These switching pulses control the corresponding switches to produce pole voltages with specific phase angles and level counts, as shown in Figs. 8 and 9. Figs. 8(a) and (b) depict the simulation and experimental results for the pole voltages V_{A0}, V_{B0}, and V_{C0} when using the LFM scheme. Each pole voltage has three voltage levels of 50 V and a phase shift of 120°

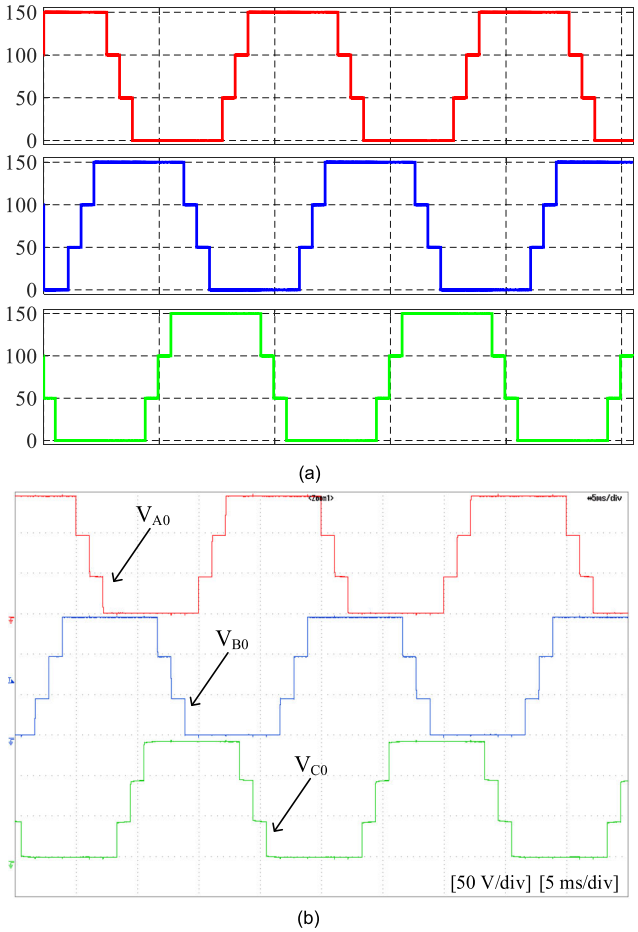

FIGURE 8. Pole voltages V_{A0}, V_{B0}, and V_{C0} using LFM (a) Simulation, (b) Experimental.

to the adjacent pole voltages. Further, the consistent pole voltage waveforms are shown in Figs. 9(a) and (b) when using LSPWM switching scheme. The three pole-voltage V_{A0}, V_{B0}, and V_{C0}, are the key waveforms for synthesising both line and phase voltages. For example, the line voltage V_{AB} is synthesized by subtracting two poles voltage V_{A0} and V_{B0} while the phase voltage V_{AN} is generated from the three poles voltages by $V_{AN} = (2V_{A0} - V_{B0} - V_{C0})/3$.

Figs. 10 and 11 show the line voltages V_{AB}, V_{BC}, and V_{CA} when using LFM and LSPWM schemes, respectively. As seen in Figs. 10 and 11, the proposed topology is capable for generating seven-level waveforms: three positive levels of 150, 100, and 50 V, zero-voltage level, and three negative levels of −50, −100, and −150 V. These line voltages are balanced and identical in both simulation and experimental tests. The proposed topology is further tested on resistive and inductive loads, as shown in Figs. 12-14. Fig. 12 illustrates the obtained simulation and experimental results of the line voltage V_{AB}, phase voltage V_{AN} and load current I_{AN} when delivering the power to the resistive loads of 40 Ω. Furthermore, the waveforms under the resistive-inductive loads of 50.86∠42.3° (R = 40 Ω and L = 100 mH) are

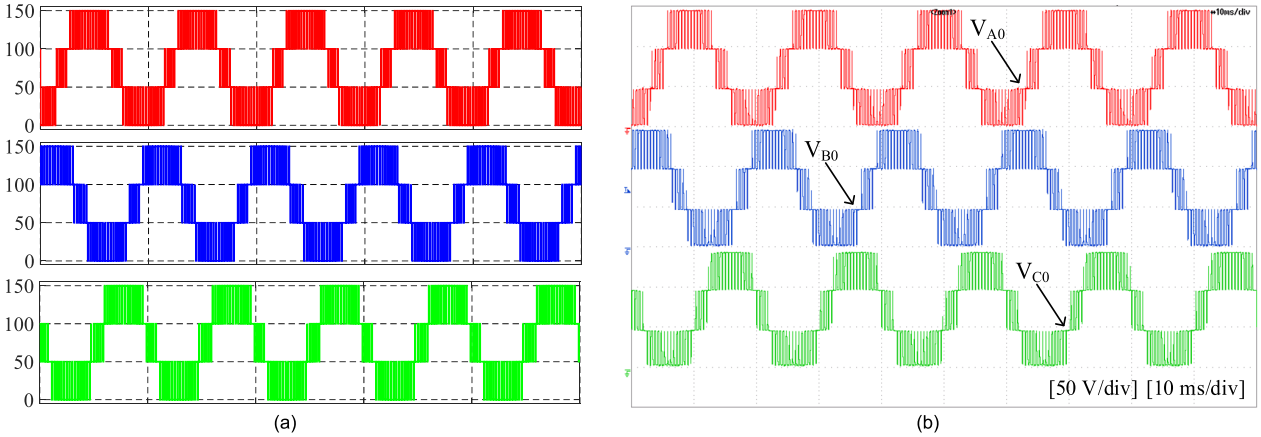

FIGURE 9. Pole voltages V_{A0}, V_{B0}, and V_{C0} using LSPWM (a) Simulation, (b) Experimental.

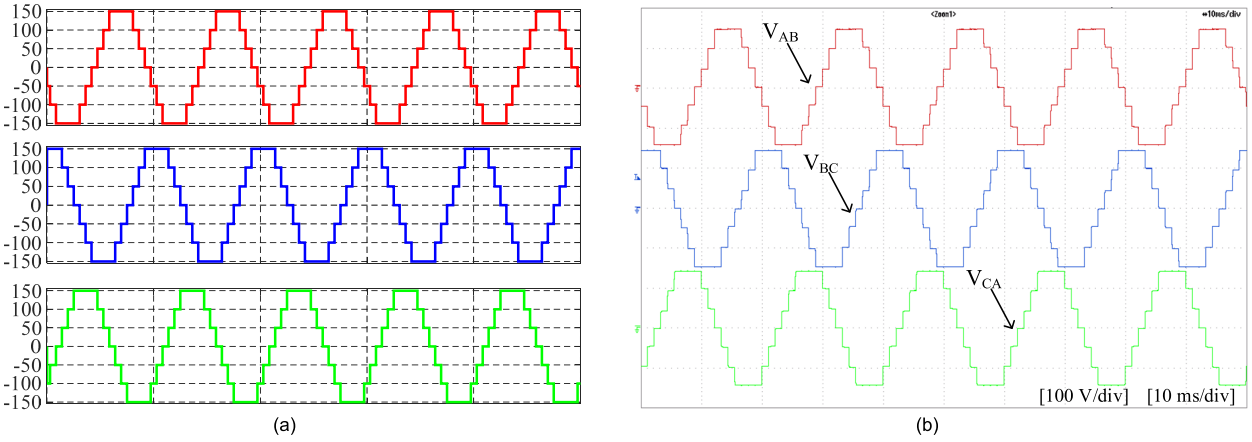

FIGURE 10. Line voltages V_{AB}, V_{BC}, and V_{CA} using LFM (a) Simulation, (b) Experimental.

described in Figs. 13 and 14 for LFM and LSPWM schemes, respectively. As seen from Figs. 12-14, the load current I_{AN} has a phase shift of 0° and 42.3° under the *R* and *R-L* loads, respectively.

The key results for the SSC of the proposed topology are presented hereafter. The DC-link voltage V_{dc} has the same value as in the experimental validation of the MSC, and is divided into three equal parts by using three capacitors of 1000 μF. The control scheme shown in Fig. 5 is used to generate the switching pulses for controlling the voltage of three DC-link capacitors at $V_{dc}/3$.

Fig. 15 shows the line voltage V_{AB}, phase voltage V_{AN} and the load current I_{AN} when a resistive-inductive load is connected to the proposed topology. Further, Fig. 16 illustrates the effectivity of the applied voltage-balance control of the DC-link capacitors C_1, C_2, and C_3. The three capacitor voltages V_{C1}, and V_{C2}, and V_{C3} are balanced for a wide range of modulation indices (MIs) as shown in Fig. 16(a), in which the MI changes from 0.9 to 0.3, keeping an acceptable tolerance of the capacitor voltages (V_{C1} = 51.21 V, V_{C2} = 50.20 V, and V_{C3} = 49.03 V). Further, Fig. 16(b) shows that the voltage-balance control can balance the capacitor voltages nearby 50 V (V_{C1} = 50.58 V, V_{C2} = 50.48 V, and V_{C3} = 49.37 V), while changing the load value by 100%, from (R = 30 Ω and L = 10 mH) to (R = 15 Ω and L = 5 mH). In Fig. 16, the voltage scale of V_{C1}, V_{C2}, and V_{C3} is 25 V/div, resulting in vague changes in the voltage waveforms when varying loads or modulation index.

VI. POWER LOSSES AND EFFICIENCY ANALYSIS

The loss analysis of the proposed topology is presented in this section to illustrate the effects of some salient parameters such as switching frequency (F_s) and load value on the conversion efficiency. The major part of the loss is dissipated in the conversion stage, i.e. in the semiconductor devices, in which the losses have three forms: conduction loss (P_{con}), switching loss (P_{sw}), and OFF-state loss (P_{off}) [38]–[40].

The ON-state resistance (R_{on}) and ON-state voltage (V_{on}) in the IGBTs devices cause conduction power loss when the load currents flow through them. The conduction loss depends on the load current and the characteristic of the device (i.e. R_{on}, V_{on}, etc.), while the switching frequency (F_s) does not have direct effects on the conduction loss, but the average value of the conduction loss depends on the

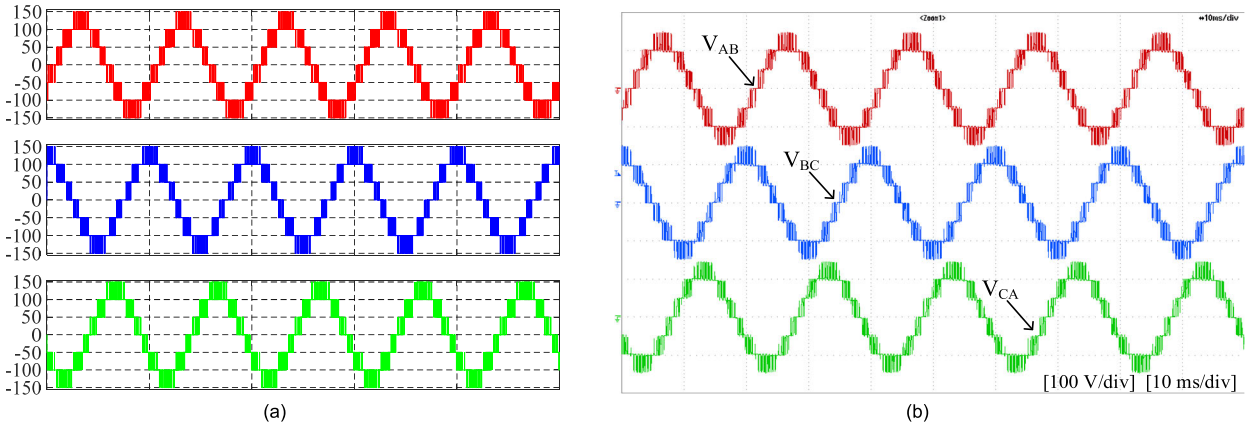

FIGURE 11. Line voltages V_{AB}, V_{BC}, and V_{CA} using LSPWM (a) Simulation, (b) Experimental.

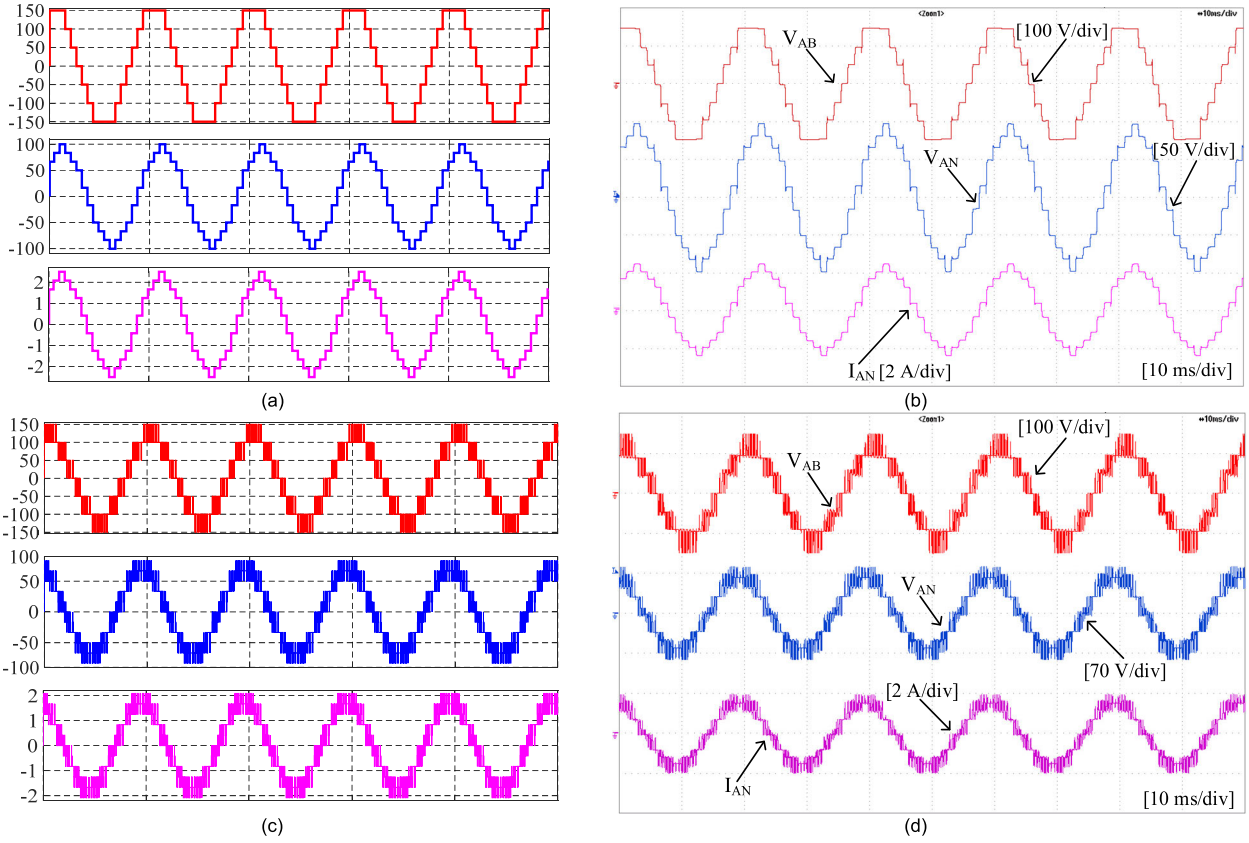

FIGURE 12. Obtained V_{AB}, V_{AN}, and I_{AN} when feeding R-load (a) Simulation (LFM), (b) Experimental (LFM), (c) Simulation (LSPWM), (d) Experimental (LSPWM).

duty cycle [40]. However, the switching loss depends on the switching frequency because of slow transitions between the switching states, i.e. transition from ON to OFF, and vice versa. Accordingly, a switching device still conducts a current when a voltage is applied to its terminal, causing a large instantaneous energy loss. For IGBTs, these energies are turn-on energy (E_{on}) and turn-off energy (E_{off}). For diodes, it is termed as reverse recovery energy (E_{rec}). The switching loss is proportional to the blocking voltage of the switching devices as well [38], [39], [41]. Non-zero currents are flowing through the switching devices during their OFF-state periods, causing OFF-state power loss. However, these non-zero currents can be neglectable and are considered as leakage currents [38]. Accordingly, the power loss during the OFF-state periods is ignored in this study. Detailed equations for calculating the power loss in the switching devices are highlighted in [38]–[41].

A medium-fast trench IGBT module with a part number of SKM300GA12E4 is used to build a model to study the power losses distribution and conversion efficiency of the proposed

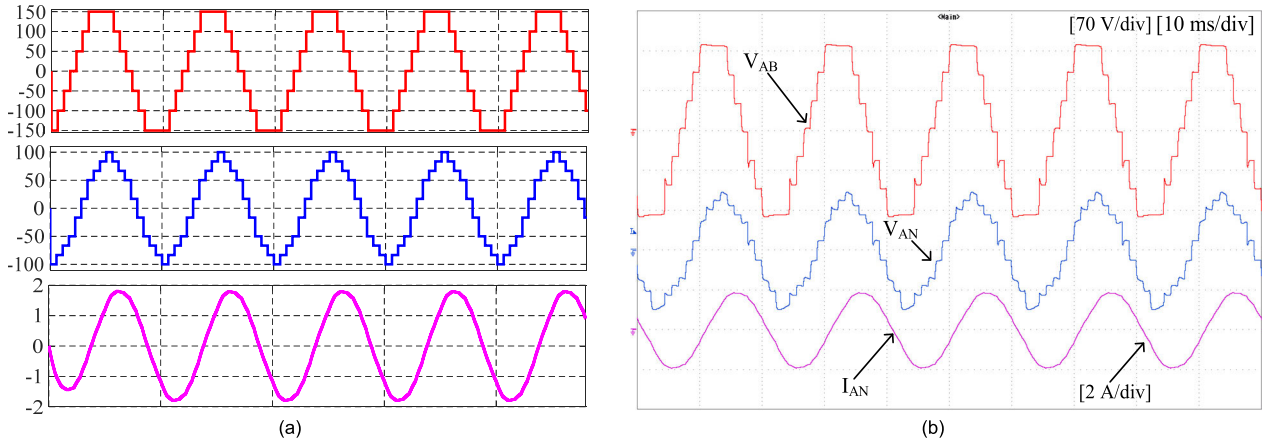

FIGURE 13. Obtained V_{AB}, V_{AN}, and I_{AN} for R-L load using LFM (a) Simulation, (b) Experimental.

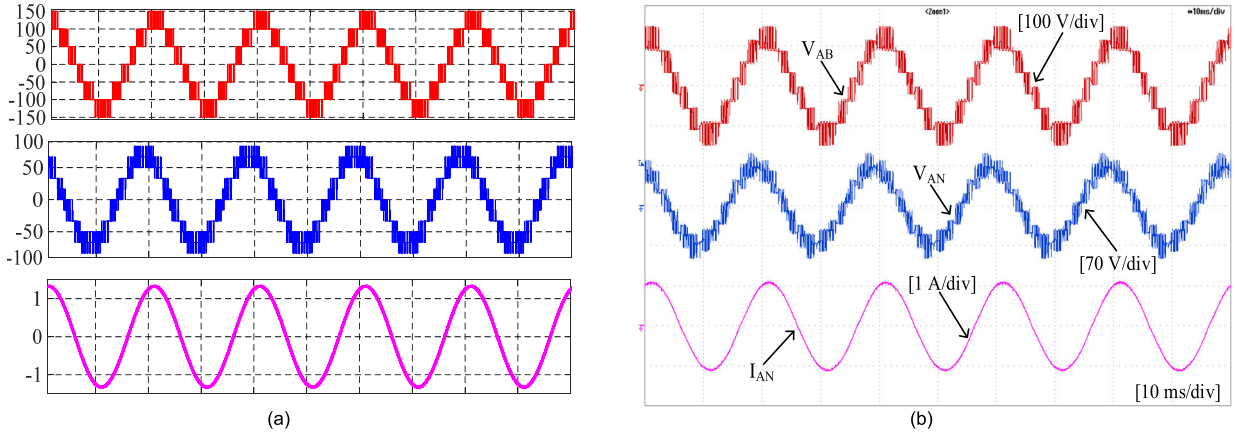

FIGURE 14. Obtained V_{AB}, V_{AN}, and I_{AN} for R-L load using LSPWM (a) Simulation, (b) Experimental.

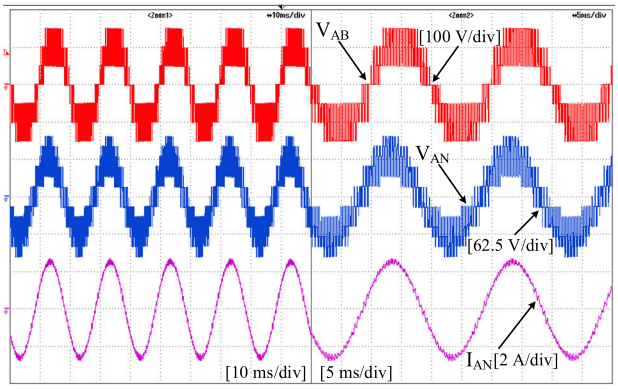

FIGURE 15. Obtained V_{AB}, V_{AN}, and I_{AN} for the SSC configuration when feeding R-L load (obtained by using OP5707).

topology. The used IGBT module has a soft-switching fourth-generation controlled axial lifetime (CAL) freewheeling diode. Table 3 lists the system specifications and the IGBT module main parameters with an assumption of a 150° C junction temperature. The detailed parameters of the used IGBT module can be found in [42].

The efficiency of the proposed topology is studied under varying the switching frequency and load. The switching frequency is changed from 2 kHz to 8 kHz in the step of 3 kHz, while the load is changed from 0.5 kW to 5 kW in steps of 0.5 kW. Fig. 17 illustrates the dependency of the efficiency on the switching frequency and load conditions. The efficiency increases when raising the load, and decreases when the switching frequency rises. For example, at the switching frequency of 5 kHz, the efficiency is increased from 96.65% to 99.15% when increasing the load from 0.5 kW to 5 kW. Contrarily, it is decreased from 99.19% to 98.41% when increasing switching frequency from 2 kHz to 8 kHz at 2.5 kW load, matching well power-loss calculations in literature [38]–[41]. It is emphasized that all switching device parameters and the other system specifications (i.e. input voltage, power factor, modulation index, etc.) are kept constant while studying the effects of the switching frequency or load on the total efficiency.

As mentioned above, both switching loss (P_{sw}) and conduction loss (P_{con}) are considered the dominant losses in semiconductor devices. Therefore, the power loss distribution of individual switches is studied and subdivided into switching and conduction losses. Fig. 18 shows the power

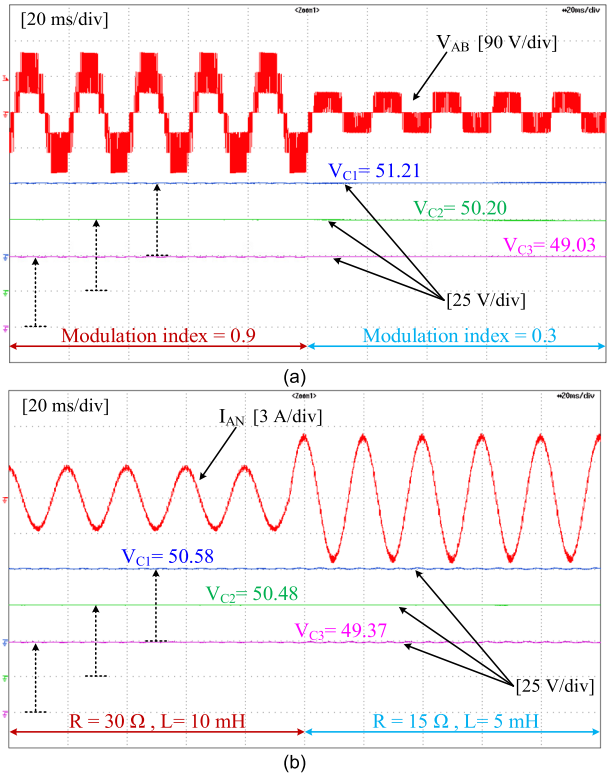

FIGURE 16. Dynamic results of the SSC configuration (obtained by using OP5707) (a) Changing the MI from 0.9 to 0.3: V_{AB}, V_{C1}, V_{C2}, and V_{C3}, (b) Changing the load value by 100%: I_{AN}, V_{C1}, V_{C2}, and V_{C3}.

loss distribution among different switches at the switching frequency of 5 kHz and the output power of 2.5 kW. Since the load and switching frequency are constant, the conduction and switching losses are directly proportional to the conduction period and switching voltage, respectively. For example, the switching losses in switches S_1, S_5, S_9 are higher than those of the remaining switches because they block higher voltages. The switches S_4, S_8, and S_{12} have the lowest conduction loss since their conduction periods are shorter than those of other switches.

The effect of modulation schemes, namely LFM and LSPWM, on the efficiency of the proposed topology is highlighted in this section. The efficiency is obtained when increasing the load power from 10% to 100%, by step of 10%. The system specifications in Table 3 are kept the same when changing the modulation schemes between LFM and LSPWM. It is noting that the switching frequencies of LFM and LSPWM are 50 Hz and 5 kHz, respectively. Using LFM at only 50 Hz results in the lower switching loss P_{sw} as compared to using LSPWM, increasing the conversion efficiency as shown in Fig. 19. As explained in Section III, LSPWM is required to control the output voltage better.

Among all addressed four-level topologies in this paper, the topology in [28] is considered as the closest circuit to the proposed topology from the structural point of view. Therefore, an efficiency comparison between the two

TABLE 3. System specifications for the loss analysis.

Parameter/Specification	Value	Unit
Collector-emitter breakdown voltage (V_{CE})	1200	V
Collector-emitter on-state voltage ($V_{CE,\,on}$)	2.45	V
IGBT on resistance ($R_{CE,\,on}$)	5.5	mΩ
Forward voltage (V_f)	2.42	V
Turn-on delay time ($T_{d,\,on}$)	220	ns
Rise time (T_r)	51	ns
Turn-off delay time ($T_{d,\,off}$)	515	ns
Fall time (T_f)	105	ns
Diode on-resistance (R_{on})	4.4	mΩ
Junction temperature (T_j)	150	°C
Switching frequency (F_s)	2, 5, 8	kHz
Modulation index (MI)	1	-
Power factor (PF)	0.897	-
Input DC sources	350	V
Rated output power (P_{out})	5	kW

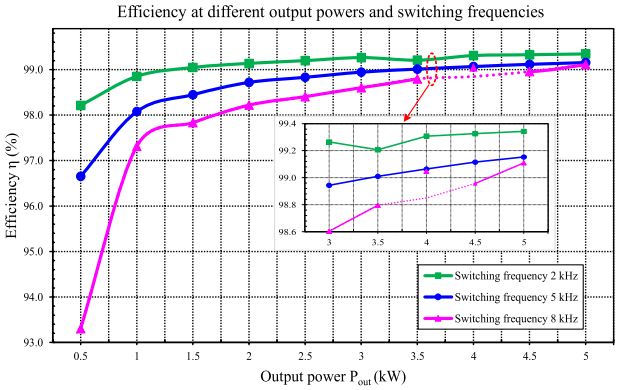

FIGURE 17. The dependency of the conversion efficiency on the switching frequency (F_S = 2, 5, and 8 kHz) and output power.

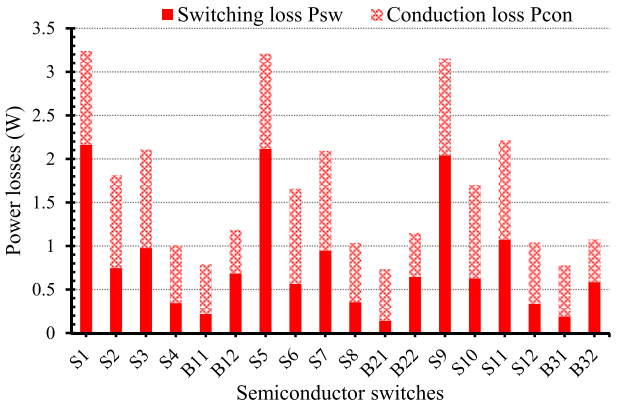

FIGURE 18. Power loss distribution in the used switches at 5 kHz switching frequency and 2.5 kW output power.

topologies is carried out while keeping system parameters identical as listed in Table 3. Fig. 20 shows the efficiency of the two circuits at different loads, proving that the efficiencies

TABLE 4. Comparison of the proposed topology with other four-level inverters [20]–[28] in terms of required components and voltage rating.

Topology	N_{DC}		N_{sw}			N_D		N_C		
								DC-link		Flying capacitors
	E/3	E	E/3	2E/3	E	E/3	2E/3	E/3	E/2	E/3
T_1 [20], EI-MLI	0	1	0	6	6	12	12	3	0	0
T_2, NPC-MLI	0	1	18	0	0	18	0	3	0	0
T_3 [21], NNPC MLI	0	1	18	0	0	6	0	0	2	6
T_4 [22], hybrid π-type MLI	0	1	18	6	0	0	0	3	0	3
T_5, FC-MLI	0	1	18	0	0	0	0	3	0	9
T_6 [23], 4L-ANPC MLI	0	1	24	0	0	0	0	3	0	0
T_7, half-HB MLI	9	0	18	0	0	0	0	0	0	0
T_8 [24-26], NT-type MLI	0	1	12	6	0	0	0	0	0	6
T_9 [27], DT-Type MLI	0	1	12	0	6	0	0	3	0	0
T_{10} [28], π-type MLI	0	1	6	6	6	0	0	3	0	0
The proposed MLI	0	1	9	6	3	0	0	3	0	0

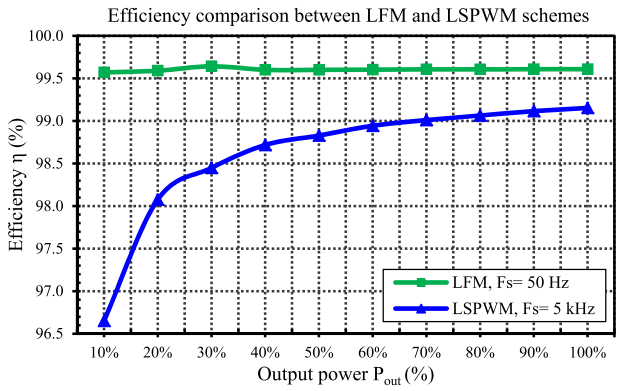

FIGURE 19. Efficiency comparison between the low-frequency modulation (LFM) and level-shifted pulse width modulation (LSPWM).

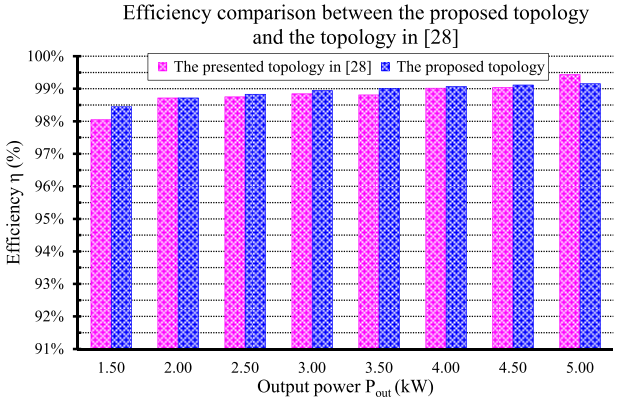

FIGURE 20. Efficiency comparison between the proposed topology and the topology in [28].

of the two topologies have a good agreement with small differences.

VII. COMPARATIVE STUDY

The SSC of the proposed topology is compared with both the recently published four-level inverters [20]–[28] and some conventional MLI topologies. A summary of this comparative study is provided in this section, clarifying the salient features of the proposed topology. The counterpart MLI topologies are labelled by T_1 to T_{10} and quantitively compared in term of the counts of DC sources N_{DC}, switches N_{SW}, diodes N_D, and capacitors N_C. Each element in any component group (e.g. the group of switches, diodes, etc.) is accompanied by its voltage rating while the current rating is assumed to be equal to the load current for all components. Some additional conditions are considered for obtaining a fair comparison among the different topologies: A) producing same output line voltages in terms of both the peak and step value, for example, V_{AB} must have seven levels of $E/3$ step and can reach a peak of $\pm E$ (i.e., E, $-2E/3$, $-E/3$, 0, $E/3$, $2E/3$, and E), B) all switching devices are counted based on unidirectional configuration, or any bidirectional switch is disassembled to its primary elements, for example, the proposed topology has three bidirectional switches: each is configured by connecting two unidirectional switches in a common emitter configuration, so they are counted as six unidirectional switches. Table 4 summarizes the component counts of three-phase configurations, where the compared topologies are listed in descending order based on the total component count.

According to Table 4, topologies T_1 and T_2 require the highest component count while T_9, T_{10}, and the proposed topology have the lowest one. In terms of switch count, the topology T_1 has the lowest number of switches (i.e. twelve switches), but it needs twenty-four diodes, being the highest count among the compared topologies. However, topologies

T_4-T_{10} and the proposed topology do not use clamping diodes. In terms of the capacitor count, T_5 requires nine flying capacitors, being the highest number among the addressed MLIs while the proposed topology and topologies T_1, T_2, T_6, T_7, T_9, and T_{10} do not need flying capacitors.

It is noted that the topologies T_9 and T_{10} have a similar component count like the proposed topology and they do not require any clamping diodes or flying capacitors, making them the possible counterparts of the proposed inverter. Nevertheless, as compared to T_9 and T_{10}, the proposed topology has advantageous features: A) it has a 50% reduction in the high-voltage switches. Only three switches must withstand to E while in the topologies T_9 and T_{10}, six switches must block E. B) the proposed topology has a total standing voltage (TSV) lower than the topology T_{10}. It has a TSV of $10E$ (TSV $=$ 9*E/3+6*2E/3+3*E) while T_{10} has TSV of $12E$ (TSV $=$ 6*E/3+6*2E/3+6*E), reducing the total cost of the required switches. C) Although both the proposed topology and the topology T_9 have a TSV of $10E$, the proposed topology has a lower switch count in the conduction paths than the topology T_9. For each inverter leg, it reduces one switch, giving the proposed topology an extra advantage in reducing the conduction loss.

VIII. CONCLUSION

This paper proposes a novel inverter topology with a reduced component count, being attractive in low- and medium-voltage applications. The proposed circuit generates four voltage levels without requiring flying capacitors or clamping diodes, reducing the size, cost, control complexity of the inverter and enhancing its reliability and lifetime. Several simulation and experimental tests were presented to validate the proposed topology performance at resistive and inductive loads. The proposed inverter was compared with the recently developed four-level topologies to highlight its merits. Moreover, its conversion efficiency was analysed when varying the switching frequency, modulation schemes, and loads.

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