IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received January 26, 2021, accepted February 15, 2021, date of publication February 24, 2021, date of current version March 10, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3061934

Ultra-High Step-Up Interleaved Converter With Low Voltage Stress

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This work was supported in part by the Railroad Technology Research Program through the Ministry of Land, Infrastructure and Transport of Korean Government, under Grant 21RTRP-B146008-04, and in part by the Korea Agency for Infrastructure Technology Advancement (KAIA) grant funded by the Ministry of Land, Infrastructure and Transport under Grant 21CTAP-C157056-02.

ABSTRACT In this paper, a new type of interleaved high step-up converter including a coupled inductor is proposed. The proposed converter has an interleaved configuration on the input side to reduce the ripple of the input current and increase the power level. Moreover, a stacked structure on the output side provides a high input/output (I/O) voltage gain. In addition, the proposed converter can avoid an extreme duty cycle, causing larger conduction losses, by combining a coupled inductor and a lossless clamp circuit with an interleaved method. These increase the efficiency by making the semiconductor device a low voltage stress and allowing the use of components with low voltage ratings. Also, the energy stored in the leakage inductor in the coupled inductor can be recycled to the output side, the MOSFETs can be partially ZCS turned ON, and the diode reverse recovery problem can be alleviated. Finally, a laboratory prototype circuit with an input voltage of 24V, an output voltage of 400V and an output of 500W was implemented to demonstrate the performance of the proposed converter.

INDEX TERMS DC/DC converter, high step-up converter, coupled inductor, switched capacitor.

NOMENCLATURE

L_1 and L_2	coupled inductors
L_{m1}, L_{m2}, and L_{mx}	magnetizing inductors
L_{k1}, L_{k2}, and L_{kx}	leakage inductors
i_{Lk1}, i_{Lk2}, and i_{Lkx}	leakage inductors current
N_{p1}, N_{p2}, N_{s1}, and N_{s2}	winding turns in the primary and secondary sides
N	turns ratio
D	duty cycle
M	voltage gain
S_1, S_2, and S_x	switches
i_{S1}, i_{S2}, and i_{Sx}	switches current
D_a, D_b, D_c, D_d, D_1, D_2, and D_x	diodes
i_{Da}, i_{Db}, i_{Dc}, i_{Dd}, i_{D1}, i_{D2}, and i_{Dx}	diodes current
C_a, C_b, C_1, C_2, C_3, and C_4	capacitors
V_{in} and V_o	input and output voltages
I_{in} and I_o	input and output currents
R_o	load resistance
T_s	switching period
f_s	switching frequency
η	efficiency
CCM	continuous conduction mode
ZCS	zero current switching
ZVS	zero voltage switching
PV	photovoltaic

The associate editor coordinating the review of this manuscript and approving it for publication was Ali Raza.

I. INTRODUCTION

High step-up converters are required in many industries based on renewable energy [1]–[3]. In the case of hybrid vehicles, the fuel cell stack has various output voltages (20V-40V), and a high DC bus voltage (380V∼400V) is required to drive the DC/AC inverter at the output stage of the DC/DC converter. Therefore, in order to increase the low voltage of the fuel cell stack to the high voltage of the DC bus, a high

step-up converter is essential [4]–[7]. In the case of PV power generation, the output voltage of the PV panel is lower than 50V. This low voltage must be passed through the front-end stage to obtain a bus voltage of about 400V (approximately ten times the voltage gain) [8]–[10].

The isolated DC/DC topology can provide high voltage gain by increasing the turns ratio of high frequency transformer. The phase-shift full bridge converters are one of the most popular converters capable of achieving zero voltage switching over a wide load range using the high leakage inductance of the transformer. However, there are significant drawbacks such as high circulating current, the voltage stress of the output diode is much higher than the output voltage, and the efficiency decreases in applications requiring high output voltage [11].

The non-isolated boost converters provide a theoretically high voltage gain. However, it is limited by parasitic elements such as inductors, switches, diodes, and capacitors. In addition, the extreme high duty cycle causes a serious reverse recovery problem and a decrease in efficiency due to the large ripple current of the output diode [12]. Therefore, a non-isolated converter having a reasonable duty cycle by achieving high efficiency, high voltage gain, and low voltage stress is essential in a renewable energy power conversion device.

The stacked method is similar to the operation principle of a flyback converter in [13], and a high voltage gain can be obtained by stacking the secondary winding of the coupled inductor on the output side in series. However, the leakage inductor energy of the coupled inductor can cause higher voltage stress on the switch. Also, it increases conduction losses by allowing large input currents and current ripple to flow through a single switch. Therefore, it affects the life of the power conversion device, the system efficiency is low, and it is not suitable for high power level. As a method to solve these problems, an interleaved method can be used to reduce input current ripple. In addition, in order to recycle the leakage inductor energy of the coupled inductor and reduce the voltage stress of the switch, a voltage multiplier cell combined with a clamp circuit is used [14]–[18]. The clamp circuits are divided into active-clamp and passive-clamp methods, which can be implemented in various topologies by combining with a coupled inductor boost converter. Another main advantage of the clamp circuit is the zero voltage/current switching (ZVS/ZCS) of the switches, which can reduce the circulating current and conduction losses of the switches through an active clamp method [19], [20]. In addition, high step-up interleaved converters can be made through an integrated single coupled inductor [9], [21], [22]. However, there are disadvantages of increasing the cost and size of the main switch and the auxiliary switch together with the isolated driver circuit [13].

Recently, the switched capacitors combined with coupled inductors have become attractive solutions for DC/DC converters with high voltage gain [2], [23]–[25]. With the switched capacitor cells, it is possible to obtain compact, lightweight converters because of high voltage gain high efficiency, and reduced electromagnetic interference problems. In addition, these cells can be easily applied to conventional boost converters to increase voltage gain and efficiency. Another advantage of this structure is the low blocking voltage stress in all semiconductors [26].

In this paper, an ultra-high step-up converter including a switched capacitor cell and a stacked coupled inductor is proposed. The proposed converter can increase the voltage gain by using the stack type method and the turns ratio of the coupled inductor on the output side. The switched capacitors connected to the coupled inductors can recycle leakage inductor energy to the output side with passive lossless clamping performance. Moreover, the switches can be partially ZCS turned ON under soft switching conditions, and the reverse recovery problem of diodes is alleviated. In addition, the switched capacitor cell connected in parallel with the output side stores energy in the capacitor during the period of alternating ON/OFF of the switches, which has the advantage of improving the low voltage stress, efficiency and power density of semiconductor devices. The composition of this paper will be discussed in section II and section III of the operating mode and steady state analysis. The loss analysis will be provided in section IV and the results of the experimental prototype will be provided in section V. Finally, Section VI presents the main features of the proposed transducer as a conclusion.

II. OPERATING PRINCIPLES OF THE PROPOSED CONVERTER

Fig. 1(a) shows the main circuit structure of the proposed ultra-high step-up converter. The primary windings N_{p1} and N_{p2} of the L_1 and L_2 are connected in parallel with the input side, and the secondary windings N_{s1} and N_{s2} of the are connected in series with the output side in the reverse direction. Fig. 1(b) depicts the equivalent circuit; magnetizing inductor ($L_{m1} = L_{m2} = L_{mx}$), leakage inductor ($L_{k1} = L_{k2} = L_{kx}$), switch ($S_x = S_1 = S_2$), diode ($D_a = D_b = D_c = D_d = D_1 = D_2 = D_x$), capacitor ($C_a = C_b = C_1 = C_2 = C_3 = C_4$), input and output voltages (V_{in}, V_o). The resulting currents are denoted by i_{Lm1}, i_{Lm2}, i_{Lk1}, i_{Lk2}, i_{S1}, i_{S2}, i_{Da}, i_{Db}, i_{Dc}, i_{Dd}, i_{D1}, and i_{D2}. The proposed converter employs the interleaved method so that the switches have a phase difference of 180 degrees and the magnetizing inductor is operated by the CCM. In addition, the D is based on 0.5 or more, and the leakage inductor currents ($i_{Lk1} = i_{Lk2} = i_{Lkx}$) are divided between above and below *0* (zero). Therefore, the operation principle of the proposed converter is explained through two operating analysis. To simplify the analysis, the resistance and parasitic capacitance components of all devices are ignored.

A. ANALYSIS OF OPERATION AT 0 < i_{Lkx}

A total of six main operation analyzes were performed based on the section in which leakage inductor currents are greater than *0* (zero) by D of the proposed converter.

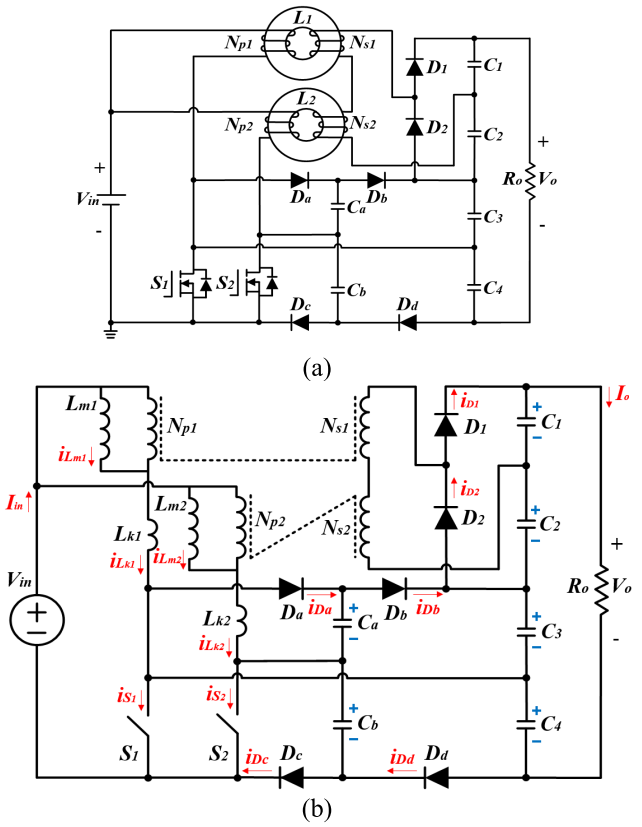

FIGURE 1. Circuit of the proposed converter. (a) Main circuit structure. (b) Equivalent circuit.

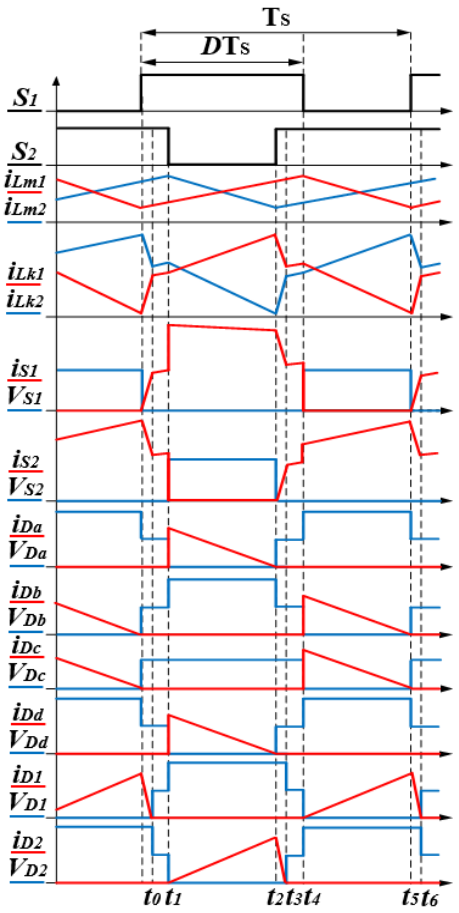

FIGURE 2. The theoretical key waveforms of proposed converter ($0 < i_{Lkx}$).

Fig. 2 illustrates the theoretical key waveforms and Fig. 3 depicts the operating modes.

1) *Mode I* $[t_0 - t_1]$, *Mode IV* $[t_3 - t_4]$: At $t = t_0$, this mode starts and it is shown in Fig. 3 (a). S_1 and S_2 are ON state and D_1, D_2, D_a, D_b, D_c, and D_d are all reverse biased. L_{m1}, L_{m2}, L_{k1}, and L_{k2} energy of L_1 and L_2 increase with slope of V_{in}. Also, the voltage of each diode is the same as the voltage clamped to each capacitor, which is given as

$$V_{D1} = V_{C1}, V_{D2} = V_{C2} \tag{1}$$

$$V_{Da} + V_{Dd} = V_{Db} + V_{Dc} = V_{Ca} + V_{Cb} = V_{C3} = V_{C4} \tag{2}$$

$$V_o = V_{C1} + V_{C2} + V_{C3} + V_{C4}. \tag{3}$$

2) *Mode II* $[t_1 - t_2]$: At $t = t_1$, S_2 is turned OFF. D_a, D_d, and D_2 are turned ON and the operation of this mode is as shown in Fig. 3 (b). The energy stored in L_{m2} of L_2 charges C_a through D_a and C_4 through D_d. In this mode, D_2 is ZCS turned ON through a linear increase of i_{Lk1}, and the main current of this mode is expressed as

$$\begin{aligned} i_{Lk1}(t) &= i_{Lm1}(t) + Ni_{D2}(t) \\ &= i_{Lm1}(t_1) + \frac{N(V_{Ca} + V_{C4} - V_{Cb}) - 2V_{C2}}{N(L_{k1} + L_{k2})}(t - t_1) \end{aligned} \tag{4}$$

$$i_{Lk2}(t) = i_{Lm2}(t) - i_{Da}(t) - i_{Dd}(t) \tag{5}$$

$$i_{S1}(t) = i_{Lm1}(t) + i_{Da}(t) + i_{Dd}(t) + Ni_{D2}(t). \tag{6}$$

3) *Mode III* $[t_2 - t_3]$: The mode starts at t_2, which is shown in Fig. 3(c). In the previous (*Mode II*), D_a and D_d are ZCS turned OFF due to a linear decrease in i_{Lk2}. In this mode, S_2 is partially ZCS turned ON through a linear increase of i_{Lk2} on the primary side of L_2. Also, the secondary side of L_1 leads to a linear decrease of i_{Lk1}, so that D_2 is ZCS turned OFF. The current in this mode is as follows

$$i_{D2}(t) = I_{D2}(t_2) - \frac{V_{C2}}{N^2(L_{k1} + L_{k2})}(t - t_2) \tag{7}$$

$$i_{Lk1}(t) = i_{S1}(t) = i_{Lk1}(t) - Ni_{D2}(t). \tag{8}$$

4) *Mode V* $[t_4 - t_5]$: The mode starts at t_4 and S_1 turns OFF. D_b, D_c, and D_1 are turned ON and the operation of this mode is as shown in Fig. 3(d). The energy stored in L_{m1} of L_1 charges C_b through D_c and C_3 through D_b. In this mode, D_1 is ZCS turned ON through a linear increase in i_{Lk2}. The resulting current is as follows

$$\begin{aligned} i_{Lk2}(t) &= I_{Lm2}(t) + Ni_{D1}(t) \\ &= I_{Lm2}(t_3) + \frac{N(V_{Ca} + V_{C3} - V_{Cb}) - 2V_{C1}}{N(L_{k1} + L_{k2})}(t - t_4) \end{aligned} \tag{9}$$

$$i_{Lk1}(t) = i_{Lm1}(t) - i_{Db}(t) - i_{Dc}(t) \tag{10}$$

$$i_{S2}(t) = i_{Lm1}(t) + i_{Db}(t) + Ni_{D1}(t). \tag{11}$$

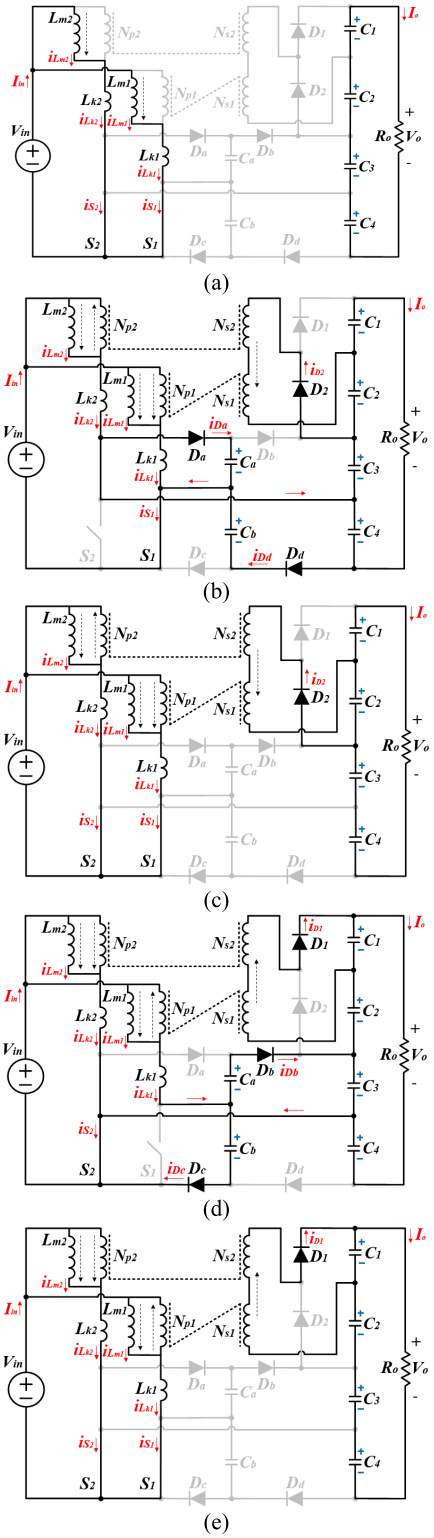

FIGURE 3. Operating modes of proposed converter ($0 < i_{Lkx}$). (a) *Mode I* $[t_0 - t_1]$, *Mode IV* $[t_3 - t_4]$. (b) *Mode II* $[t_1 - t_2]$. (c) *Mode III* $[t_2 - t_3]$. (d) *Mode V* $[t_4 - t_5]$. (e) *Mode VI* $[t_5 - t_6]$.

5) *Mode VI* $[t_5 - t_6]$: The mode starts at t_5, which is shown in Fig. 3(e). In the previous (*Mode V*), D_b and D_c are ZCS turned OFF due to a linear decrease in i_{Lk1}. In this mode, S_1 is partially ZCS turned ON through a linear increase of i_{Lk1}

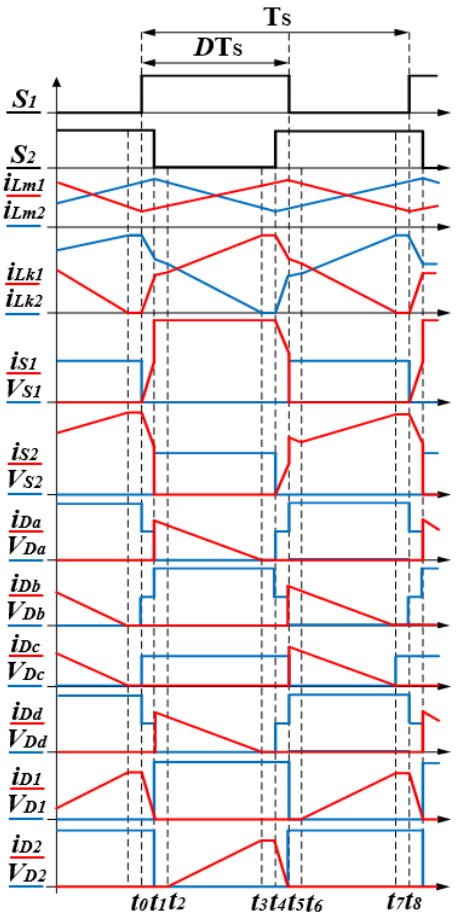

FIGURE 4. The theoretical key waveforms of proposed converte r ($i_{Lkx} \leq 0$).

on the primary side of L_1. Also, the secondary side of L_2 leads to a linear decrease of i_{Lk2}, so that D_1 is ZCS turned OFF.

B. ANALYSIS OF OPERATION AT $i_{Lkx} \leq 0$

In this section, there are a total of eight main theoretical analyzes according to D. Sections similar to the $0 < i_{Lkx}$ section (*Mode I* $[t_0 - t_1]$ = *Mode VI*; *Mode III* $[t_2 - t_3]$ = *Mode II*; *Mode V* $[t_4 - t_5]$ = *Mode III*; *Mode VII* $[t_6 - t_7]$ = *Mode V*) are excluded. Fig. 4 shows the theoretical main waveforms and Fig. 5 depicts the operating modes.

1) *Mode II* $[t_1 - t_2]$: The mode starts at $t = t_1$, which is shown in Fig. 5(a). S_1 is ON, S_2 is OFF, and the primary side L_{m1} of L_1 increases linearly by the input voltage. The L_{m2} energy of L_2 is transferred by gradually forming two paths; $L_{k2} \rightarrow D_a \rightarrow C_a$ and $L_{k1} \rightarrow C_4 \rightarrow D_d \rightarrow C_b$. The resulting current is as follows

$$i_{Lk1}(t) = i_{Lm1}(t), i_{Lk2}(t) = i_{Lm2}(t) \tag{12}$$

$$i_{S1}(t) = i_{Lm1}(t) + i_{Da}(t) + i_{Dd}(t). \tag{13}$$

2) *Mode IV* $[t_3 - t_4]$: This mode starts at $t = t_3$, as shown in Fig. 5(b). The mode starts after D_a and D_d are ZCS turned OFF through a linear decrease in i_{Lk2}. D_2 remains ON and the L_{m2} energy still charges C_2 through D_2 on the secondary

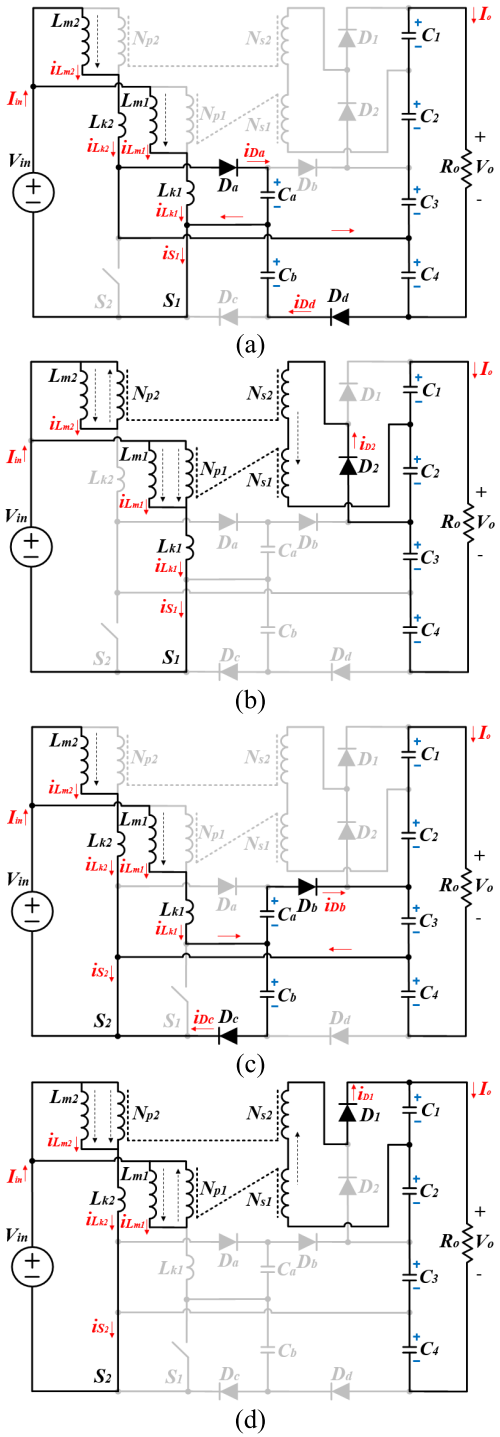

FIGURE 5. Operating modes of proposed converter ($i_{Lkx} \le 0$). (a) *Mode II* $[t_1 - t_2]$. (b) *Mode IV* $[t_3 - t_4]$. (c) *Mode VI* $[t_5 - t_6]$. (d) *Mode VIII* $[t_7 - t_8]$.

side of L_2, the main current of this mode is expressed as

$$i_{Lk1}(t) = i_{S1}(t) = i_{Lm1}(t) + i_{Lm2}(t) \tag{14}$$

$$i_{Lk2} = i_{Da}(t) = i_{Dd}(t) = 0. \tag{15}$$

3) *Mode VI* $[t_5 - t_6]$: This mode starts when S_2 remains ON and S_1 is OFF when $t = t_5$. The L_{m1} energy of L_1 is transferred by gradually forming two paths; $L_{k1} \rightarrow C_a \rightarrow D_c$ and $L_{k1} \rightarrow C_a \rightarrow D_b \rightarrow C_3$. In this mode, the operating mode is shown in Fig. 5(c).

4) *Mode VIII* $[t_7 - t_8]$: The mode ($t = t_7$) is started after D_b and D_c are ZCS turned OFF through a linear decrease in i_{Lk1}. S_2 remains ON and the L_{m1} energy still charges capacitor C_1 through D_1 connected to the secondary side of L_1. The operating mode is shown in Fig. 5(d).

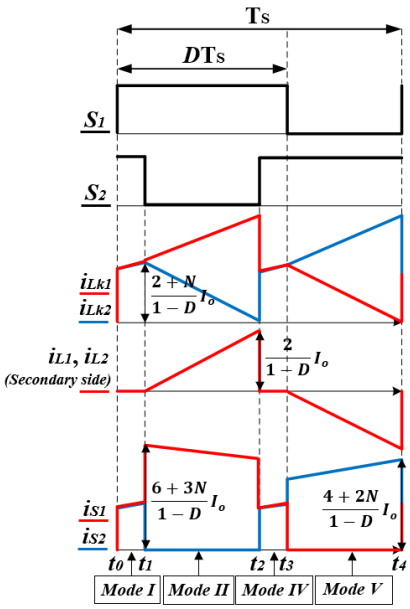

FIGURE 6. Simplified circuit waveforms.

III. STEADY-STATE PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTER

In this section, the transient characteristics of the circuit are ignored and the coupling coefficient (k) is assumed to be the minimum value, and the k is defined as

$$k = \frac{L_{mx}}{L_{mx} + L_{kx}} \tag{16}$$

Fig. 6 illustrates the simplified circuit waveforms excluding the interval of Fig. 2 (*Mode III* $[t_2 - t_3]$ and *Mode VI* $[t_5 - t_6]$).

A. HIGH STEP-UP GAIN

Simplified steady-state analysis of the proposed converter uses Fig. 3 *Mode I*, *Mode II*, *Mode IV* and *Mode V*, which are related to Fig. 6. The leakage inductor, primary and secondary voltages of L_1 and L_2 are given as

$$V^I_{Lk2} = V^{III}_{Lk1} = \frac{L_{k2}}{L_{m2} + L_{k2}} V_{in} = (1 - k) V_{in} \tag{17}$$

$$V^I_{Np2} = V^{III}_{Np1} = \frac{L_{m2}}{L_{m2} + L_{k2}} V_{in} = k V_{in} \tag{18}$$

$$V^I_{Ns2} = V^{III}_{Ns1} = N k V_{in}. \tag{19}$$

Applying the voltage-second balance of the primary and secondary sides of L_2 can be written as

$$\int_0^{DT_s} V_{Lk2}^{I} dt + \int_{DT_s}^{T_s} V_{Lk2}^{II} dt = 0 \tag{20}$$

$$\int_0^{DT_s} V_{Np2}^{I} dt + \int_{DT_s}^{T_s} V_{Np2}^{II} dt = 0 \tag{21}$$

$$\int_0^{DT_s} V_{Ns2}^{I} dt + \int_{DT_s}^{T_s} V_{Ns2}^{II} dt = 0. \tag{22}$$

Substituting (17)–(19) into (20)–(22) can be written as

$$V_{Lk2}^{II} = V_{Lk1}^{IV} = -\frac{D(1-k)}{1-D} V_{in} \tag{23}$$

$$V_{Np2}^{II} = V_{Np1}^{IV} = -\frac{Dk}{1-D} V_{in} \tag{24}$$

$$V_{Ns2}^{II} = V_{Ns1}^{IV} = -\frac{NDk}{1-D} V_{in}. \tag{25}$$

The voltages C_a and C_b connected to the primary side of the coupled inductors are given by

$$V_{Ca} = V_{Cb} = V_{in} - V_{Np2}^{II} - V_{Lk2}^{II} = \frac{1}{1-D} V_{in}. \tag{26}$$

By using the energy stored in C_a and C_b, the voltages of C_3 and C_4 can be written as

$$\begin{aligned} V_{C3} &= V_{C4} = V_{in} - V_{Np1}^{IV} - V_{Lk1}^{IV} + V_{Ca} \\ &= V_{in} - V_{Np2}^{II} - V_{Lk2}^{II} + V_{Cb}. \\ &= \frac{2}{1-D} V_{in} \end{aligned} \tag{27}$$

The voltages C_1 and C_2 connected to the secondary side of the coupled inductors are given by

$$\begin{aligned} V_{C1} &= V_{C2} = V_{Ns2}^{IV} - V_{Ns1}^{IV} \\ &= V_{Ns1}^{II} - V_{Ns2}^{II}. \\ &= \frac{kN}{1-D} V_{in} \end{aligned} \tag{28}$$

The voltage gain of the proposed converter is the sum of the capacitors connected in series, which can be written as

$$V_o = V_{C1} + V_{C2} + V_{C3} + V_{C4} = \frac{4+2kN}{1-D} V_{in}. \tag{29}$$

Therefore, the M of the proposed converter is derived as

$$\therefore M = \frac{V_o}{V_{in}} = \frac{4+2kN}{1-D} = \frac{4+2N}{1-D}_{k=1}. \tag{30}$$

Based on (30), Fig. 7 depicts M of the proposed converter according to D and N. For example, the proposed converter can achieve a high step-up gain of twenty times V_{in} when $D = 0.7$ and $N = 1$. Also, it is possible to increase the voltage gain by using N.

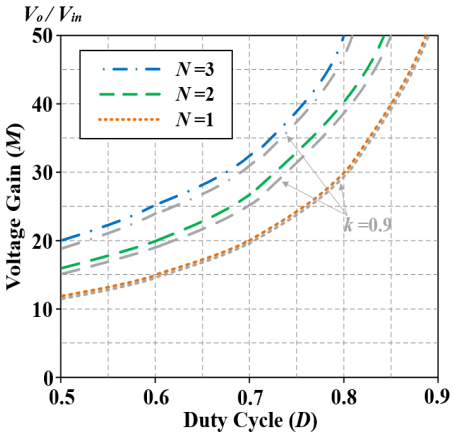

FIGURE 7. Association according to M, D, N.

B. VOLTAGE STRESS

With the voltage clamping performance of the switched capacitor, the switch and diode are expressed as

$$V_{S1} = V_{S2} = V_{Ca} = V_{Cb} = \frac{1}{1-D} V_{in} = \frac{1}{4+2N} V_o \tag{31}$$

$$V_{D1} = V_{D2} = V_{C1} + V_{C2} = \frac{2N}{1-D} V_{in} = \frac{N}{2+N} V_o \tag{32}$$

$$V_{Da} = V_{Ca} + V_{Cb} = \frac{2}{1-D} V_{in} = \frac{1}{2+N} V_o \tag{33}$$

$$V_{Db} = V_{C3} = \frac{2}{1-D} V_{in} = \frac{1}{2+N} V_o \tag{34}$$

$$V_{Dc} = V_{Cb} = \frac{1}{1-D} V_{in} = \frac{1}{4+2N} V_o \tag{35}$$

$$V_{Dd} = V_{C4} = \frac{2}{1-D} V_{in} = \frac{1}{2+N} V_o. \tag{36}$$

Based on (31)–(36), Fig. 8 depicts the voltage stress of semiconductor devices related to N and V_o. Although the voltage gain of the proposed converter is sufficiently high, increasing N for a higher voltage gain significantly increases the voltage stress on D_1 and D_2. Therefore, the proposed converter is designed with $N = 1$, because it already has high step-up gain and the voltage stress on D_1 and D_2 should be reduced, which enables the secondary diodes to have device characteristices such as lower forward voltage and better reverse-recovery.

C. CURRENT STRESS

By (30), the ratio of the output current to the input current is given as

$$\frac{I_o}{I_{in}} = \frac{1-D}{4+2N}. \tag{37}$$

Since the input side of the proposed converter is a two-phase parallel structure, the *average* current of the magnetizing inductor can be written as

$$I_{Lm1\_avg.} = I_{Lm2\_avg.} = \frac{I_{in\_avg.}}{2} = \frac{2+N}{1-D} I_{o\_avg.}. \tag{38}$$

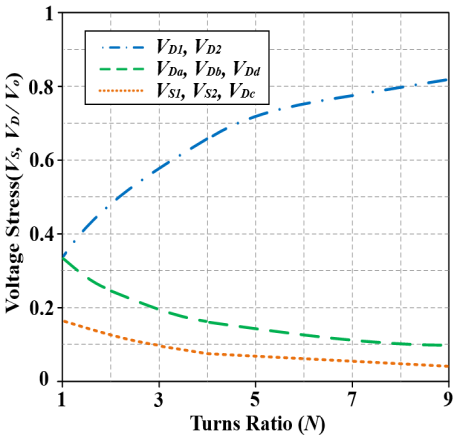

FIGURE 8. Voltage stresses on semiconductor devices versus turns ratio.

Also, based on the current waveform in Fig. 4, *rms* current flowing on the leakage inductors in the primary and secondary sides of L_1 and L_2 is expressed as follows

$$I_{Lk1\_rms} = I_{Lk2\_rms} = I_{Lkx\_rms} = I_{in}\sqrt{\frac{5-2D}{12}} \tag{39}$$

$$I_{L1+L2\_rms(\text{sec.})} = \frac{1-D}{4+2N} I_{in}\sqrt{\frac{8}{3(1-D)}}. \tag{40}$$

To simplify the current analysis of the proposed converter, S_1 and S_2 are represented by S_x, and diodes D_1, D_2, D_a, D_b, D_c and D_d are represented by D_x. In steady state analysis, the *average* current, *peak* current, and *rms* current flowing through the diode can be expressed as

$$I_{Dx\_avg.} = I_{o\_avg.} \tag{41}$$

$$I_{o\_avg.} = \frac{I_{Dx\_peak}}{2}(1-D) \rightarrow I_{Dx\_peak} = \frac{2}{1-D} I_{o\_avg.} \tag{42}$$

$$I_{Dx\_rms} = I_{Dx\_peak}\sqrt{\frac{1-D}{3}} = \frac{2I_{o\_avg.}}{\sqrt{3(1-D)}}. \tag{43}$$

Also, the *peak* current and *rms* current flowing through the switches can be expressed as

$$I_{S1\_peak} \simeq \frac{I_{in\_avg}}{2} + I_{Da\_peak} + NI_{Dd\_peak} + NI_{D2} = \frac{6+3N}{1-D} I_o \tag{44}$$

$$I_{S2\_peak} \simeq \frac{I_{in\_avg}}{2} + I_{Db\_peak} + NI_{D2\_peak} = \frac{4+2N}{1-D} I_o \tag{45}$$

$$I_{S1\_rms} = \frac{I_{in}}{2}\sqrt{3-2D} \tag{46}$$

$$I_{S2\_rms} = \frac{I_{in}}{2+N}\sqrt{\frac{3(3-2D)N^2+12(2-D)N-7D+19}{12}}. \tag{47}$$

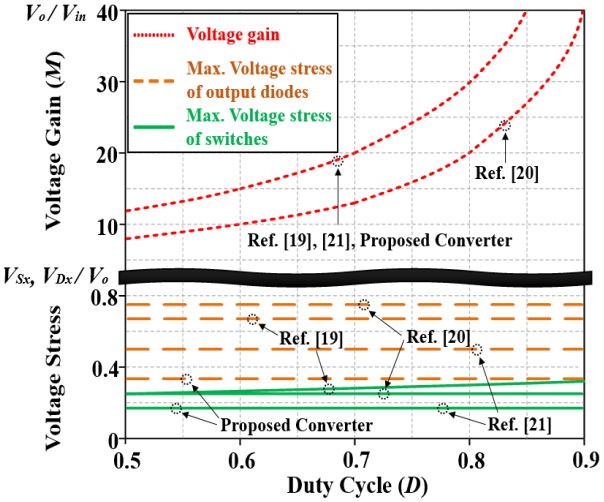

FIGURE 9. M and voltage stress comparison under table 1.

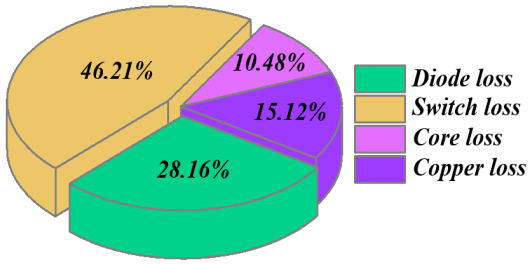

FIGURE 10. Device theoretical loss breakdown of proposed converter.

TABLE 1. Comparison between similar topologies.

Topologies	Proposed converter	Ref. [19]	Ref. [20]	Ref. [21]
Voltage gain	$\frac{2(2+N)}{1-D}$	$\frac{2(2+N)}{1-D}$	$\frac{2(1+N)}{1-D}$	$\frac{2(1+2N)}{1-D}$
Max. Voltage stress (switches)	$\frac{V_o}{2(2+N)}$	$\frac{(1+DN)V_o}{2(2+N)}$	$\frac{V_o}{2(1+N)}$	$\frac{V_o}{2(1+2N)}$
Max. Voltage stress (diodes)	$\frac{NV_o}{2+N}$	$\frac{(1+N)V_o}{2+N}$	$\frac{(1+2N)V_o}{2(1+N)}$	$\frac{V_o}{2}$
Number of switches	2	3	4	4
Number of diodes	6	6	6	4
Number of cores	2	3	2	1
Soft switching conditions	ZCS	ZVS ZCS	ZVS ZCS	ZVS ZCS

D. KEY CIRCUIT PERFORMANCE COMPARISON

Table 1 compares the main characteristics of the proposed converter and similar topologies Ref. [19]–[21], and these high step-up converters have the characteristics of achieving high voltage gain without using the extreme value of D. (D is limited from $0.5 \leq D < 1$.)

In comparsion with Ref. [19], the M of the proposed converter is the same, but the voltage stress of the switch

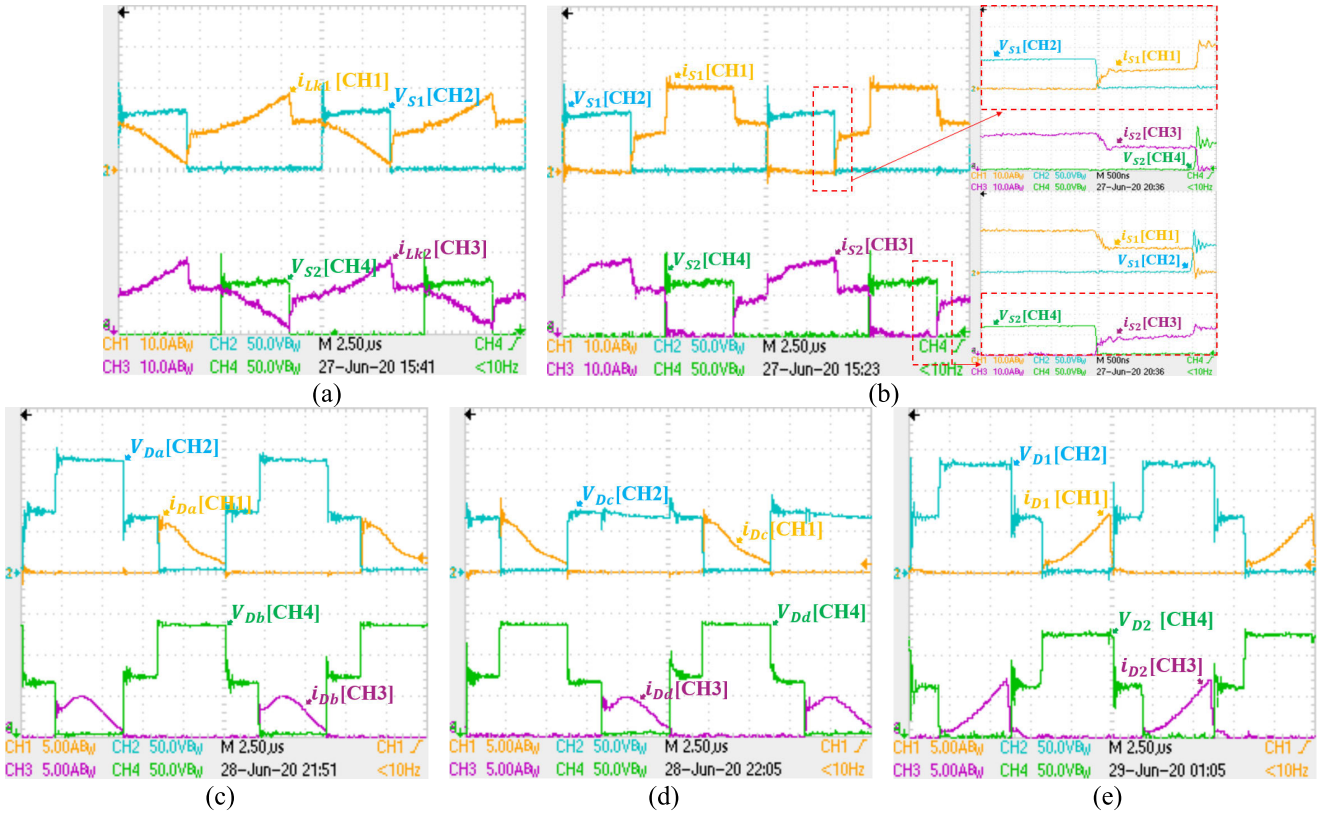

FIGURE 11. Experimental result waveforms (V_{in} = 24V, R_o = 333Ω). (a) V_{S1}, V_{S2}, i_{Lk1}, i_{Lk2}, (b) V_{S1}, V_{S2}, i_{S1}, i_{S2}, (c) V_{Da}, V_{Db}, i_{Da}, i_{Db}, (d) V_{Dc}, V_{Dd}, i_{Dc}, i_{Dd}, (e) V_{D1}, V_{D2}, i_{D1}, i_{D2}.

increases as the D increases. When $D = 0.5$, the voltage stress of the switch is 50% higher. In addition, the diode maximum voltage stress is 100% higher than that of the proposed converter, and the number of switches and cores is one each smaller. However, in Ref. [21], the main switches are ZVS turn-ON and turn-OFF, and the auxiliary switches are also ZCS turn-ON and turn-OFF. Therefore, efficiency can be improved without switching loss.

In comparsion with Ref. [20], since the M of the proposed converter is 50% larger, a high step-up M can be obtained with a low D. In addition, the maximum voltage stress of the switches is 50%, and the maximum voltage stress of the diode is 125% less. Therefore, low-rated-voltage MOSFETs and diodes can be used to reduce conduction losses and converter cost [8]. However, Ref. [20] states that the main switches are ZVS turned ON and ZVS turned OFF under the ZCS condition, and the auxiliary switches are also ZCS turned ON and ZVS turned OFF. Therefore, the four switches can increase the efficiency because the switching loss is small.

In comparsion with Ref. [21], the M and the maximum voltage stress of the proposed converter are the same, but the maximum voltage stress of the diodes is 50% smaller and there are two more the switches. In general, the cost of MOSFETs is high, and semiconductor devices with low-rated-voltage are formed at low cost. Therefore, the proposed converter can be an effective choice with only semiconductor devices. However, Ref. [21] has a small number of cores and diodes. In addition, since the main switches and the auxiliary switches are ZVS turned ON, switching loss can be reduced and efficiency can be improved.

As a result, Fig. 9 depicts the voltage gain and voltage stress of similar topologies under Table 1. The proposed converter has a higher number of devices than recent Ref. [19]–[21] and the switching losses of the switches can be greater. Nevertheless, the proposed converter has the advantage of the lowest number of power semiconductor devices (MOSFETs). In addition, the detailed differences of the compared Ref. [19]–[21] are as follows; a) The complex driving method of active clamp switches; b) Conduction loss of the auxiliary switches through large circulating current; c) Auxiliary switch, gate driver, DSP (coding and control), and circuit configuration through PCB layout. Also, the design of semiconductor devices is the most important part of the power conversion system. Among them, minimizing the MOSFETs (number, low-rated-voltage, low $R_{DS(ON)}$) and diodes (low-rated-voltage) of the proposed converter would be attractive in terms of design and cost.

IV. LOSS BREAKDOWN OF PROPOSED CONVERTER

The loss of the converter mainly accounts for the loss of semiconductor devices and the loss of inductor. Based on the steady state analysis in section III and the experimental

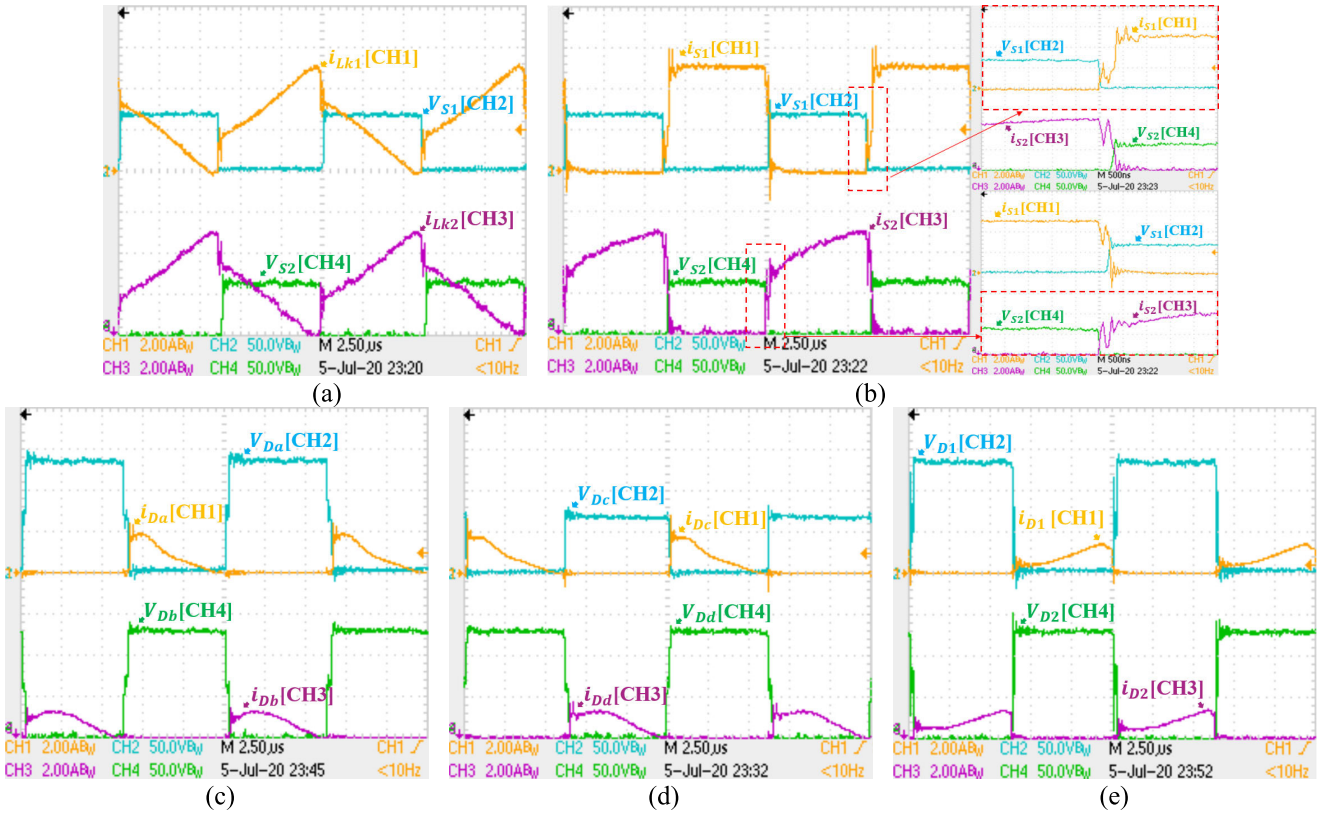

FIGURE 12. Experimental result waveforms (V_{in} = 32V, R_o = 1kΩ). (a) V_{S1}, V_{S2}, i_{Lk1}, i_{Lk2}, (b) V_{S1}, V_{S2}, i_{S1}, i_{S2}, (c) V_{Da}, V_{Db}, i_{Da}, i_{Db}, (d) V_{Dc}, V_{Dd}, i_{Dc}, i_{Dd}, (e) V_{D1}, V_{D2}, i_{D1}, i_{D2}.

parameters in section V, the loss breakdown in the maximum power (P_o = 500W) of the proposed converter was performed.

A. DIODE

The diode loss (P_{Dx_loss}) is divided into conduction loss ($P_{Dx\_con.}$) and reverse recovery loss ($P_{Dx\_rev.}$), which can be written as

$$P_{Dx\_loss} = P_{Dx\_con.} + P_{Dx\_rev.}. \tag{48}$$

The conduction loss ($P_{Dx\_con.}$) is the power consumed while the diode conducts in the forward direction, which is given by

(V_F: forward voltage, $I_{Dx\_arg.}$: diode average current)

$$P_{Dx\_con.} = V_F \cdot I_{Dx\_avg.}. \tag{49}$$

Since the diodes of the proposed converter are turned OFF ZCS under soft switching conditions, the total reverse recovery loss ($P_{Dx\_tot\_rev}$) of the diode is ignored. Therefore, the total loss ($P_{Dx\_tot.\_loss}$) of all diodes can be written as ($V_{F\_D1} = V_{F\_D2} = 0.66V, V_{F\_Da} = V_{F\_Db} = V_{F\_Dd} = 0.78V, V_{F\_Dc} = 0.71V, I_{Dx\_avg.} = 1.5A$)

$$\begin{aligned} P_{Dx\_tot.\_loss} &= P_{Dx\_tot.\_con.} \\ &= P_{D1\_con.} + \ldots + P_{Dd\_con.} = 6.55W. \end{aligned} \tag{50}$$

TABLE 2. Components and parameters of the prototype.(V_{in} = 18 ~ 32V, V_o = 400V, P_o = 500W, N = 22 : 22, f_s = 80kHz).

(V_{in}=18~32V, V_o=400V, P_o=500W, N=22:22, f_s=80kHz)

Components	Parameters
S_1, S_2	IRF100P219(V_{DS}=100V, $R_{DS(ON)}$=1.4mΩ)
D_1, D_2	STTH2002(V_{RRM}=200V, V_F=0.78V)
D_a, D_b, D_d	VS-20CTQ150(V_{RRM}=150V, V_F=0.66V)
D_c	MBR10100(V_{RRM}=100V, V_F=0.85V)
L_{m1}, L_{k1}	65.24μH, 1.54μH
L_{m2}, L_{k2}	65.18μH, 1.49μH
C_1, C_2, C_3, C_4	220μF

B. SWITCH

The losses of switches (P_{Sx_loss}) are divided into conduction losses ($P_{Sx\_con.}$) and switching losses ($P_{Sx\_SW.}$), which can be simply written as follows

$$P_{Sx\_loss} = P_{Sx\_con.} + P_{Sx\_SW.}. \tag{51}$$

The conduction loss ($P_{Sx\_con.}$) of the switch uses the ON state drain-source resistance (R_{DSx_ON}) and rms current (I_{Sx_rms}), which can be written as

($R_{DS1\_ON} = R_{DS2\_ON} = 1.4\text{m}\Omega, I_{S1\_rms} = 16.39\text{A}, I_{S1\_rms} = 14.43\text{A}$)

$$P_{Sx\_con.} = R_{DS\_ON} \cdot I^2_{Sx\_rms} \tag{52}$$

$$P_{Sx\_tot.\_con.} = P_{S1\_tot.\_con.} + P_{S2\_tot.\_con.} = 0.66W. \tag{53}$$

TABLE 3. Comparison among semiconductor devices in similar topologies.

Topologies	Proposed Converter	Ref. [19]	Ref. [20]	Ref. [21]
Theoretical & Experimental Value	V_{S1}=V_{S2}=66.6V	V_{S1}=V_{S2}=66.6V V_r=100V(D=0.5)	V_{S1}=V_{S2}= V_{Sr1}=V_{Sr2}=67.5V	V_{S1}=V_{S2}= V_{Sr1}=V_{Sr2}=88.2V
	V_{Da}=V_{Db}=V_{Dd}=V_{D1}=V_{D2}=133V V_{Dc}=66.6V	V_{Dr1}=V_{Dr2}=100V(D=0.5) V_{Dc1}=V_{Dc2}=133V V_{Do1}=V_{Do2}=266V	V_{Dc1}=V_{Dc2}=67.5V V_{Df1}=V_{Df2}= V_{Do1}=V_{Do2}=202.5V	V_{Dr1}=V_{Dr2}= V_{Do1}=V_{Do2}=300V
Data of Selected Switches	IRF100P219 x 2 (V_{DS}=100V, $R_{DS(ON)}$=1.4mΩ)	IRFP3710 x 2 (V_{DS}=100V, $R_{DS(ON)}$=25mΩ) IRF640 x 1 (V_{DS}=200V, $R_{DS(ON)}$=180mΩ)	IXFP76N15T2 x 4 (V_{DS}=150V, $R_{DS(ON)}$=22mΩ)	IPP076N15N5 x 4 (V_{DS}=150V, $R_{DS(ON)}$=7.6mΩ)
Data of Selected Diodes	STTH2002 x 2 (V_{RRM}=200V, V_F=0.86V) VS-20CTQ150 x 3 (V_{RRM}=150V, V_F=0.66V) MBR10100 x 1 (V_{RRM}=100V, V_F=0.7V)	MUR460 x 6 (V_{RRM}=600V, V_F=1.05V)	MUR1560T x 6 (V_{RRM}=600V, V_F=1.68V)	RFN20NS6SFHTL x 4 (V_{RRM}=600V, V_F=1.25V)
Specification	18~32V → 400V	30V → 400V	15~30V → 270V	30~40V → 600V
Frequency/N	80kHz/1	100kHz/1	50kHz/1	100kHz/1.2
Max. Power	500W	200W	1kW	1kW
Max. Efficiency	97.29%	96.3%	97.26%	97.5%

The switching losses (P_{Sx_SW}. are composed of the cross area of the drain-source voltage (V_{DS}) and the drain current (I_D) in the turn-ON and turn-OFF transients of the switches. Since the proposed converter is partially ZCS turned ON, only the turn-OFF period is considered, and the current rise time (tri) and fall time (tfv) are added, which can be written as

($V_{DSx} = 66.66\text{V}, I_{D(OFF)} = 12.5\text{A}, tri = 124.79\text{ns}, tfv = 1.32\text{ns}, fs = 80\text{kHz}$)

$$P_{Sx\_SW.} = \left[V_{DS} \cdot I_{D(OFF)} \cdot (tri + tfv)/2\right] \cdot f_s \quad (54)$$

$$P_{Sx\_tot.\_SW} = P_{S1\_tot.\_SW(OFF)} + P_{S2\_tot.\_SW(OFF)} = 8.54W. \quad (55)$$

C. COUPLED INDUCTOR

The losses of inductors ($P_{C.I.\_loss}$) are mainly divided into core losses due to the core ($P_{C.I.\_core}$) and copper losses ($P_{C.I.\_cop.}$) resulting from the winding. The losses generated by the coupled inductor are divided into the primary side and the secondary side of the transformer type. The copper loss must be additionally considered and the total loss ($P_{C.I.\_tot.\_loss}$) can be written as

$$P_{C.I.\_loss} = P_{C.I.\_core} + P_{C.I.\_cop.}. \quad (56)$$

The core loss ($P_{C.I.\_core}$) is usually expressed as hysteresis loss, which can be calculated using the steinmetz equation as follows [27];

($k_1 = 66.66\text{V}, k_2 = 2.165, k_3 = 1.78, V_L = 1.32\text{V}, fs = 80\text{kHz}$)

$$P_{C.I.\_core} = k_1 \cdot B_{\max}^{k_2} \cdot f_s^{k_3} \cdot V_L \quad (57)$$

$$P_{C.I.\_tot.\_core} = P_{L1\_core} + P_{L2\_core} = 2.44W. \quad (58)$$

The copper losses ($P_{C.I.\_cop.}$) of the coupled inductor are of the transformer type and are calculated in nanometers for the primary and secondary sides, and this can be written as

($I_{Np1\_rms} = 13.92\text{A}, I_{Ns1\_rms} = 4.08\text{A}, R_{dc} = 8.37\text{m}\Omega$)

$$P_{L1\_cop.} = I_{Np1\_rms}^2 \cdot R_{dc} + I_{Ns1\_rms}^2 \cdot R_{dc} \quad (59)$$

$$P_{C.I.\_tot.\_cop.} = 2(P_{L1\_cop.} + P_{L2\_cop.}) = 3.52W. \quad (60)$$

As a result, Fig. 10 depicts the distribution of each power device used in the proposed converter according to the loss breakdown as a graph.

V. EXPERIMENTAL VERIFICATION

To verify the performance of the proposed converter, a prototype was built and tested. The components and parameters used in the prototype are listed in Table 2. Each experiment was performed with input voltage, output voltage, and output power. The section requiring a high D of V_{in} = 18V, 24V is the section of $0 < i_{Lkx}$. In the light load section that requires a low D of V_{in} = 32V, it is driven with the $i_{Lkx} \leq 0$ section. The coupled inductors used toroidal cores and all semiconductor devices were selected with a 150% rated-voltage margin.

Fig. 11 shows the waveforms operating under the $0 < i_{Lkx}$ section of input voltage 24V. Fig. 11(a) shows the voltage of switches and the current of leakage inductors. Also, Fig. 11(b) shows the voltage and current of the switches. The voltage stress of S_1 and S_2 is about 66V, which matches the calculation of (30). Therefore, conduction losses can be reduced by using MOSFETs with low voltage ratings. Fig. 11(c)~11(e) show the voltage and current of diodes. The voltage stress of D_1, D_2, D_a, D_b, D_d is about 133V, and the voltage stress of D_c is about 66V, which is consistent with the calculation of (31)~(36).

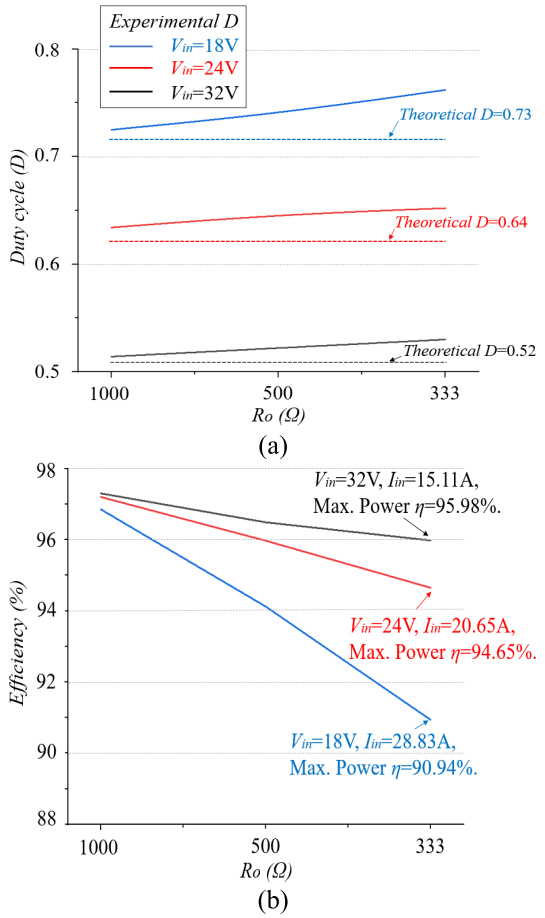

FIGURE 13. **Measurement data of the experiment. (a) Duty cycle under output load and input voltage. (b) Efficiency under output load and input voltage.**

Fig. 12 shows the waveforms operating under the $i_{Lkx} \leq 0$ section of the input voltage 32V. Fig. 12(a) shows the voltage of switches and the current of leakage inductors, and Fig. 12(b)∼12(e) shows the voltage and current of diodes. The leakage inductor, switch, and diode current waveforms similar to those in the theoretical key waveform in Fig. 4 were confirmed.

In Figs. 11(b) and Fig. 12(b), it was confirmed that the switch current waveform is partially ZCS turned ON under soft switching conditions as the slope of the leakage inductor current increases. In Fig. 11(c)∼11(e) and Fig. 12(c)∼12(e), it was shown that there is no reverse recovery loss because the diode current waveform is ZCS turned OFF by the falling slope of the leakage inductor current.

Fig. 13 depicts the measured data of the experimental prototype. Fig. 13(a) depicts the change in duty cycle under the difference between the output load and the input voltage, which requires a larger D as the power increases. Fig. 13(b) depicts the measured efficiency under the difference between the output load and the input voltage. When the input voltage is 32V, the maximum efficiency is 97.29%.

Table 3 compares the experimental parameters of the proposed converter and similar topologies. The switches of the proposed converter consist of the smallest number of components, rated voltage, and $R_{DS(ON)}$. In addition, the prototype was tested through the widest range of M (twenty two times). Assuming the input/output specfication is equal in all converters, the diodes with the lowest rated voltage and V_F, can be used in the proposed converter.

VI. CONCLUSION

A new high step-up interleaved converter with a coupled inductor was proposed. The proposed converter has the following features.

1) The power level and input current ripple are respectively increased and reduced by interleaved operation on the input side, and high voltage gain is obtained by the series stack method on the output side.‘

2) The conduction loss and efficiency are improved by using lower voltage rated MOSFETs and diodes.

3) The leakage inductor energy is efficiently recycled to the output energy.

4) The switches are partially ZCS turned ON under soft switching conditions, and the reverse recovery problem of the diodes is alleviated.

These features of the proposed converter can be a promising candidate in renewable energy fields that require low input voltage and high output voltage.

REFERENCES

[1] M. L. Alghaythi, R. M. O'Connell, N. E. Islam, M. M. S. Khan, and J. M. Guerrero, "A high step-up interleaved DC-DC converter with voltage multiplier and coupled inductors for renewable energy systems," *IEEE Access*, vol. 8, pp. 123165–123174, Jul. 2020.

[2] A. Ajami, H. Ardi, and A. Farakhor, "A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4255–4263, Aug. 2015.

[3] W. Chen, X. Wu, L. Yao, W. Jiang, and R. Hu, "A step-up resonant converter for grid-connected renewable energy sources," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3017–3029, Jun. 2015.

[4] K. Jyotheeswara Reddy and N. Sudhakar, "High voltage gain interleaved boost converter with neural network based MPPT controller for fuel cell based electric vehicle applications," *IEEE Access*, vol. 6, pp. 3899–3908, Feb. 2018.

[5] H. Bi, P. Wang, and Y. Che, "A capacitor clamped H-type boost DC-DC converter with wide voltage-gain range for fuel cell vehicles," *IEEE Trans. Veh. Technol.*, vol. 68, no. 1, pp. 276–290, Jan. 2019.

[6] V. F. Pires, A. Cordeiro, D. Foito, and J. F. Silva, "High step-up DC–DC converter for fuel cell vehicles based on merged quadratic Boost–Cuk," *IEEE Trans. Veh. Technol.*, vol. 68, no. 8, pp. 7521–7530, Aug. 2019.

[7] Y. Zhang, H. Liu, J. Li, M. Sumner, and C. Xia, "DC-DC boost converter with a wide input range and high voltage gain for fuel cell vehicles," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4100–4111, May 2019.

[8] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[9] W. Li, X. Xiang, C. Li, W. Li, and X. He, "Interleaved high step-up ZVT converter with built-in transformer voltage doubler cell for distributed PV generation system," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 300–313, Jan. 2013.

[10] Z. Chen, S. Liu, and L. Shi, "A soft switching full bridge converter with reduced parasitic oscillation in a wide load range," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 801–811, Feb. 2014.

[11] C.-T. Pan, C.-F. Chuang, and C.-C. Chu, "A novel transformer-less adaptable voltage quadrupler DC converter with low switch voltage stress," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4787–4796, Sep. 2014.

[12] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001, pp. 55–56.
[13] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of high-step-up coupled-inductor boost converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 689–704, Jun. 2016.
[14] C.-T. Pan and C.-M. Lai, "A high-efficiency high step-up converter with low switch voltage stress for fuel-cell system applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 1998–2006, Jun. 2010.
[15] W. Li, Y. Zhao, Y. Deng, and X. He, "Interleaved converter with voltage multiplier cell for high step-up and high-efficiency conversion," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2397–2408, Sep. 2010.
[16] W. Li, Y. Zhao, J. Wu, and X. He, "Interleaved high step-up converter with Winding-Cross-Coupled inductors and voltage multiplier cells," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 133–143, Jan. 2012.
[17] K.-C. Tseng and C.-C. Huang, "High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1311–1319, Mar. 2014.
[18] X. Hu, G. Dai, L. Wang, and C. Gong, "A three-state switching boost converter mixed with magnetic coupling and voltage multiplier techniques for high gain conversion," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2991–3001, Apr. 2016.
[19] B. Akhlaghi, N. Molavi, M. Fekri, and H. Farzanehfard, "High step-up interleaved ZVT converter with low voltage stress and automatic current sharing," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 291–299, Jan. 2018.
[20] L. He, X. Xu, J. Chen, J. Sun, D. Guo, and T. Zeng, "A plug-play active resonant soft switching for current-auto-balance interleaved high step-up DC/DC converter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7603–7616, Aug. 2019.
[21] H. Moradisizkoohi, N. Elsayad, and O. A. Mohammed, "An integrated interleaved ultrahigh step-up DC–DC converter using dual cross-coupled inductors with built-in input current balancing for electric vehicles," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 644–657, Mar. 2020.
[22] W. Li, L. Fan, Y. Zhao, X. He, D. Xu, and B. Wu, "High-step-up and high-efficiency fuel-cell power-generation system with active-clamp flyback–forward converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 599–610, Jan. 2012.
[23] G. Wu, X. Ruan, and Z. Ye, "High step-up DC-DC converter based on switched capacitor and coupled inductor," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5572–5579, Jul. 2018.
[24] X. Zhang, L. Sun, Y. Guan, S. Han, H. Cai, Y. Wang, and D. Xu, "Novel high step-up soft-switching DC-DC converter based on switched capacitor and coupled inductor," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9471–9481, Sep. 2020.
[25] S.-W. Seo, D.-K. Lim, and H. H. Choi, "High step-up interleaved converter mixed with magnetic coupling and voltage lift," *IEEE Access*, vol. 8, pp. 72768–72780, Mar. 2020.
[26] A. M. S. S. Andrade, L. Schuch, and M. L. D. S. Martins, "Analysis and design of high-efficiency hybrid high step-up DC-DC converter for distributed PV generation systems," *J. Magn. Magn. Mater.*, vol. 320, no. 20, pp. 2494–2498, May 2019.
[27] F. G. J. Landgraf, M. F. de Campos, and J. Leicht, "Hysteresis loss subdivision," *IEEE Trans. Mag.*, vol. 51, no. 4, pp. 3860–3868, Oct. 2008.

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