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Field-Circuit Co-Simulation Method for Electrostatic Discharge Investigation in Electronic Products

LANLAN YANG, CHANG YANG, YAN TU, XIANGJI WANG, AND QIAN WANG
School of Electronic Science and Engineering, Southeast University, Nanjing 210096, China

Corresponding author: Lanlan Yang (jujube_yang@seu.edu.cn)

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ABSTRACT Electrostatic discharge (ESD) plays an important role in the hard or soft failure of electronic products due to its high voltage, strong electric field, instantaneous high current, and a wide spectrum electromagnetic radiation. A field-circuit co-simulation method combining circuit elements and full-wave 3D model is applied to investigate ESD effects on a system including ESD generator, electronic device and IC chips on PCB, which can obtain both the electromagnetic field and the voltage/current information. The signal transmitting can be monitored under ESD-event when different discharge voltage polarity and protective enclosures are applied. Moreover, transient voltage suppressors can be appended to the field-circuit co-simulation model and their effects to ESD protection are investigated. The research on the field-circuit co-simulation of electronic products puts forward a more practical simulation method for electrostatic discharge.

INDEX TERMS Electrostatic discharge, field-circuit co-simulation, full-wave 3D model, signal transmitting.

I. INTRODUCTION

Electrostatic discharge(ESD) is an important part of the electromagnetic interference(EMI) problem in the field of electromagnetic compatibility(EMC),which is very common in our daily life and industrial production. When it occurs, it is often accompanied by high voltage, strong electric field, instantaneous high current, and a wide spectrum electromagnetic radiation.

In recent years, the main research of ESD focuses on electronic products. With the development of integrated technology, electronic parts and components are packed into a single small package, where they are more easily interfered by the internal and external electromagnetic environment in general. ESD is the most important reliability problem that causes the failure of chips or electronic circuits in electronic equipment. It is reported that more than 45% of electronic component failures are caused by ESD [1]. More and more attention has been paid to the research of failures in electronic products due to electrostatic discharge.

Compared with the experiments related to IEC 61000-4-2 standard, the electromagnetic simulation can eliminate the uncertainty of the results brought by different discharge equipment and various experimental environments, and has good repeatability, which makes the complex and variable random process of ESD relatively controllable. And the information obtained by electromagnetic simulation is more abundant, which can quickly locate the position of electronic equipment vulnerable to ESD, the propagation path on PCB and the impact on specific chip.

Equivalent circuit modeling was firstly proposed to simulate ESD generators and then extended to system-level ESD simulation including various circuit models [2]–[5]. Besides the circuit analysis methods, numerical solution of the Maxwell equations was used to simulate ESD generators which was also compared with circuit analysis and measurements [6]–[8]. Inductive and capacitive coupling due to ESD using partial element equivalent circuit(PEEC) method was calculated under various victim

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structures [9]–[10]. Current information obtained by full-wave simulation including the ESD generator and device under test(DUT) was presented [11]–[13]. ESD generator full wave model and SPICE air discharge model were combined to simulate the air discharge [14], [15]. ESD generator and coupling into the DUT were analyzed, but the IC input response model was not included [16]. Several measurement techniques were developed to detect ESD-induced soft failures [17]. The methodology combining transmission line pulse(TLP) full-wave simulation with system-level and TLP measurements was used to investigate ESD-induced soft failures [18]. To sum up, the circuit analysis method alone ignores the influence of ESD field, and cannot analyze the location of hard failure caused by the discharge process. However, electromagnetic field solver alone cannot consider the complex circuit elements, such as IC chips, so the soft failure to the signal cannot be concerned in the simulation.

Therefore, a field-circuit co-simulation method needs to be developed to investigate ESD effects on a system including ESD generator, DUT and IC chips on PCB. This method divides the whole system into two parts: electromagnetic structure and circuit module. It uses full wave methods such as time-domain finite difference or finite element method to accurately solve various complex packaging and interconnection structures, circuit analysis method to solve circuit module. And then an interface will couple the two parts, and finally realize the co-simulation of electromagnetic field and circuit. This method can accurately describe the wave effect in high-speed integrated circuit, and obtain the electromagnetic information in addition to the voltage and current information in the circuit. Therefore, this method is great helpful in the analysis of electromagnetic compatibility, signal integrity, electromagnetic interference and other issues in high-speed integrated circuit [19], [20]. CST-MWS and CST-DS (Computer Simulation Technology-Microwave Studio and Design Studio) can provide an convenient interface for co-simulating the interactive effects of the electromagnetic field and circuit [21]. Transient electromagnetic (i.e. field-circuit) co-simulation has been used to estimate the currents/fields information of electrostatic discharge, and also used to predict a victim trace in electronic products [22]–[24]. A complete model combining a full-wave model and PCB with a behavior model of D flip-flop IC was built to predict the induced voltage, where the co-simulation is not simultaneous [25]. Therefore, the signal transmission and its interference caused by ESD event as well as the electromagnetic field variation simultaneously have not been investigated together to predict the failure.

In this paper, a field-circuit co-simulation method combining circuit elements and full-wave 3D model based on CST is used to investigate ESD effects on a system including ESD generator, electronic device and IC chips on PCB. Signal transmitting under ESD event is investigated to obtain a helpful analysis to ESD protection as well as the electromagnetic field variation simultaneously. Effects of ESD on both ends of a transmission line are compared. And also, Poynting vector norm at different positions is introduced to predict the failure. Finally, transient voltage suppressors (TVS) is applied to reduce the signal interference. Therefore, the signal transmission and its interference as well as the synchronous variation of the electromagnetic field, including the IC chips and TVS, are investigated in this paper.

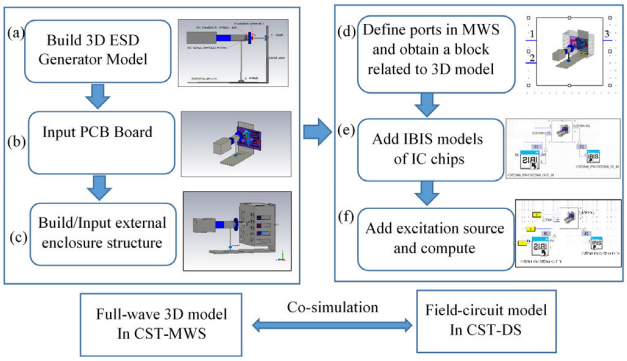


FIGURE 1. Flow diagram of field-circuit co-simulation method based on CST for ESD investigation.

II. SIMULATION METHODS AND PARAMETERS SETTING

Fig.1 shows the flow diagram of field-circuit co-simulation method based on CST for ESD investigation. Firstly, a full-wave 3D ESD generator model is built in CST-MWS(Fig.1(a)). And then a PCB board is added to a proper position of ESD generator(Fig.1(b)). Finally, protective enclosure such as phone shell or PEC case is added to the above model and a complete full-wave 3D model is obtained(Fig.1(c)). In CST-MWS, electromagnetic field can be solved after applying appropriate boundary conditions, mesh generation and simulating parameters. However, some circuit elements such as input/output buffer information specification(IBIS) models of IC chips cannot be added to this full-wave 3D model because they may require non-linear circuit solver. Therefore, some ports are defined in this full-wave 3D model to obtain a 3D-block which acts as an interface between full-wave 3D model and circuit simulation(Fig.1(d)). We treat the 3D simulation model as a black box, which can be regarded as a container of all possible transfer functions both for voltages and currents on conductors as well as fields in the space surrounding the structure. That is to say, full-wave 3D model with ports in CST-MWS is converted to a 3D-block in CST-DS. Then IBIS models of IC chips are appended to the 3D- block(Fig.1(e)). And excitation, termination and other components are connected to obtain a complete circuit including this 3D-block (Fig.1(f)).

Fig.2 shows the top layer of a simplified PCB board used in this paper and the port definitions on PCB. The PCB board mainly includes a CPU(IC100) and four high-speed double data rate (DDR) caches(IC200-IC203). In the simulation, an address line between CPU(IC100) and DDR cache(IC200) is selected to investigate the signal transmitting. As shown in Fig.2, two ports(Port 2 and Port3) at both ends of the address line are defined. These two ports are also used in the

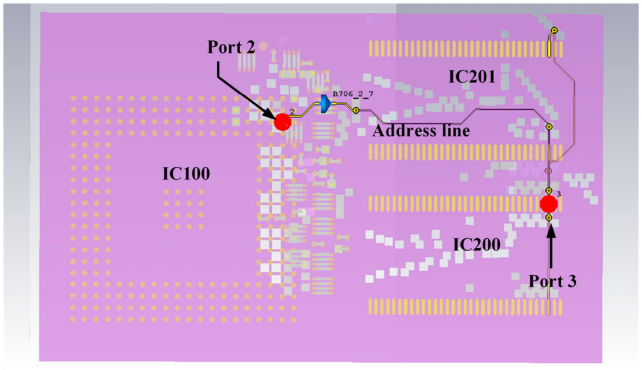


FIGURE 2. PCB top layer and port definitions on PCB.

3D-block to connect to other circuit components(as shown in Fig.1(d)). Port1(as shown in Fig.1(d)) is varied according to its discharge point, which is connected to ESD discharge voltage.

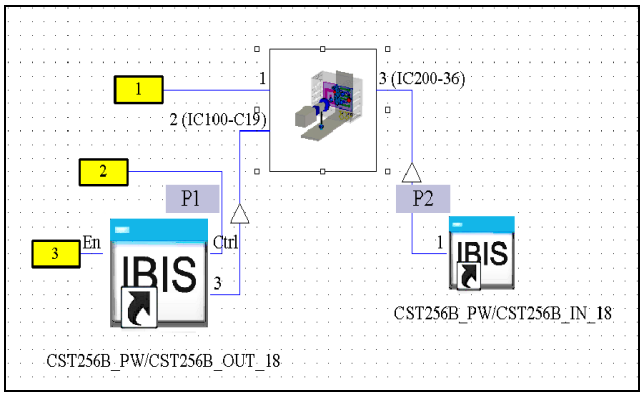


FIGURE 3. Schematic of field-circuit co-simulation method.

Fig.3 shows the schematic of the field-circuit co-simulation method. As shown in Fig.1, the first step is to build a full-wave 3D model including ESD generator and DUT, where all ports need to be defined in CST-MWS. As shown in Fig.2 and Fig.1(d), three ports are defined in the 3D-block. Then two IBIS models(the left one represents CPU chip(IC100) while the right one represents high speed DDR cache chip(IC200)) are connected to the 3D-block in CST-DS. Three excitation terminals (black character on yellow background as shown in Fig.3) are added to the combined model: Terminal1 is the excitation terminal of ESD discharge, Terminal2 and Terminal3 are connected to CPU control terminal and CPU enable terminal respectively. An address line is selected from CPU(IC100) to DDR(IC200), which transmits a signal from IC100-C19 to IC200-36. Two probes of P1 and P2 are placed at both ends of the address line, which can monitor the signal transmitting. Specifically, Probe P1 is at IC100-C19 and Probe P2 is at IC200-36. Finally, the co-simulation model combined with full-wave 3D and circuit elements are built in CST, and the field and circuit information can be obtained in the simulation.

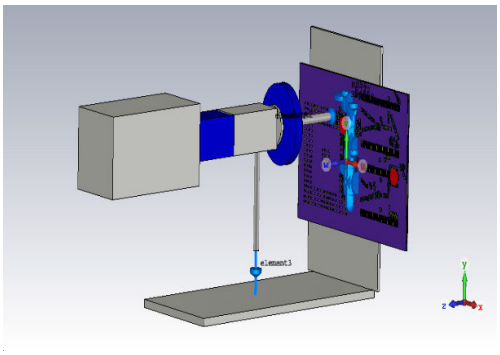


FIGURE 4. Full-wave 3D model without any protective enclosures, which is direct-discharge-to-PCB.

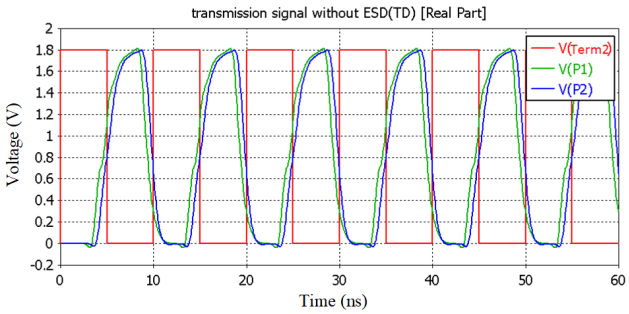


FIGURE 5. Signal transmitting under no-ESD event.

III. SIMULATION RESULTS OF FIELD-CIRCUIT CO-SIMULATION METHOD

A. ESD VOLTAGES

In order to investigate the ESD effects on signal transmitting, the tip of ESD generator contacts the PCB directly without any protective enclosures, as shown in Fig.4. The ground layer of PCB is connected to the reference ground with a large capacitance. Based on this direct-discharge-to-PCB full-wave 3D model, the field-circuit co-simulation model is constructed as described in the previous flow diagram as shown in Fig.1. Fig.5 shows the signal transmitting under no-ESD event. No-ESD event means that 0V is applied to excitation Terminal1. As shown in Fig.5, the control signal waveform(V_{Term2}) is a 100MHz square wave with an amplitude of 1.8V. It can be seen that the control signal is delayed about 3ns from excitation Terminal2 to IC100-C19(Probe P1) under no-ESD event. It is the result of IBIS model of CPU(IC100). The signal is delayed by about 0.6ns from IC100-C19 to IC200-36 through the address line on PCB, which is monitored by Probe P1 and P2. All these results are simulated under no-ESD event. It can be seen that the effects of IBIS model of CPU(IC100) lead to the distortion and delay of the signal while the address line only results in a small delay. Therefore, it can be concluded that the signal passes through the address line only with a small delay under no-ESD event, but the IBIS model corresponding to CPU has a greater impact on the original control signal, which causes a 3ns delay in the signal.

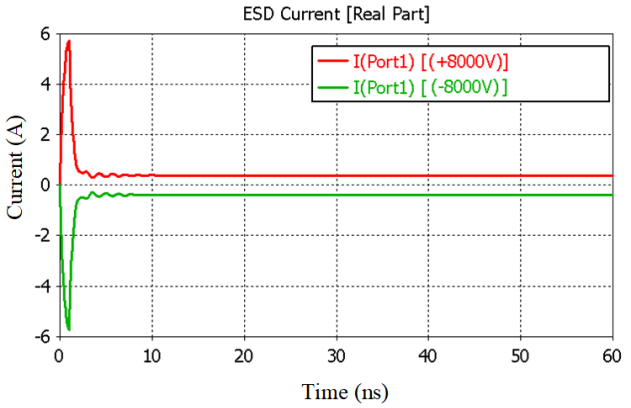


FIGURE 6. Discharge current under ± 8000V ESD voltages.

Fig.6 shows the discharge current under +8kV and -8kV ESD voltage. As the addition of PCB board, the impedance of the equivalent circuit increases correspondingly. It leads to the change of discharge current compared to the standard discharge current. The discharge current obtained from ± 8000V voltage is completely symmetrical. The discharge current pulse lasts about 3ns and it has small oscillation from 3ns to 10ns.

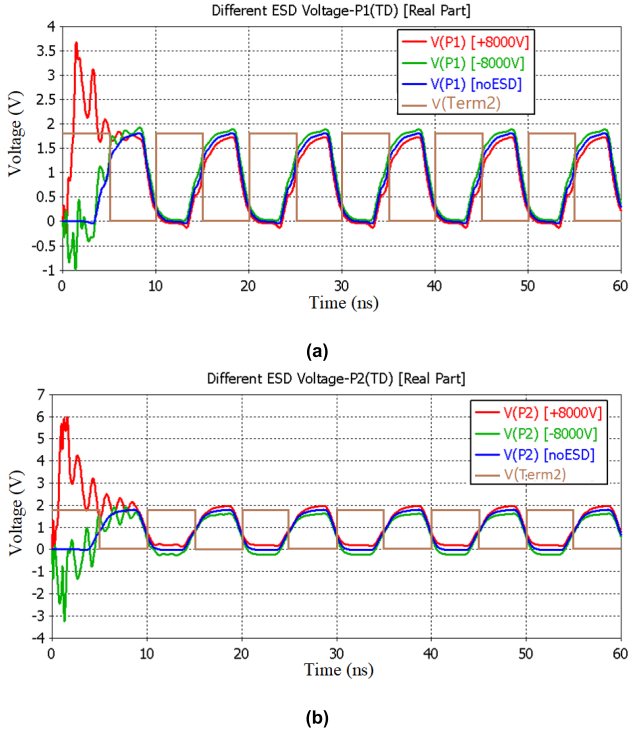


FIGURE 7. Voltage detected at probes P1 and P2 for a 100MHz square waveform transmitting (a) at P1 (b) at P2.

Fig.7 presents the voltage waveform detected at probes P1 and P2 for a 100MHz square waveform transmitting (a) at P1 (b) at P2 under ± 8000V ESD voltage compared to 0V ESD voltage. Although the discharge current generated by ±8000V discharge voltage is basically symmetrical, its influence on the signal transmitting is not symmetrical. It can be seen that the signal distortion caused by + 8000V is more serious than that caused by -8000V in the first 10ns of discharge. The interference amplitude caused by + 8000V has reached 3.7V at Probe P1, exceeding 1.8V, the high level of the transmission signal, but the value of the interference amplitude is only -1V under – 8000V discharge voltage. The interference amplitude becomes larger at probe P2 at the other end of the address line. At probe P2, the interference amplitude of + 8000V is close to 6V, while that of –8000V is about −3V. Due to the different polarity of the voltage, the direction of the current on the PCB surface is also different. The voltage caused by the current and the 1.8V signal superposition result in the final voltage waveform on the probe P1 and P2. Taking the signal voltage of 1.8V as a reference, the interference voltage is also roughly symmetrical when the voltage polarity is opposite. For example, 6-1.8 = 4.2V and 1.8-(-3) = 4.8V are approximately equivalent for Probe P2 under ± 8000V ESD voltage. The results show that the discharge process caused by different polarity discharge voltage has a great impact on the signal transmitting of the selected address line. And also, it should be noticed that interference pulses are also different at different positions of the address line. For example, Probes P1 and P2 are at both ends of the address line and they show different interference pulses.

B. PROTECTIVE ENCLOSURE EFFECTS

At present, due to the consideration of functionality and protection, the packaging shell of different electronic products has certain differences in the shape, material and position setting of internal PCB. We select the protective enclosures of mobile phone and computer-like for their wide use in modern society, which is two typical enclosures of most electronic products.

Fig.8 shows the full-wave 3D model with two different protective enclosures, one is phone shell and the other is perfect electric conductor (PEC) case(computer-like). The size of the phone shell is 120mm×82.5mm×22.5mm. The main body of the phone shell is made of aluminum metal (yellow part), and a piece of glass is embedded in the front of the phone shell. The dimension of the PEC case is: 84.5mm×61.5mm×41.5mm. The front of the PEC case has two rows of circular holes symmetrical to the left and right, and there are four rectangular holes on both sides.

The inner PCB board is same in these two protective enclosures. The connection mode of the two protective enclosures and PCB is to connect the ground layer of PCB with four grounding capacitors, and then connect the protective enclosures with the grounding plate of ESD generator with a large capacitance. It can be seen that the discharge point of the two kinds of protective enclosures is in the center of the protective enclosure. Because the center of the mobile phone shell is located in the glass panel, the materials of the discharge point of the two kinds of protective shells are different, one is dielectric and another is PEC. Then as the flow diagram shown in Fig.1, the signal transmitting under

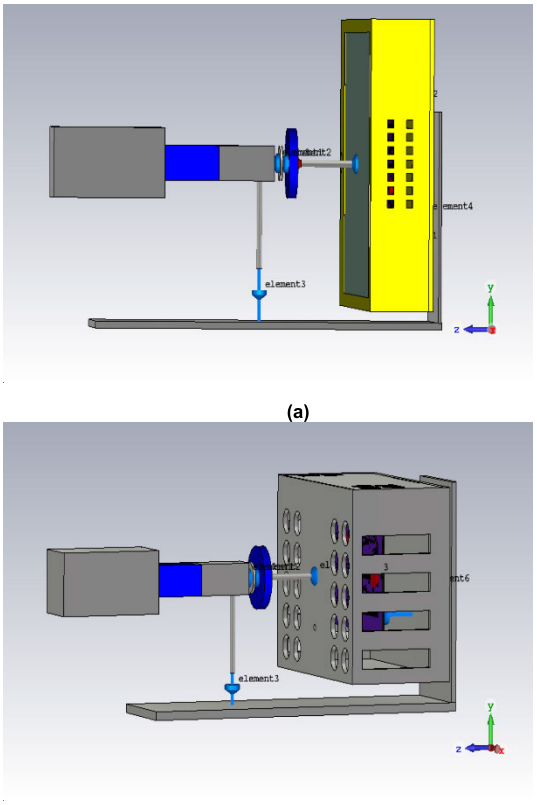


FIGURE 8. Full-wave 3D model with two different protective enclosures (a) phone shell (b) PEC case.

these two protective enclosures can be investigated. It should be noted that the discharging on a dielectric similar to contact discharge is used, one reason is that it is similar to air discharge in some cases, and the other reason is that it may bring more serious signal interference, even if the discharge current is relatively small.

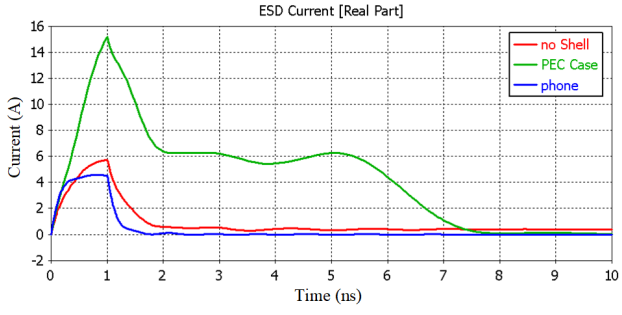


FIGURE 9. Discharge current under different protective enclosures.

Fig.9 shows the discharge current under two protective enclosures compared to no protective enclosure. It can be seen that the direct discharge to PCB(no shell) has a similar trend with that of discharge to phone shell. It is because that both of them are similar to dielectric discharge in these two situations. The discharge point of direct discharge model is connected to pins, but dielectric layer exists between the discharge point and the reference ground. And the glass panel of mobile phone model can also be regarded as a kind of dielectric. However, the discharge point is on the conductor for PEC case. Therefore, the discharge current amplitude for PEC case is larger than that on the dielectric due to different impendences at the discharge point. Actually, Fig.9 shows two typical discharge current waveforms, one is discharge on the conductor and the other is discharge on the dielectric (or the existence of dielectric layer). Even in the same phone shell model, the discharge current waveforms of the two cases with the discharge point on the conductor and on the dielectric is similar to that in Fig.9.

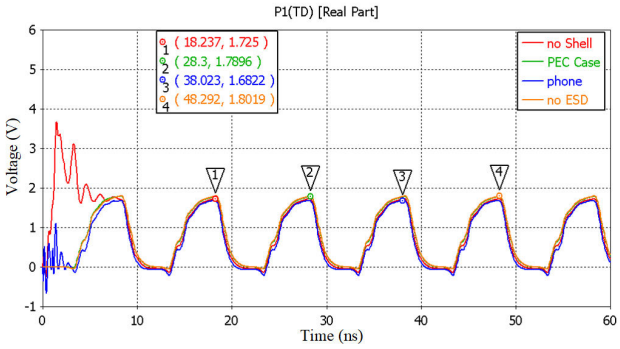


FIGURE 10. Voltage detected at probes P1 and P2 for a 100MHz square waveform transmitting (a) at P1 (b) at P2 under different protective enclosures.

In order to compare the signal transmitting with and without protective enclosures, the same field-circuit co-simulation method as shown in Fig.3 is used to simulate the signal transmitting and the electromagnetic field distribution on the PCB inside the protective enclosure. Fig.10 shows the voltage detected at probes P1 and P2 for a 100MHz square waveform transmitting under different protective enclosures. Four different models: no shell(direct discharge to PCB), phone shell, PEC case and no-ESD event are investigated and compared. It can be seen that the influence of ESD on the signal transmitting is still concentrated in the first 10ns for the model with the added phone shell as is the case of direct discharge to PCB(no shell). But the degree of signal

oscillation caused by the two models is quite different. The influence of ESD on both ends of the address line is relatively large under direct discharge, and the peak value of oscillation reaches 3.7V and 6V respectively at Probes P1 and P2. The model of adding mobile phone shell also has obvious oscillation, but the amplitude is significantly lower than that of direct discharge to PCB, only 1.1V and 1.7V at Probes P1 and P2 respectively. Compared with the former two models, the influence of ESD on the address line under the PEC case is very weak, and the signal transmission waveform almost coincides with the waveform of no-ESD event.

If the ESD interference voltage to the signal exceeds or approaches the high level of the digital circuit, it may lead to an extra high-level signal (i.e. an extra "1"). For sequential logic circuit, the extra "1" will be memorized, which will lead to a logic function error of the whole circuit. This means the interference of signal leads to soft failure. As shown in Fig.10, soft failure may occur at P1 and P2 for no shell model while it may occur at P2 in phone shell model according to its interference voltage.

Through the above analysis, we can see that the PEC case has a good shielding effect for electrostatic discharge. This kind of structure with a certain number of specified-size holes is similar to a Faraday cage, which plays a good role in shielding electromagnetic field and discharge current. When discharging on the glass panel of the mobile phone shell, it has the similar effect with the direct discharge to the PCB for the discharge current. However, the difference lies in the degree of interference to signal. Therefore, it is necessary to avoid direct discharge on PCB. It can be speculated that the PCB may also be protected by adding a metal layer similar to the PEC case inside the mobile phone shell to reduce the signal interference.

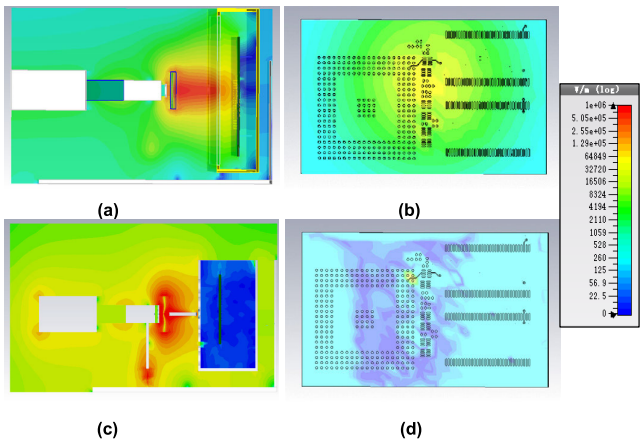


FIGURE 11. Electric field norm at t=1.2ns under two different protective enclosures (a)on whole region with phone shell (b) on PCB inside phone shell (c)on whole region with PEC case (d) on PCB inside PEC case.

Fig.11 shows the electric field norm at t=1.2ns under two different protective enclosures. In the phone shell model, the glass plate is facing the discharge tip. According to Gauss's law in Maxwell's equation, electric field can easily affect internal PCB through glass plate and air layer inside the phone shell. It can be seen that the electric field on the internal PCB can still reach the order of 10^5V/m, and the existence of such a large electric field and its variation may still affect the chip pin and the signal transmitting on the PCB. Compared with the phone shell model, the external electric field of the PEC case is stronger while the internal electric field is smaller as PEC material is an excellent shield for electric fields. At this time, the electric field on the internal PCB in the PEC case model is $10^2 \sim 10^3$V/m, which is about 2-3 orders of magnitude lower than that of the phone shell model. This shows that the PEC case has a better protection effect to the internal PCB. However, the holes on the PEC case lead to leakage of external fields into the internal of the PEC case, so the holes should be carefully designed.

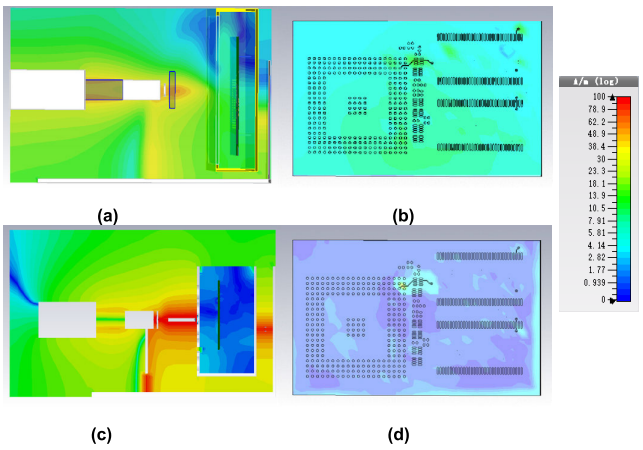


FIGURE 12. Magnetic field norm at t=1.2ns under two different protective enclosures (a)on whole region with phone shell (b) on PCB inside phone shell (c)on whole region with PEC case (d) on PCB inside PEC case.

Fig.12 shows the magnetic field norm at t=1.2ns under two different protective enclosures. Compared with the phone shell model, the magnetic field on the PCB is weaker although the magnetic field in the whole area is stronger in the PEC case model. That is to say, the PEC case with specified-size holes still plays a better role in the discharge process. It is almost free from the interference of external magnetic field on the internal PCB, only with a certain change of magnetic field around the hole. Therefore, it can be said that the shielding effect of PEC case with some specified- size holes is obvious.

In order to better observe the electromagnetic field inside the protective enclosure, we can observe the specific value of the electromagnetic field at some certain positions in addition to the above electromagnetic distributions. Four electromagnetic field probes on PCB, which is used to detect the electromagnetic field at the designated positions. They are distributed at the four corners (top left, bottom left, bottom right, top right) on the front of the PCB, which is 5mm apart from the front layer of the PCB.

The electric field value of four probes at different positions is shown in Fig.13. In the phone shell model, ESD has a great influence on the inner part of the protective enclosure, and its electric field waveform increases quickly within 1ns as the

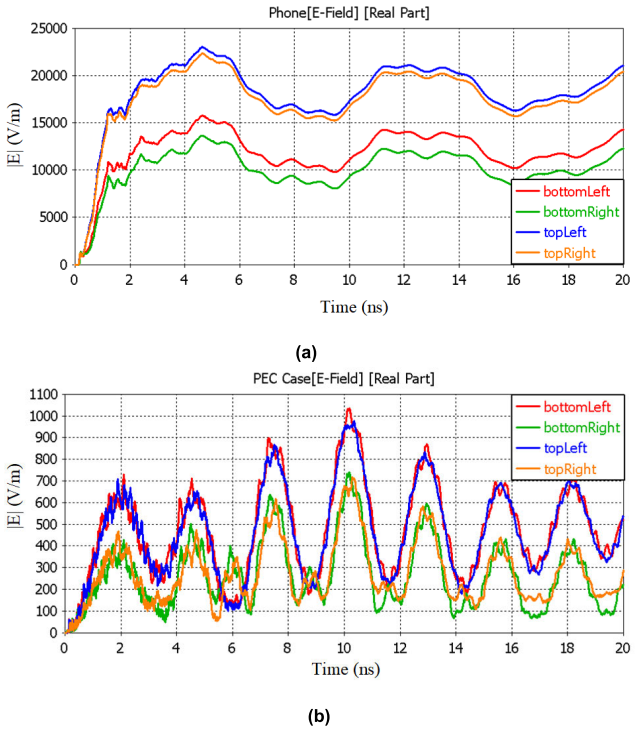


FIGURE 13. Electric field norm at four different probes under two protective enclosures (a)phone shell(b) PEC case.

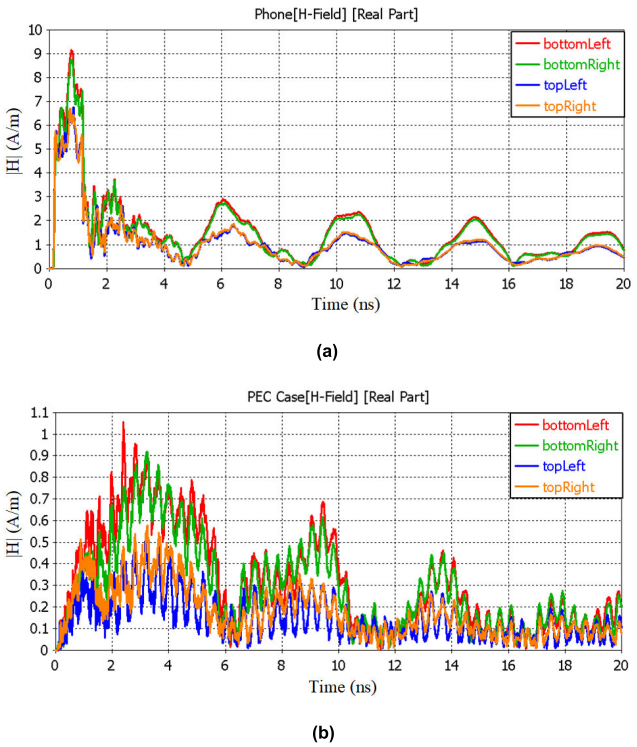


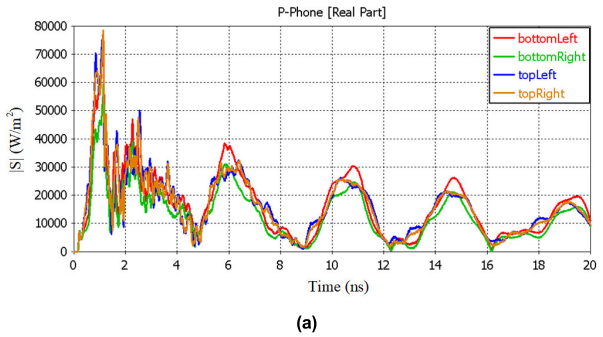
FIGURE 14. Magnetic field norm at four different probes under two protective enclosures (a)phone shell(b) PEC case.

ESD discharge voltage increases from 0V to 8kV. At the same time, we can see that the influence of internal transmission signal voltage on the electric field waveform after 1ns. The electric field at the top is larger than that at the bottom. This is because that the discharge point is closer to the top, which can also be seen from the results of the electromagnetic field distribution as shown in Fig.11. At the same time, the electric field waveform of the left probe is also larger than that of the right probe. In the PEC case model, the internal electric field mainly reflects the influence of transmission signal voltage due to the shielding of external electromagnetic field. And the overall amplitude is reduced by about 20 times compared with the phone shell model. Because the two probes (top left and bottom left) on the left side of PCB are closer to the transmission signal voltage (Port2), the electric field of the two probes on the left side is also larger than that of the two probes on the right side.

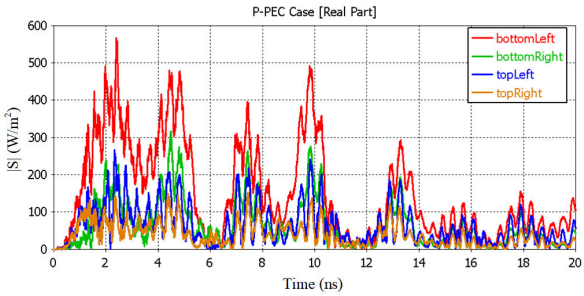
Fig.14 shows the magnetic field norm at four different probes under two protective enclosures. It should be noted that the system shown in Fig.3 is voltage excited. The voltage excitation causes the change of the current and eventually leads to the change of magnetic field according to Ampere-Maxwell law. To simplify the description, we use voltage as excitation to describe the change of magnetic field. In the phone shell model, the magnetic field intensity on the inside of protective enclosure is affected by both ESD voltage and the transmission signal voltage. It can be seen that the magnetic field norm waveform has a large pulse within 2ns, while the discharge current waveform increases first and then decreases to zero within 2ns. These two 2ns periods are consistent, so we can say that the first large pulse in the magnetic field norm waveform is caused by discharge current due to ESD voltage. After 2ns, there are several small pulses on the magnetic field norm waveform, which should be the result of transmission signal voltage superposition. At the same time, it can be found that the amplitude of the magnetic field waveform at two bottom positions is larger than that at the top, which can also be reflected in its magnetic field distribution. Due to the good shielding to the external magnetic field in the PEC case model, the overall amplitude of the magnetic field waveform is at a low level, which is about dozens of times lower than that of the phone shell model. It can also be seen that the whole magnetic field waveform is mainly influenced by the transmission signal waveform.

Through the analysis of the above results, it can be seen that the internal electromagnetic field is mainly affected by the internal transmission signal for the PEC case with better shielding. While for the phone shell, the internal electromagnetic field is mainly affected by the external electrostatic discharge, and the transmission signal voltage also has an impact on the electromagnetic field after the discharge voltage is stable. The influence of the ESD voltage and signal voltage on the electromagnetic field is also related to the transmission signal pin position and ESD discharge position.

For electromagnetic field, we can introduce Poynting vector, which refers to the energy flow density vector in electromagnetic field. The norm of Poynting vector indicates the



(a)



(b)

FIGURE 15. Poynting vector norm at four different probes under two protective enclosures (a)phone shell(b) PEC case.

energy per unit time passing through the vertical unit area. Based on the data value of electromagnetic field, we can calculate the Poynting vector norm at four different probes under two protective enclosures. Fig.15 shows the pointing vector norm at four different probes under two protective enclosures. In the phone shell model, the Poynting vector norm reaches the peak value $8 \times 10^4 \mathrm{W/m^2}$. In the PEC case model, the Poynting vector norm level is only $10^2 \mathrm{W/m^2}$, which is two orders of magnitude lower than that of the phone shell model. Compared with the PEC case model and the phone shell model, we can find that there is almost no interference to the signal in the PEC case model, while in the phone shell model, the interference voltage(1.7V at P2) is almost equivalent to the high level (1.8V) of the circuit. Therefore, we can think that the electromagnetic field of the PEC case model (Poynting vector norm is $10^2 \mathrm{W/m^2}$) will not cause soft failure, while the electromagnetic field of phone shell model will cause soft failure (Poynting vector norm is $10^4 \sim 10^5$ W/m^2). The specific critical value may be related to the high level of the circuit. The electromagnetic field causing hard failure is generally considered to be greater than that of soft failure, and the Poynting vector norm should be greater than 10^5 W/m^2. And also, the magnitude of the Poynting vector at specific locations can roughly point out the location of hard failure.

C. TVS EFFECTS

TVS is a kind of commonly used ESD protection device. In order to investigate effects of TVS to ESD, field-circuit co-simulation model of adding TVS as shown in Fig.16.

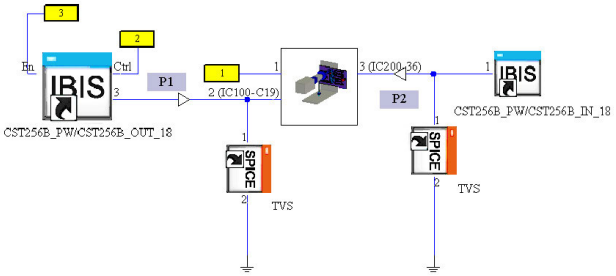


FIGURE 16. Field-circuit co-simulation model after adding TVS.

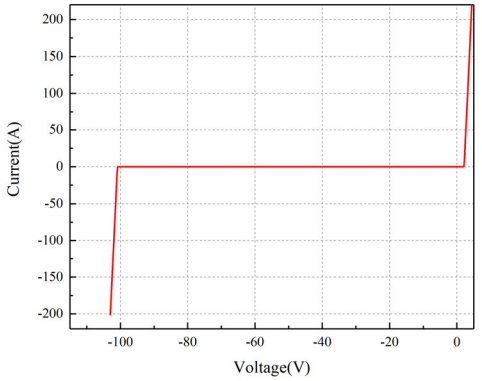
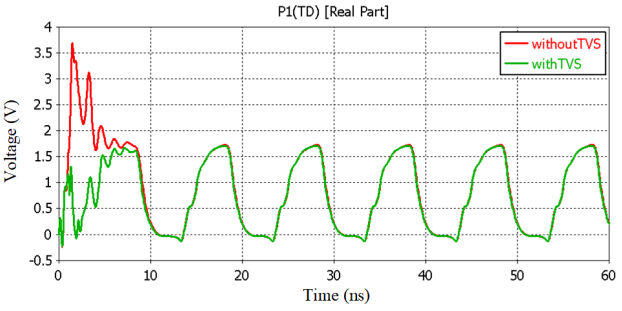
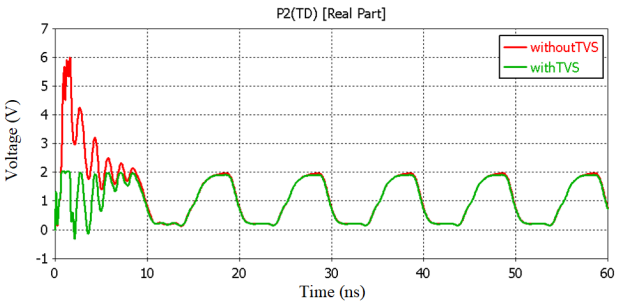


FIGURE 17. I-V curve of the TVS diode.



(a)



(b)

FIGURE 18. Effects to signal transmitting with TVS and without TVS (a) at P1 (b) at P2.

The method is to add TVS SPICE model at the chip pin, which is also at two ends of the investigated address line. Fig.17 shows the I-V curve of the TVS diode. The protection ability of adding TVS is verified by comparing the models

with TVS and without TVS. In order to reflect the protection effect of ESD, the direct discharge to PCB model is selected in this section. The transmission signal frequency is still 100MHz, and other settings remain unchanged. Fig.18 shows the effects to signal transmitting with TVS and without TVS. It can be seen that the oscillation that previously reaches 6V and is limited to 2V after adding TVS at Probe P2. In general, adding TVS tube outside the chip can effectively reduce the influence of ESD on the device. The effect of TVS will be further studied in the future work.

IV. CONCLUSION

A field-circuit co-simulation method combining circuit elements and full-wave 3D model is used to investigate ESD effects on electronic devices which includes an inner printed circuit board with IC chips and external protective enclosure. Discharge current, electromagnetic field distribution and signal transmitting are investigated. The simulation results indicate that different polarity of electrostatic discharge voltage has a different interference pulse to the transmission signal waveform in the early stage. The internal PCB of phone shell has a large amplitude electromagnetic field under ESD event due to the lack of good shielding, which makes the signal transmission of the address line greatly affected, while in PEC case model it has a small impact on the signal transmission due to the good shielding effect of the electromagnetic field. And also, the electromagnetic field on the PCB is affected by the ESD voltage and the signal voltage, and the field strength at different positions is related to the application positions of ESD voltage and signal voltage. Moreover, TVS can be appended to the field-circuit co-simulation model and its effects to ESD protection is verified.

In this paper, the research on the field-circuit co-simulation of electronic products puts forward a practical simulation method for electrostatic discharge. Through the field-circuit co-simulation, the influence of different discharge factors on electronic products is analyzed, which provides theoretical guidance for reducing the influence of electrostatic discharge in the process of product design. In addition, the hard failure can be predicted with the maximum electromagnetic point or the pin current position while the soft failure can be predicted by the signal interference. However, the detailed experimental studies for more accurate verification of this method need to be made in future research.

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LANLAN YANG was born in Anhui, China. She received the M.S. degree in electronic science and technology and the Ph.D. degree in physical electronics from Southeast University, Nanjing, Jiangsu, China, in 2003 and 2008, respectively.

From 2006 to 2009, she was a Lecturer with the Department of Electronic Engineering. From 2009 to 2016, she was an Associate Professor with the School of Electronic Science and Engineering, Southeast University, where she is currently a Professor. During her Ph.D. thesis, she was involved on the plasma discharge display both for simulation and measurements. She is engaged in the research of simulation and measurements related with circuits and electromagnetic field in display fields. She is the author of more than 100 articles and more than 50 inventions.

CHANG YANG received the B.S. and M.S. degrees in electronic science and technology from Southeast University, in 2017 and 2020, respectively.

His research interests include the electrostatic discharge and the electromagnetic compatibility of printed circuit board.

YAN TU received the B.S. and M.S. degrees in electronic engineering from Xi'an Jiaotong University, Xi'an, Shanxi, China, in 1985 and in 1988, respectively, and the Ph.D. degree in physical electronics from Southeast University, in 1993.

She is currently a Professor with the School of Electronic Science and Engineering, Southeast University. She is the author of three books, more than 200 articles, and more than 30 inventions. Her research interests include novel display devices, electromagnetic field simulation, and plasma discharge simulation.

XIANGJI WANG received the B.S. degree in optoelectronic information science and engineering from the Changshu Institute of Technology, in 2018. She is currently pursuing the M.S. degree in electronic science and technology with Southeast University.

Her research interest includes the electrostatic discharge especially air discharge to printed circuit board.

QIAN WANG received the B.S. degree in electronic science and technology from Xidian University, in 2019. She is currently pursuing the M.S. degree in electronic science and technology with Southeast University.

Her research interest includes the electrostatic discharge and the signal integrity of printed circuit board.