IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 17, 2021, accepted February 18, 2021, date of publication February 22, 2021, date of current version March 2, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3060939

Voltage-Mode Elliptic Band-Pass Filter Based on Multiple-Input Transconductor

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This work was supported by the School of Engineering, King Mongkut's Institute of Technology Ladkrabang.

ABSTRACT This paper presents a new voltage-mode elliptic band-pass filter based on a multiple-input transconductor (MI-OTA). The MI-OTA's structure employs the multiple-input MOS transistor technique that simply enables to increase the number of OTA's inputs without increasing the number of current branches or the differential pairs. The MI-OTA features high linearity over a wide input range with a compact and simple CMOS structure. From the advantage of multiple inputs, it enables to construct the arbitrarily summing and subtracting under the proposed voltage-mode filter design procedure. The filter is designed and simulated in Cadence environment using 0.18 μm TSMC CMOS technology. The filter offers 72.9 dB dynamic range for 2 % total harmonic distortion (THD) for sine input signal of 0.5 Vpp @ 1kHz with voltage supply $\pm$ 0.9V. The simulation results of the filter are in agreement with the RLC prototype. The experimental results using commercially available IC are also included to confirm the proposed filter that are in good agreement with the simulation results.

INDEX TERMS Elliptic filter, band-pass filter, transconductor, multiple-input OTA.

I. INTRODUCTION

The elliptic filter is an efficient type of a filtering circuit, which can find many applications in telecommunication, medical and other kinds of electronic systems. In the past, high-order ladder elliptic filters were always realized based on passive elements. Nowadays, such filters are realized rather in integrated form. Integrated filters should be electronically tunable to compensate for possible process, temperature and supply voltage (PVT) variations. Precise operation can be achieved using switched-capacitor (SC) realization, however, SC elliptic filters are rather complex, operate in discrete time and need floating capacitors [1], [2]. In 1992, Nauta [3] introduced an elliptic LPF using a simple linear transconductor, adjusted by its supply voltage. This realization was less complex than its SC counterparts, but the filter still required floating capacitors, as well as, precise controlling of supply voltage, that increased the overall complexity and power consumption. Over the next period, researchers presented elliptic LPFs using dual-output OTAs and the same design methods as in previous research [4]–[7]. These filters were relatively simple, but they still required floating capacitors and they could not be tuned [8]. Multiple feedback loop technique is another way to design active integrated filters [9]. Even though such filters use only grounded capacitors, their structures are rather complex and difficult to be tuned. There are also some other methods to design elliptic active filters in microelectronic technology, based on frequency dependent negative resistors (FDNR) [10], or combinations of OTAs and current conveyors [11]–[13], but they still show the disadvantages of the structures mentioned previously. The source follower-based biquad LPF [14], and its modification by capacitors feedback [15], were introduced but the frequency response cannot be tuned. The transistorized third-order LPF relied on RLC ladder prototype was presented but the electronically tunability cannot be achieved [16]. The two compact structures of LPF were presented with electronic tunability feature. The first LPF, floating emulated inductor and floating capacitors are required [17]. The second LPF, Chebyshev-II is introduced by adding floating capacitors to the core filter circuit [18]. The fourth-order LPF based on two cascaded second-order LPF cells was presented [19]. The

The associate editor coordinating the review of this manuscript and approving it for publication was Yong Chen.

TABLE 1. The comparison of recent Elliptic BPF with proposed Elliptic BPF.

	Technology	VM/CM	Design Technique	Floating capacitors	Frequency tuning	No. Active Element	Complexity Level (1-10)
[21]	CMOS OA & Switch Cap	VM	SFG	Y	N	7 OA + 80 MOS SW.	10
[22]	CMOS Transconductor	VM	Complexificatio n State space	Y	N	24 OTA	9
[23]	MCDTA	CM	Cascade 3 biquads	N	Bias current	6 MCDTA+ Gain	8
[24]	VDTA	VM	GIC Network	Y	N	5 VDTA	8
[25]	CMOS integrator	CM	SFG	N	Bias current	7 Integrators + Gain	8
[26]	CMOS MO-OTA	CM	Multiple Feedback Loop	N	N	7 OTA and 1 MO-OTA	8
[27]	BJT/log-domain	CM	SFG	N	Bias current	8 log-cell	8
[28]	CMOS MO-OTA	CM	SFG	N	Bias current	10 MO-OTA	7
Proposed	CMOS-MI-OTA	VM	SFG	N	R-Bias	9 MI-OTA	6

floating capacitors were required and the frequency tunable had not reported. The second-order BPF using CMOS source feedback (SFB) was introduced with low-complex structure but not practically tuned the frequency response [20].

In this work we propose a new approach to design elliptic band-pass filters (BPF). In order to point out the advantages of the proposed approach, we compare our circuit with some previous works in Table 1. The significant advantage of the proposed approach, compared with other designs, is its smaller complexity. For example, in SC realizations, an external clock signal is required [21]. The OTA-C circuit in [22] is very complex and needs floating capacitors. In [23] a cascade of 3 biquad filters based on modified current differencing transconductance amplifier (MCDTA) and capacitors was applied. This realization requires a large number of transistors. In addition, the notch filter requires the adjustability of the current gain, which makes the circuit large, complex, and cumbersome to tune. Both, V/I and I/V converters are also required due to the current-mode approach.

In [24], inductor emulators are used with voltage differencing transconductance amplifier (VDTA) (internally consisting of 2 OTAs) to replace passive inductors. The circuit still uses many floating capacitors and provides no tuning. In [25] the integrator circuits are designed with signal flow graphs (SFG). Although the circuit operates at high frequency, it is highly complex due to many biasing current sources. In addition, both, V/I and I/V converters are required due to the current-mode operation. The multiple feedback loop realization in [26] is rather complex, because of a complex realization of the tuning function. The circuit operates in current-mode as well. The realization in [27] is based on log-domain integrators and differentiators. It requires a large number of bias currents and consume high power due to the bipolar technology used in this design. Similar techniques are applied with 10 MO-OTAs operated in current-mode [28]. Although this reduces the complexity, the V/I and I/V conversion circuits are required as well.

This article presents a new solution for an elliptic BPF, which is less complex than competitive designs. The circuit is based on multiple-input OTAs (MI-OTA), operating as integrators or differentiators, and uses only grounded capacitors. The frequency response can be tuned with regulating the transconductance of MI-OTA. Relatively low number of active components was achieved thanks to the use of the summing function of MI-OTA. The circuit operates in a voltage-mode.

The paper is organized as follows: Sections 2 describes the multiple-input transconductance stage. Section 3 presents the voltage-mode band-pass elliptic filter application. Section 4 and 5 include the simulation and experimental results, respectively. Finally, section 6 concludes the paper.

II. THE MULTIPLE-INPUT TRANSCONDUCTANCE STAGE

Voltage-to-current converter known as a transconductor or OTA is a basic building block for analog signal processing systems [29]–[31]. One of the effective linearization techniques for this block is the use of a voltage follower (VF), created by a negative feedback connection, linear resistor (R) connected to the output of the VF and a current mirror at the output stage of the VF [34]–[39]. This linearization technique provides a wide range of transconductance tuning without degrading other parameters like input range and linearity [34]–[39]. Although this technique had been used previously in several works, the CMOS structures could be further improved in order to reduce the count of transistors, chip area, and power consumption without degrading the circuit's performances. The transconductor in [32] offers only single input that limits its applications. The transconductors in [33]–[39] offer differential input, however, these CMOS structures are constructed by two voltage to current (V-I) conversion units (VF or current conveyor) that increase the chip area and the total power consumption. The transconductor in [40] offers differential input with single V-I conversion unit based on promising structure of differential difference current conveyor (DDCC). Although this transconductor use one V-I conversion unit its CMOS structure use two differential pairs that increase the number of current branches, power consumption and the chip area. Therefore, the presented transconductor has a differential input with one multiple-input V-I conversion unit and one differential pair (instead of conventional two pairs) by using the multiple-input MOS transistor technique [41]–[47].

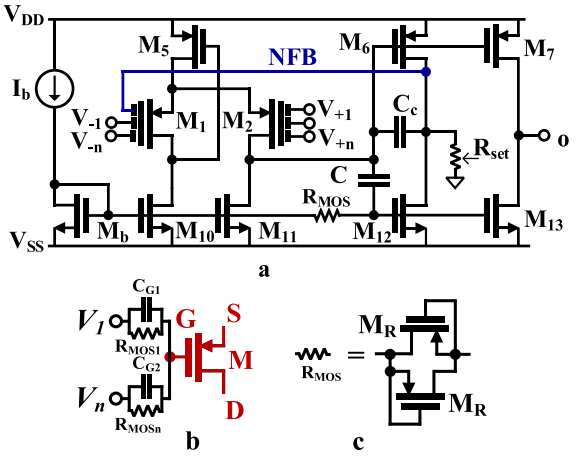

FIGURE 1. a) The CMOS structure of the multiple-input transconductor, b) realization of the MI transistor, and c) realization of the R_{MOS} resistor.

The compact and innovative structure of the OTA is shown in Fig. 1 (a). The structure is based on a two-stage OTA with a negative feedback connection (NFB) that convey the differential input voltage ($V_{id} = (V_{+1} + ..V_{+n}) - (V_{-1} + ..V_{-n})$) to the output which is connected to a linear resistor (R_{set}). This R_{set} performs the V-I conversion where $I_{Rset} = V_{id}/R_{set}$. The output current of the linear resistor I_{Rset} is copied to the output (o) of the OTA using simple current mirrors (M_6-M_7 and M_{12}-M_{13}). The transconductance value of the transconductor is then given by [32]:

$$G_{mset} = \frac{g_m}{1 + g_m R_{set}} \tag{1}$$

where g_m is the internal transconductance of the transconductance. For $R_{set} \gg 1/g_m$, the transconductance G_{mset} can be approximated as follows:

$$G_{mset} \approx 1/R_{set} \tag{2}$$

Note, that there are several ways to achieve electric tuning for this OTA, for example using a resistor divider to split the resistor current [37], using digitally programmable resistor to adjust the current attenuation [40] or simply using an MOS transistor operating in a triode region [32].

The MI-OTA in Fig. 1 (a) has one differential stage M_1, M_2, M_5, M_{10}, M_{11}. The differential pair M_1, M_2 is based on multiple-input technique. The realization of this MI MOS transistor is shown in Fig. 1 (b) where the input gate "G" of transistor M is connected to arbitrary n number of inputs by n number of couples of capacitor C_G and a high resistance MOS resistor R_{MOS} realized by two transistors M_R operating in a cut-off region as shown in Fig. 1 (c). The first and second output stages of the OTA is created by M_6, M_{12} and M_7, M_{13}, respectively. The R_{set} is connected to the first output stage and set the value of the OTA's transconductance. The output current is obtained from the second stage of the OTA. The capacitor C along with R_{MOS} create a simple class AB output stage [39]. The compensation capacitor C_c is used to ensure the stability of the transconductor. The bias current I_b and transistor M_b set the currents of the circuits. Note, that the multiple-input technique gives a freedom to simply increase the number of inputs without increasing the number of current branches or the differential pairs, hence the circuit structure is kept as simple as possible.

III. THE VOLTAGE-MODE BAND-PASS ELLIPTIC FILTER APPLICATION

The design of the proposed BPF is based on an LPF RLC prototype shown in Fig. 2. The network transformation method, and signal flow graph technique are used to form an active BPF circuit operating in a voltage-mode. Finally, the branches of SFG are replaced by MI-OTA circuits. The good performances, and the tunability of frequency response can be achieved with low-complexity structure.

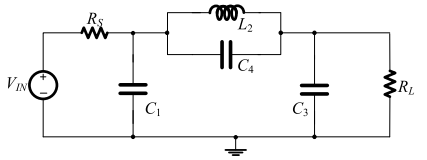

FIGURE 2. RLC elliptic LPF prototype.

According to the network transformation method [48], the elements of the LPF prototype are replaced with elements of a BPF prototype as illustrated in Table 2. The transformed RLC elliptic BPF is shown in Fig. 3.

TABLE 2. Network transformation between LPF and BPF.

Normalized LP prototype (ω=1)	BP Denormalized
L_{LP}	L_{LP}/B, $B/\omega_0^2 L_{LP}$
C_{LP}	$B/\omega_0^2 C_{LP}$, C_{LP}/B
R_{LP}	R_{LP}

$B = \omega_H - \omega_L$, $\omega_0^2 = \omega_H \omega_L$

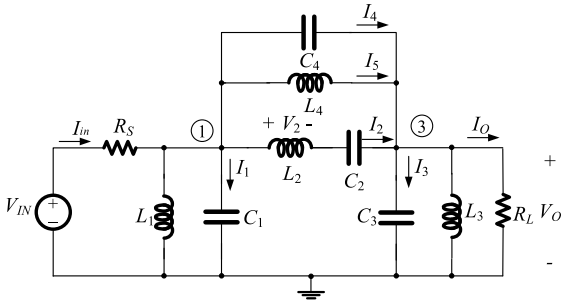

FIGURE 3. Transformed RLC elliptic BPF using LPF prototype.

Using KCL in Fig. 3, the currents and voltage relationship of each designated node or branch can be written as (3)-(12)

$$\frac{V_{in} - V_1}{R_S} = I_{in} \tag{3}$$

$$V_1 = \frac{I_1}{sC_1} \tag{4}$$

$$I_1 = \frac{(V_{in} - V_1)}{R_S} - I_2 - I_4 - I_5 - \frac{V_1}{sL_1} \tag{5}$$

$$V_2 = V_1 - V_3 - \frac{I_2}{sC_2} \tag{6}$$

$$I_2 = \frac{V_2}{sL_2} \tag{7}$$

$$I_3 = I_2 + I_4 + I_5 - \frac{V_3}{sL_3} - \frac{V_3}{R_L} \tag{8}$$

$$V_3 = \frac{I_3}{sC_3} \tag{9}$$

$$I_4 = \frac{V_1 - V_3}{sL_4} \tag{10}$$

$$I_5 = (V_1 - V_3)sC_4 \tag{11}$$

$$I_4 + I_5 = (V_1 - V_3)\left(\frac{1}{sL_4} + sC_4\right) \tag{12}$$

From (3)-(12), the first signal flow graph can be created as shown in Fig. 4. Some nodes of this graph represent current variables, while we need voltage variables for a voltage-mode circuit. Suppose that, the doubly terminated resistors are equal to each other ($R_S = R_L = R$) and the transconductance of OTA is assumed to be $g_m = 1/R$. The current variables can be transformed into voltage variables by incorporating the transconductance (g_m) in suitable branches, thus achieving a new graph, with voltage variables only. The new graph is shown in Fig. 5.

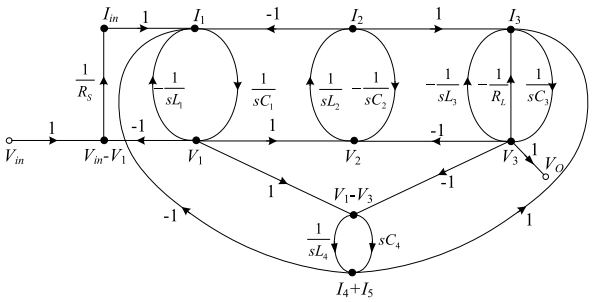

FIGURE 4. First signal flow graph using RLC based elliptic BPF.

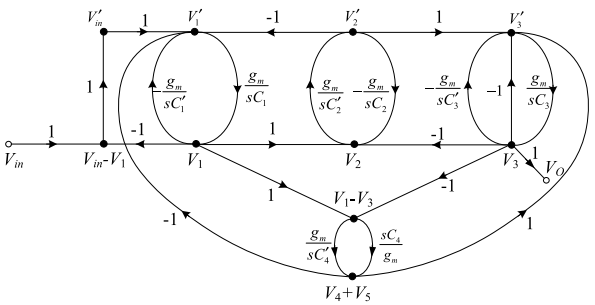

FIGURE 5. Voltage-mode signal flow graph of elliptic BPF.

A. OTA-BASED VOLTAGE-MODE MULTIPLE-INPUT INTEGRATOR

The voltage-mode integrator used in this design is a lossless integrator. It can easily be created by using OTA and a grounded capacitor as shown in Fig. 6. The output voltage of the multiple-input lossless integrator can be expressed by:

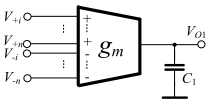

FIGURE 6. OTA-based multiple-input lossless integrator.

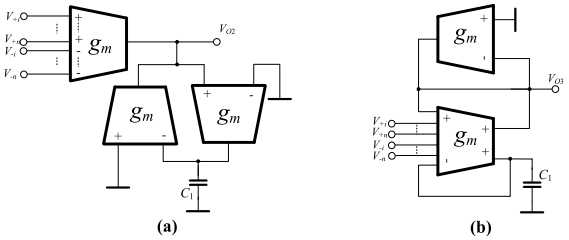

FIGURE 7. OTA-based multiple-input lossless integrator.

$$V_{O1} = \sum_{i=1}^{n} (V_{+i} - V_{-i}) \frac{g_m}{sC_1} \tag{13}$$

B. OTA-BASED VOLTAGE-MODE DIFFERENTIATORS

The voltage-mode lossless differentiator used in this design can be realized in two ways. Type 1 can be realized using 3 OTAs, while Type 2 can be realized using 2 OTAs and a grounded capacitor, as shown in Fig. 7 (a) and (b), respectively. The output voltage of both circuits can be expressed as:

$$V_{O2} = V_{O3} = \sum_{i=1}^{n} (V_{+i} - V_{-i}) \frac{sC_1}{g_m} \tag{14}$$

C. REALIZATION OF A VOLTAGE-MODE ELLIPTIC BPF USING MI-OTA

Using the SFG in Fig. 5, the voltage-mode elliptic BPF can be realized with the integrators and differentiators discussed in sections 3.1 and 3.2. The summations and subtractions can be obtained by using the multiple inputs of OTA, which simplifies the overall design. Based on the type 1 differentiator, the elliptic BPF can be realized using 10 MI-OTAs and 8 capacitors as shown in Fig.8 (a). From Fig. 8, the maximum of four inputs ($n = 4$) of MI-OTA are required. Note that, the unused inputs are grounded. The number of the used MI-OTAs can be decreased if one of the used MI-OTAs has dual positive output. Based on the type 2 differentiator, the elliptic BPF type 2 is realized with 9 MI-OTAs and 8 capacitors as shown in Fig. 8 (b).

IV. SIMULATION RESULTS

The circuit was simulated and designed in Cadence environment using 0.18μm TSMC technology. The transistors aspect ratio in Fig. 1 are: M_1, M_2 = 90μm/3μm, M_5, M_6, M_7 = 2 × 90μm /3μm, M_{10}, M_{11}, M_b = 30 μm /3 μm, M_{12}, M_{13} = 2×30μm /3μm, M_R = 4μm/5μm. The value of

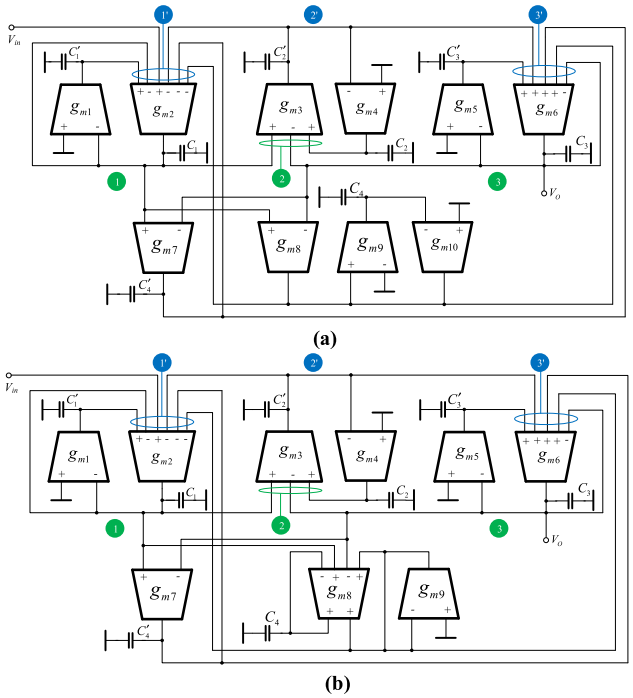

FIGURE 8. Multiple OTA-C based elliptic BPF (a) Type 1 (b) Type 2.

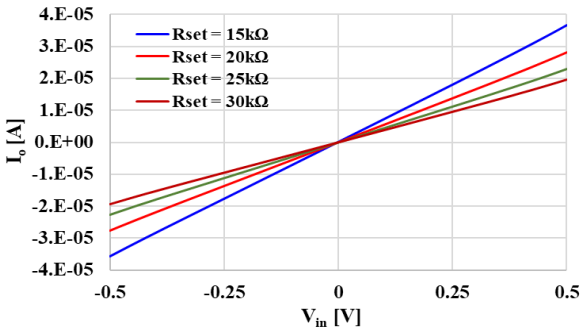

FIGURE 9. The transfer characteristic of the MI-OTA for different R_{set}.

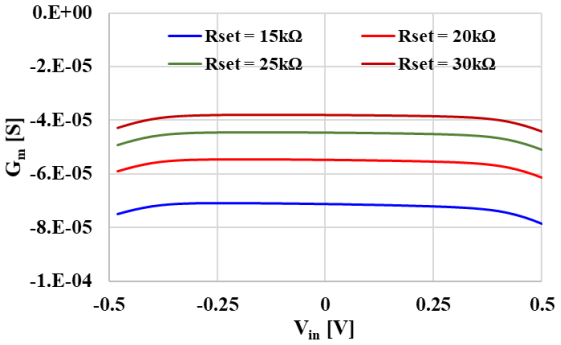

FIGURE 10. The transconductance value versus V_{in} of the MI-OTA for different R_{set}.

capacitors are: C_c, C = 2.6 pF, C_{in} = 0.5pF. The bias current I_b = 50 μA and the total power consumption is 630μW for one-output OTA and 810 μW for two-output OTA.

Figs. 9 and 10 show the transfer characteristic and the transconductance value versus Vin of the MI-OTA for different R_{set} (15kΩ, 20 kΩ, 25 kΩ, 30 kΩ). The MI-OTA shows good tunability and linearity in the range of −0.5 to 0.5V. The

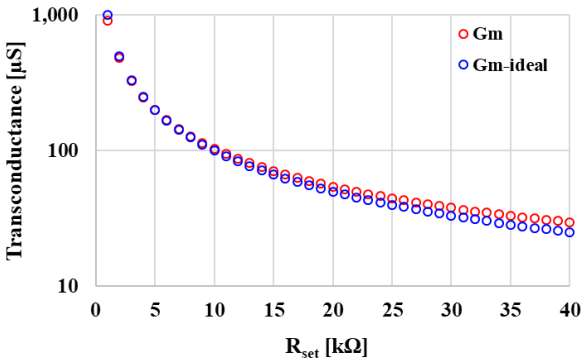

FIGURE 11. The transconductance value of the simulated and ideal OTA versus R_{set}.

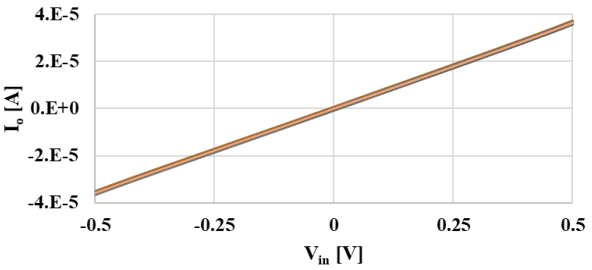

FIGURE 12. The Monte Carlo analysis of the transfer characteristic of the MI-OTA for R_{set} = 15kΩ.

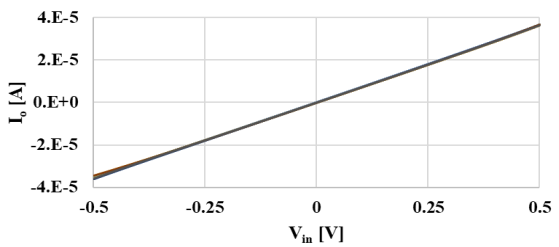

FIGURE 13. The PVT corner analysis of the of the transfer characteristic of the MI-OTA for R_{set} = 15kΩ.

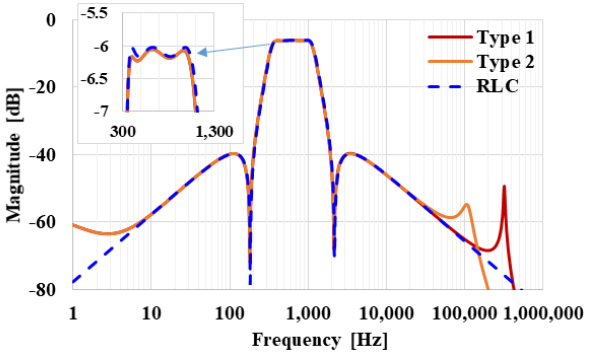

FIGURE 14. The frequency characteristics for the filters and RLC.

relation of the simulated and ideal transconductance versus R_{set} is shown in Fig. 11, where the curves match for lower value of R_{set}.

The Monte Carlo (MC) analysis with 200 runs and the process, voltage, temperature corners are shown in Figs. 12 and 13, respectively. The process corner for the MOS transistor are (ss, sf, fs, ff), for capacitors (fast, slow), for voltage supply (V_{DD} = −V_{SS} = 890mV, 910mV), for

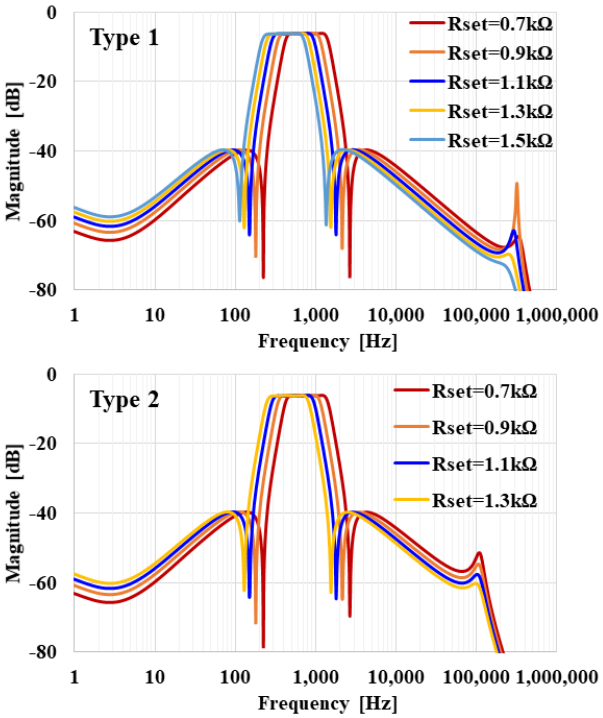

FIGURE 15. The tunability of the 2 types filters for different R_{set}.

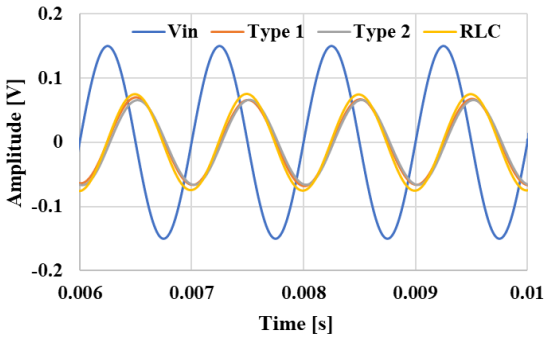

FIGURE 16. The transient characteristic of the filters with input sine wave of 300mVpp @1 kHz.

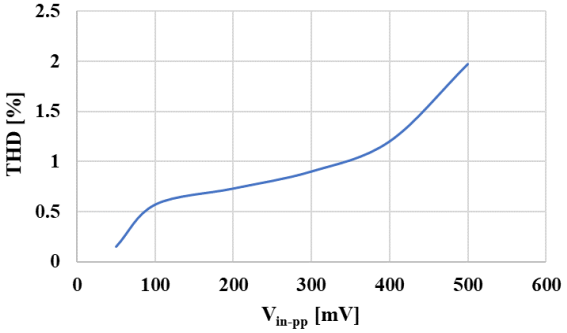

FIGURE 17. The THD versus peak-to-peak input signal @ 1 kHz.

temperature (−10°C, 70°C). As it is shown, the deviation is in acceptable range.

Using the values of passive elements as in Table 3, the frequency characteristics of the proposed BPF filter and its RLC prototype are shown in Fig. 14. For Type 1 the bandwidth (BW)=844.2Hz, mid band gain = −0.605dB, for Type 2 the BW=845.2Hz, mid band gain = −0.605dB, for RLC the

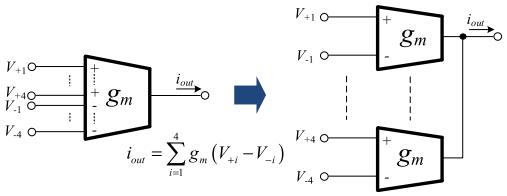

FIGURE 18. Four-input MI-OTA realized with four single-input OTAs.

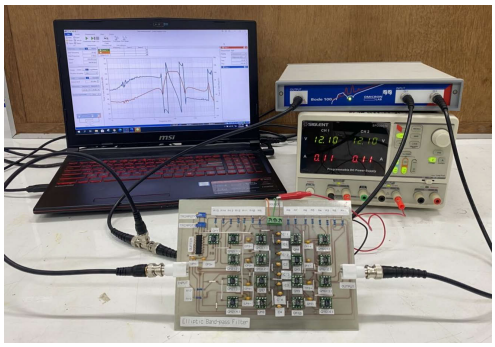

FIGURE 19. Experimental setup of the proposed elliptic band-pass filer.

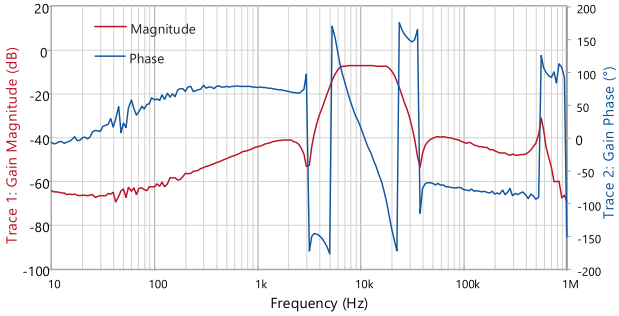

FIGURE 20. Magnitude and phase response of proposed elliptic band-pass filer for $I_B = 60\mu$A.

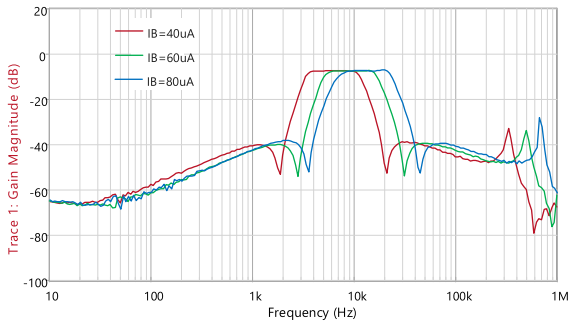

FIGURE 21. Magnitude response of the proposed elliptic band-pass filer for I_B = 40, 60 and 80μA.

BW=858.3Hz, mid band gain = −0.602dB. The −3dB band pass is around 334 Hz - 1.1 kHz. The tunability of the filters for different R_{set} = 0.7kΩ, 0.9 kΩ, 1.1 kΩ, 1.3 kΩ, 1.5 kΩ is shown in Fig. 15.

The transient characteristic of the filters with input sine wave of 300mVpp @1 kHz is shown in Fig. 16, the total harmonic distortion (THD) was 0.9%. The THD versus the input peak-to-peak signal is shown in Fig. 17. The simulated value of the output noise was 40μVrms hence the dynamic range of the filter was 72.9 dB for 2% THD.

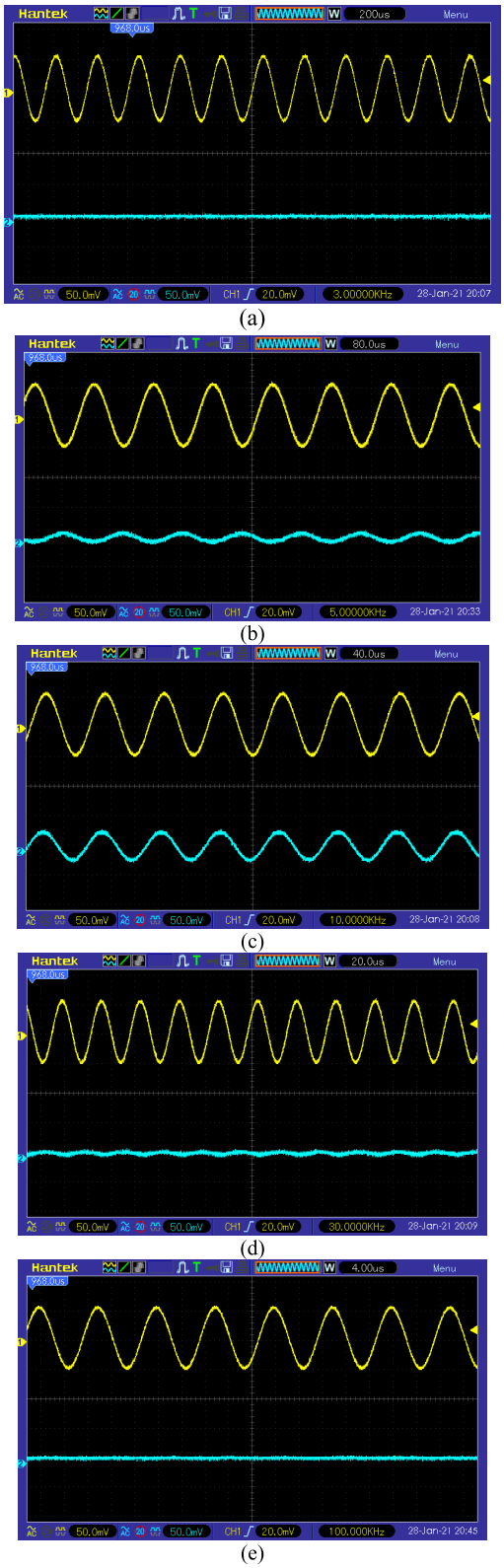

FIGURE 22. Output and input signals of the proposed elliptic BPF at $I_B = 60\mu$A ($f_0 = 10$kHz) for different frequencies (input is upper trace and output is lower trace) (a) 3kHz, (b) 5kHz (c) 10kHz (d) 30kHz (e) 100kHz.

V. EXPERIMENTAL RESULTS

In addition, to confirm practical operation of the proposed BPF, the experiment was conducted using commercially available OTA (LT1228) with ±12V power supply. The values of the used capacitors were $C_1 = C_2 = C_3 = C_1' = C_2' = C_3' = 10$nF, $C_4 = 1$nF, $C_4' = 100$nF. The four-input MI-OTA was implemented using four OTAs, as shown in Fig. 18. The experimental setup is shown in Fig. 19. For measurement of the frequency characteristics, the Bode 100 vector network analyzer has been used.

Fig. 20 shows the magnitude and phase response at $I_B = 60\mu$A. The center frequency (f_0) was around 10kHz, −40dB stop-band and 15kHz bandwidth agree well with simulations. The phase shift was around 10^o at $f = 10$kHz. The filter tunability was verified by adjusting the bias current between 40μA and 80μA as shown in Fig. 21. The magnitude response of the proposed elliptic band-pass filer, for different I_B, was in agreement with simulation results.

The transient response of the filter was verified by applying an input sine-wave signal with 100mVpp amplitude and five different frequencies (1kHz, 3kHz, 10kHz, 30kHz and 100kHz), with $I_B = 60\mu$A. From Fig. 22, the filter can provide the sinusoidal output signal at passband frequency ($f_0 = 10$kHz), while other frequencies cannot be passed to the output. The results of transient response agreed well with the magnitude and phase response in Fig. 20.

Given the bias current $I_B = 60\mu$A for $f_0 = 10$kHz, the sinusoidal signal with amplitude of 100mVpp was applied at the input of the proposed filter. The filter provides an output sine-wave signal as shown in Fig. 22(c) and its spectrum is shown in Fig. 23. The measured HD_2, HD_3 and HD_4 harmonic distortions compared to the fundamental frequency (10kHz) were equal to −32dB, −36dB and −38dB, respectively. Thus, the calculated THD was 3.2%.

TABLE 3. The Passive Elements used in the elliptic BPF.

Prototype	MI-OTA*	LT1228*
C_1=C_2=C_3=250μF	C_1=C_2=C_3=250nF	C_1=C_2=C_3=10nF
L_1=L_2=L_3=250μH	C'_1=C'_2=C'_3=250nF	C'_1=C'_2=C'_3=10nF
C_4=25μF	C_4=25nF	C_4=1nF
L_4=2.5mH	C'_4=2500nF	C'_4=100nF

*For OTA, possible to use the same scaled factor ($1/k_m$) with every passive elements of prototype (for example k_m=100)

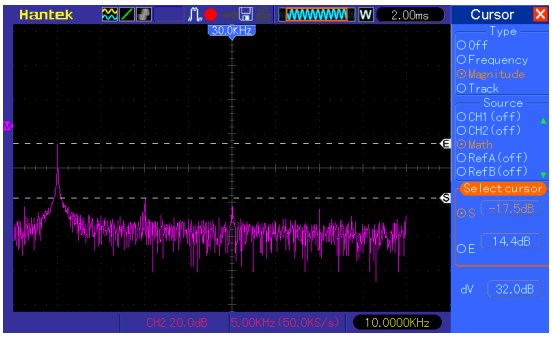

FIGURE 23. Output spectrum of the elliptic BPF when input applied 100mVpp/10kHz with $I_B = 60\mu$A.

VI. CONCLUSION

This paper presents a new voltage-mode elliptic Band-pass Filter based on multiple-input transconductor. As it was

shown, the MI-OTA facilitates filter's construction with less count of active elements and with reduced complexity, compared with other solutions presented in literature. Thanks to the unity gain negative feedback and the capacitive divider, the linearity of the OTA is increased. The proposed circuit was designed in Cadence environment using 0.18 μm TSMC CMOS technology. Intensive simulation results including Monte Carlo and PVT analysis are presented. The simulation and experimental results prove the advantages of the proposed filter.

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