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Digital/Analog Performance Optimization of Vertical Nanowire FETs Using Machine Learning

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ABSTRACT Vertical nanowire field-effect transistors (NWFETs) have been optimized to maximize digital and analog performances using fully-calibrated TCAD and machine learning (ML) technique. Digital performance is quantified by RC delay ($C_{gg}V_{dd}/I_{on}$, where C_{gg} is gate capacitance, V_{dd} is operation voltage, and I_{on} is on-state current) at the fixed off-state currents, and analog performance is quantified by the product of cut-off frequency (F_t) and transconductance efficiency (G_m/I_{ds}). ML accurately predicted the geometry and doping parameters suggesting the best device performances. All the optimized NWFETs have larger drain diameters but smaller source diameters at the minimum of gate lengths, gate oxide thicknesses, drain junction gradients, and source/drain spacer lengths. Small source diameters are needed to tightly control the energy barrier to reduce the short-channel effects, whereas large drain diameters increase current drivability than C_{gg}. Small drain junction gradients increase the lateral electric field from source to drain, which increases the carrier velocity. Longer spacer lengths decrease both I_{on} and C_{gg}, but the I_{on} degradation is critical. These device characteristics validate the optimization results from ML, and ML-based optimization is fast and effective to maximize both digital and analog performances.

INDEX TERMS Machine-learning (ML), python, vertical, nanowire, RC delay, transconductance efficiency, TCAD, device optimization.

I. INTRODUCTION

Fin field-effect transistors (FinFETs) have been scaled down to 5-nm node successfully by full-fledged EUV and SiGe channel [1]. Gate-all-around nanowire (NW) and nanosheet FETs have also been introduced to enhance the gate electrostatics and current drivability [2]. Also, design-technology co-optimization including complementary FET [3]-[5] and buried power rail (BPR) [6] enables further technology node scaling in terms of front-end- and back-end-of-lines. Middle-of-line (MOL) schemes such as self-aligned contact and contact-over-active-gate contact increases the device density by placing metal contacts within the active layout region [7]. However, it is a technology bottleneck to scale down the contacted poly pitch (CPP) below 5-nm node due to process variability and design complexity.

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Meanwhile, vertical NWFET is one of the promising candidates which can have device design flexibility by large CPP margin since the channel is aligned vertically [8]–[11]. In addition, vertical NWFETs along with BPR possibly ease 3D MOL layout schemes by forming power delivery lines at the bottom. Vertical NWFETs have great potential to increase the device density by aligning transistors and selectors vertically [11]–[14]. However, since the fabrication flows are different from conventional horizontal FETs, it is needed to optimize the device structure to boost its performance and finally to provide the device guideline.

Therefore, in this work, we optimize digital and analog performances of vertical NWFETs using fully-calibrated TCAD and machine learning (ML) technique which has been adopted for the optimization of silicon-on-insulator FETs [15], [16]. DC/AC characteristics of vertical NWFETs in terms of geometry and doping have been studied in detail.

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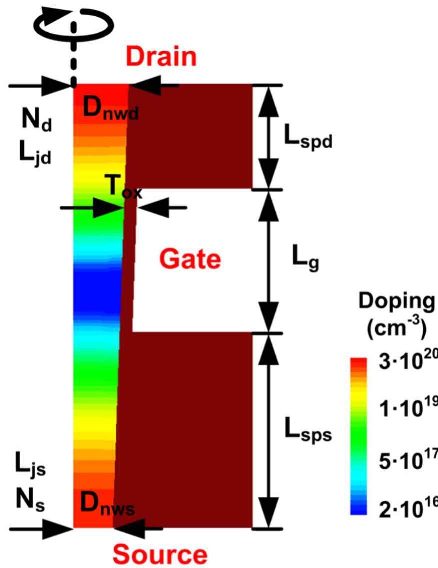

FIGURE 1. 2-D schematic diagram of n-type NWFET. 10 device parameters used for randomization are specified.

TABLE 1. Device parameters and their minimum/maximum values.

Device Parameters		Unit	Minimum	Maximum
L_g	Gate length	nm	15.0	50.0
D_{nws}	NW diameter (S)	nm	7.0	30.0
D_{nwd}	NW diameter (D)	nm	7.0	30.0
L_{sps}	Spacer length (S)	nm	10.0	50.0
L_{spd}	Spacer length (D)	nm	10.0	50.0
T_{ox}	Oxide thickness	nm	1.0	5.0
N_s	Peak doping (S)	cm^{-3}	10^{20}	$4\cdot10^{20}$
N_d	Peak doping (D)	cm^{-3}	10^{20}	$4\cdot10^{20}$
L_{sj}	Junction (S)	nm/dec	2.5	20.0
L_{dj}	Junction (D)	nm/dec	2.5	20.0

* S: Source-side, D: Drain-side

II. DEVICE STRUCTURE AND SIMULATION METHOD

All the silicon vertical NWFETs were simulated using Sentaurus TCAD [17]. Hydrodynamic transport model was solved self-consistently with Poisson and electron/hole continuity equations. Jain-Roulston bandgap narrowing model was used for highly-doped source/drain regions. Density-gradient quantization model was used to consider the quantum confinement effect within the channel. Inversion and accumulation layer mobility degradation model was used to consider impurity, phonon, and surface roughness scatterings. Shockley-Read-Hall, and Hurkx band-to-band tunneling recombination models were used.

Fig. 1 shows 2-D schematic diagram of n-type NWFET. Cylindrical coordinate system is used instead of 3-D device structure to reduce TCAD computation time. 10 device parameters are specified, and their minimum and maximum values are indicated in Table 1. These values are chosen under the feasible condition for vertical NWFETs [10], [11]. Before parameter randomization, n- and p-type NWFETs are calibrated to Samsung NWFETs [18] as shown in Fig. 2. Calibration has been done first by modifying low-field mobility and surface roughness scattering parameters to fit the drain current (I_{ds}) in the linear region. Then, saturation velocity is modified to fit the I_{ds} in the saturation region. Detailed fabrication flow of the NWFETs is shown in [19]. 10 device parameters are randomized uniformly within their boundaries, and total 15,000 devices are used for each device type. Train and test datasets are split randomly into 80:20.

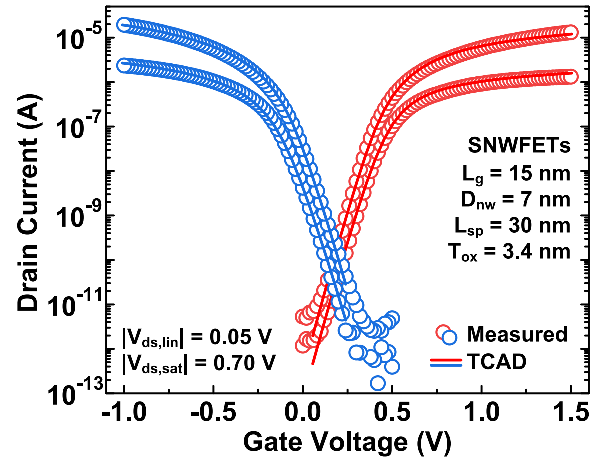

FIGURE 2. Calibration results of n-type and p-type single NWFETs.

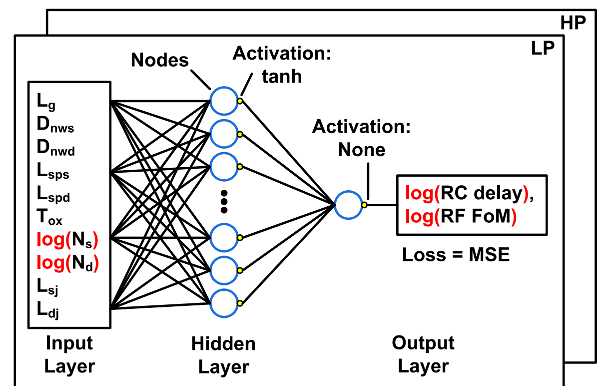

FIGURE 3. Neural network for device optimization according to RC delay and RF figure-of-merit (FoM).

Fig. 3 shows simple schematic neural network using fully-connected multi-layer perceptron (MLP) for the optimization of vertical NWFETs. There is one hidden layer with 20 nodes and hyperbolic tangent (*tanh*) as an activation function. Loss function is a mean-squared-error (MSE). N_s and N_d are logged, and then all the parameters are standardized by subtracting their means and then dividing by their standard deviations. Output parameters are the logarithmic values of RC delay at the off-state currents (I_{off}) of 10^{-10} and 10^{-8} A for low-power (LP) and high-performance (HP) applications, respectively, and RF figure-of-merit (FoM). RC delay and RF FoM are given by

$$RCDelay = \frac{C_{gg}V_{dd}}{I_{on}} \tag{1}$$

$$RFFoM = \max\left(\frac{F_t G_m}{I_{ds}}\right) \tag{2}$$

where C_{gg} is gate capacitance, V_{dd} is operation voltage fixed to 0.7 V, I_{on} is on-state current, F_t is cut-off frequency, and G_m is transconductance. Here F_t is simply calculated

TABLE 2. Spearman correlations between input and output parameters.

Input par.	N-type			P-type		
	(L) RC delay	(H) RC delay	RF FoM	(L) RC delay	(H) RC delay	RF FoM
L_g	0.197	<u>0.254</u>	-0.144	0.182	<u>0.249</u>	-0.137
D_{nws}	-0.019	-0.033	0.056	-0.019	-0.029	0.061
D_{nwd}	-0.087	-0.136	-0.012	-0.085	-0.139	0.008
L_{sps}	<u>0.542</u>	<u>0.563</u>	<u>-0.559</u>	<u>0.564</u>	<u>0.596</u>	<u>-0.575</u>
L_{spd}	0.119	<u>0.210</u>	0.151	0.103	0.195	0.112
T_{ox}	0.076	-0.018	<u>-0.261</u>	0.087	-0.005	<u>-0.253</u>
N_s	-0.062	-0.060	0.059	-0.065	-0.063	0.068
N_d	-0.036	-0.042	0.012	-0.034	-0.039	0.015
L_{sj}	<u>-0.476</u>	<u>-0.454</u>	<u>0.497</u>	<u>-0.494</u>	<u>-0.469</u>	<u>0.522</u>
L_{dj}	-0.036	-0.070	-0.063	0.009	-0.023	-0.066

* Coefficients greater than 0.2 are underlined

as $G_m/(2\pi C_{gg})$, which is valid to non-planar devices [20]. RC delay and RF FoM are logged and then standardized to improve the ML training as in [15].

Weights and biases of hidden and output layers are initialized according to Glorot and Bengio [21], and their values are updated using Adam optimizer [22]. After ML training is finished, using 100 individual trained networks, input parameters are predicted each by gradient descent method numerically [15]. Finally, best input parameters predicting minimum RC delay or maximum RF FoM are chosen. All the ML works were performed using python on a personal computer with Intel i7-7700 (3.60 GHz) and 32.0 GB RAM.

III. RESULTS AND DISCUSSION

A. PERFORMANCE ESTIMATION OF NWFETs USING DEVICE PHYSICS AND CORRELATION ANALYSIS

Digital and analog performances of NWFETs have been analyzed thoroughly in the past. T_{ox} scaling, along with high-k dielectrics, is essential to maintain the gate electrostatics. Shorter junction gradients decrease the short-channel effects (SCEs) as well as the parasitic capacitances including overlap and outer-fringing capacitances, resulting in smaller RC delay [23]-[26]. But too small source-side extension doping increases parasitic resistance (R_{sd}), leading to smaller I_{on} [23], [26]. Smaller NW diameters increase the gate-to-channel controllability, thus showing smaller RC delay in the 5-nm node [27], but the vertical NWFETs have enough design margin to control L_g, L_{sps}, and L_{spd} under the feasible condition to prevent the SCEs. Thus, there are more design options to increase the device performances.

Table 2 shows Spearman correlations between the device parameters and the RC delay for LP and HP applications and the RF FoM. Compared to Pearson correlation, Spearman correlation can find out non-linear relationships between input and output parameters [28]–[30]. All the device parameters are randomized independently, thus are not correlated between them. Among the device parameters, L_{sps} and L_{sj} are the most dominant ones to affect RC delay and RF FoM. According to the correlation analysis, minimum RC delay or maximum RF FoM is achieved when L_{sps} is shorter and L_{sj} is longer. However, this monotonic approach cannot optimize the devices because source-side doping penetrates greatly into the channels and thus increases the SCEs. Thus, it is needed to use other approach, rather than device physics or correlation analysis, in order to optimize the vertical NWFETs.

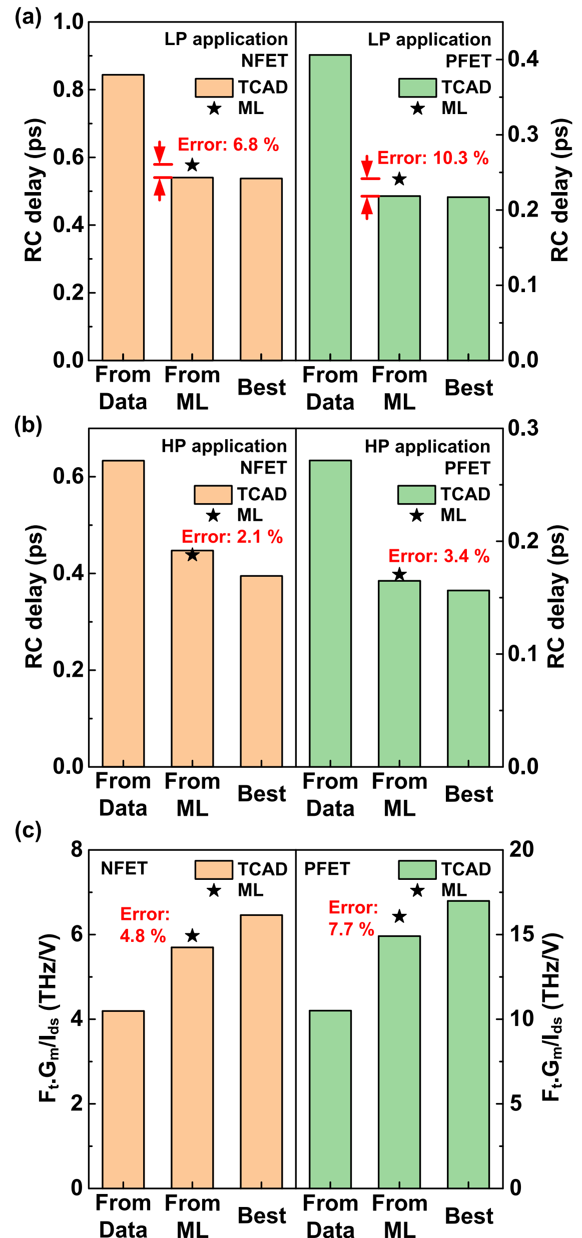

FIGURE 4. (a) RC delay for LP, (b) RC delay for HP applications, and (c) RF FoM of n-type (left) and p-type (right) NWFETs from datasets, ML estimation, and the best one within the input parameter ranges.

B. PERFORMANCE OPTIMIZATION USING ML APPROACH

Errors of RC delay and RF FoM between datasets and prediction, averaged from 100 networks, are smaller than 5 % (not shown), providing that ML accurately predicted RC delay and RF FoM. Computation times for prediction and optimization per network are about 10 seconds each.

Fig. 4 shows the output parameters of n-type and p-type NWFETs from datasets, ML, and best one within the input

TABLE 3. Input parameters predicted by ML and having the best performances.

Input par.	N-type						P-type					
	(L) RC delay		(H) RC delay		RF FoM		(L) RC delay		(H) RC delay		RF FoM	
	Pred.	Best	Pred.	Best	Pred.	Best	Pred.	Best	Pred.	Best	Pred.	Best
L_g	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0
D_{nws}	7.0	7.0	7.0	8.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0
D_{nwd}	10.0	9.0	13.0	11.0	9.0	7.0	9.0	8.0	12.0	10.0	8.0	7.0
L_{sps}	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0
L_{spd}	10.0	10.0	10.0	10.0	14.0	10.0	10.0	10.0	10.0	10.0	15.0	10.0
T_{ox}	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
N_s	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	10^{20}	$2\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	10^{20}	$2\cdot10^{20}$
N_d	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$	$4\cdot10^{20}$
L_{sj}	9.0	10.0	13.0	10.0	12.0	10.0	10.0	10.0	12.0	10.0	12.0	10.0
L_{dj}	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5

* The parameters which are not matched between ML and the best are underlined

parameter ranges in Table 1. ML predicts the devices having better performance than those in the datasets. Errors are smaller when predicting RC delay of n-type NWFETs for HP application because the output ratio ($output_{max}/output_{min}$) from the datasets is small [16]. This factor means the difference of the output parameters used for ML because the output parameters are logged on the RC delay and the RF FoM. For example, the output range of RC delay (LP) is 676.9 for n-type (838.3 for p-type), whereas that of RC delay (HP) is 225.5 for n-type (366.2 for p-type) and that of RF FoM is 445.4 for n-type (800.8 for p-type). More datasets, whose input parameters are different from those in the current datasets, are needed to reduce the error between ML and TCAD, especially for RC delay (LP). Best performances are obtained by fine-tuning the input parameters with respect to those predicted by ML. Input parameters except N_s and N_d are tuned to an interval of 1 nm. N_s and N_d are tuned to an interval of 10^{20} cm^{-3}. P-type NWFETs have greater performances than n-type NWFETs because the p-type devices used for calibration have larger I_{on} and G_m [31], [32].

Table 3 summarizes the input parameters predicted from ML and those having the best performance. The input parameters which are not accurately predicted by ML are underlined. The best input parameters are slightly deviated from those predicted by ML because the datasets are not densely populated near the optimum enough to train ML and to predict the best input parameters accurately. Most of the input parameters are predicted well at the boundaries: L_g of 15 nm, D_{nws} of 7 nm, L_{sps} and L_{spd} of 10 nm, T_{ox} of 1 nm, and L_{dj} of 2.5 nm/dec. N_s and N_d are $4\cdot10^{20}$ cm^{-3} for minimum RC delay, but the N_s is $2\cdot10^{20}$ cm^{-3} for maximum RF FoM. N-type and p-type NWFETs have almost the same input parameters having the best performances, explaining that the optimum device structures are irrespective of the intrinsic device performances such as mobility and velocity calibrated to Samsung NWFETs [18].

Fig. 5 shows the device structures having the best digital or analog performances. All the devices have shorter L_{dj} than the L_{sj}, having the channel junctions near the drain.

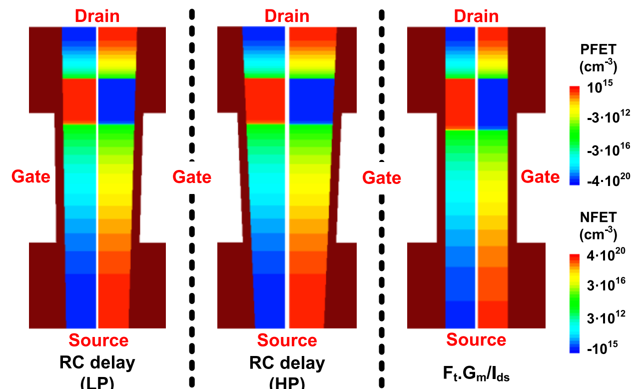

FIGURE 5. Device structures having the minimum RC delay or maximum RF FoM.

All the devices have underlapped drain regions which neglect gate-induced drain leakage currents and thus increase I_{on}/I_{off} ratio [25], [26], [33]. D_{nwd} are larger than D_{nws} for digital applications, but both D_{nws} and D_{nwd} are same as 7 nm for analog applications. That is going to be discussed in the following sub-section.

C. PERFORMANCE ANALYSIS WITH RESPECT TO THE BEST DATA

The input parameters are varied each to understand how they affect the RC delay and the RF FoM. Firstly, it is clear that shorter L_g and thinner T_{ox} increases the DC performances (I_{on} and G_m) and thus RC delay and RF FoM as long as the small SCEs are maintained. All the following figures are about n-type NWFETs, but p-type NWFETs show almost exactly same device physics as n-type ones and thus are not shown in this work.

Fig. 6 shows the I_{on} and C_{gg} variations with respect to D_{nws} and D_{nwd} of n-type NWFETs for HP application. C_{gg} increases at constant rate, but I_{on} increases at smaller rate because the SCEs degrade as either D_{nws} or D_{nwd} increases [33]. But the best RC delay is formed at the D_{nwd} of 11 nm which is larger than the D_{nws} of 8 nm. D_{nws} greatly impacts on the SCEs than D_{nwd} because the top of energy

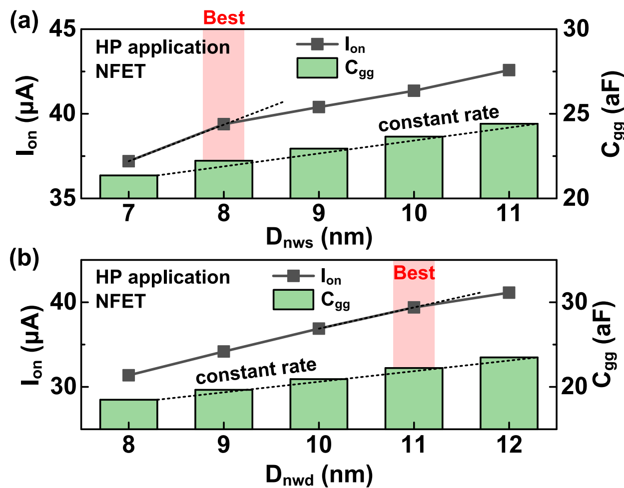

FIGURE 6. (a) D_{nws} and (b) D_{nwd} dependences of I_{on} and C_{gg} of n-type NWFETs for HP application. The devices having the minimum RC delay are also indicated.

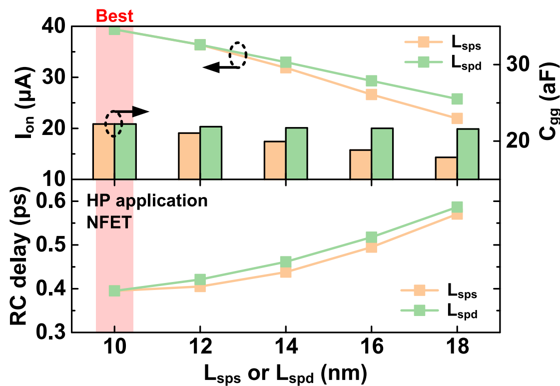

FIGURE 7. I_{on} and C_{gg} variations of n-type NWFETs as a function of L_{sps} or L_{spd} for HP application. The devices having the minimum RC delay are also indicated.

barrier is formed near the source. Larger D_{nws} or D_{nwd} reduces the R_{sd} but degrades the SCEs instead. RC delay is determined by the SCEs rather than the on-state performances under the small V_{dd} of 0.70 V [23]. So, small D_{nws} enough to maintain good gate electrostatics is preferred.

Fig. 7 shows the I_{on} and C_{gg} variations of n-type NWFETs with respect to L_{sps} or L_{spd} for HP application. L_{sps} varies I_{on} and C_{gg} much greatly than does L_{spd}. The source-side regions reside larger amounts of inversion carriers whereas the inversion carriers at the drain-side regions are depleted by high V_{ds} equal to V_{dd}, so the large portion of C_{gg} is gate-source capacitance (C_{gs}). Since longer L_{sps} underlaps the device much, C_{gs} and thus C_{gg} decrease greatly. But this underlapped device loses the amount of inversion carriers flowing from source to drain, so the I_{on} decreases as well. But overall, RC delay variations as a function of L_{sps} and L_{spd} are not different much.

Fig. 8a shows the I_{on} and C_{gg} variations as a function of L_{dj}. Longer L_{dj} increases the drain-side overlap regions, C_{gd}, and thus C_{gg}. Although L_{dj} does not affect the SCEs (not shown),

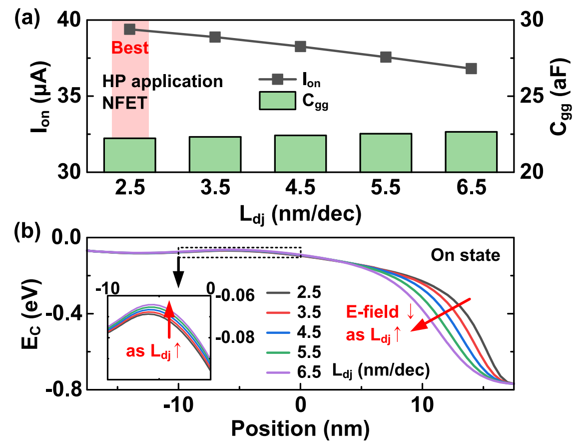

FIGURE 8. (a) I_{on} and C_{gg} variations of n-type NWFETs as a function of L_{dj} for HP application and (b) Conduction band energy at the center of n-type NWFETs at on state.

I_{on} decreases by smaller electric field near the drain (Fig. 8b). Smaller lateral electric field, induced by much gradual drain junction (= longer L_{dj}), decreases carrier velocity near the drain. L_{dj} from 10 to 18 nm varies the energy barrier about 4 meV, which is smaller than thermal voltage (25.9 mV at 300 K) and is not effective. I_{on} and C_{gg} variations as a function of L_{sj} are similar to the previous studies in FinFETs [23], [24], [26]; longer L_{sj} degrades the SCEs and increases the C_{gg}, but shorter L_{sj} loses the amount of inversion carriers at on state (not shown). Thus, there is an optimum L_{sj} at 10 nm/dec.

To achieve high RF FoM, the devices should have high G_m. So, $F_t G_m/I_{ds}$ is maximum in the saturation region where the maximum G_m is formed. As L_{sps} or L_{spd} increases, all the factors (F_t, G_m, I_{ds}) decrease, and RF FoM decreases (not shown). RF FoM as a function of L_{sj} and L_{dj} is explained similarly as RC delay. Longer L_{dj} decreases F_t by larger C_{gg} and decreases transconductance efficiency (G_m/I_{ds}) by smaller electric field, thus decreasing RF FoM. There is a trade-off between F_t and G_m/I_{ds} as a function of N_s and L_{sj}, so the maximum RF FoM is formed at the N_s of $2{\cdot}10^{20}$ cm^{-3} and the L_{sj} of 10 nm/dec.

Fig. 9 shows G_m/I_{ds}, F_t, and RF FoM of n-type NWFETs with respect to D_{nws} and D_{nwd}. P-type NWFETs have the same device characteristics as n-type ones. Considering velocity saturation for nanoscale devices, I_{ds} and G_m are simplified as [34],

$$I_{ds} = v_{sat} Q_n = v_{sat} W C_{ox} (V_{gs} - V_{th}) \quad (3)$$

$$G_m \equiv \frac{dI_{ds}}{dV_{gs}} = v_{sat} W C_{ox} \quad (4)$$

where v_{sat} is carrier velocity, Q_n is carrier density, W is device width, C_{ox} is oxide capacitance, V_{gs} is gate-source voltage, and V_{th} is threshold voltage. According to the eqs. (3) and (4), G_m/I_{ds} is given by $1/(V_{gs} - V_{th})$. Since D_{nws} than D_{nwd} affects the SCEs much, it decreases V_{th} and thus G_m/I_{ds}. Larger D_{nws} decreases G_m/I_{ds}, F_t, and thus RF FoM greatly. On the other hand, D_{nwd} from 7 to 9 nm maintains high RF FoM because F_t increases despite the decrease of G_m/I_{ds}. The reason that

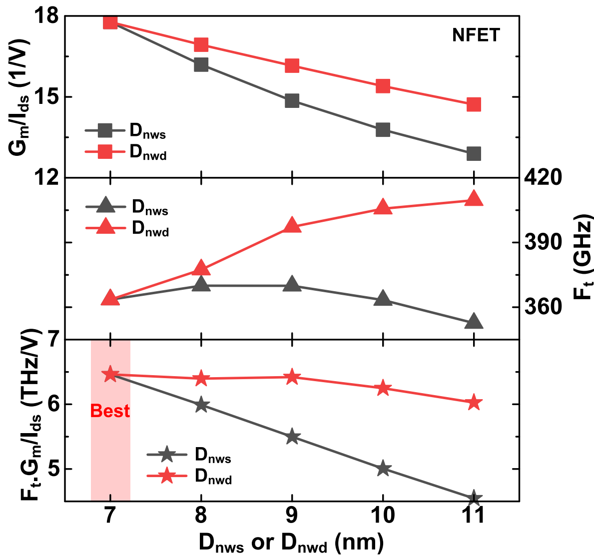

FIGURE 9. G_m/I_{ds}, F_t ($= G_m/2\pi C_{gg}$), and RF FoM ($= F_t \cdot G_m/I_{ds}$) of n-type NWFETs with respect to D_{nws} and D_{nwd}.

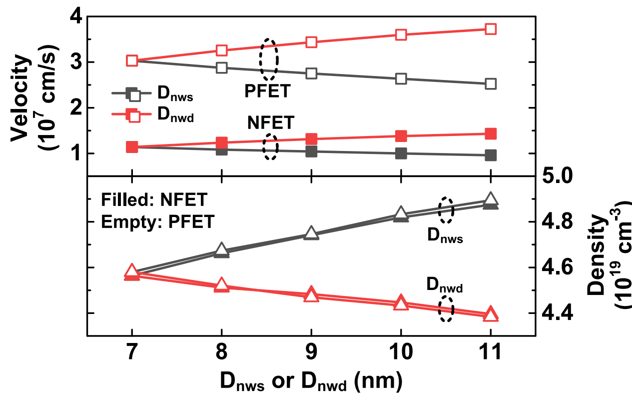

FIGURE 10. Carrier velocity and density of n-type NWFETs with respect to D_{nws} and D_{nwd} at the maximum RF FoM.

larger D_{nwd} increases F_t is because the increasing rate of G_m is greater than that of C_{gg}. Larger D_{nws} increases G_m as well, but it is not large enough to increase F_t.

The difference of RF FoM between D_{nws} and D_{nwd} can be understood by v_{sat} and Q_n with respect to D_{nws} or D_{nwd} (Fig. 10). v_{sat} and Q_n are calculated by averaging the NW channel at maximum RF FoM [35]. For both n- and p-type devices, larger D_{nws} (D_{nwd}) increases Q_n (v_{sat}) but decreases v_{sat} (Q_n). Larger D_{nws} supplies more amount of inversion carriers, whereas larger D_{nwd} lessens the gate-to-drain coupling and expands the channel regions where high lateral electric field is formed, inducing high average v_{sat}. According to eq. (4), G_m is proportional to v_{sat}, but not directly related to Q_n. Using eq. (3), Q_n is represented as $WC_{ox}(V_{gs} - V_{th})$, but because larger D_{nws} increases $V_{gs} - V_{th}$, WC_{ox} increase is compensated by larger $V_{gs} - V_{th}$. Therefore, D_{nwd} increases G_m much compared to D_{nws}.

IV. CONCLUSION

Vertical NWFETs are optimized for digital and analog applications using fully-calibrated TCAD and ML approach. Neural network adopted fully-connected MLP with one hidden layer having 20 nodes and *tanh* as an activation function. ML accurately predicted the input parameters which minimize the RC delay or maximize the RF FoM. Each of the input parameters were varied to understand the device physics of vertical NWFETs and to validate ML optimization results. All the predicted NWFETs have smaller D_{nws} to reduce the SCEs by tightly controlling the energy barrier. Smaller L_{dj} and larger D_{nwd} also increase the v_{sat} by larger lateral electric field, but too large D_{nwd} loses the gate-to-channel controllability. Longer L_{sps} and L_{spd} decrease both I_{on} and C_{gg}, but the I_{on} decreases much and thus RC delay increases. Therefore, ML-based optimization is feasible, fast, and effective to provide device design guideline for both digital and analog applications.

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