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Ultra-Low Power Oscillator Collapse Physical Unclonable Function Based on FinFET

AMIN A. ZAYED[1], HANADY HUSSEIN ISSA[2], KHALED A. SHEHATA[2], AND HANI FIKRY RAGAI[1]

[1]Department of Electronics and Electrical Communication Engineering, Faculty of Engineering, Ain Shams University, Cairo 11566, Egypt
[2]Department of Electronics and Communications, Arab Academy for Science, Technology and Maritime Transport, Cairo 11799, Egypt

Corresponding author: Hanady Hussein Issa (hanady.issa@aast.edu)

ABSTRACT The main purpose of this paper is to achieve ultra-low power Physical Unclonable Function (PUF) to meet the requirements for Internet of Things (IoT) applications. PUFs are promising hardware security primitives that are based on the uniqueness and the unclonability of the device's physical characteristics to provide a unique identifier for devices. PUFs can be used in device authentication and for secure key storage and generation. This paper presents Oscillator Collapse Physical Unclonable Function (OC-PUF), which is suitable for low power applications. The power consumption is reduced based on designing the most power-hungry modules in the OC-PUF. An Oscillator Collapse (OC) is designed to work in the near-threshold voltage region, which reduces the power consumption. More power reduction is achieved by designing a new Collapse Time Comparator (CTC). Due to the process variations, the oscillations period of each OC is different. The CTC generates the output response bit by comparing the oscillations periods of the two selected OCs. The simulation results demonstrate that the proposed OC-PUF can effectively reduce the power consumption. The proposed PUF is designed using 20 nm triple gate FinFET technology. The Simulation results for 1000 different chips with the same input challenge, show that the average power is 140 nW, with the worst case being 740 nW. The best case is 63 nW per challenge-response pair at supply voltage 0.5 V. The averaged reliability of the OC-PUF is 99.8%, at temperatures from −40 to 125 °C and supply voltage 0.5 ± 10%. The proposed OC-PUF decreases the power consumption while retaining high-performance metrics.

INDEX TERMS Authentication, hardware security, low power consumption, process variation, reliability, transient effect of ring oscillator.

I. INTRODUCTION

The Internet of Things (IoT) mostly describes a network where all the devices are associated with the internet [1]. The IoT is one of the focuses of research topics because of the numerous advantages and the significant impact it can have on our life [2]. Now, the devices at home can communicate with each other, and people can control the components in a house with their smartphones. Security and protection are significant issues in IoT technology. Cryptographic techniques may not be suitable for some IoT devices which have energy constraints [2]. These algorithms consume a large amount of power, and they are subject to many types of attacks, like semi-invasive attacks [1].

Physical unclonable functions (PUFs) are a security solution for low power applications [3]. They can be used to generate a secret key and device authentication. PUF is a circuit that produces a unique and unpredictable output, which depends on the unique characteristics of the physical hardware [4]. PUF circuit exploits the manufacturing process variation to form a random function between its input and output [5]. These process variations can occur at any step of the fabrication process, such as photolithography, oxidation, or implantation. Due to these manufacturing variations, the device's parameters are influenced, which causes changes in the device output [6]. PUFs are designed to amplify the physical variations to provide a hardware unique function. The PUF input is named the challenge while the output is named the response, and both are known as challenge-response pair (CRP). For the PUF, it is required to generate the same response for the same challenge and generate a new response for each challenge. In literature, many architectures of PUFs have been proposed and implemented, such as Ring Oscillator PUF (RO-PUF) [6]–[9], Arbiter PUF [10], [11],

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Transient Effect Ring Oscillator PUF (TERO-PUF) [12]–[15], and SRAM PUF [16]–[19]. The Arbiter PUF is delay-based. It employs a signal on two identically implemented delay lines which end with an arbiter circuit. The arbiter circuit generates logic '1' if the first path is faster than the second one. Otherwise, it gives logic '0'. It is not easy to implement a fully symmetric Arbiter PUF on FPGA [6]. The RO-PUF has been proposed by Lee [20]. It consists of multiple ROs each has an odd number of inverters that are connected in series. The RO-PUF generates its output response by comparing the frequencies of its ROs [21]. RO-PUFs can easily be implemented using both ASICs or FPGAs. Merli *et al.* [22] have used an electromagnetic side-channel analysis to extract the frequencies of ROs and their physical location inside the chip. Therefore, the main security factors of the RO-PUF, which are hiding the RO-PUF location and its locked frequency are no longer guaranteed. The TERO-PUF uses TERO loops to generate transient oscillations for a small period at the rising edge of the enable signal. These transient oscillations are counted and compared to generate the output response. Unlike the RO-PUFs, the TERO-PUFs output response is based on the number of oscillations rather than locking oscillation frequency [23].

Along with the PUF security requirements, its total power consumption is considered another vital issue. Therefore, numerous PUF structures have been proposed and implanted in the literature to reduce power consumption. A low-power RO-PUF [24] reduces the power consumption by biasing half of the RO inverters in the subthreshold region. In order to achieve more power reduction, only one RO is active. The bulk-controlled oscillator PUF (BCO-PUF) [25] replaces the counters and the comparator utilized in the RO-PUFs, which consume a lot of power, along with a phase/frequency detector to reduce the power consumption. Another low-power RO-PUF [26] uses a diode-clamped inverter instead of the regular inverter to reduce the power consumption. The Dopingless Field-Effect Transistors (DLFET) RO-PUF is proposed in [27]. The DLFET decreases the leakage current, which reduces the total RO power consumption. This PUF generates its output response by sensing the first rising edge of the two selected ring oscillators. Therefore, the PUF output key may be unreliable. The ring oscillator collapse PUF (ROC-PUF) is proposed by Yoo *et al*. in [28]. The ROC-PUF uses the oscillator collapse (OC) to generate the oscillations instead of the conventual RO. The OC is composed of two identical branches. Each branch consists of an activation gate (AND gate, or NAND gate) and n-number of inverters. When the enable signal goes high, the OC starts to oscillate for a short period, and then its output collapses at either logic '0' or logic '1'. The multiple-valued PUF (MPUF) is proposed by Zhang *et al.* in [29]. It extends the hardware efficiency by processing multiple values per one operation. The capacitive PUF (CPUF) is proposed by Kamal *et al.* in [30]. The CPUF uses one frequency oscillator to drive eight frequency dividers, with each driver connected to a counter. The role of the challenge bits is to control the eight comparators that control the counters to generate the output response bits. An arbiter PUF with high-temperature stability is proposed in [31]. The delay lines are implemented using current-starved (CS) inverters to reduce the power consumption. A cascode current mirror array PUF is proposed in [32]. Each PUF cell consists of a single-stage cascode amplifier. Accordingly, the cell output impedance increases, which improves the reliability against temporal noise. A weak PUF is proposed in [33] which utilizes only cross-coupled NMOS transistors to create the PUF cell. Each cell consists of four NMOS transistors to reduce the process size. The PUF can produce a 128-bit key length in one clock cycle. Other ultra-low power PUFs have been proposed in [34]–[37].

In this paper, we propose a new FinFET based Oscillator Collapse Physical Unclonable Function (OC-PUF). Our contributions in this paper are as follows:

- The proposal of a new OC-PUF consumes less power while maintaining high reliability against both supply voltage and temperature variations.
- The proposed OC design operates in the near-threshold voltage region, reducing the drain current and reducing power consumption. It consumes less power than both traditional ROs and TEROs.
- Designed a collapse time comparator (CTC) module and replaced the power-hungry circuits (counters and comparator) in the traditional PUF with it. The proposed CTC module consumes less power than the traditional ones. It generates the output response based on the oscillations time.
- The simulation results show that the proposed OC-PUF consumes 740 nW to produce one output response bit. The OC-PUF consumes the least power compared to other designs in the literature. As a result, the OC-PUF is suitable for secure chip authentication ultra-low power applications.

The rest of this paper is organized as follows; Section II describes the background of a conventional RO-PUF and TERO-PUF. Section III explains the proposed OC-PUF. Simulations and results of OC-PUF are presented in section IV. Finally, section V concludes the paper.

II. BACKGROUND

This section discusses the main features of conventional RO-PUF and TERO-PUF.

A. CONVENTIONAL RO-PUF

The first RO-PUF was proposed in [12]. It consists of multiple ring oscillators; each oscillator composes of an odd number of inverters whose last output feeds back to its first input gate as shown in Fig. 1. The basis of the oscillation is the instability of the inverters due to the odd number of inverter stages. Owing to this property, the RO oscillates with a period proportional to the total propagation delays of each inverter [38]. The manufacturing process variation is the main factor that causes changes in the oscillation frequency of each RO [8]. The ring

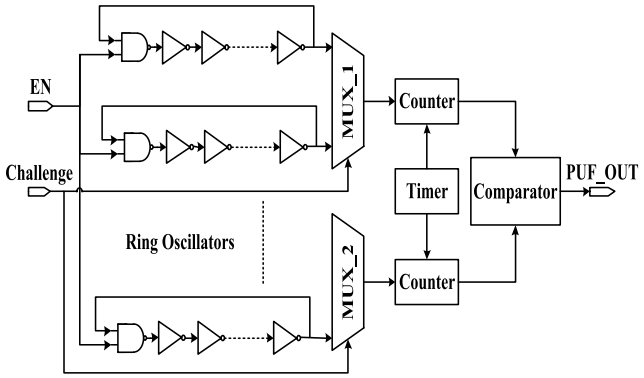

FIGURE 1. Basic RO-PUF.

oscillator's outputs feed two multiplexers, which pass only two selected frequencies based on the given challenge. The two counters count the number of oscillating signals in a fixed interval time. Finally, the comparator module generates logic '1' if the first frequency is higher than the second one. Otherwise, it generates logic '0'. The RO-PUF has some drawbacks, such as the ROs frequencies and ROs location on the chip can be retrieved using electromagnetic analysis [22].

B. TERO-PUF

The TERO-PUF was first proposed in [6]. It generates the output response bit by subtracting the number of oscillations of two identically implemented TEROs. The TERO-PUF proposed in [23] is shown in Fig. 2. It consists of two blocks, and each block has n numbers of TERO, two demultiplexers, two multiplexers, two counters, and a subtractor. According to the input challenge, the two demultiplexers pass the signals from one TERO per block. Afterward, the multiplexers drive the two selected TEROs output to the two counters that count the total number of oscillating signals. Finally, the outputs of the counters are sent to a subtractor, which generates logic '1' if the first number of oscillations is higher than the second one otherwise it gives logic '0'. The activation time of the enable signal (EN) must be larger than the oscillations time of any TERO [23].

The TERO loop composes of two identical branches B1 and B2 as shown in Fig. 3. Each branch consists of an AND gate and even number of inverters. The two branches have the same number of inverters. The TERO loop starts oscillating when EN signal goes high. Accordingly, the two electrical events begin to propagate in both branches [39]. Depending on the mismatch between these branches, these events propagate with different delays. The TERO loop oscillation stops when the two branches collapse due to the propagation delay of the event. This behavior results in a finite number of oscillations of the TERO loop output [39]. As a result, the number of oscillations and the final stable state of each TERO is different due to the process variation.

III. PROPOSED OSCILLATOR COLLAPSE PUF DESIGN

In this paper, we proposed a FinFET based oscillator collapse PUF that aims to reduce the total power consumption.

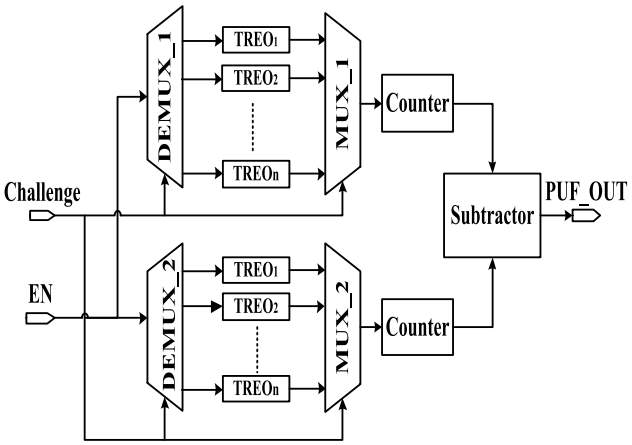

FIGURE 2. TERO-PUF architecture.

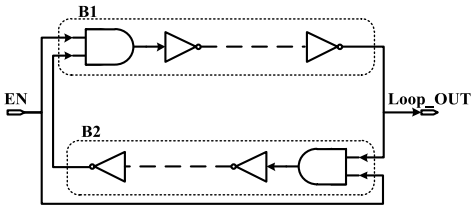

FIGURE 3. The TERO loop structure.

Fig. 4 shows the schematic of the proposed OC-PUF, which includes two demultiplexers (DEMUX-A, DEMUX-B), m-OR gate, m-oscillators collapse (m-OC), two multiplexers (MUX-A, MUX-B), and a CTC. In the RO-PUF, the ROs are the major components that consume considerable high power. Therefore, in the proposed OC-PUF, we introduced a new oscillator collapse structure to consume less power than traditional ROs and TEROs. To achieve more power reduction, we replaced the power-hungry circuits (counters and subtractor) in TERO-PUF with the proposed CTC module.

The OC-PUF starts its operation when the input EN signal goes high for a short time, which is called the activation time (AT). According to the challenge input signal, the demultiplexers pass the EN signal to the m-OR gate. Each OR gate has two inputs, one from DEMUX-A and the other one from DEMUX-B. As a result, only two OR gates will pass the EN signal and the others will not. The OR gates role is to ensure that the enable signal will drive only the randomly selected OCs. The two selected OCs will oscillate for a short period before collapsing and then their outputs go high. The oscillations period of each OC, which is referred to as oscillations time (OT) is different due to the manufacturing process variation [23]. The OCs outputs feed MUX-A and MUX-B, which pass only the output of the two selected OCs based on the given challenges. The two multiplexers then drive the CTC circuit, which compares the OT for the selected OCs. Finally, the CTC module generates logic '1' if the OT of UP signal is greater than the OT of DN signal otherwise it gives logic '0'. The following subsections describe the proposed core modules of OC-PUF.

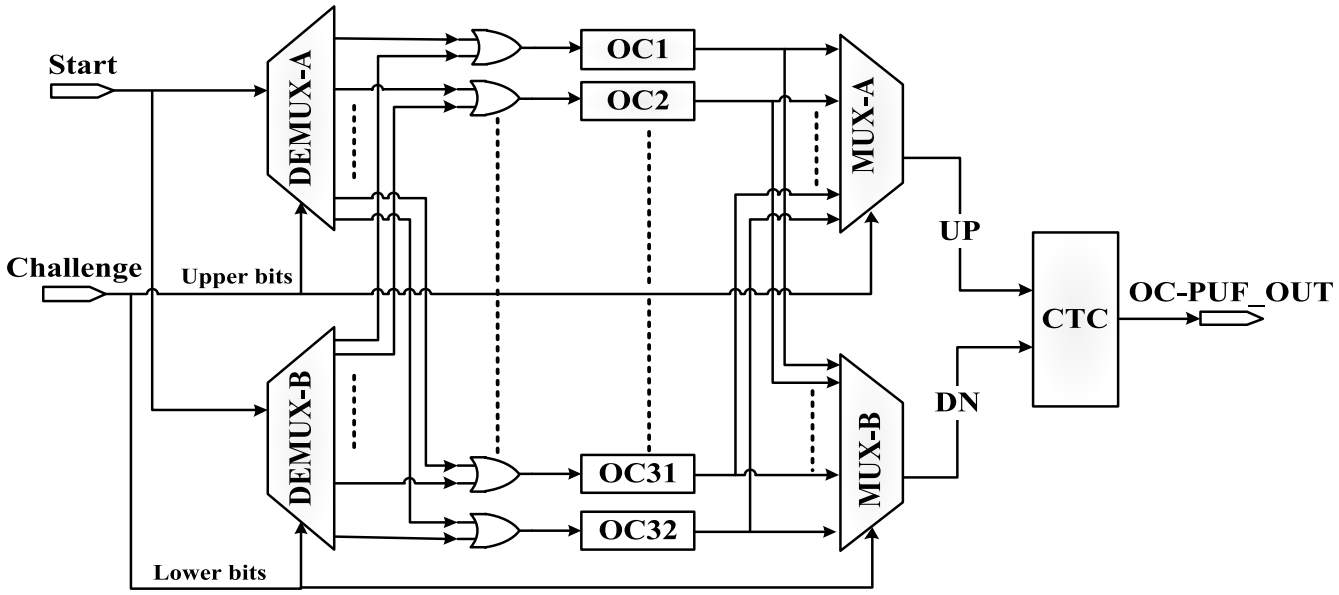

FIGURE 4. Proposed OC-PUF.

A. OSCILLATOR COLLAPSE (OC)

The OC module is considered as a specific configuration of RO, whereas the number of inverters is even. The OC is composed of two identical branches. Each branch consists of an activation gate (AND gate, or NAND gate) and an n number of inverters. The OC has two functioning modes, an oscillation mode followed by a stable state mode [39]. In order to choose the number of inverters for the proposed OC, we designed five different OCs with different number of inverters. The five designed OCs compose of 4, 6, 8, 10, and 12 inverters. The power consumption and the reliability are the main factors considered to choose one of these OCs. Each OC design utilizes two NAND gates as activation gates. The simulations show that the OC with eight inverters and two NAND gates consumes acceptable power, while maintaining high reliability against temperature and VDD variations. Therefore, the OC which consists of eight inverters and two NDND gates is selected. To improve the function of the selected OC design, we performed three different modifications. Fig. 5 shows the proposed OC. These modifications involve the addition of 8 inverters, 3 NAND gates, and ten loading capacitors. The first modification is performed on the OC loop as shown in Fig. 5 (a). The output of the OC is affected by the process variations in three ways, the oscillations period, the oscillation frequency, and the final stable state of the output signal which is either 0 V (GND) or power supply voltage (VDD) [41]. To compare the OTs of the OCs in our design, the final stable state output must be constant at VDD. Consequently, we added an N3 NAND gate to the OC circuit that is fed by the two branches B1 and B2. As the final stable state outputs of B1 and B2 branches are opposite to each other, the N3 NAND gate final state output will be kept at VDD.

The second modification performed to reduce the dynamic power consumption of the OC circuit was done by utilizing a current starved inverter which is proposed in [40]. This inverter was modified by adding one p-type transistor at the top and one n-type transistor at the bottom of the regular inverter circuit, as shown in Fig. 5 (b). The main role of these transistors is to guarantee that the inverter operates in the near-threshold region by adjusting the bias voltages Vp and Vn. Hence these transistors limit the current passing in the inverter which reduces the oscillation frequency. As a result, the average dynamic power consumption of the OC is reduced. The bias voltages Vp and Vn are obtained from the voltage divider circuit shown in Fig 5 (c). The third modification was achieved by adding ten identical loading capacitors to the OC circuit. The capacitors are connected at the output of the eight inverters and the two NAND gates output. These capacitors increase the gates delay, which reduces the oscillation frequency of the OC. Accordingly, the power consumption of the following modules (multiplexers and the CTC) can be reduced. Moreover, the robustness to temperature variation is improved by adding these capacitors. The schematic of the NAND gate is shown in Fig. 5 (d).

Fig 6 shows the principle of operation for the proposed OC. When the enable signal EN switches from logic level '0' to logic level '1', two signals begin to propagate in the B1 and B2 branches. Due to the process variations, the duty cycle of one branch drops to 0%, and the other rises to 100% [42]. The OC will oscillate until the duty cycle is less than any inverter delay causing the OC to stop oscillating. As shown in Fig. 6, the duty cycle in branch B2 increases until the signal off-time becomes less than the delay of one of its inverters. Currently, the OC enters the final stable state and the OC output (OC_OUT) settles at VDD.

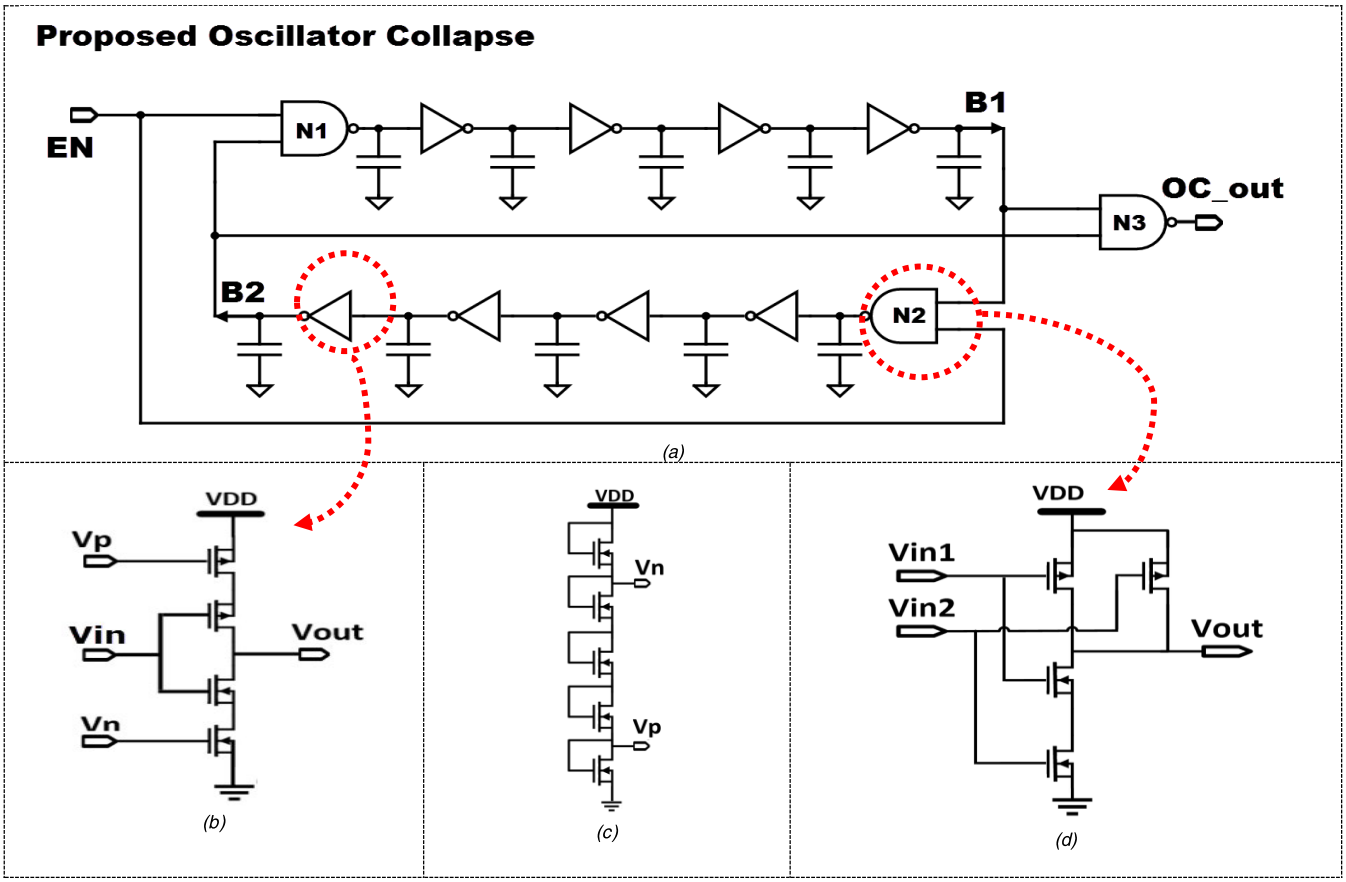

FIGURE 5. Schematic of (a) the Proposed Oscillator Collapse, (b) inverter, (c) Bias circuit, and (d) NAND gate.

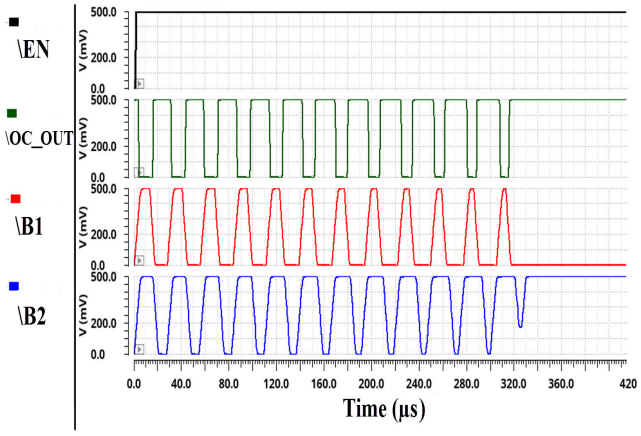

FIGURE 6. Oscillator collapse simulation output.

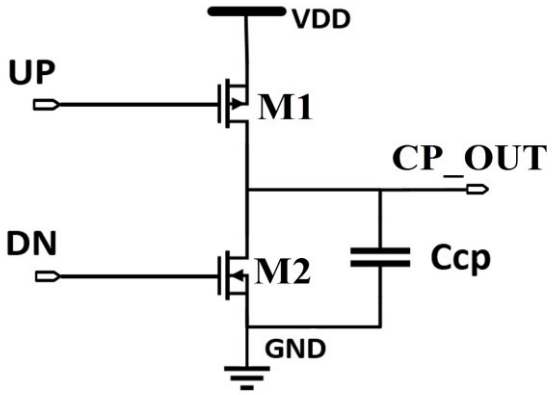

FIGURE 7. Charge Pump circuit [43].

B. COLLAPSE TIME COMPARATOR (CTC)

The function of the proposed CTC circuit is to compare the OT of the two selected OCs and afterward generate the output response bit. It receives the UP and DN signals from MUX-A and MUX-B, respectively as shown in Fig. 4. The CTC produces logic '0' when the UP signal reaches the final stable state and the DN signal still oscillating, otherwise, it generates logic '1'.

To design the CTC circuit, we modified the conventional Charge Pump (CP) circuit in [43] to meet our design requirements. A conventional CP circuit consists of a capacitor (Ccp), N-type transistor (M1), and P-type transistor (M2), as shown in Fig. 7 [43]. The circuit can operate in four different modes, according to the input signals UP and DN. The first mode occurs when both UP and DN signals are low, thus allowing the two transistors M1 and M2 to be ON and OFF, respectively. In this case, CP output (CP_OUT) is equal

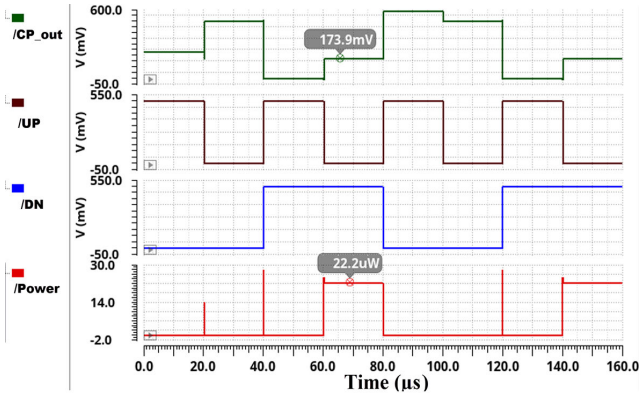

FIGURE 8. Charge Pump output signal and the instantaneous power.

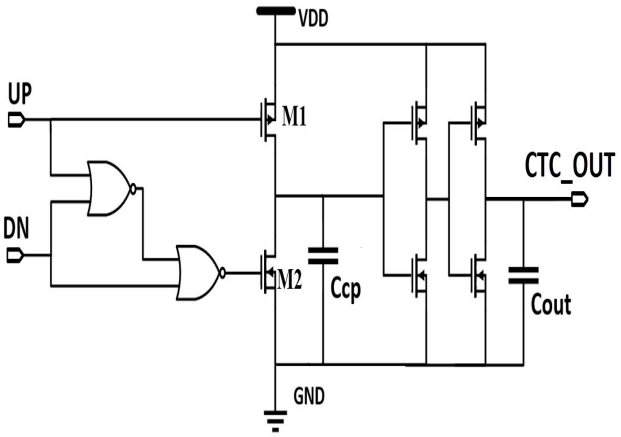

FIGURE 9. Proposed Collapse Time Comparator (CTC).

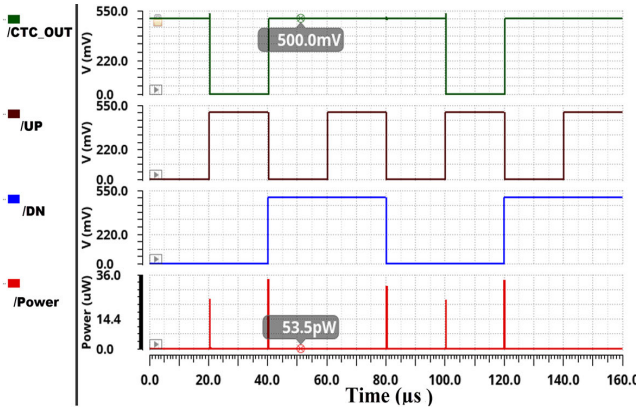

FIGURE 10. CTC output signal and its instantaneous power.

to VDD because the capacitor Ccp is directly charged from the voltage source VDD. The second mode takes place when the input signal UP is high and the input signal DN is low. In this case, both M1 and M2 transistors are OFF, and hence the Ccp keeps its charges. Consequently, CP_OUT is the same as the previous state. The third mode occurs when both signals DN and UP are high, the transistor M1 is OFF and M2 is ON. The Ccp is directly connected to the ground and begins to discharge. Therefore, the output signal CP_OUT equals to GND. The fourth mode occurs when the UP and DN input signals are low and high respectively, hence both M1 and M2 are ON. This results in a short circuit between the voltage source and the ground, which consumes a large power from the supply. The capacitor Ccp charges or discharges to the same voltage across M2. Fig. 8 illustrates the simulation results of the CP circuit in all modes of operation and circuit power consumption.

The second and third modes of the CP circuit must be modified to produce the required outputs. In the CP fourth operation mode, where both M1 and M2 are ON, the power consumed is high as shown in Fig. 8. To overcome these issues and reaches the desired requirements, two NOR gates were added at the input of the M2 transistor as shown in Fig. 9. In the second mode, the CTC output is adjusted by GND (Cp discharge), instead of no change in the CP. The final value of UP and DN signals equal to VDD, then the third mode must be the last one to take place to keep the output constant. Therefore, the CTC third mode is adjusted to keep its previous state instead of GND in the CP. In the CTC fourth mode, M1 is ON, M2 is OFF, and the Ccp is charging. Hence, the instantaneous power in the CTC fourth operation mode is reduced. The instantaneous power of the CTC circuit for all operation modes is shown in Fig 10. The CTC circuit consumes around 54 pW in the fourth mode of operation which is much lower than the CP circuit's consumed power.

The proposed CTC provides its output based on which of UP and DN signals can reach the final stable state first. If the UP signal enters the stable state first, the CTC must generate its output bit before the DN signal enters the stable state. Consequently, the time required by the CTC to produce the output must be as small as possible. However, the time required by CTC to produce the output response depends on the Ccp charge/discharge time. Therefore, the Ccp charge/discharge time must be small. There are two ways to reduce the Ccp charge/discharge time, either by using a small value for the Ccp capacitor or by increasing the charging current. In the proposed circuit, we used a small value for Ccp and increased the transistors drain current. To achieve the latter, the number of Fin for M1 and M2 transistors is increased. The simulations show that the proposed CTC can generate the output bit even if the time difference between the UP and DN signals to reach the final stable state is 10 ps. Due to the small value of Ccp, it cannot keep the charges on it for the AT. Therefore, an output stage is added to keep the CTC output (CTC_OUT) constant over the AT. It consists of two successive inverters followed by a capacitor (Cout) with a higher value than Ccp. The Cout can maintain the output voltage constant for the time required by the OC-PUF to produce the output response bit.

Table 1 shows the results for the CP and CTC circuits in the four operation modes. As shown, the first mode output is the same in the CP and CTC circuits. The second and the third modes switch the CP and CTC outputs between each other.

TABLE 1. Charge Pump and Collapse Time Comparator.

Mode	UP	DN	CP		CTC	
			Ccp	CP_OUT	Ccp	CTC_OUT
First	0	0	Charge	VDD	Charge	VDD
Second	1	0	Previous state	Previous state	Discharge	GND
Third	1	1	Discharge	GND	Previous state	Previous state
Fourth	0	1	Forbidden state	VDD/3	Charge	VDD

In the fourth mode, the CTC circuit output is VDD instead of VDD/3 in the CP circuit.

IV. SIMULATION RESULTS AND COMPARISON

The proposed OC-PUF circuits are designed using North Carolina State University (NCSU) PDK [44]. All the simulations are based on the Predictive Technology Model (PTM) provided by Arizona State University (ASU). The model files for 20 nm triple gate bulk FinFET Low-Standby Power (LSTP) technology are used. Cadence Spectre is used for simulations. The nominal operating condition is VDD = 0.5 V at 27 °C. Table 2 shows the nominal values of the parameters which are applied during the simulations. The variation in gate length, Fin height, Fin thickness, oxide thickness, and doping parameters all affect the threshold voltage (VT) [45]. In the simulation, the variation in the threshold voltage is considered as the main factor of manufacturing process variation.

The proposed OC-PUF consists of 32 identical OCs that generates a 64 bits long key. It is verified by applying the most common performance metrics which are uniqueness, reliability, and uniformity. For evaluation purposes, 1000 different PUF chips are emulated by running Monte-Carlo simulations 1000 times. The threshold voltage parameter is varied with a 5% standard deviation of the mean value [46]. The supply voltage and temperature variations are also considered in the simulations. The simulation results are subjected to Matlab program to compute the performance metrics.

A. UNIQUENESS

The PUF uniqueness measures the ability to produce a unique key for different PUF instances with the same challenge at the same environmental conditions. To evaluate the PUF uniqueness U, the average inter-chip Hamming Distance (HDinter) of the output responses from m different PUF instances is calculated by (1) [47].

$$U = \frac{2}{m(m-1)} \sum_{x=1}^{m-1} \sum_{y=x+1}^{m} \frac{HD(R_x, R_y)}{n} \times 100\% \qquad (1)$$

where, HD (R_x, R_y) denotes the Hamming distance between the responses R_x and R_y, and x ≠ y. R_x and R_y are the n-bit responses of two different PUF instances, for the same challenge C.

TABLE 2. FinFET Parameters.

Parameter	Value
Gate Length (L_g)	24 nm
Fin Thickness (T_{fin})	15 nm
Fin Height (H_{fin})	28 nm
Oxide thickness (T_{ox})	1.4 nm
Source/Drain Doping (NSD)	$3x10^{26}$ m^{-3}
Fin body doping (N_{BODY})	$5x10^{23}$ m^{-3}

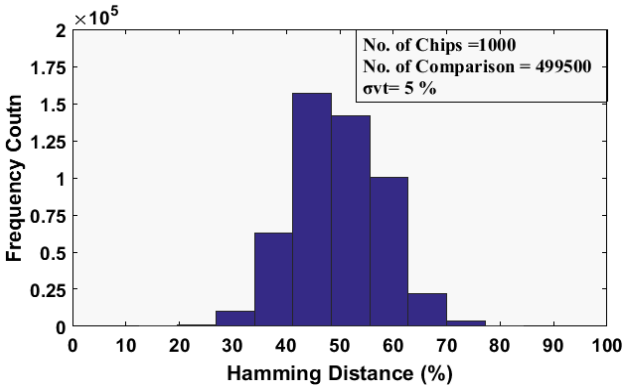

FIGURE 11. Frequency distribution of the OC-PUF Inter Hamming Distance.

Ideally, the uniqueness U between any two responses should be 50%. The simulation is performed on 1000 OC-PUF instances and the results show that the average HD between any two OC-PUF responses is 50.01%, which is akin to the ideal value. Fig. 11 shows that the HDs are concentrated around the ideal value. The simulation results demonstrate that the proposed OC-PUF has significant improvements in the uniqueness performance metric.

B. RELIABILITY

Reliability is the ability of a PUF to generate the same response for the same challenge at varying environmental conditions. To evaluate the reliability R, the average intra-chip Hamming Distance (HDintra) for responses for the same challenge on the same OC-PUF instance is obtained at different temperatures and different supply voltages are calculated. The HD between two responses generated by a PUF for the same challenge at different environmental conditions should be zero. The reliability of the OC-PUF is calculated by (2) [48]:

$$R = \left[1 - \frac{1}{w} \sum_{y=1}^{w} \frac{HD\left(R_x, R_{x,y}\right)}{n} \right] \times 100\% \qquad (2)$$

where w is the number of samples for PUF response, R_x is the response generated from the chip x, n is the number of bits of a response produced by the PUF, and HD (R_x, $R_{x,y}$) refers to

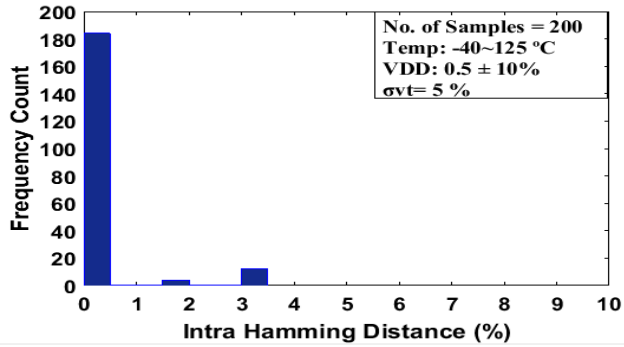

FIGURE 12. Frequency distribution of the OC-PUF Intra Hamming Distance.

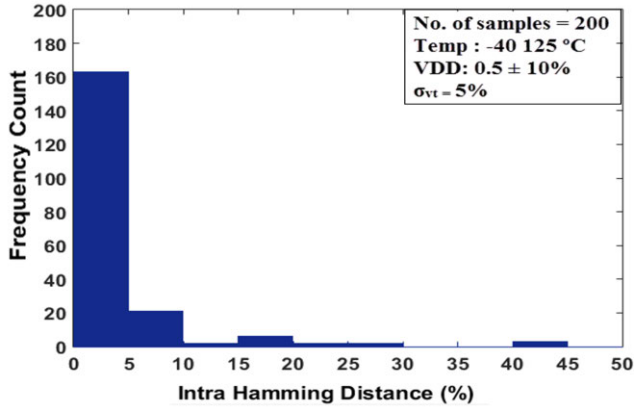

FIGURE 13. Frequency distribution of the OC-PUF Intra Hamming Distance, without using capacitors.

the Hamming distance between the response R_x and the y-th sampling $R_{x,y}$.

The OC-PUF reliability is calculated using the same challenge to generate a total of 200 responses under varying temperatures and supply voltages. 160 responses were generated by varying the temperature from −40 °C to 125 °C with 27 °C as a reference temperature. 40 responses were generated by varying the supply voltage V_{DD} of 0.5 V by ±10%. The simulation results show that the average reliability of OC-PUF is 99.8%, which is close to the akin value. In addition to that, the maximum Hamming distance is 3.1%, the minimum is 0% and the average is 0.2%. Fig. 12 shows the frequency distribution of the OC-PUF Intra Hamming Distance.

We have performed the reliability simulations before adding the 10 capacitors to each OC circuits. The simulation results show that the reliability has been improved from 95.6 % to 99.8% by adding the capacitors. Fig. 13 shows the frequency distribution of the OC-PUF Intra Hamming Distance before adding the capacitors to the OC circuits. The simulation results show that the maximum Hamming distance is 42%, the minimum is 0% and the average is 4.4. As a result, these capacitances contributed to improvement of the OC-PUF reliability against supply voltage and temperature variations.

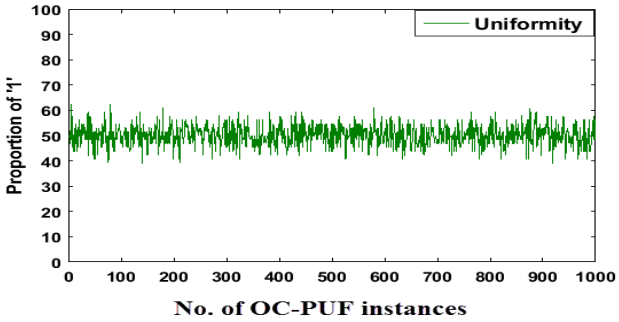

FIGURE 14. Uniformity of the OC-PUF.

C. UNIFORMITY

The uniformity of a PUF can be calculated by getting the average of the proportion of '1's in the PUF responses [49]. The proportion must be around 50% for any response, since any bias towards '1' or '0' makes the PUF secret key not random. The uniformity of OC-PUF is calculated by (3) [49].

$$Uniformity = \frac{1}{z}\sum_{y=1}^{z}\sum_{x=1}^{n}\frac{R_{x,y}}{n} \times 100\% \tag{3}$$

where z is the number of chips, $R_{x,y}$ is a y-th binary bit of n-bit response generated from chip x. The uniformity is calculated using 1000 responses which are generated by 1000 different OC-PUF instances for the same challenge. The OC-PUF uniformity is evaluated and presented in Fig. 14. The simulation results show that the maximum uniformity is 61.5%, the minimum is 39.8%, and the average is 50.08%, which is akin to the ideal value.

D. POWER ANALYSIS

As we discussed before, the OC has two states, oscillation state, and non-oscillation state. In the oscillation state, the OC consumes most of the power resulting from the dynamic power and leakage power. However, the leakage power consumption in the non-oscillation state is considerably low (in the order of Pico Watt). Cadence Virtuoso tool computes the average power for any circuit by calculating the total instantaneous power in the simulation time and then gets the average over that time. Therefore, to compute the average power of the OC, the simulation time must be chosen carefully. In following the simulations, we set the simulation time equal to the AT. The AT of the EN signal must be greater than the maximum OT for any OCs to ensure that all OCs reach the non-oscillation state before performing the comparison operation. To determine the maximum OT, 1000 Monte Carlo simulations are performed to calculate the OT for the 32 OCs. From the simulations, 32000 OTs have been produced. The simulation results show that OC14 has the maximum OT, which is 1.83 μs. Therefore, the AT is set to be 2 μs, which is enough for the OC-PUF to generate a one-bit response. For all the following simulations the AT is set to 2 μs. Fig. 15 shows the OT histogram for the OC14, the maximum OT is 1.83 μs, the minimum OT is 12 ns, the mean is 185 ns, with 501 ns standard deviation. Fig. 16 shows the

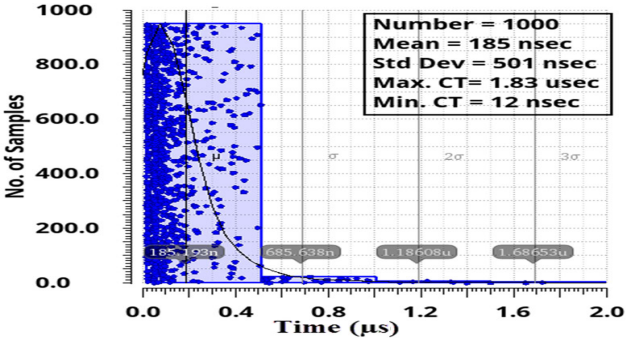

FIGURE 15. OT histogram for OC14, which has the maximum OT.

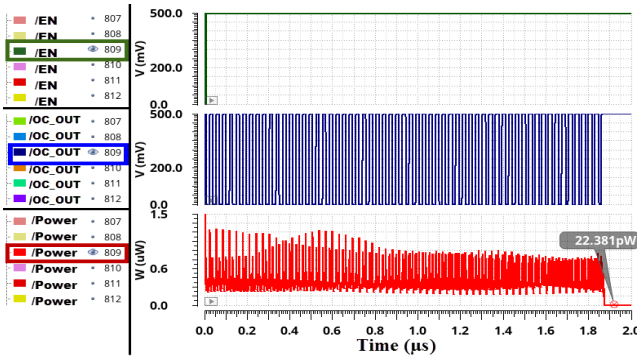

FIGURE 16. The output signal and instantaneous power for OC14, run number 809 from 1000 runs, which has maximum OT.

TABLE 3. Performance comparison among proposed OC, conventional OC, and c0nventional RO.

	RO regular	OC (with conventional inverter)	OC (proposed)
Number of Stages	9 inverters	8 inverters and 2 NAND	8 inverters and 2 NAND
VDD	0.5 V	0.5 V	0.5 V
Oscillations Time	Continuous	430 ns	1.85 µs
Frequency	2.2 GHz	175 MHz	33 MHz
Power	1.4 µW	940 nW	323 nW

EN signal, the OC_OUT signal, and the instantaneous power for the OC14. The simulation results for OC14 show that the maximum OT happened in the run number 809 out of 1000 runs, and the maximum instantaneous power is 12.5 μW and the minimum instantaneous power is 22.4 pW.

As can be observed from Fig 14, due to the process variation, the OT of each OC is different. Accordingly, the average consumption power for each OC is different. We performed a Monte Carlo simulation to compute the average consumption power for 1000 different OCs. The simulation results show that the average consumption power for the OC is 323 nW for the worst-case, 3 nW for the best case, and the mean is 32 nW, with 56 nW standard deviation.

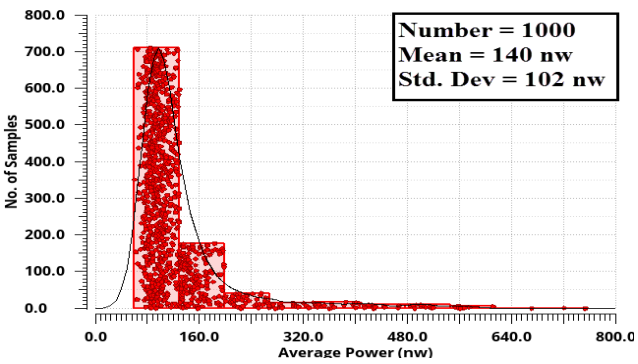

FIGURE 17. Histogram for the OC-PUF average consumption power.

For comparison, three modules were designed, the proposed OC module, the proposed OC module with a conventional inverter, and a conventional nine-stage RO circuit. All were designed using 20 nm triple gate bulk FinFET, with the same number of fins for inverter transistors. Table 3 illustrates the comparison between the three modules. The worst-case average power consumption is listed for the proposed and conventional OC. As observed, the average consumption power for the proposed OC is almost one third the conventional OC, and one-fifth of regular RO. The proposed OC has the lowest frequency, which reduces the consumption power in the following circuits of the OC-PUF.

A power analysis to the CTC circuit is done by applying 1000 random inputs to compute the average power consumption. The power consumption is averaged over all the inputs. The simulation results show that the average power consumption in the CTC is 45 nW, whereas in [24], the average power consumption in the counters is 8 μW.

To calculate the total consumption power for the proposed OC-PUF, a Monte Carlo simulation is performed to compute the average power consumption for 1000 different chips for the same response. Fig 17 shows the histogram for the OC-PUF average power consumption. The simulation results show that the OC-PUF worst case average power is 740 nW, the best average power is 63 nW, the mean is 140 nW, and the standard deviation is 102 nW.

There are many factors in the proposed OC-PUF design that combinedly decrease the power consumption, such as:

- The designed OC-PUF operates at a low supply voltage (0.5V), which reduces the total power consumption while maintaining high reliability.
- Ultra-low power consumption CTC circuit replaced the counters and the comparator in the conventional PUF. To generate one CRP, the CTC circuit average power consumption is 45 nW.
- Adding two transistors to the inverters in the designed OC causes it to operate near the threshold voltage. By adjusting the bias voltages of these transistors, the drain current decreases, which in turn reduces the power consumed.
- Demultiplexer and OR gates at the input of the OC-PUF ensure that only two OCs are working, and

TABLE 4. Summary of the measurement results and comparison with the state-of-the-art strong PUFs.

Metric	This work	Tao [25], 2017	Venkata [27], 2018	Yoo [28], 2018	Zhang [29], 2019	Kamal [30], 2019	Cao [31], 2019	Zhao [32], 2019	Gang [33], 2020
Technology (nm)	20 FinFET	65 CMOS	10 FinFET	28 CMOS	65 CMOS	45 CMOS	65 CMOS	65 CMOS	65 CMOS
Experimental/ Simulation	Simulation	Simulation	Simulation	Experimental	Experimental	Experimental	Experimental	Experimental	Experimental
Average Power (μW)	0.740	36.4	121	367	11.2	921	68.63	1.24	2710
Architecture Used	OC	RO	RO	OC	MPUF	RO	Arbiter	SRAM	SRAM
Number of possible CRPs	$4.3x10^{9}$	$6.8x10^{10}$	$1.8x10^{19}$	1024	5120	$3.4x10^{38}$	$1.8x10^{19}$	-	$2.5x10^{28}$
Response Size (bit)	64	128	32	-	512	128	64	256	128
Frequency (MHz)	33	1290	-	-	780	3096	25	-	-
Uniqueness (%)	50.01	49.97	74	50.67	50.42	-	46.8	49.94	50.004
Reliability (%)	99.8	-	-	98.3	95	-	99.2	99.14	99.59
Temperature range (°C)	-40 ~ 125	0 ~ 100	-	-20 ~ 60	0 ~ 90	-55~125	-40 ~ 150	-40 ~ 120	-40 ~ 125
Voltage range (V)	0.5 ± 10%	0.9 ± 10%	0.5 ~ 1	0.5 ~ 1	0.7 ~ 1.8	1 ~ 1.2	1.08 ~ 1.32	0.7 ~ 1.2	1 ~ 1.4

the other OCs are off. Thus, the power consumption is reduced.

- Using FinFET technology which consumes low power.

E. COMPARISONS

The performance of the proposed OC-PUF is summarized and compared with prior works in Table 4. The process technology is only slightly higher, but it consumes much lower power in comparison to others in [27]. The proposed OC-PUF is advantageous in terms of reliability, uniqueness, and power consumption. The simulation results show that the OC-PUF consumes only 740 nW on average at the frequency of 33 MHz with the largest inter-die Hamming distance ratio of 65.75%.

V. CONCLUSION

This paper presents an ultra-low power PUF design with high-performance metrics. The proposed PUF utilizes two new modules, the oscillator collapse and the collapse time comparator to decrease the power consumption. The proposed OC-PUF circuit was implemented using NCSU PDK 20 nm FinFET technology. The simulation results for 1000 different chips show that the average power is 140 nW, the worst case is 740 nW, and the best case is 63 nW per challenge-response pair at supply voltage 0.5 V. The OC-PUF reliability is 99.8%, with temperature changing from −40 to 125 °C and supply voltage 0.5 ± 10%. The OC-PUF has a uniqueness of 50.01%, which is close to the ideal value. The proposed PUF decreases the power consumption while maintaining high-performance metrics. Accordingly, the proposed OC-PUF is suitable for lightweight security services for low power applications.

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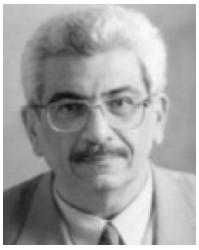
AMIN A. ZAYED received the B.S. degree in electronics and communication engineering from Benha University, Egypt, in 1998, and the M.S. degree in electronics and communication engineering from the Arab Academy for Science and Technology (AAST), Egypt, in 2016. He is currently pursuing the Ph.D. degree in electronics and communication engineering with Ain Shams University (ASU), Egypt. His research interests include digital design for communication systems based on FPGA, low-power design, and VHDL-based system design.

HANADY HUSSEIN ISSA received the B.Sc. degree in electronics and communications, Faculty of Engineering, Arab Academy for Science and Technology (AAST), in 1998, the M.Sc. degree from AAST, Egypt, in 2003, and the Ph.D. degree in electronics and communication engineering from Ain Shams University, Egypt, in 2009. She worked as a Teacher Assistant with AAST. In 2016, she was the Director of the Education Planning Unit, AASTMT. In 2017, she was a Director of the Center of Excellence (COE) in Nanotechnology, AASTMT. She is currently a Professor with the Electronics and Communication Department, AASTMT, Egypt. Since 2009, she has been supervised more than 20 master/Ph.D. theses in the areas of digital design for communication systems based on FPGA and low power design. She has coauthored more than 30 articles. Her research interests include analog/digital circuits design, VHDL-based FPGA design simulation and synthesis, and low power design.

KHALED A. SHEHATA received the B.Sc. degree from the Military Technical College, Cairo, Egypt, in 1981, the M.Sc. degree from Cairo University, Egypt, in 1991, and the Ph.D. degree from the Naval Postgraduate School, Monterey, CA, USA, in 1996. He worked as a Research Assistant. He worked as a Researcher in Egypt and the Director of the VLSI Design Center, AOI, Egypt. Since 2000, he has been a Professor with the College of Engineering, Arab Academy for Science and Technology. He is currently the Dean of the College of Engineering and Technology, Arab Academy of Science and Technology and Maritime Transport, Egypt. His research interests include analog and digital VLSI design, and electronics and communications system design. He has more than 100 scientific research articles in these areas.



HANI FIKRY RAGAI received the B.Sc. and M.Sc. degrees from Ain Shams University (ASU), Cairo, Egypt, in 1967 and 1972, respectively, the Doctorat de Specialite degree in electronics from Grenoble University, in 1976, and the Doctorat d'Etat degree in electronics from INPG, France, in 1980. From 1972 to 1979, he was a Research Assistant with LETI, CEA, Grenoble, France, and THOMSON-EFCIS, Grenoble. From 1979 to 1980, he was with the Electronics and Communication Engineering Department, Faculty of Engineering, ASU, as an Assistant Professor. From 1981 to 1984, he was with the Solar Energy Consultancy Sector, CEDUST, French Embassy in Cairo. From 1982 to 1984, he was involved in the Solar and Photovoltaic Joint Research Project between Alex University and Delft University. From 1985 to 1990, he was with King Saud University, Riyadh, Saudi Arabia. Since 1990, he has been a Professor of electronics with the Department of Electronics and Electrical Communication Engineering, ASU, where he was also the Director of the Integrated Circuits Laboratory, until 2006. From 1997 to 2002, he was a Consultant with Mentor Graphics and MEMScAP, Egypt. From 2006 to 2011, he was a Professor Emeritus with ASU and was also seconded to the French University of Egypt, as the Head of the Information and Communications Technology Department. Since 1981, he has been co-advising more than 80 M.Sc./Ph.D. theses and has coauthored more than 160 articles and one book on electronic devices. His research interests include modeling and characterization of solar cells and MOS devices, ASICs for wireless sensor nodes, wireless sensor networks for industrial applications, and MEMS-based sensors and energy scavenging. He served as the Co-Chair for the International Conference in Microelectronics (ICM 2007).