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Scalable, High-Sensitivity X-Band Rectenna Array for the Demonstration of Space-to-Earth Power Beaming

BRIAN B. TIERNEY[1], (Member, IEEE), CHRISTOPHER T. RODENBECK[1], (Senior Member, IEEE), MARK G. PARENT[1], AND AMANDA P. SELF[2]

[1]U.S. Naval Research Laboratory, Washington, DC 20375-5307, USA
[2]Air Force Research Laboratory, Kirtland AFB, NM 87117-5776, USA

Corresponding author: Brian B. Tierney (brian.tierney@nrl.navy.mil)

ABSTRACT This paper presents a large, modular X-band rectenna array developed for the planned demonstration of a space-to-Earth power beaming link operating at 10 GHz. The array is composed of 16 tiles assembled into a panel greater than 1 m × 1 m in size. To accommodate tests during the early development and construction of the space-based transmitter, the rectenna cells are designed to maximize performance at low power densities using commercial-off-the-shelf Schottky diodes. To increase efficiency at the expense of some field-of-view, each rectenna cell employs a 4-antenna subarray to feed a single diode. Array performance is validated over a 30-dB range of power densities from 1 mW/m^2 to 1 W/m^2, reaching a total rectenna efficiency in excess of 39% at 1 W/m^2. The rectenna array's field of view, defined by the 3-dB beamwidth of its antenna subarray, is 36° × 36°. The DC power collected by each tile is combined in a reconfigurable manner to control the output voltage level for the protection of electrical loads. These results are expected to directly influence the first demonstrations of space-to-Earth power transfer.

INDEX TERMS Wireless power transmission, rectennas, solar power, satellites.

I. INTRODUCTION

The space-to-Earth transfer of power has long been an attractive proposal for generating environmentally clean energy at a large scale. The concept is that a solar-power satellite (SPS) in Earth's orbit would convert solar power into microwave power that is beamed down to Earth and collected by rectenna (rectifying antenna) arrays [1], [2].

Despite being originally envisioned in 1968 and assessed for decades, no prototype SPS systems have actually been deployed due to high costs and technological challenges [2]. However, given the maturity of modern space technology, the Air Force Research Laboratory (AFRL) has announced plans to develop and deploy the first-ever prototype SPS system under a new program: Space Solar Power Incremental Demonstrations and Research (SSPIDR) [3]. The prototype will focus on a smaller scale but critical application: delivering power to forward operating bases in areas that do not otherwise have access to power. Using SPS systems, power can be beamed from space to wherever it is needed on the ground.

This paper presents the first rectenna-array prototype developed for SSPIDR. The design is required to receive left-hand circularly polarized (LHCP) RF power at 10 GHz over a 1 mW/m^2 to 1 W/m^2 range of incident power densities. This low level of incident RF power is targeted to accommodate the reduced transmit levels that will be available in early development of the SSPIDR SPS. For rapid development and deployment, the array features interconnecting, modular tiles based on commercial-off-the-shelf technology.

Rectenna arrays themselves are not new. The first arrays were developed in the 1960s and 1970s by William Brown, who embedded an array of Schottky-diode rectifiers into dipole antennas to rectify incident S-band microwave power [4]–[8]. A historical overview of these experiments is provided in [4]. Since then, numerous rectenna and rectifier designs have been demonstrated at a variety of frequency bands. Fig. 1 presents a survey of rectifier and rectenna efficiencies at 915 MHz [9]–[22]; 2.45 GHz [6], [20]–[36]; 5.8 GHz [35]–[46]; 8-12 GHz [47]–[55]; 24-35 GHz [55]–[62]; and 90-95 GHz [62]–[69].

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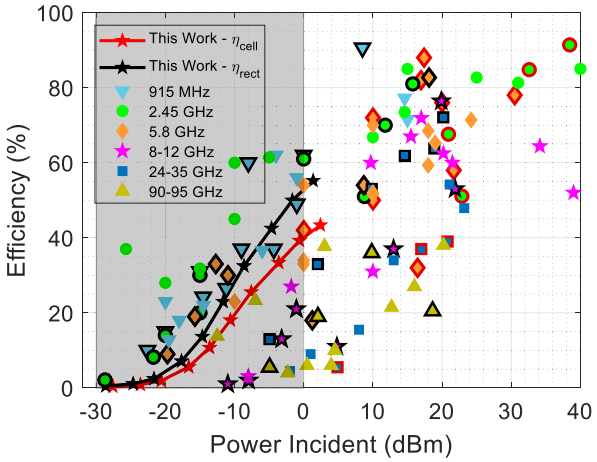

FIGURE 1. A survey of measured rectifier and rectenna efficiencies in the literature for a variety of frequencies. Markers with a red outline are rectenna efficiencies, plotted versus power incident into a rectenna cell. Markers with a black outline are rectifier efficiencies estimated from rectenna measurements, as explained in Section IV-E. Markers with no outline are simply rectifier measurements. The shaded portion of the plot represents the estimated rectifier power levels for the power densities prescribed by the SSPIDR program. For comparison, the measured rectenna cell efficiency η_{cell} and estimated rectifier efficiency η_{rect} from this work are also plotted (see Section IV-E).

Two well-known trends are clear from Fig. 1: (1) the rectifier efficiency increases as incident power level increases and (2) rectifier efficiency drops with increasing frequency. The first trend is due to the required forward voltage drop across the diode(s) in the rectifier. As incident power level decreases, a larger proportion of the generated DC voltage (and thus power) is lost to the diodes [70]. The second trend is due to the low-pass filter effect caused by the diode junction capacitance and series resistance [70].

Although the efficiency of rectifiers decreases with increasing frequency and the atmospheric attenuation generally increases with increasing frequency [71], the required transmit-aperture sizes decrease with frequency [4] and can therefore be easier to deploy. The 10-GHz transmit frequency of SSPIDR represents a compromise between transmit-aperture size and rectifier efficiency; in addition, at 10 GHz, total standard atmospheric attenuation from sea level to space at zenith is estimated to be less than 0.06 dB for typical atmospheric conditions [71], making this an attractive frequency for space-to-Earth microwave power beaming. Unfortunately, Fig. 1 indicates that no designs found in the literature in the 8-12 GHz range are optimized for the low power levels required for the SSPIDR demonstration. The rectenna panel design presented in this paper fills that void and exhibits efficiencies that significantly exceed the limited results from the literature.

The new rectenna array is designed with large-scale manufacturability and simplicity in mind. Most examples of rectenna arrays approaching a size of 1 m × 1 m in the literature appear to involve the manual assembly of individual rectenna elements [8], [32], [72], [73] and the suspension of elements $\lambda/4$ above a metallic reflector [8], [32], [72], [73], [74]. The design presented here employs modular printed-circuit-board (PCB) tiles, which are more conducive to large-scale manufacturability and ease of repair. The tiles can be arranged into a panel of arbitrary size. In addition, to allow safe connection of multiple tiles to a single DC load, this paper presents a double-pole, double-throw (DPDT) switch matrix; the switch matrix provides reconfigurable control of the output current and voltage levels to maintain a safe connection to a variety of practical DC loads and to improve the efficiency of subsequent DC-to-DC conversion by presenting an input voltage that minimizes dissipative loss.

This paper is structured as follows: Section II presents the design of the rectenna unit cell. Section III describes the population of the rectenna cell into 36-cell tiles that comprise the 1.0 m × 1.1 m panel. Section IV presents experimental results detailing the performance of the rectenna tiles and panel versus incident power density and angle. Section V concludes this paper by summarizing its extension of the state of the art in terms of efficiency, sensitivity, scalability, and reconfigurable tile interconnectivity. These results are expected to influence multiple demonstrations of space-to-Earth power beaming within this decade.

II. RECTENNA CELL DESIGN

A rectenna consists of one or more antennas for receiving RF power and a rectifier for converting the RF power into DC power. Most low-power rectifier designs, including the design in this paper, employ Schottky diodes. Schottky diodes have low forward voltages that yield higher efficiency at low power levels compared to transistors and other diode devices [70]. Also, the low junction capacitance of Schottky diodes improves efficiency when operating in the microwave range.

The DC outputs of numerous rectennas can be connected together [8], [32], [72], [73], [74] to collect RF power over larger aperture areas. In this paper, the individual rectennas are referred to as *cells*. The entire rectenna array is referred to as a *panel*. The panel is comprised of PCB *tiles* that serve as an intermediate between the cell and panel.

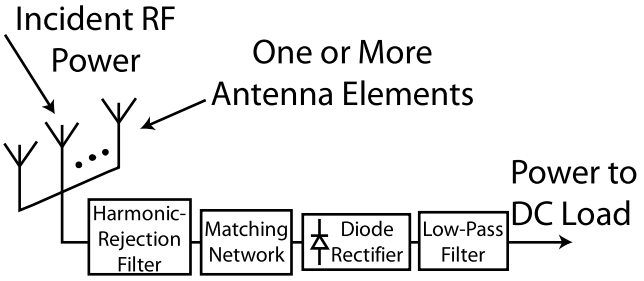

FIGURE 2. Block diagram of the rectenna topology used in this paper. This topology is based on the original rectenna designs by William Brown [4]–[8].

Fig. 2 illustrates the block diagram of the rectenna cell topology used in this paper. Multiple antenna elements

receive incident RF power. A matching network provides a complex-conjugate impedance match between the antennas and the Schottky-diode rectifier, to minimize reflected RF power. The Schottky diode converts the RF power to DC power. A low-pass filter supplies DC power to the load while containing RF power within the rectenna. A harmonic-rejection filter suppresses the radiation of harmonic frequencies generated by the diode and improves efficiency by containing harmonic power within the rectenna for additional rectification.

The number of antenna elements per cell is a key tradeoff in low-power-density rectenna arrays. At the lowest power densities prescribed by the SSPIDR program, the rectenna efficiency is expected to be very low (see Fig. 1). Combining RF power from multiple antenna elements can boost the rectifier's input drive level in order to increase RF-to-DC conversion efficiency. This increase in efficiency, however, comes at the expense of a narrower field of view, which may be problematic for SPS applications since the position of a low-Earth-orbit (LEO) transmitter may be changing or imprecisely aligned relative to the rectenna array. As a tradeoff between the conflicting requirements of a wide field of view and sensitivity to very low levels of incident power, the design presented in this paper combines RF power from four antenna elements.

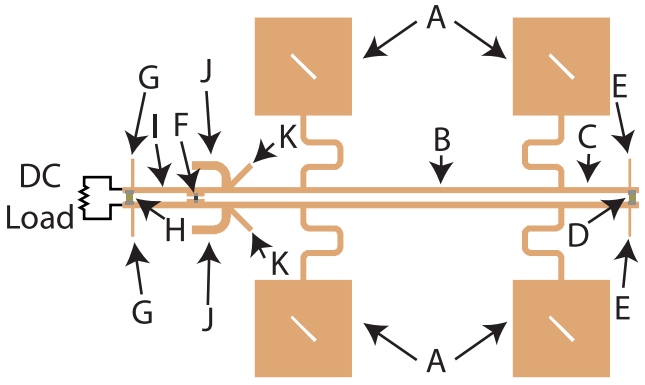

FIGURE 3. PCB layout of the rectenna unit cell, measuring 42.2 mm × 42.2 mm. The cells are comprised of four LHCP microstrip antennas (A) connected together by coplanar strips (B) of length 360° and terminated on the right by a 90° line (C); 2-pF, ceramic, 0402 capacitor (D); and 90° open stub (E). The antennas are connected to a differential Schottky-diode (F) rectifier on the left. A 90° open stub (G) and a 2-pF, shunt capacitor (H) are located 90° away (I) from the diode to isolate RF power from the DC load while providing a Class-F termination to the diode. The matching network is comprised of open stubs (J) for matching and open-stub, 20-GHz-harmonic shorts (K) for reducing the radiation of the 20-GHz harmonic.

The rectenna unit cell, shown in Fig. 3, was fabricated on a 0.76-mm-thick Rogers 3003 ($\epsilon_R = 3$) printed circuit board (PCB) with 18-μm-thick rolled-copper metallization and immersion-silver plating. Four identical left-hand circularly polarized (LHCP) microstrip antenna elements [75] are spaced 21.1 mm ($0.7\lambda_0$) center to center, resulting in a 3-dB beamwidth of 36° by 36°.

The antennas in Fig. 3 are connected to a differential Schottky-diode rectifier using coplanar strips [4], [45]. The single-diode approach maximizes rectifier sensitivity and efficiency [70]. The Skyworks SMS7630-061 Schottky diode was selected for its low forward voltage, low junction capacitance (0.14 pF), and minimal package parasitics at 10 GHz. A 90° open stub and 2-pF, shunt capacitor are located 90° away from the diode to isolate RF power from the DC load. At the plane of the diode, these terminations ideally present an open-circuit condition for all odd harmonics and a short-circuit condition for all even harmonics, corresponding to a Class-F harmonic load [76]. All microstrip dimensions in Fig. 3 are designed based on electromagnetic simulation with a modified version of the manufacturer-provided diode model, as described in Section IV-A.

An open-stub matching network provides a complex-conjugate impedance match between the Schottky-diode rectifier and the antennas at an incident power density of 200 mW/m^2 and 10 GHz operation. Reflection loss is kept small over the entire 1 mW/m^2 to 1 W/m^2 range. An open stub of length 90° at 20 GHz is embedded within the matching network to minimize radiation of the second harmonic.

III. RECTENNA ARRAY DESIGN

To demonstrate scalability toward an array of significant size, 36 rectenna cells are incorporated into a 250 mm x 280 mm tile, which serves as the modular building block for the panel. The DC outputs of all 36 cells are combined to form a single DC output for the tile. The panel is comprised of a 4-by-4 grid of 16 tiles and measures 1.0 m × 1.1 m. The DC outputs of each tile are combined in a reconfigurable matrix using a series of DPDT switches.

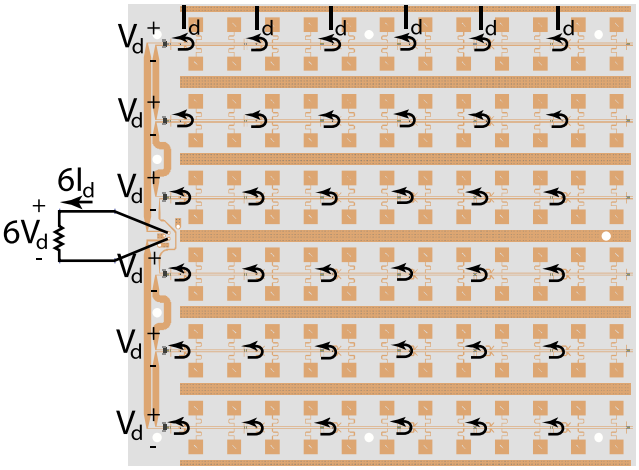

FIGURE 4. The rectenna tile PCB layout. The tile consists of 6 rows, each containing 6 cascaded rectenna cells. Since the cells within a row are connected in parallel, the DC currents generated by each cell are summed together. The DC outputs of each row are then connected in series, thereby adding their DC voltages. This graphic assumes that each cell generates the same voltage and current, but these values will vary slightly from cell to cell in practice.

Fig. 4 illustrates the rectenna tile design. The tile is comprised of 6 rows. Each row sums the DC currents from 6 cascaded rectenna cells. On the left-hand side of Fig. 4,

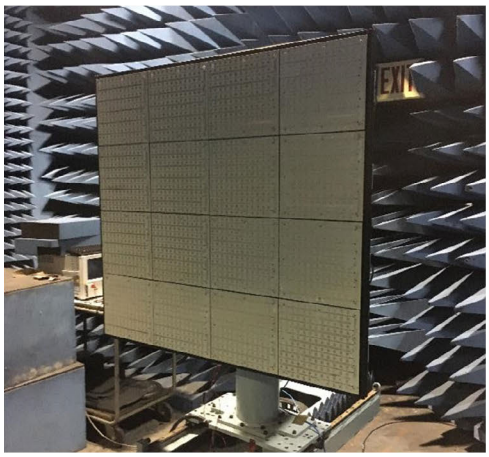

FIGURE 5. The front-side view of the assembled rectenna panel, comprised of a 4-by-4 array of rectenna tiles. The panel is shown here mounted on a mechanical positioner for testing in an anechoic chamber.

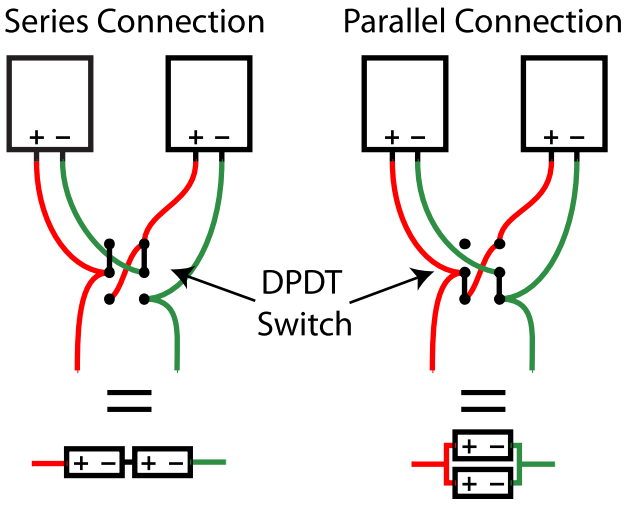

FIGURE 6. A wiring diagram for a double-pole, double-throw (DPDT) switch that selects between a series connection and a parallel connection for a pair of rectenna tiles. The switch is represented by its 6 pins (black circles), with the electrical connection between pins shown for both toggle states.

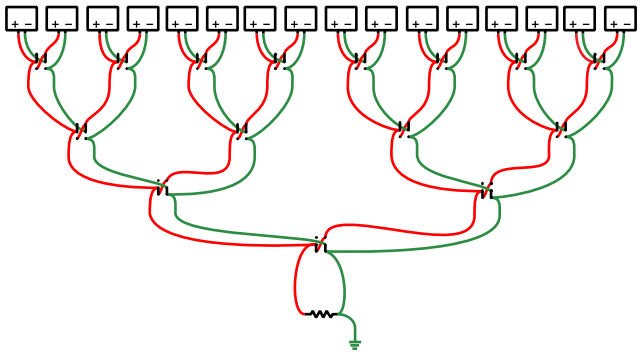

FIGURE 7. The wiring diagram employed by the rectenna panel for reconfigurable connection of the rectenna tiles. Using this switching scheme, the rectenna panel can be connected in configurations of 16:1, 8:2, 4:4, 2:8, 1:16, where M:N indicates groups of M tiles connected in series and N such groups connected in parallel.

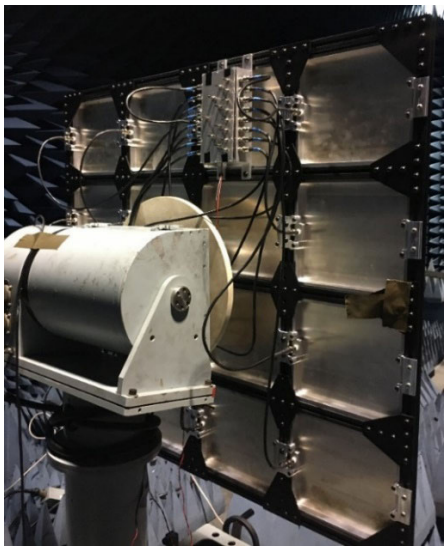

FIGURE 8. The back-side view of the assembled rectenna panel. Twin-axial cables feed the DC output from each tile to a box housing the reconfigurable switch matrix. Mechanical switches are used in this implementation in order to minimize DC power consumption during experimental demonstrations. The panel is shown here mounted on a mechanical positioner for testing in an anechoic chamber.

the differential outputs of the 6 rows connect in series to sum together their DC voltages. Assuming uniform illumination and identical performance for all cells, the tile will produce 6x the current and 6x the voltage of a single rectenna cell. This represents 36x the DC power of a single rectenna cell and the same field of view as a single rectenna cell since only the DC output power is combined rather than any RF power. A 1.8-V Zener diode at the end of each row protects the Schottky diodes from an overvoltage condition. To provide mechanical rigidity, the tile is bonded to a 1.6-mm FR4 substrate, with no associated electrical impact.

A total of 16 tiles assemble into a 4-by-4 array, incorporating 576 rectenna cells, as shown in Fig. 5. Each of the 16 tiles provides a differential DC output. These 16 outputs can connect to a common load (*i*) in series, (*ii*) in parallel, or (*iii*) with some in series and some in parallel. Prior work [72], [77], [78], provides comparisons between these three options and shows that, although DC power is nearly identical in all cases, DC voltage and current varies significantly. Connecting tiles in series will sum their voltages together while connecting tiles in parallel will sum their currents together. At the lowest prescribed incident power density of 1 mW/m^2, it is best to connect all outputs in series to maximize the output voltage. However, at the highest prescribed power density of 1 W/m^2, the summation of all tile voltages may exceed the voltage limits of a practical output load, e.g., a voltage regulator connected to a battery. In this case, parallel connections may be better.

Reconfiguring the DC connections between tiles allows the panel to adapt load voltage and current for a wide range of

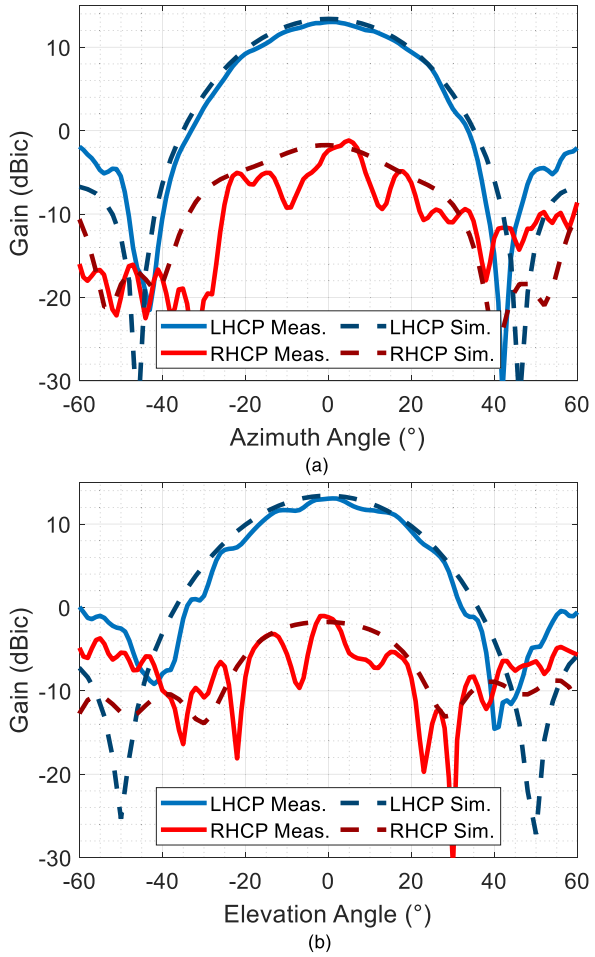

FIGURE 9. Measured and simulated two-axis antenna patterns: (a) azimuth and (b) elevation. The simulated results were computed using the commercial electromagnetic solver Ansys HFSS.

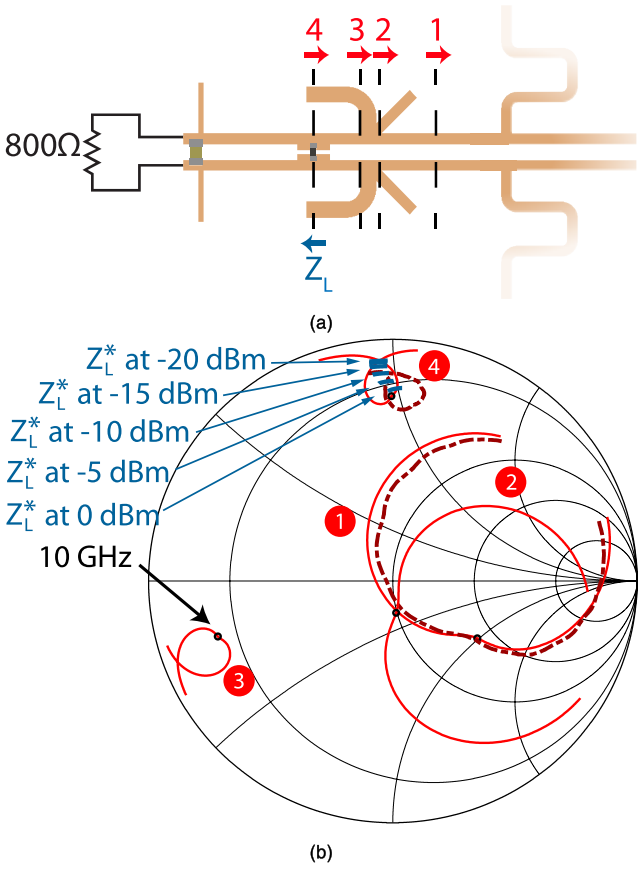

FIGURE 10. The impedance transformation between the antenna and rectifier: (a) reference plane locations and (b) matching-network impedance transformation plotted on a Smith chart over 9.5 to 10.5 GHz. The solid curves are simulated results; the dashed curves are measurements at Planes 1 and 4. Complex-conjugate load impedances are shown in blue for a variety of power levels incident upon the rectifier and indicate some variation vs. input power level.

incident power densities. Fig. 6 shows a wiring diagram for a DPDT switch that selects between a series connection and parallel connection for a pair of rectenna tiles. The wiring diagram in Fig. 7 extends this DPDT scheme to all 16 tiles used in the rectenna panel. Tiles are interconnected using DPDT switches in a recursive, four-layer hierarchy until there is only one DC output, the load for which is represented by a resistor in the figure. When all the switches in any given layer of the hierarchy are thrown in the same direction, all 16 tiles are loaded with an equal output resistance, which is useful for ensuring that the effective output resistance seen by each tile is set to the optimal value for RF-to-DC conversion efficiency. Under this constraint, the switching scheme depicted in Fig. 7 can drive five different connection configurations: 16:1, 8:2, 4:4, 2:8, and 1:16, where M:N indicates groups of M tiles connected in series and N such groups connected in parallel. Unlike the alternative switching scheme presented in [77], this topology is "fail safe" in that no choice of switch configuration will result in an opened or shorted output.

The DC switching circuitry is housed in a metal box on the back of the rectenna panel, with twin-axial cable connecting the switch matrix to the 16 individual tiles, as shown in Fig. 8. Mechanical switches are used here in order to minimize DC power consumption during experimental demonstrations, which may feature power densities as low as 1 mW/m^2. For future demonstrations with higher power densities, transistor-based switches or electromechanical relays can also be considered to enable a simple and efficient method of controlling the DC output voltage digitally.

IV. EXPERIMENTAL RESULTS

Experiments were conducted on breakout PCBs for the rectifier, antenna, and matching network to verify performance. Measurement and simulation results for these subcomponents are presented first, followed by the measurement and simulation results for the rectenna tiles and panel.

A. RECTIFIER DIODE

The rectifier was individually fabricated on a breakout PCB, without any matching network included. The measured DC I-V curve of the Schottky diode deviates slightly from the manufacturer-provided SPICE model; a least-squares curve fit of the Shockley diode equation to the measured data

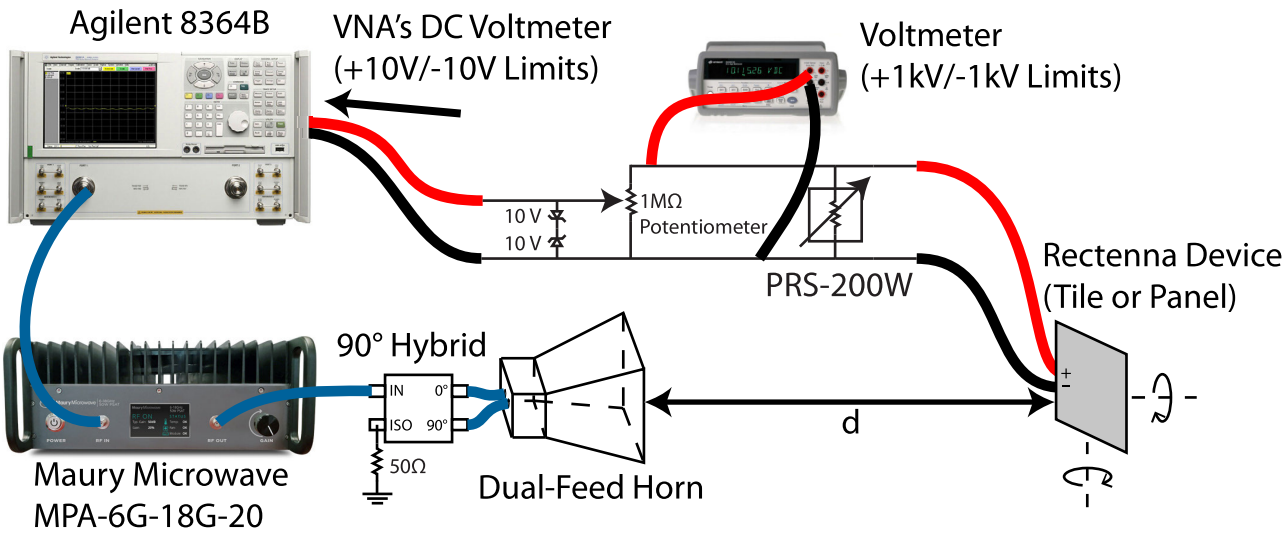

FIGURE 11. Rectenna measurement setup in the anechoic chamber.

resulted in three adjusted SPICE parameters: $R_S = 13.2\ \Omega$, $I_S = 4.2{\cdot}10^{-6}$ A, N = 1.1725. Additionally, the model junction capacitance was adjusted to $C_{J0} = 0.11$ pF based on the measured DC output voltage versus accepted RF power characteristic.

B. ANTENNA

The 2 × 2 differential antenna was fabricated on a breakout PCB. It was measured in an anechoic chamber using a 2-port vector network analyzer (VNA) and a transmit horn of known gain. The measured two-axis antenna patterns provided in Fig. 9 show excellent agreement with simulation. The measured pattern has a beamwidth of 36° in both azimuth and elevation; the measured gain is 13.0 dBic at broadside. The measured polarization loss factor [75], representing the polarization mismatch loss between the antenna and an ideal LHCP wave, is 0.1 dB.

C. MATCHING NETWORK

Fig. 10 illustrates the impedance transformation between the antenna and the rectifier. The simulated results are provided by the commercial electromagnetic simulation software Advanced Design System. The measured results are provided by a VNA, which measured a breakout PCB containing only the matching network and a breakout PCB containing only the antenna. Deembedding was used to remove fixture effects from the measurements. The impedance looking to the right of Plane 4 matches well with the complex conjugate of the rectifier impedance Z_L looking to the left of Plane 4 for a wide range of power levels incident upon the rectifier. The rectifier was connected to a load resistance of 800 Ω. Note that the length of transmission line between Plane 1 and Plane 2 controls the size of the "loop" shown in the impedance contour at Plane 4 and is chosen to broaden the impedance-matching bandwidth to provide tolerance to fabrication variance.

D. RECTENNA

The total efficiency η_t of a rectenna array is best defined as

$$\eta_t = \frac{\text{DC Output Power}}{\int_A P_D(x, y) \cdot dA}, \tag{1}$$

where the denominator is an integral of the incident power density $P_D(x, y)$ over the area of the rectenna. This definition thus accounts for all sources of loss: aperture efficiency, polarization loss, impedance mismatch, RF-to-DC conversion efficiency, and all other dissipative losses within the rectenna. The efficiency η_t was measured in an anechoic chamber using the measurement setup depicted in Fig. 11. A VNA provided the signal source, which was amplified by a 20-W commercial power amplifier. A 90° hybrid and dual-feed horn antenna were used in tandem to produce left-hand circularly polarized (LHCP) radiation. The rectenna under test was mounted on a positioner that can roll and yaw, enabling pattern measurements. The separation distance d was chosen so that the tapering of power density from the center to the edge of the rectenna under test was less than 1 dB. The distance d was set to 2.0 m for the rectenna tiles and 4.8 m for the rectenna panel. The incident power density at the plane of the rectenna was calibrated using a Narda 640 receiver horn and a power meter. The DC voltage produced by the rectenna tile or panel was measured by the VNA's DC voltmeter for automated data collection. A 1-MΩ potentiometer was used to step down the voltage to within the limits of the VNA's voltmeter. A second voltmeter was used for calibration of the potentiometer settings.

Using this setup, the DC output from a single rectenna tile was measured while sweeping the load resistance using a variable resistor (PRS-200W from IET Labs) to determine the optimal value, which was found to be 800 Ω. Fig. 12 shows the measured total efficiency η_t for 20 fabricated rectenna tiles, each driving an 800-Ω load. An average total efficiency η_t of 39% was measured at $P_{AVG} = 980\ \text{mW/m}^2$, where P_{AVG}

is the average incident power density over the surface of the rectenna tile. The figure shows excellent agreement between simulation and measurement.

The 1.0 m × 1.1 m rectenna panel was assembled using the best 16 of the 20 rectenna tiles. The total efficiency η_t for all five DPDT-switch configurations is plotted in Fig. 12. Each configuration yielded approximately the same efficiency. For the 5 panel configurations (16:1, 8:2, 4:4, 2:8, 1:16), the load resistance was scaled as needed (12.8 kΩ, 3.2 kΩ, 800 Ω, 200 Ω, 50 Ω) to provide the optimal 800-Ω load condition to each tile. An average total efficiency 41% was measured at $P_{AVG} = 920$ mW/m^2.

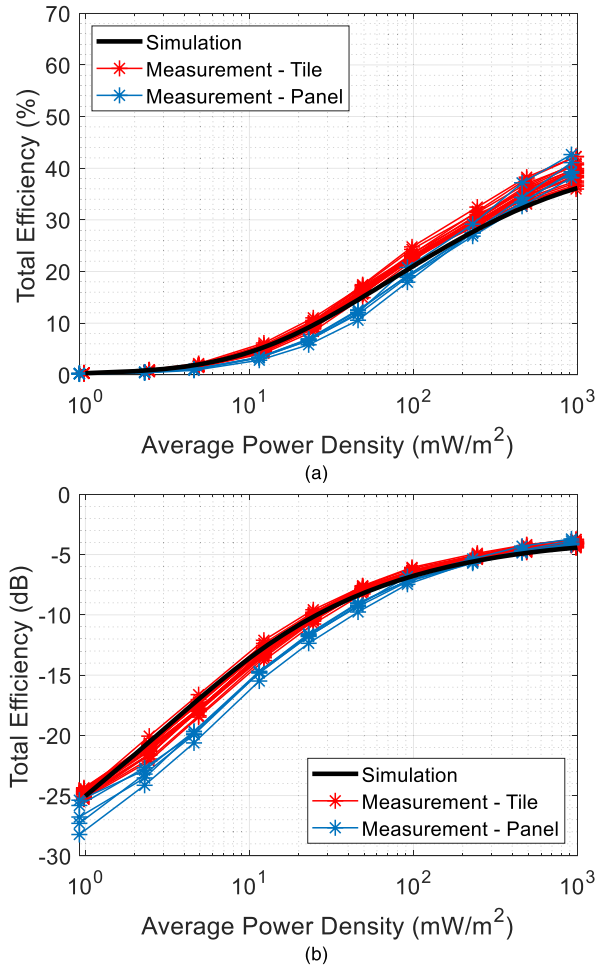

FIGURE 12. Measured and simulated rectenna efficiencies for the tile and panel in (a) linear and (b) dB scale. The x-axis indicates the incident power density averaged across the entire face of the rectenna. A load resistance of 800 Ω was used for the tiles. For the 5 panel configurations (16:1, 8:2, 4:4, 2:8, 1:16), the load resistance was scaled as needed (12.8 kΩ, 3.2 kΩ, 800 Ω, 200 Ω, 50 Ω).

To demonstrate the utility of the DPDT-switch matrix to provide efficient rectification over a wide range of load resistances, Fig. 13 provides the efficiency versus load resistance for the panel at $P_{AVG} = 920$ mW/m^2. An alternative way of viewing these results is that the switch matrix provides coarse control over the panel's output voltage, which can range from 5 to 71 V in this example. When connecting to a battery-charging circuit comprised of a DC-to-DC voltage converter, this coarse control can maintain a safe input voltage level and could potentially be used to optimize charging efficiency. The 1:16 configuration can be used for high power densities to minimize output voltage while the 16:1 configuration can be used for the lowest power densities to maximize output voltage.

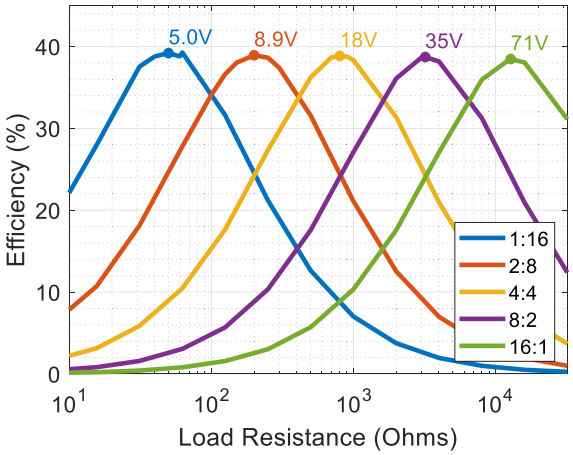

FIGURE 13. Rectenna panel efficiency versus load resistance at 920 mW/m^2 average power density. The output voltage at each efficiency peak is provided.

Fig. 14 shows the received DC power for the rectenna panel versus angle at several incident power densities in the 1 mW/m^2 to 1 W/m^2 range. Because the antenna subarray's field of view was sacrificed for higher gain (see Sec. II), the received power begins to roll off beyond ±20°. Due to the roll off, the transmitter source should be located within the ±20° cone for most efficient power transfer.

E. LITERATURE COMPARISON

Comparing the rectenna panel performance to prior work is not simple for a three reasons:

1. As discussed in Sec. I, there are very few prior designs presented in the 8-12 GHz band that focus on such low power densities. Instead, rectenna designs have been primarily concentrated in the 915 MHz, 2.45 GHz, and 5.8 GHz bands. However, a direct comparison of efficiencies when frequencies differ does not provide the entire picture. One should also consider the advantages of a higher frequency, such as the reduced size of the space-based transmitter.
2. Efficiency comparisons lack validity if the antenna designs differ significantly in gain (e.g., the 4-patch antenna presented in this paper versus a single patch). The tradeoff in field of view must also be considered.
3. Most designs surveyed in Fig. 1 are single rectenna cells that are not arrayed, making it difficult to define a fair physical area for the purposes of (1).

A good comparison to start with is that of estimated rectifier efficiency. Since the rectifier is the dominant source of loss, such a comparison is quite significant and avoids the second and third issues above. Moreover, comparisons can be

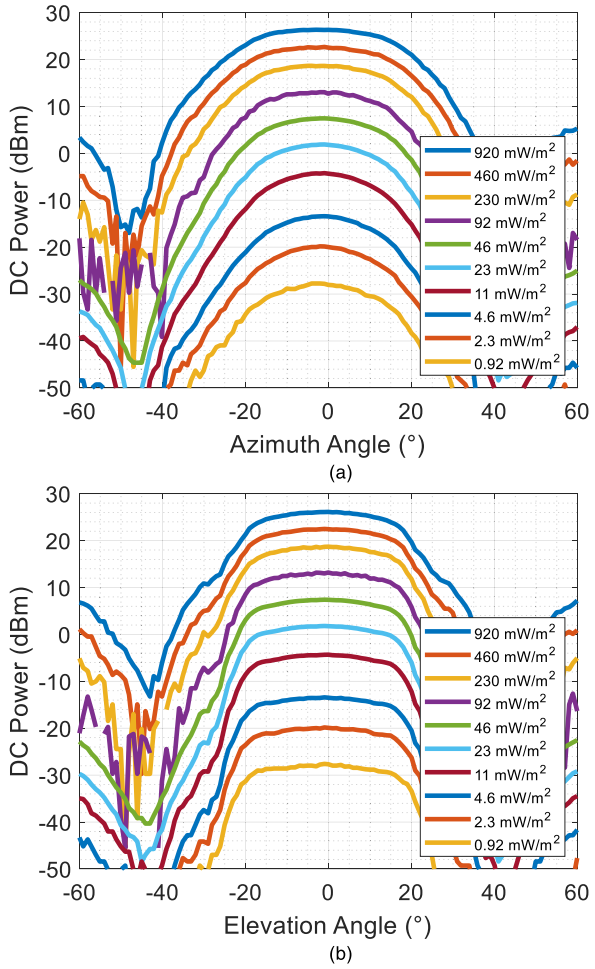

FIGURE 14. Rectenna panel DC output power versus (a) azimuth and (b) elevation for the 16:1 case with $R_L = 12.8\Omega$ for a range of average power densities.

made to papers that only discuss rectifiers. For rectenna measurements, the rectifier efficiency can be estimated after computing the effective area A_e of the rectenna cell's antenna using the measured or simulated antenna gain and polarization loss factor [75]:

$$A_e = \frac{\lambda^2 \cdot G \cdot PLF}{4\pi}, \tag{2}$$

where G is the antenna gain and PLF is the polarization loss factor. The estimated rectifier efficiency is then given by

$$\eta_{rect} = \frac{P_{DC}}{P_{AVG} \cdot N \cdot A_e}, \tag{3}$$

where P_{DC} is DC output power of the device, N is the number of rectenna cells in the device, and P_{AVG} is the average incident power density over the surface of the rectenna aperture. The disadvantage of using the η_{rect} metric is that it does not penalize for low aperture efficiency or high polarization loss.

For arrays, an even better metric of comparison than η_{rect} is the rectenna cell efficiency η_{cell}, which can be computed as

$$\eta_{cell} = \frac{P_{DC}}{P_{AVG} \cdot N \cdot A_{cell}}, \tag{4}$$

where A_{cell} is the physical area of a single rectenna cell. However, for single-element results in the literature, it is difficult to define A_{cell}.

Fig. 1 plots both η_{rect} and η_{cell} of this paper alongside the efficiencies found in the literature. η_{rect} is calculated using the measured antenna gain of 13.0 dBic, measured PLF of 0.1 dB, and the average, measured efficiencies of the 20 rectenna tiles. At an average incident power density of 980 mW/m^2, 2.4 dBm is incident upon a rectenna cell and an estimated 1.4 dBm is incident upon the rectifier. In this case, η_{rect} and η_{cell} are 55% and 43% respectively. The metric η_{cell} exceeds η_t because the DC connections on the left side of the tile occupy area over which incident power density is not collected, corresponding to an estimated 10% decrease in efficiency. The figure shows that the efficiencies measured in this work exceed all previous work above 8 GHz at the power levels of interest.

V. CONCLUSION

A large X-band rectenna panel design optimized for low power densities was presented. The panel was comprised of 16 interconnecting, modular rectenna tiles made using printed-circuit-board (PCB) technology. The average, measured total rectenna efficiency η_t was 39% at 10 GHz for an average incident power density P_{AVG} of 980 mW/m^2 across a given rectenna tile. At this power density, the rectifier efficiency η_{rect} and η_{cell} are estimated to be 55% and 43% respectively. Using a multilayer board design, the DC connections within the tile could be moved to the backside of the rectenna array to let η_t equal η_{cell}.

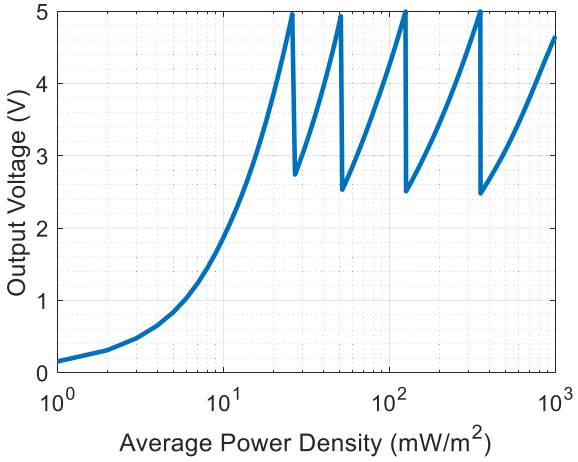

FIGURE 15. A hypothetical plot of rectenna panel output voltage versus incident power density using the reconfigurable tile-interconnection scheme. The voltage can be kept below a prescribed level (e.g., 5 V) over the 30-dB dynamic range of incident power density. This is advantageous for connection to a battery-charging circuit comprised of a DC-to-DC voltage converter, as it maintains a safe voltage level and can result in more efficient charging.

The rectenna tiles' DC outputs were interconnected in a reconfigurable manner using an array of DPDT switches to produce a single DC output for the entire panel. As shown in Fig. 15, the DPDT-switch matrix can be used to constrain

the panel's output voltage below a threshold (e.g., 5 V in this case) with negligible loss over the entire 30-dB dynamic range of incident power density. For low-power applications, such control of the output voltage can also improve the efficiency of subsequent DC-to-DC voltage conversion, e.g., in battery-charging applications.

Multiple rectenna panels can be interconnected for even more DC output power. Parallel connections between panels are recommended since they will be easier to cascade together over large outdoor facilities. For large-scale applications, an individual tile should be sized while keeping in mind that the minimum voltage achievable by the switch matrix is equal to the output voltage of a single tile. Likewise, the number of tiles assembled into parallel-connected panels should be chosen while keeping in mind that maximum voltage achievable from each panel sets the maximum voltage available from the parallel cascade of panels.

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BRIAN B. TIERNEY (Member, IEEE) received the B.S. degree in electrical engineering from Kansas State University, Manhattan, KS, USA, in 2011 and the M.S.E and Ph.D. degrees in electrical engineering from the University of Michigan at Ann Arbor, Ann Arbor, MI, USA, in 2014 and 2016, respectively.

Since 2016, he has been with the Radar Division of the U.S. Naval Research Laboratory in Washington, DC, USA. His current research interests include advanced radar concepts, microwave circuits, wireless power transfer, electromagnetic theory, and digital signal processing.

CHRISTOPHER T. RODENBECK (Senior Member, IEEE) received the B.S. (*summa cum laude*), M.S., and Ph.D. degrees in electrical engineering from Texas A&M University, College Station, TX, USA, in 1999, 2001, and 2004, respectively. His graduate studies were supported by fellowships from NASA, the State of Texas "to advance the state of the art in telecommunications," Texas A&M, and TxTEC in addition to grants from Raytheon, TriQuint Semiconductor, the Office of the Secretary of Defense, NASA Jet Propulsion Lab, NASA Glenn Research Center, and the US Army Space Command.

Dr. Rodenbeck is currently an Office Head at the US Naval Research Laboratory in Washington, DC where he leads the Radar Division's Advanced Concepts Group and is responsible for multiple research programs in millimeter-wave airborne radar and advanced electronics. From 2004 to 2014, he led a multidisciplinary advanced/exploratory technology development program for radar and sensor applications at Sandia National Laboratories in Albuquerque, NM. The success of this work was twice the subject of Congressional testimony by Sandia's President. He is responsible for numerous radar innovations, including the development of high power amplifiers with integrated drain modulators, a spatial power combining technique mitigating interference between colocated radar systems, detection-at-the-limit digitizers sensitive to the 1-μV level, a novel radiation-hardening-by-design technique applicable to commercial semiconductor processes, electro-optical imaging of vector leakage in radar modules, reliable plasma cleaning techniques for CMOS ICs, software-defined fusion of radar and telemetry signals, electrically small antennas for radar responsive tags, and a technique for analyzing and eliminating transient oscillations in UWB transmitters.

Dr. Rodenbeck received the 2016 Texas A&M University Outstanding Early Career Professional Achievement Award from among more than 100,000 engineering alumni. He received the IEEE MTT-S Outstanding Young Engineer Award in 2015, was the Principal Investigator for an R&D program receiving the prestigious 2012 NNSA Award of Excellence, received a Sandia Innovator Award in 2013, and was awarded an internal citation for "Excellence in Radar Technology Leadership" in 2011. He is an Associate Editor of the *Encyclopedia of Electrical and Electronics Engineering* (New York, NY, USA: Wiley), responsible for the Microwave Theory and Techniques subject area. Chris has mentored numerous engineers in the radar electronics application area. He has authored or coauthored 38 refereed journal papers, 21 patents and patent applications, 29 conference papers, and 27 government reports.

MARK G. PARENT received a B.S. in electrical engineering and a M.S. in physics from Michigan Technological University in 1982 and 1985, respectively.

He briefly worked at Northrup Grumman in Rolling Meadows, Illinois, and since 1985 has been working at the Naval Research Laboratory in Washington, DC. His research has included optical beamforming, HF vector sensors, high-isolation system development, RCS measurements, monopulse beamformers, low-sidelobe corrugated horns, and various antenna-related projects. He has authored and coauthored numerous journal articles and conference papers and holds several patents.

AMANDA P. SELF received the B.S. and M.S. degrees in aerospace engineering from Georgia Institute of Technology, Atlanta, GA, USA in 2009 and 2012.

Ms. Self is currently the Chief Engineer of the SSPIDR Program. Since 2011, she has been with the Air Force Research Laboratory, both as a contractor and civilian, in the Space Vehicles Directorate. She served as the Lead Mission Planner for the EAGLE spacecraft (launched in Apr. 2018) and executed the first successful deployment of an ESPA-Class satellite from a propulsive ESPA bus as well as coordinated the execution of mission objectives for EAGLE's nine different payloads during experimental and high-tempo on-orbit operations. From 2011 to 2016, Ms. Self was the Lead Systems Engineer of the AFRL's University Nanosat Program (UNP), serving as the SME for over forty universities as they developed, integrated, and test 10 small satellites, seeing four of those satellites through the operations phase.