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Design of High Performance Hybrid Type Digital-Feedback Low Drop-Out Regulator Using SSCG Technique

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ABSTRACT This paper proposes a high-performance Digital Feedback low-dropout voltage regulator (DF-LDO) for low power applications. In the DF-LDO regulator, digital feedback and applying spectrum spread clock generator (SSCG) technique are used to reduce output voltage ripples. In addition, it has triple operation modes i.e. coarse, fine, and retention for high efficiency and transient enhancement. The proposed hybrid DF-LDO uses arrays of PMOS transistors in coarse and fine mode whereas in retention mode, only one comparator and NMOS are active and digital controller goes into the sleep mode. This results in the reduction of the power consumption and improves the output voltage ripples. In the retention mode, minimum number of blocks operate that reduces the current consumption as compared to coarse and fine modes. To further reduce the current consumption, the comparator with hysteresis is used. The proposed circuit is designed using CMOS 55 nm process. The input voltage range is from 0.8 $\sim$ 1.5 V and the measured output voltage range is 0.756 $\sim$ 1.456 V. The measured line regulation is 6 mV / V, and the regulation starts when the input voltage is 0.8 V. The measured load regulation is 2.3 mV/mA for maximum load current of 5 mA. The peak current efficiency of the proposed DF-LDO is 99.996 % with a maximum output voltage ripples value of 1.9 mV. The proposed digital LDO regulator active chip area is 0.012 mm^2.

INDEX TERMS Digital LDO, fast settling time, hybrid type, low quiescent current, SSCG technique.

I. INTRODUCTION

The recent rapid growth of portable electronic devices such as battery-powered smartphones, laptops, and Bluetooth earphones requires the integration of circuits that require many functions in a limited area and low quiescent current. The Internet-of-Things (IoT) and battery operated devices also have limited life cycle, so it is vital to warranty the operation of the wireless devices for a longer period without charging [1]–[3]. Reference [4] explains the real challenge faced by the fine-grained supply management. In the line with this trend, the CMOS process is gradually developed as a deep submicron process, and the supply voltage of analog circuits is also lowered below 1V, and the LDO that supplies the voltage has a sub-threshold dropout voltage for maximum efficiency [5]–[7]. Need conventional analog LDOs to consume more current when the input voltage is lowered, which makes it difficult to catch the bias voltage and uses a large power transistor to supply voltage to a block that consumes large currents [8], [9]. In this regard, the design of digital LDO is necessary and has many advantages over analog LDO. First of all, it operates in a relatively low voltage operating area, and can also expect a reduction in current consumption and area, and also good inter-process scalability. The digital control method is insensitive to PVT change because it can be controlled by logic 0 or 1 only, and short circuit design time and relatively easy to design [10], [11]. A lot of research have been carried out to address this major challenge as digital LDOs can usually deliver optimal output voltage under low power condition's, such as near threshold

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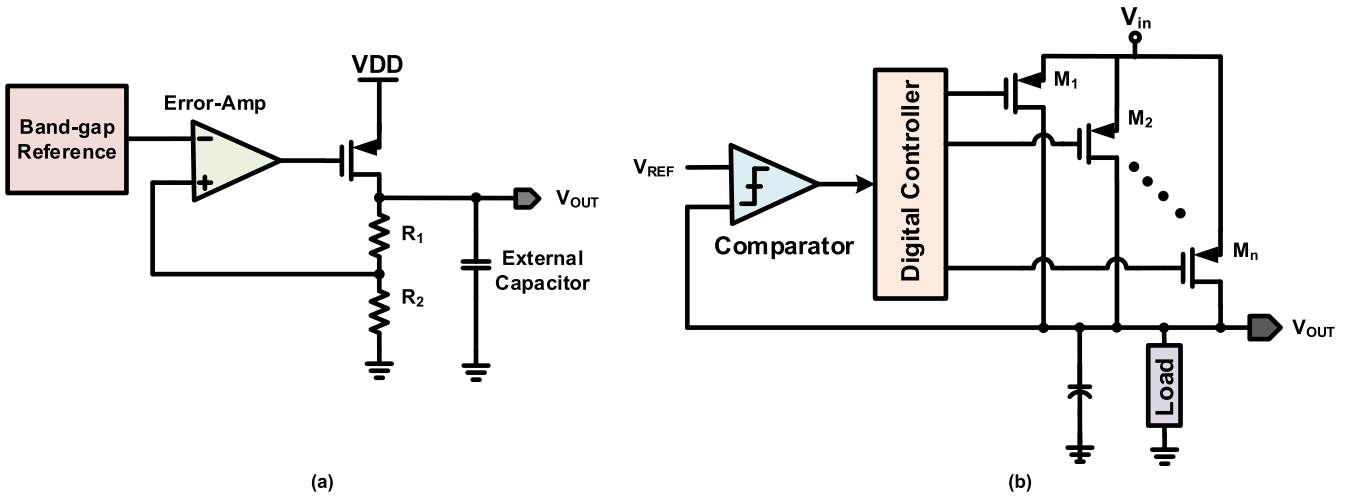

FIGURE 1. Block diagram of a conventional (a) analog LDO regulator and (b) digital LDO regulator.

voltage (NTV) levels. Furthermore, digital LDOs do not require compensation conditions and stability unlike analog LDOs [12].

In the literature review, many digital LDO regulator architectures are introduced. The baseline digital LDO [10] consists of a digital controller, latch comparator and switch array transistor. For fast transient response use long shift register. However, it is a tradeoff between fast transient response and quiescent current. Asynchronous D-LDOs have been designed to reduce power consumption of the shift registers [13]–[15]. On contrary, in asynchronous D-LDO, prestage output of the comparator triggers clock, eliminating the need for synchronous clock and thus reduces the static power of the shift register. However, under low supply voltage, the asynchronous D-LDO are more sensitive to process, voltage, and temperature (PVT) variations, degrading the robustness of the circuit robustness [16]. Power-speed tradeoff inevitably affects the load transient performance of the synchronous D-LDOs. During a load current transient, a large voltage is induced to D-LDO under over-shoot and a long recovery time is required [12]. In order to advance speed and power tradeoff, coarse/fine-tuning strategies have been adapted to speed up the response process by turning on/off transistor arrays of the large power MOS switch per bit [13], [17], and [15]. The analog-to-digital (ADC) converter or time-to-digital (TDC) converter can be used for multi-bit quantization [19]–[22]. However, there is a nonlinear relationship between propagation delay of buffer-gate and the supply voltage which results the degradation of TDC resolution [4]. Then, binary search control [19], [21], [23] and other compensation algorithms [11], [24]–[26] are utilized for digitized VOUT. In [12], [27], unary-weighted scale power transistor arrays are used in the D-LDO. Though, these techniques resolved tradeoffs between VRIPP-speed and power speed to some extent, there is still speed limitations suffered by using these approaches.

In this regard, we propose a digital feedback regulator design structure applying a hybrid type SSCG technique for low voltage systems. The power transistor fully turned on, hybrid type DF-LDO using NMOS and PMOS in coarse and fine mode. In retention mode, only one comparator and NMOS are active, and the digital controller in sleep mode. Because of this reduce the power consumption and enhance the output ripples. Only the minimum block operates, and the current consumption is less as compared to other modes. Furthermore, to reduce the current consumption, the comparator with hysteresis is used and the first stage of the inverter stage of the comparator output part is designed using NOR gate logic.

II. STRUCTURE

A. CONVENTIONAL STRUCTURE OF LDO REGULATOR

The conventional structure of the analog LDO regulator consists of an error amplifier, pass transistor, band-gap reference circuit, feedback resistor, external capacitor. It can be divided into two types according to the MOSFET type of pass transistor. Fig.1 shows an analog LDO and digital LDO regulator. The difference between the two types of regulators depends on which type of pass transistor is used, and they are all widely used. In addition, the feedback loop is formed differently into positive and negative accordingly. For NMOS type LDO regulator of Fig. 1(a). The gate voltage should be higher than the output voltage because of the threshold voltage. Therefore, the minimum drop-out voltage is determined by the threshold voltage. For PMOS type LDO regulator pass transistor is on when the gate voltage is lower than the supply voltage, so there is no limit to the supply voltage for the output voltage. Therefore, the drop-out voltage can be implemented low. The principle of operation is that part of the output voltage of the amplifier is feedback to amplifier according to the distribution ratio of the feedback resistor, and it outputs the signal amplified by the difference compared

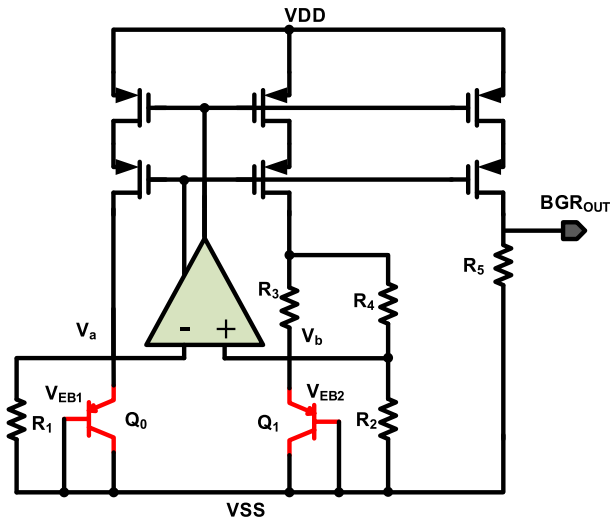

FIGURE 2. Block diagram of a conventional band-gap reference (BGR).

with the reference voltage which is the output of BGR, and the signal is driven by the pass transistor. As the output drops, the gate is controlled to make the output voltage constant. This can be represented by equation (1) [7].

$$V_{\text{out}} = V_{\text{REF}} \cdot (1 + R_1/R_2) \tag{1}$$

The conventional structure of digital LDO as shown in Fig. 1(b) is consists of a comparator, digital controller, PMOS and switch array. The comparator compares feedback voltage with a reference voltage and generate high/low output in binary form. In the digital controller long shift register used to true-on/off the PMOS in switch array [8].

Process parameters and temperature have a large impact on the circuit. So all analog circuits require circuits to generate reference voltages and currents that are insensitive to process and temperature. Among them, a band-gap reference (BGR) circuit is widely used to generate a reference voltage independent of process, temperature, and voltage. Fig. 2 shows the BGR schematic diagram of the basic structure. A typical BGR circuit is consist of temperature compensation circuit with a bipolar transistor and a resistor, an operational amplifier to help provide a stable supply of bias reference current, and a start-up circuit that helps start-up of the entire circuit when the feedback circuit and the supply voltage are applied and when the operation mode is switched from the sleep mode [9].

B. PROPOSED DIGITAL FEEDBACK LDO REGULATOR

Fig. 3 shows the proposed digital feedback low-dropout voltage regulator (DF-LDO) block diagram. The components include comparators, digital controller, resistor divider, PMOS and NMOS switch array and an external capacitor. The working principle is to compare the reference voltage ($V_{BGR1} = 0.46$ V, $V_{BGR2} = 0.42$ V) and the DF-LDO output voltage with a comparator, and then output is 'Low' or 'High' signal to produce a transistor array composed of MOS. It keeps the output voltage remain constant by turning it on and off. For low current consumption and quick transient response the three modes, coarse, fine, and retention, are using. The PMOS and NMOS switches sizes in coarse, fine, and retention mode respectively are 1 mm, 0.5 mm, and 0.25 mm. In addition, the clock is generated a periodically when using SSCG mode to minimize the ripple of the output voltage.

First, in the coarse mode, one comparator, a digital controller, and two PMOS switches operate in a flash type for high speed. In the fine mode, when output voltage of one comparator is set to Low, the CEN signal is activated as High which keeps the two comparators in the flash type. Since two comparators are turned on to consume more current, fast charging results in faster settling times. In fine mode, one comparator, digital controller, and seven PMOS switches operate as a SAR type. The voltage VBGR = 0.46 V and VFB is the feedback voltage generated by the voltage divider and given to the comparator. In the retention mode, the digital controller doesn't operate when retention enable (REN) signal is high as it turns-off the clock. Therefore, no ripple occurs in the output voltage. Only the comparator and retention mode NMOS switch are operating. It can reduce power consumption and occupy less area than the PMOS switch. If the positive input voltage is essentially dependent on the voltage given to the negative input, each comparator calibrated in digital LDO outputs 'High,' and outputs 'Low' if the positive input voltage is small.

C. DIGITAL LDO WITH FAST-SETTLING TIME

Fig. 4 shows the coarse and fine mode path diagram. For faster settling time, activate coarse mode by turning on 'CEN2'. At this time, the flash type comparator and two PMOS are operated. It compares the reference voltage and the analog input voltage, the outputs are high level. The speed is fast because the input voltage is received and compared at one time. Before the coarse mode is activated, it is operating in fine mode. In fine mode, SAR type comparator receives the input voltage and compares the status from MSB to LSB in order. When the DF-LDO regulator output voltage is less than the reference voltages (V_{BGR1}, V_{BGR2}), all zeroes are output and the load current changes abruptly, so the DF-LDO has a fast settling time. Fig. 5 is timing diagram of coarse and fine mode. When LDO_{OUT} is smaller than, V_{BGR1}, V_{BGR2}, the comparator one and two booth output is zero.

D. DIGITAL LDO WITH LOW POWER

In the retention mode minimizes the current and power consumption. by turning off the clock, the digital controller does not operate, and only one comparator and one NMOS switch operate. The retention mode has no output voltage ripple because the controller is off, and the implementation of NMOS takes up less area than the PMOS, it is maximizing the advantages of digital LDO. Fig. 6 shows retention mode path in the proposed DF-LDO regulator.

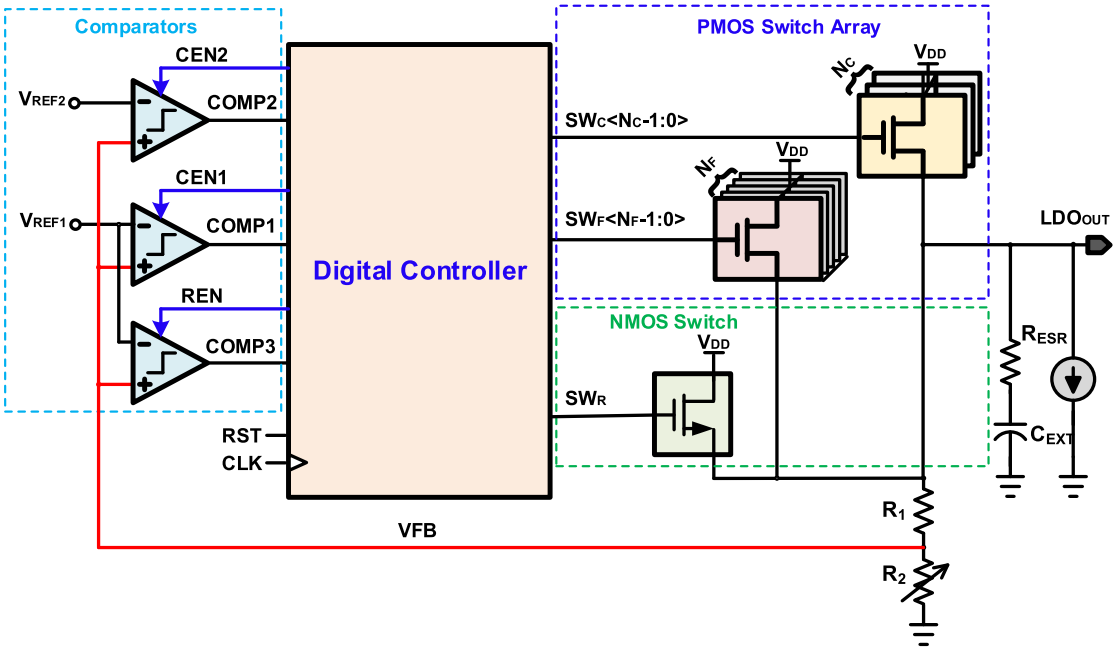

FIGURE 3. Block diagram of a proposed Digital-Feedback regulator (LDO DF-LDO).

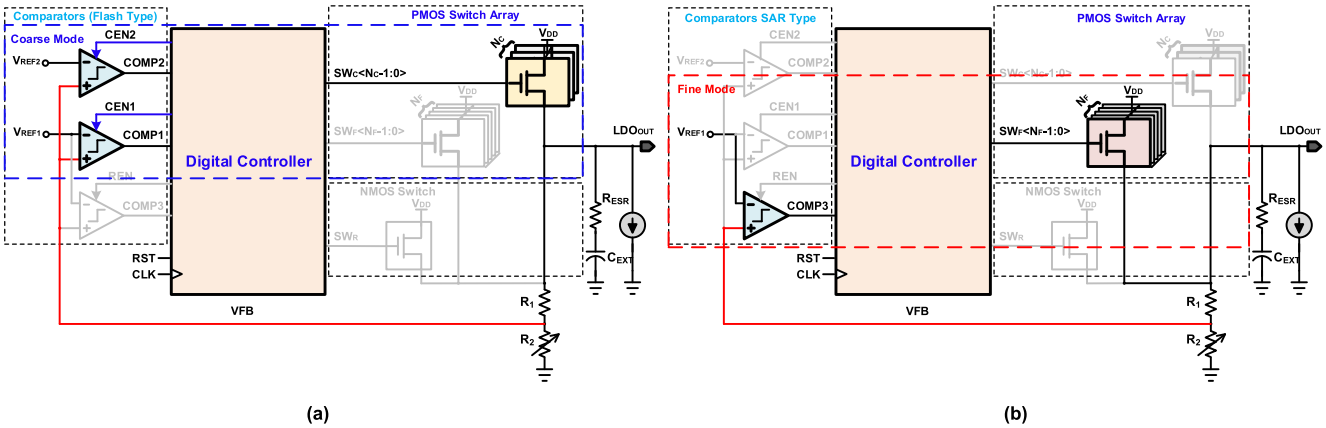

FIGURE 4. Block diagram of a proposed digital LDO (a) coarse mode and (b) fine mode.

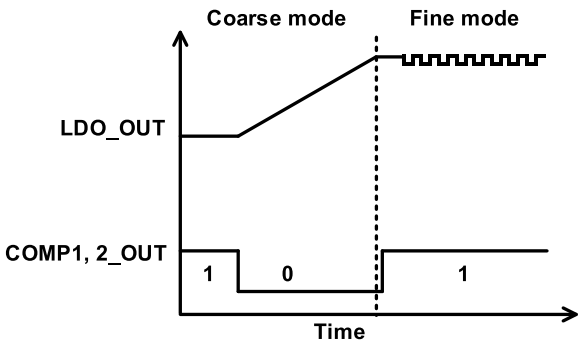

FIGURE 5. Timing diagram of coarse and fine mode.

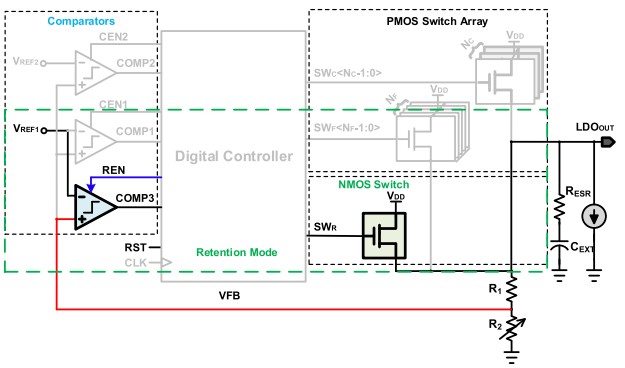

FIGURE 6. Block diagram of retention mode.

E. DIGITAL CONTROLLER FLOWCHART

The digital controller is the key building block and brain of proposed DF-LDO. It senses the load conditions through comparators and controllers the coarse and fine PMOS switch arrays and NMOS switch for fast transient. Fig. 7 shows the

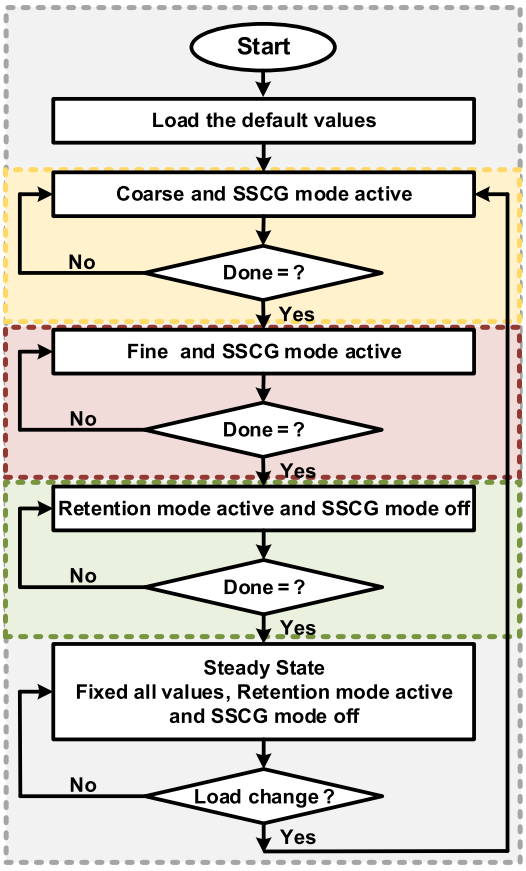

FIGURE 7. Digital controller finite-state machine (FSM).

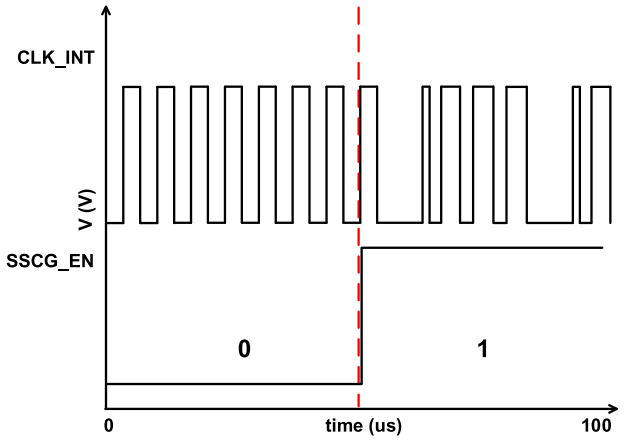

FIGURE 8. Concept of SSCG technique in digital LDO.

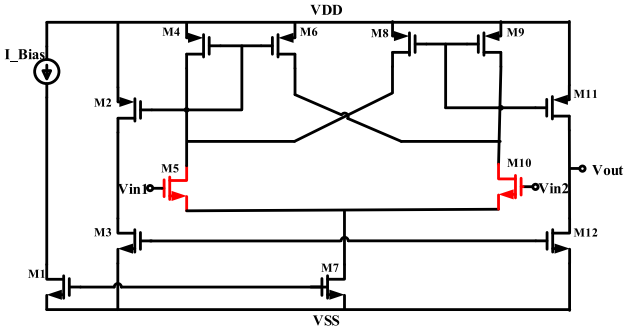

FIGURE 9. Diagram of a comparator with hysteresis architecture.

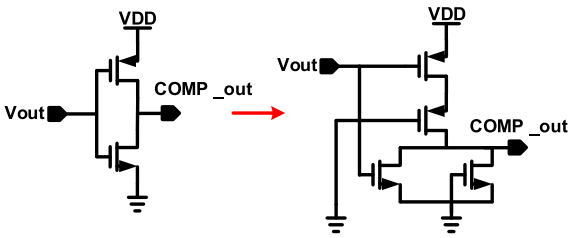

FIGURE 10. Diagram of decrease current architecture.

flow diagram of digital controller. It is designed as finite state machine (FSM) controller. On power up, it loads the default parameters. Initially, it enters in coarse state and controllers the coarse switch array with SWC<NC-1:0> signals. The SSCG mode is active to suppress noise. In this state, it turns on one switch at a time and after some settling delay, observes the feedback signals CMP1 and CMP2 through comparator. During heavy load or initial power-on (CMP1 = 0, CMO2 = 0), multiple coarse PMOS switches are on for fast transient and behaves in flash mode. After achieving first reference condition, (CMP2 = 1), controller enters to Fine state. In this state, SSCG mode remains active and controller turns on fine PMOS switch transistors in SAR manner to achieve desired output (CMP1 = 1). The controller then moves to Retention state and turns on NMOS switch by SWR signal. After settling, REN becomes high to turn off SSCG and clock. In this state, controller continuously monitors feedback signal through REN. Whenever load variation is sensed in steady state, clock is enabled and controller moves to coarse state for finding new switch conditions for desired load.

F. DIGITAL LDO WITH SSCG TECHNIQUE

A clock generator is used in most digital circuits. As the clock frequency increases clock edges may cause electromagnetic interference (EMI). The spread spectrum clock generator (SSCG) has recently become a popular method adopted to solve EMI issues and decrease peak energy value. The SSCG means that the clock operates only where you want it by spreading the clock period. It is mainly used to reduce the noise peak tone of the output. The clock signal in the frequency domain is high spike energy at the frequency clock. The SSCG is a way to distribute this spike over a band of frequencies to reduce the power at the frequency of signal. In order to eliminate the peak tone of the digital LDO output voltage, the design of this SSCG technique was applied. To implement this, a random generator in Digital Controller is constructed. The SSCG technique is implemented in digital controller, so the architecture independent of the process variation. The concept of SSCG technique in DF-LDO regulator is display in Fig. 8.

TABLE 1. Efficiency of cores mode.

Input		Output
A	B	Y
1	0	0
0	0	1

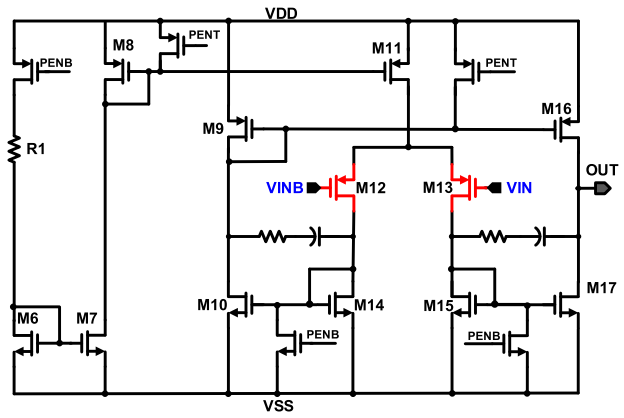

FIGURE 11. Block diagram of a proposed BGR amplifier.

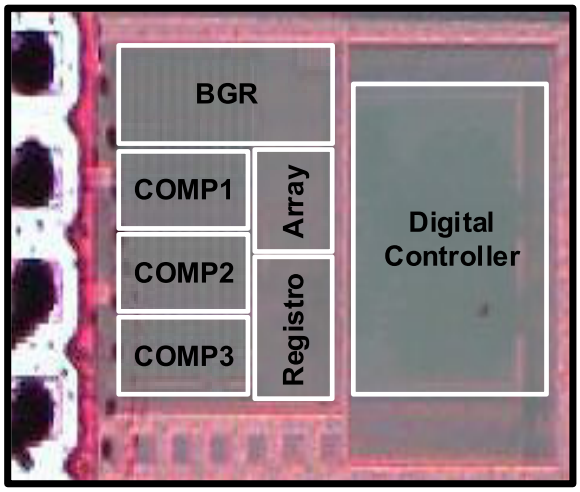

FIGURE 12. Layout of proposed DF-LDO regulator.

G. COMPARATOR WITH HYSTERISIS ARCHITECHTURE

In order to reduce the current consumption, the comparator was designed with a hysteresis structure as shown in Fig. 9. Since the voltage output from the V_{OUT} of the comparator is not a certain logic output, several inverter stages are used to make the output a certain logic output 'High' or 'Low'. At this time, the leakage current flows the most in the first inverter stage receiving the voltage. Therefore, tried to reduce the current consumption of the first stage inverter. The NOR gate is used instead of inverter using a logic circuit like NOR gate circuit of Fig. 10 and NOR gate truth table of Table 1.

One input is connected to the VSS voltage and fixed, and the inverter operates, but the impedance of the current path is increased to minimize the flowing current. As a result, the current flowing in the first stage inverter decreased from 20 nA to 1.8 nA and the current of the entire comparator also decreased from 3 uA to 1 uA. Table 1. shows the efficiency according to the number of cores.

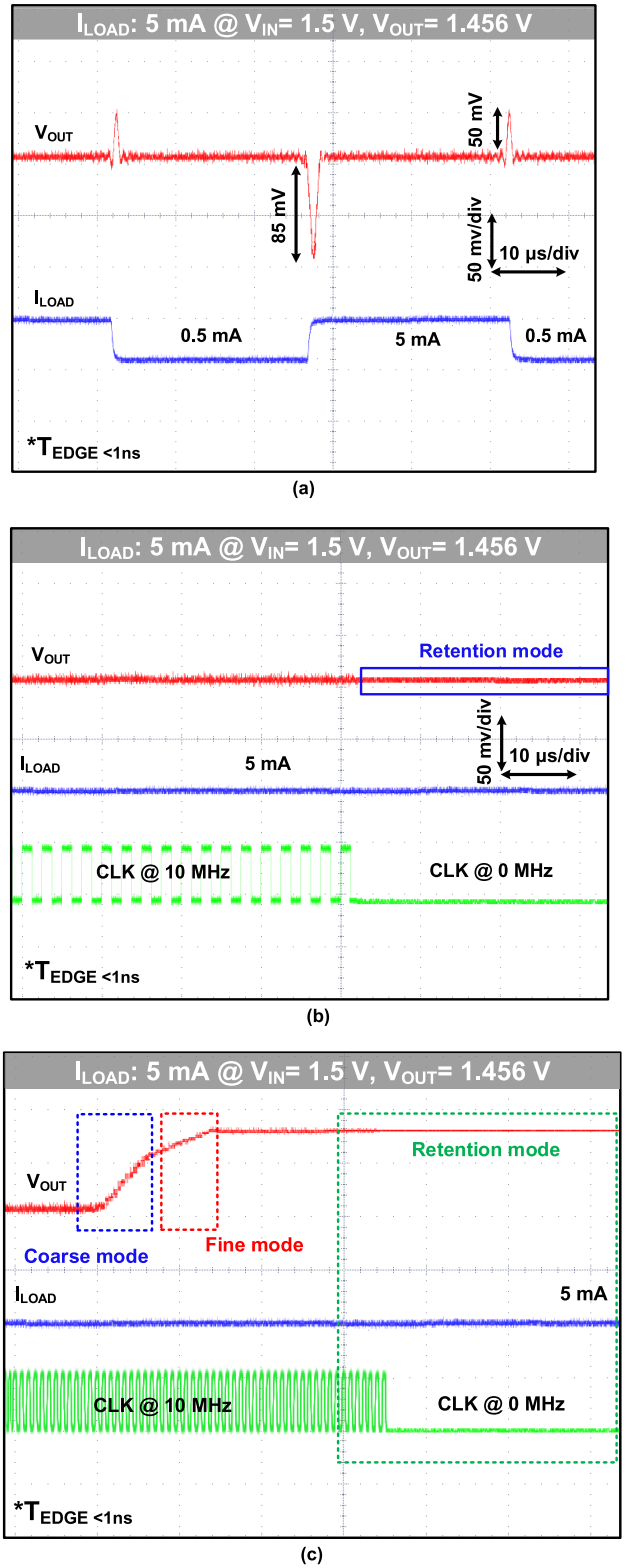

FIGURE 13. Measured load transient response (a) VIN = 1.5 V, VOUT= 1.456V, ILOAD = (0.5-5 mA), CLK = 10 MHz (b) Retention mode at VIN = 1.5 V, VOUT=1.456V, ILOAD = 5 mA, CLK = 0 MHz (c) Full operation at same conditions.

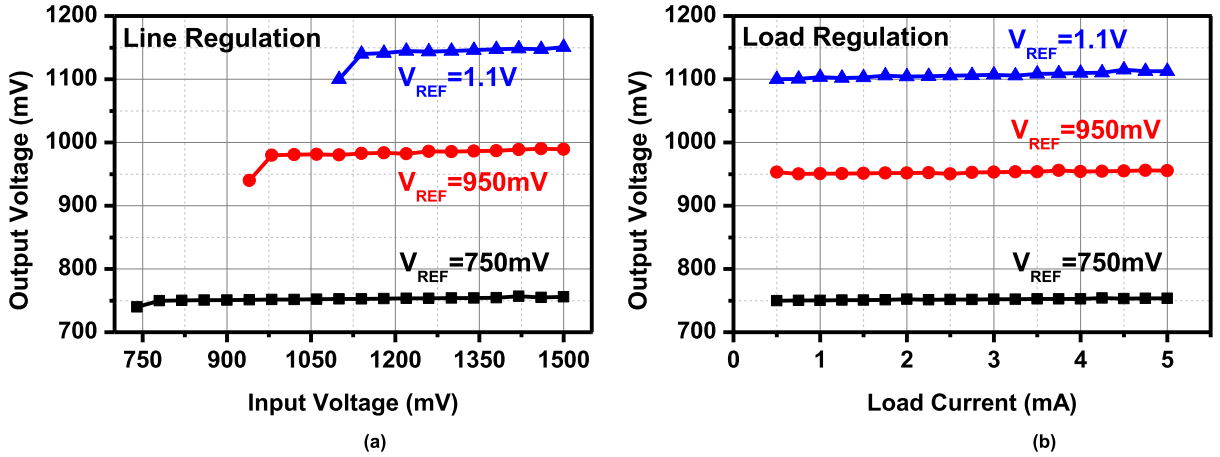

FIGURE 14. Measured (a) line regulation (b) load regulation at different reference voltage.

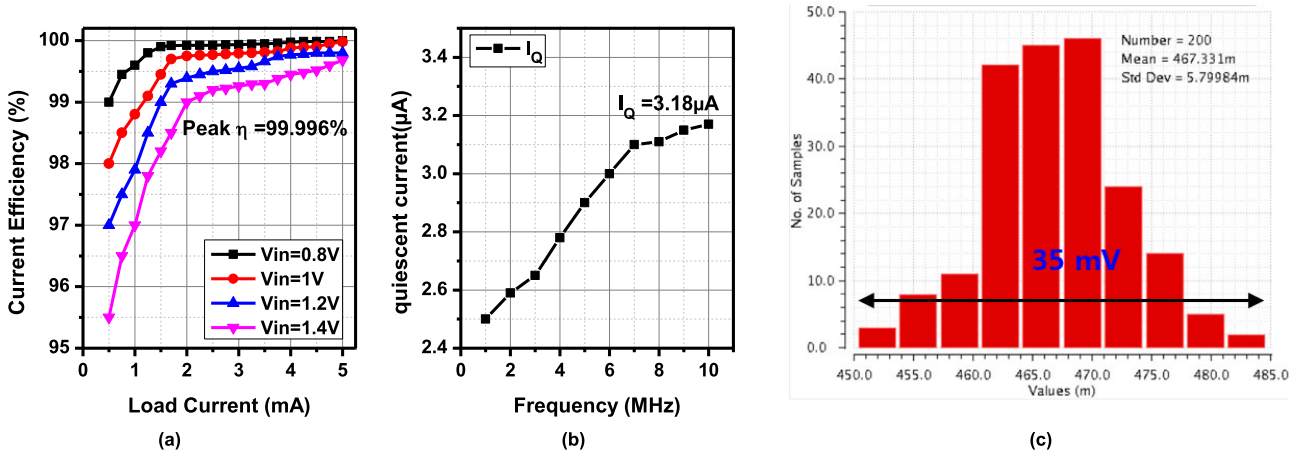

FIGURE 15. Measured (a) current efficiency with different input supply (b) quiescent current with frequency (c) BGR monte-carlo post-layout simulation.

H. LOW-NOISE BAND-GAP REFERENCE (BGR)

The band-gap reference (BGR) circuit is used to supply the reference voltage applied to the negative input. Fig. 11 shows the schematic of the amplifier used in BGR. The proposed BGR attempts to improve the variation of the BGR circuit's output voltage to maximize the advantages of the digital LDO which is insensitive to PVT changes. In addition, by using the deep n-well elements to reduce the noise of output voltage, noise generated in process is prevented, and flicker noise is reduced by adding RC filter at output stage. The monte-carlo simulation was used to analyse circuits without amplifier or core stage circuits to analyse circuits that mismatch is dominant among BGR core circuits that form BGR amplifier, PTAT and CTAT current. In simulation results, when the mismatch is applied only to the amplifier, it is confirmed that the variation of the output voltage is large. Secondly, to find the dominant part of the noise, noise simulation of amplifier and analysis noise summary an d monte-carlo simulation to analyse the dominant circuit among core circuit and bias circuit including input MOS, monte-carlo Simulation was conducted as before. As a final result, we confirmed that input MOS and core circuit of BGR Amplifier are dominant in noise.

In order to reduce mismatch and noise, increase the aspect ratio (Ratio of Width/Length) of the input MOSFET of the amplifier from 1.5 times to 2 times. Also, noise filter was performed once more by adding RC filter at output stage. In Layout, symmetrically place the layout, core MOSs including the input MOS sharing the source were layout as one MOSFET.

III. EXPERIMENTAL RESULTS

The proposed digital feedback low-dropout voltage regulator (DF-LDO) layout is exposed in Fig.12. It is fabricated in 55-nm CMOS technology with 0.012 mm^2 chip area. Fig. 13 show the transient measurement results. Fig. 13 (a) display the proposed DF-LDO regulator output voltage 1.456 V when the input voltage is 1.5 V at 5 mA load current and the operating frequency is 10 MHz. The maximum undershoot and overshoot are 85 mV and 50 mV when

TABLE 2. Performance comparison.

Parameter		This Work	[24]	[11]	[26]	[25]
Type		Digital	Digital	Digital	Digital	Digital
Process (nm)		55	65	65	65	130
Chip Area (mm^2)		0.012	0.17	0.034	0.012	0.114
INPUT (V)		0.8-1.5	0.6	0.5-1	0.5-1	0.5-1.2
OUTPUT (V)		0.756-1.456	0.5	0.45-0.95	0.35-0.95	0.45-1.14
ILOAD (mA)		0.5-5	0-100	10	2.8	3
Output Capacitor (pF)		22	100	100	100	100
IQ (μA)		3.18	34.6	4.2	45.2	24
Vdrop_Out (mV)		44	100	50	60	750
Operating Frequency (MHz)		10	100	10	12	10
Output Ripple (mv)	Fine Mode	1.9	37-53	3	10	3
	Retention Mode	0				
Transient Time (μs)		0.33	-	10	0.37	1.3
Load Regulation (mV/mA)		2.3	10	2.3	46	10
Line Regulation (mV/V)		6	-	30	-	3.5
Current Efficiency (%)		99.996	99.96	95.5	98.4	> 90
Power Efficiency (%)	SSCG ON	91.2	-	93.6	88.6	-
	SSCG OFF	95.14				

loading current change from 0.5 mA to 5 mA. Fig. 13(b) show retention mode, when REN is activated is high the NMOS switch operates. In addition, the clock is disabled and the digital controller stop working. So the average current as compared to normal mode is to reduce and eliminate the output voltage ripple. In Fig. 13(c) display full operation using same parameters. When the SSCG is OFF, the ripple of the output voltage is 3.2 mV, and after activation, the ripple of the output voltage is reduced by about 45% to 1.9 mV.

The proposed circuit has measured minimum 6mV/V line regulation when a reference voltage is 750mV at 5mA load current and maximum 12.3mV/V when a reference voltage is 1.1V as shown in Fig. 14(a). The load regulation is also checked at three different reference voltage when load variation is from 0.5mA to 5mA. When reference voltage is 750mV the minimum load regulation is 2.3mV/mA and maximum load regulation is 6mV/mA at 1.1V reference voltage as shown in Fig. 14(b). Fig. 15(a) shows the current efficiency at different supply voltage with different load currents. The proposed DF-LDO regulator measured power efficiency is 95.12 and peak current efficiency (η) is 99.996% at 0.8V input supply voltage and minimum current efficiency is 99.5% at 1.4V input supply voltage. The quiescent current IQ measurement with sampling frequency as shown in Fig.15(b). The maximum IQ is 3.18 μA at 10MHz sampling frequency. The monte-carlo post-layout simulation for band-gap reference (BGR) is shown in Fig. 15 (c). The BGR variation measurement results before and after the BGR amplifier's MOS size and layout arrangement, and the monte-carlo simulation results (200 times of Mismatch & Process). After revision, the variation decreased by 48.5% to 35 mV.

Table. 2 listed the comparison of high performance proposed DF-LDO regulator with the previous design. The proposed architecture has a fast transient response with low quiescent current and superior line and load regulation. It also has high current efficiency as compared to the published papers.

IV. CONCLUSION

This paper proposes a high-performance Digital Feedback low-dropout voltage regulator (DF-LDO) for low power applications. In the DF-LDO regulator, digital feedback and applying spectrum spread clock generator (SSCG) technique are used to reduce output voltage ripples. In addition, it has triple operation modes i.e. coarse, fine, and retention for high efficiency and transient enhancement. The proposed DF-LDO regulator is designed using CMOS 55 nm process. The active chip area is 0.012 mm^2. The input voltage is 0.8 $\sim$ 1.5 V and the output voltage range is 0.756 $\sim$ 1.456 V. The line regulation is 6 mV / V, and regulation starts when the input voltage is 0.8 V. The maximum load current is 5 mA in coarse, fine mode and load regulation is 2.3 mV / mA. The peak current and power efficiency is 99.997 % and 95.14 % with a maximum ripple voltage is 1.9 mV in fine mode.

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