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Enhanced Time Average Model of Three Phase Voltage Source Converter Taking Dead-Time Distortion Effect Into Account

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ABSTRACT Average switch simulation has the advantage of being much faster to simulate than the switching simulation but it lacks any harmonics or distortion on the converter current waveform. In a hardware converter, the current distortion is caused by the dead-time between high side and low side switching devices provided to avoid switch shoot-through. To improve the fidelity of average switch simulation, this paper provides a simple method to induce the distortion resulting from the dead-time. The result of average switch simulation can thus closely resemble the result of switching simulation in a fraction of the simulation time. To validate the accuracy of this average switch simulation, the result of this simulation is compared with the detail switching simulation and the waveform from actual hardware measurement.

INDEX TERMS Voltage source converter, time average modeling, dead-time distortion.

I. INTRODUCTION

Medium-and-high-voltage power switches such as MOSFETs and IGBT, are used in a variety of converter applications. Due to their finite turn-on and turn-off times, insertion of dead-time in the switching gate signal is needed to prevent short-circuits between the upper and lower switches of power converters. Nevertheless, this results in many negative effects on system operation such as output fundamental voltage reduction, current clamping [1] (zero-crossing distorton), and voltage and current harmonic distortions. To simulate the dead-time effect by means of electromagnetic transient simulators such as PSCAD/EMTDCS or PSIM, the simulation time step needs to be much smaller than the dead-time (typically 2 to 5 μs) to capture the distortions/non-idealities caused by the dead-time, leading to excessively long simulation times. This problem can be overcome by simplifying the detailed device models, and simulating the circuit using behavior mode models [2]. A time average model (TAM) is a behavior mode models where all switches are replaced with time-invariant equivalents. Although a TAM neglects the switching details and retains only the low-frequency harmonic components, such a model is sufficient for a practical converter system. Fig. 1 shows a typical current waveform of a three-phase, inductor filtered, VSC, operating at 60 Hz grid frequency and 12 kHz switching frequency. From the waveform and its corresponding harmonic spectra (Fig. 2), one observes that the harmonic components higher than switching frequency are negligible because they can be easily filtered by the current filters, demonstrating the validity of the TAM. Nevertheless, the zero-current clamping due to the dead-time effect is inevitable as shown in Fig. 1. The purpose of this paper is to incorporate the dead-time effects with the TAM for a voltage source converter (VSC).

Wu *et al.* [3], [4] have extended the double fourier series of pulse width modulated waveform (PWM) introduced by Black in 1953 [5] to account for the dead-time by adding a correction term. Chierchie *et al.* [6] extended these results to account for the dead-time in arbitrary band-limited

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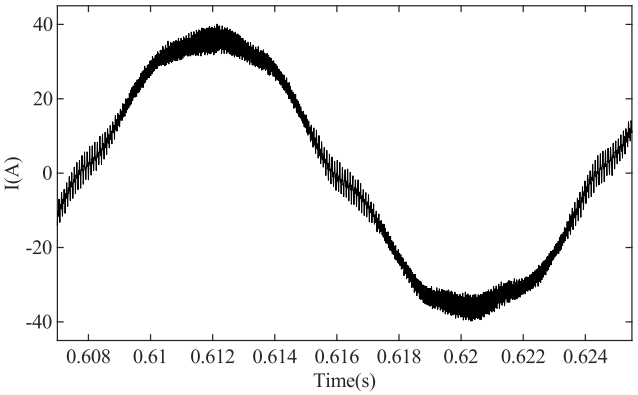

FIGURE 1. Experimental measurement of input current waveform on a three-phase VSC ($V_{grid} = 230$ V, $V_{DC} = 450$ V, $P_{out} = 10$ kW, $F_s = 12$ kHz, $T_d = 2$ μs).

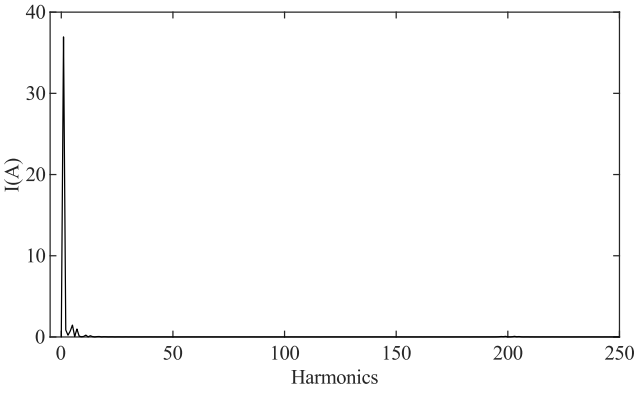

FIGURE 2. Harmonics of experimental measurement of input current waveform ($V_{grid} = 230$ V, $V_{DC} = 450$ V, $P_{out} = 10$ kW, $F_s = 12$ kHz, $T_d = 2$ μs).

modulating signals. However, all these methods can only be applied to a switching function model and cannot be applied to a TAM.

Mohan [7] explained the dead-time generation and also its effect on output distortion. Ahmed *et al.* [8] proposed an enhanced TAM of a VSC by calculating the effective duty cycle and applying the distortion using the definition from [7] and by modeling the voltage drop of diode and IGBT as error of duty cycle. However, such a method neglects the distortion of effective duty cycle in the vicinity of current zero crossing being null. Additionally, the voltage drop of the switches should not be represented as duty cycle distortion, because the voltage drop does not directly affects the DC-link current. Another approach proposed in [9] is to model a motor drive in the synchronous reference frame by adding the error introduced by the dead-time to the space vector using same distortion principle as [7]. Nevertheless, the effect of voltage drops of IGBT and freewheeling diodes (FWDs) are not considered.

While the TAM-VSC simulation with RL and induction motor load can be enhanced using method mentioned earlier, from our test the same method exhibits excessive distortion around the zero crossing region when used to simulate grid connected VSC. To address this issue, we propose an

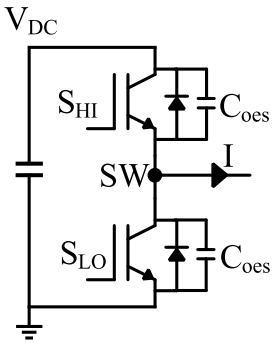

FIGURE 3. Half bridge structure consisted of upper and lower switches.

TABLE 1. Gating signal on time.

Switches	Ideal	With dead-time
S_{HI}	$D_{cmd}T_s$	$D_{cmd}T_s - T_d$
S_{LO}	$(1 - D_{cmd})T_s$	$(1 - D_{cmd}T_s) - T_d$

improved TAM distortion model, which has the following advantageous attributes:

- The zero-clamping distortion is well captured.
- The low harmonic distortions are modeled.
- The voltage drop of the switches and diodes are included and properly modeled.
- The proposed model can be easily added to the conventional TAM.
- The simulation time is minimum.
- The proposed model works very well for passive RL load and also for grid connected simulation.
- The resulting voltage and current waveform closely resemble with conventional simulation and experimental measurement.

II. ZERO CROSSING CURRENT DISTORTION ON VSC

A. PWM DEAD-TIME GENERATION METHOD

Fig. 3 shows the half-bridge structure, which is the basic building block of a two-level VSC. The upper (S_{HI}) and lower switches (S_{LO}) are switched in a complementary fashion with small amount of dead-time inserted in between the gating signal transition. The resulting on-time of each switches after dead-time insertion is shown in Table 1.

There are two timing arrangements on the implementation of the dead-time as depicted in Figs. 4 and 5. The first, is implemented by using rising edge delay by T_d on S_{HI} and S_{LO} while leaving the falling edge the same as without dead-time waveform. The second, is implemented by using two different duty cycles for S_{HI} and S_{LO} which can be calculated as $D_{HI} = D_{cmd} - 0.5T_dT_s$ and $D_{LO} = D_{cmd} + 0.5T_dT_s$ respectively. For both arrangements, the gate signals on time are equally reduced by T_d, but the difference is the second method maintains the symmetry of the gating signals while the first method causes a time delay of T_d. While the first method is generally more popular due to its long origin from analog controller IC, the second method is preferred in a

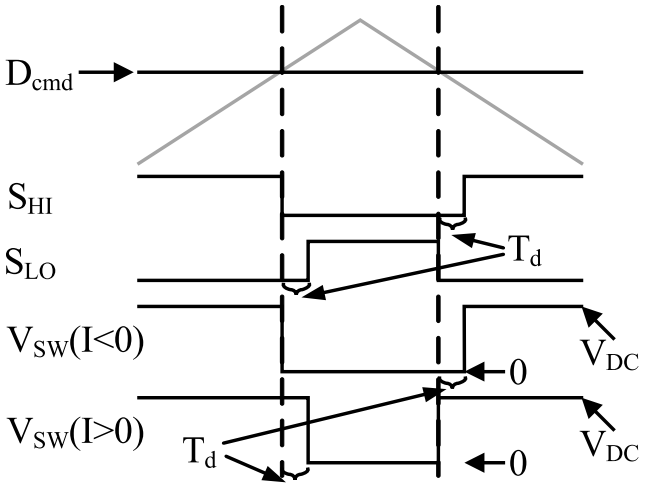

FIGURE 4. Delayed turn on based dead-time generation [7].

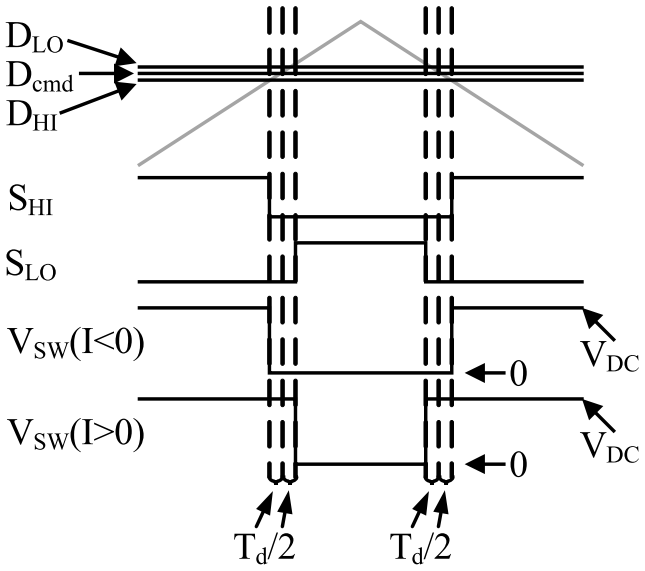

FIGURE 5. Delayed turn on + advance turn off based dead-time generation.

three-phase VSC and was selected to be used in this study due to the resulting lower harmonics thanks to its waveform symmetry characteristic.

B. DEAD-TIME INDUCED ZERO CROSSING DISTORTION

Current zero crossing distortion on a three-phase VSC is the result of dead-time causing deviation on the duty cycle of phase leg output voltage (D_o) from the duty cycle command by controller output (D_{cmd}). Alternatively, D_o is defined as a ratio of the duration of $V_{SW} = V_{DC}$ to the T_s within one period. This phenomenon is a result of output current I forcing V_{SW} to be equal to V_{DC} if $I > 0$ or zero if $I < 0$ during the duration of dead-time, effectively resulting in D_o to differ from D_{cmd} as described in Eq. 1 [7]. This definition will be referred to as the two level distortion approximation (2L-DA). Switching period average of the output current ($\bar{I}$) are used to define the distortion behavior since D_o is also defined in the similar manner.

$$D_o = \begin{cases} D_{cmd} - T_d F_s, & 0 < \bar{I} \\ D_{cmd} + T_d F_s, & \bar{I} < 0 \end{cases} \tag{1}$$

The previous commonly held understanding of this distortion, assumed that in one switching period there are two durations of dead-time and the V_{SW} are always the same for both within each switching period. However, [10] improves the definition of this distortion, by dividing the distortion of D_o into a three-level distortion approximation (3L-DA). The logic of this definition is, if during one switching period minimum peak ripple current and the maximum peak ripple current of I have different polarities, this results in different V_{SW} during the two dead-time duration, effectively resulting in $D_o = D_{cmd}$. Eq. 3 describes the mathematical definition of this phenomenon by using three levels based on $\bar{I}$ relative to the values of I_p and $-I_p$.

$$I_p = \frac{\Delta I_{pp}}{2} \tag{2}$$

$$D_o = \begin{cases} D_{cmd} - T_d F_s, & I_p < \bar{I} \\ D_{cmd}, & -I_p \le \bar{I} \le I_p \\ D_{cmd} + T_d F_s, & \bar{I} < -I_p \end{cases} \tag{3}$$

C. PEAK-TO-PEAK RIPPLE CURRENT ESTIMATION

The peak-to-peak ripple current (ΔI_{pp}) of a three-phase VSC is required to accurately obtain the behavior of D_o deviation from D_{cmd}. The literature [11] provides good explanation of ΔI_{pp} behavior on a three-phase VSC as a function of modulation index (m_i) and duty cycle phase angle (θ) as defined in Eq. 4.

$$\Delta I_{pp} = \frac{V_{DC}}{2 L_f F_s} \times f(m_i, \theta) \tag{4}$$

with $f(m_i, \theta)$ defined as
if $0 \le \theta \le \frac{\pi}{3}$

$$f(m_i, \theta) = \begin{cases} k_1, & 0 \le m_i \cos(\theta) \le \frac{1}{3} \\ k_1 + k_2, & \frac{1}{3} \le m_i \cos(\theta) \le \frac{1}{\sqrt{3}} \end{cases} \tag{5}$$

for

$$k_1 = m_i \cos(\theta) \left[1 - \sqrt{3} \sin\left(\theta - \frac{\pi}{3} \right) \right] \tag{6}$$

$$k_2 = 2\sqrt{3} m_i \sin(\theta) \left[m_i \cos(\theta) - \frac{1}{3} \right] \tag{7}$$

if $\frac{\pi}{3} < \theta \le \frac{\pi}{2}$

$$f(m_i, \theta) = m_i \left[\frac{1}{\sqrt{3}} \sin(\theta) - 3 m_i \cos^2(\theta) \right] \tag{8}$$

and m_i is defined as

$$m_i = \frac{D_{peak}}{V_{carrier}} \tag{9}$$

where $V_{carrier}$ is the peak to peak voltage of the carrier waveform.

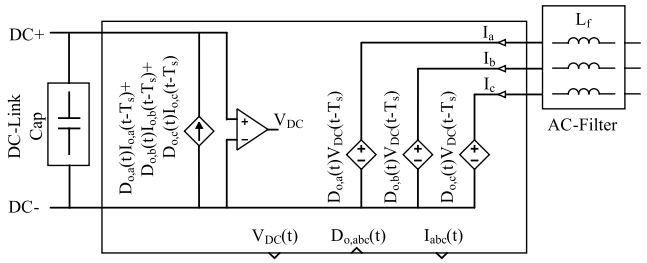

FIGURE 6. Conventional TAM structure.

For m_i in the range of 0 to $1/\sqrt{3}$ for space vector pulse-width modulation (SVPWM) in the linear operation range. Assuming, for phase A $D_a = m_i \cos(\theta)$ (without the zero sequence component) zero crossing occurs at $\theta = \pi/2$, the ripple current only needs to be observed at $\theta = \pi/2$, thus the equation can be simplified as Eq. 10

$$\Delta I_{pp}\Big|_{\theta=\frac{\pi}{2}} = \frac{V_{DC}}{2L_f F_s} \times \frac{m_i}{\sqrt{3}} \tag{10}$$

III. TIME AVERAGE MODEL

The structure of TAM for a three-phase VSC [2] consists of a pair of controlled voltage source and controlled current source to replace the switching circuit and duty cycle command D_{cmd} ranging from 0 to 1. In the converter output side, which is to be connected to output inductor filter, a controlled voltage source provides the output voltage $V_{o,abc}$ based on Eq. 11. In the DC-link side, which is to be connected to DC-link capacitor, a controlled current source is used to calculate the input current I_{DC} based on Eq. 12. Both voltage and current equations use previous value of V_{DC} and I_{abc} for the calculation to avoid algebraic loop issue, and its implementation schematic is shown in Fig. 6. Using simple linear equation for the TAM, allows the use of simulation step equal to the sampling period, which directly results in a fast simulation execution time.

$$\begin{bmatrix} V_a(t) \\ V_b(t) \\ V_c(t) \end{bmatrix} = V_{DC}(t - T_s) \begin{bmatrix} D_{o,a}(t) \\ D_{o,b}(t) \\ D_{o,c}(t) \end{bmatrix} \tag{11}$$

$$I_{DC}(t) = \begin{bmatrix} I_a(t - T_s) \\ I_b(t - T_s) \\ I_c(t - T_s) \end{bmatrix}^T \begin{bmatrix} D_{o,a}(t) \\ D_{o,b}(t) \\ D_{o,c}(t) \end{bmatrix} \tag{12}$$

IV. PROPOSED ENHANCED TIME AVERAGE MODEL

Although TAM-VSC simulation offers very fast simulation execution time, the use of all linear equation in place of switching networks combined with ideal D_{cmd} for the simulation resulting in an ideal waveform with zero harmonics/distortions. Another downside of TAM, is the lack of capability for start-up simulation since it cannot simulate the gate signal in the off condition prior to enabling the controller. Fig. 7 shows the overall proposed enchanced TAM structure, consisting of (a) distortion model to approximate the D_o, (b) modulation index estimator, and (c) auxiliary

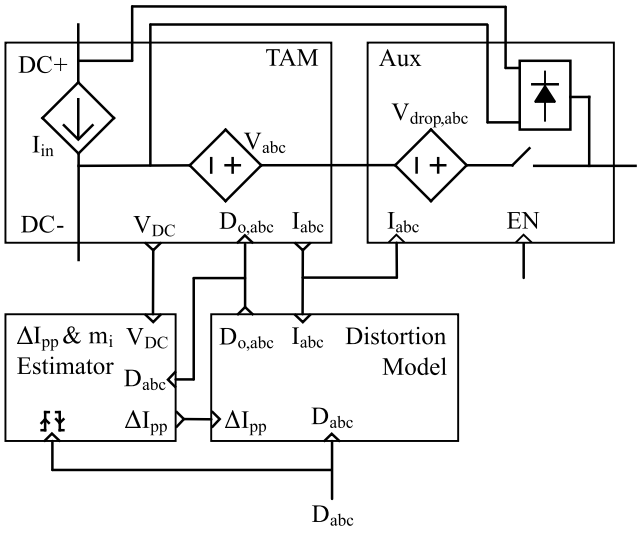

FIGURE 7. Complete structure of the proposed enhanced TAM.

circuit to enable TAM-VSC for the start-up simulation. The individual blocks of the proposed enhanced TAM structure will be explained in the following subsections.

A. DISTORTION MODEL

A distortion model is needed to enhance TAM simulation so its waveform can be more accurate when compared to the switching element model (SEM) simulation and hardware measurement. The enhanced TAM using a two level model for D_o method was previously conducted by [8]. However, such method only works well on a VSC with passive load as can be seen in Figs. 13 and 14, but it exhibits significant current zero crossing errors when used in a grid connected circuit especially at lower output power level (as shown in Fig. 16). The three-level model for D_o mentioned in Section III.B was used in enhanced TAM, which performs better than the conventional 2L-DA. Nevertheless, it exhibits strong current discontinuity during the zero crossing (this can be seen in Fig. 17). Although the SEM waveforms appear to have discontinuity in the transition between different distortion levels, this does not exist in measurement waveform as shown in Fig. 23.

The difference between actual hardware prototype and SEM and 3L-DA originated from the basic binary assumption on the V_{SW} of being 0 V or V_{DC} throughout the whole dead-time duration only depending on the current direction, and it causes a step transition between one level to the next level. Nevertheless, the actual transition between one level to another is a gradual transition resulting from output capacitance of the switches (C_{oes}). C_{oes} is the output capacitance for IGBT + FWD, as depicted in Fig. 3.

If the current flow through the switch has negative direction (current flows through FWD) right before the dead-time duration, then the voltage V_{SW} will remain the same as prior to dead-time duration.

If the current flow through the switch is in the positive direction (from collector to emitter for IGBT) right before dead-time duration, then there is a possibility for V_{SW} to change to another state. The time to discharge the output capacitance can be calculated based on the charge balance principle as stated in Eq. 13. When the $\bar{I}$ is not in the vicinity of the zero crossing, it is safe to assume that t_{dis} is very small, and V_{SW} can quickly transition from 0 V to V_{DC} or V_{DC} to 0 V accordingly. Nevertheless, when $\bar{I}$ is near zero crossing, t_{dis} can be anywhere from a fraction of dead-time duration to be even greater than the T_d. Thus, the average voltage of V_{SW} throughout the T_d is no longer discrete, and the assumption used in 3L-DA is incorrect. The behavior of V_{SW} during dead-time duration is illustrated in Fig. 8 in which the realistic behavior is shown on the left side of the figure and its discrete behavior approximation is depicted on the right side of the figure.

$$t_{dis} = \frac{2C_{oes}V_{DC}}{I} \tag{13}$$

In order to improve the simulation result of TAM, such behavior must be accounted for. For best accuracy, a distortion model based on explained characteristic can be used. That can be performed by analyzing individual dead-time instances within the switching period according to Eq. 13, by which the average V_{SW} voltage during the dead-time duration can be determined accordingly and can be converted into the equivalent duty cycle distortion. However, this method is complex and it does not guarantee accuracy because of the non-linear C_{oes} will significantly deteriorate the accuracy.

To further simplify the simulation approach, simple 5-level distortion approximation (5L-DA) as shown in Eq. 14 is introduced. The main idea originated from the effect caused by the IGBT output capacitance resulting in gradient transition between one distortion level to the next one. In this case the gradient transition is implemented by introducing two additional level to the 3L-DA. In this study, the additional distortion levels was placed at $+0.5\ I_p$ and $-0.5\ I_p$, which shows good agreement between the simulation and experimental results. In fact, this level setting is a very good approximation because normally the dead-time interval is very small (typically, 2 5 μs). A half point approximation is a simple and good approximation.

$$D_o = \begin{cases} D_{cmd} - T_d F_s, & I_p < \bar{I} \\ D_{cmd} - 0.5T_d F_s, & 0.5I_p \le \bar{I} \le I_p \\ D_{cmd}, & -0.5I_p \le \bar{I} \le 0.5I_p \\ D_{cmd} + 0.5T_d F_s, & -I_p \le \bar{I} \le -0.5I_p \\ D_{cmd} + T_d F_s, & \bar{I} < -I_p \end{cases} \tag{14}$$

The 5L-DA can also be represented in the schematic view as shown in Fig. 9 which combines the proposed model with ΔI_{pp} estimator from another subsystem and output limiter to limit D_o to 0 and 1. The addition of a limiter is necessary, since 5L-DA can results in D_o outside the allowable boundary

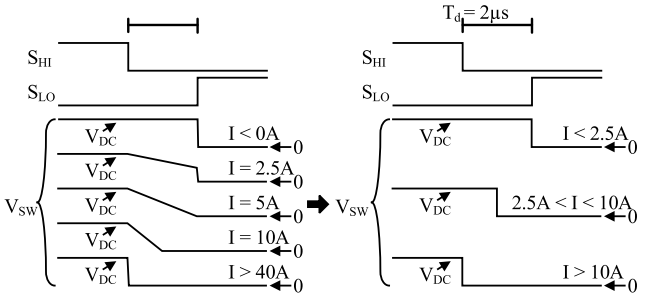

FIGURE 8. V_{SW} behavior during dead-time duration as a function of current direction and magnitude assuming constant value of $C_{oes} = 10nF$ and $V_{DC} = 500$ V, (left) realistic physical behavior, (right) simplified approximation.

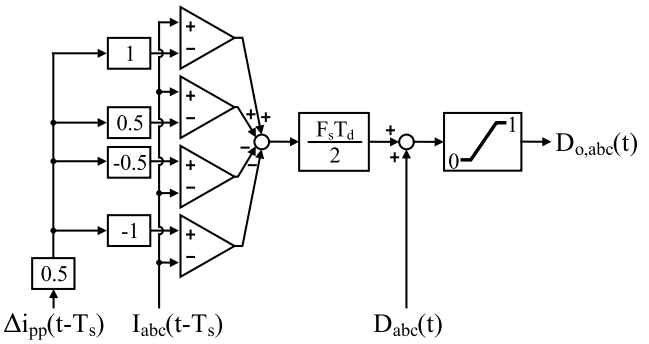

FIGURE 9. Proposed distortion model.

especially when D_{cmd} is already near the boundary such as during a transient which can cause the simulation to diverge.

B. MODULATION INDEX AND CURRENT RIPPLE ESTIMATOR

The performance of distortion model presented in section IV.A greatly relies on the accuracy of the current ripple estimation. This requires an accurate estimate of the modulation index of the control signal. One way of performing this estimation is by using three-phase PLL. However this method may require a complex tuning procedure and may not work well over a wide frequency range, leading to poor performance when the input signal has high distortion and/or a zero sequence component. Moreover, it also takes up a large amount of computation resource.

We developed a simple modulation index estimator based on simple trigonometric relationship between the three duty cycles of the VSC. The evaluation of the modulation indices is conducted at every zero crossing using the formula presented in Fig. 10. First, the zero-crossing event is detected when $D(t)$ is crossing 0.5 for any of the three phases. Then, the modulation index can be estimated by taking the absolute difference of the other two phases divided by $\sqrt{3}/2$, the trigonometry value of the two phases at this moment. m_i value calculated during zero crossing, is then held until the next zero crossing. Using the estimated m_i, ΔI_{pp} can be estimated by Eq. 10. The overall estimation structure is shown in Fig. 10.

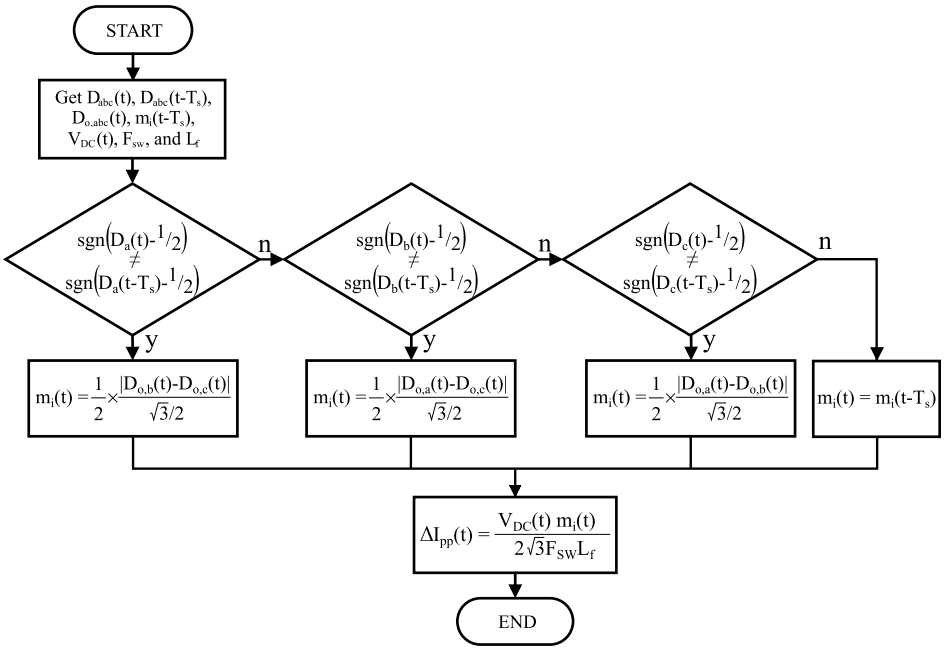

FIGURE 10. Flowchart of modulation index and ΔI_{pp} estimation.

C. AUXILIARY CIRCUITRY MODEL

The auxiliary circuit model is the last part of this enhanced TAM model, which aims to improve the proposed TAM by (a) modeling the voltage drop of IGBT and the FWDs and (b) diode rectifier and an enable switch.

First, in this paper, the total voltage drop (V_{drop}) of the IGBT ($V_{f(S)}$) and FWD ($V_{f(D)}$) is modeled as a controlled voltage source instead of distortion added to duty cycle as presented in [8]. While there is no significant difference in the simulation result, physically the voltage drop does not affect D_o. Thus such a model is not realistic. V_{drop} can be calculated by using Eq. 15, which describes V_{drop} as a function of D_o and I to calculate the time ratio of current flowing through IGBT and FWD.

$$V_{drop} = \begin{cases} D_o V_{f(D)} + (1 - D_o) V_{f(S)}, & \bar{I} > 0 \\ -D_o V_{f(S)} - (1 - D_o) V_{f(D)}, & \bar{I} < 0 \end{cases} \quad (15)$$

Second, the diode rectifier and enable switch are added so that the TAM can be used to simulate the VSC condition prior to turning on the controller. In the hardware VSC, i.e. before and during system start up, all control signals are off and the IGBT module will behave as a three-phase diode bridge rectifier. Although such a behavior can be easily captured by a SEM simulation, it cannot be simulated in a conventional TAMs because they are modeled by linear equation and lack body diode models. In fact, TAM during startup will short circuit the three phases. To overcome this, a simple enable switch and three-phase diode bridge rectifier is added as shown in Fig. 11, which simply disconnects the TAM circuit before controller is initiated. Thus leaving the diode rectifier as the only device connected between TAM and the rest of the circuit, similar to the behavior of ordinary IGBT module before controller is initiated.

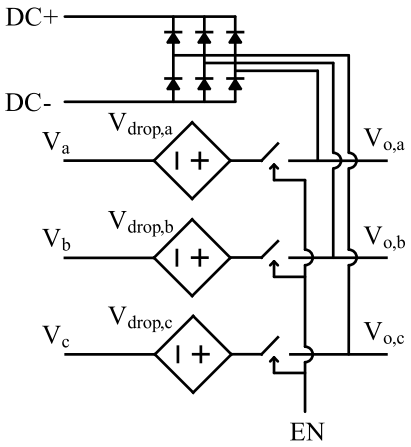

FIGURE 11. Auxiliary circuit schematic.

V. SIMULATION AND EXPERIMENTAL MEASUREMENT

In this section, the performance of the TAM with the proposed 3L-DA and 5L-DA is compared to TAM with 2L-DA, SEM, and experimental measurement. Simulation was developed on MATLAB/Simulink R2019b environment with SimScape to model the electrical circuit used in SEM and all TAM simulations. The proposed enhanced TAM algorithm was implemented using "MATLAB Function" blocks for all the algorithm parts and SimScape blocks for the electrical circuit model (controlled voltage sources and three phase diode bridge rectifier). Table 2 shows the circuit parameters used in the simulation for both passive load and PFC circuit,

TABLE 2. Circuit parameters.

Parameters	Value
IGBT Module	FS400R07A1E3-S7
V_f (IGBT // FWD)	1.5 V // 1.5 V
C_{DC}	1.39 mF
T_s	1/12000 s
T_d	2 μs
Passive load parameters	
V_{DC}	450 V
L_f // C_f	5 mH // 1.5 μF
R_{load}	10 Ω
PFC parameters	
L_f // C_f	500 μH // 1.5 μF
V_{grid} (line-line) // F_{grid}	230 V_{rms} // 60 Hz
V_{out}	450 V
Current Controller Gain	K_p = 0.64 // K_i = 179.4
Voltage Controller Gain	K_p = 0.36 // K_i = 30

and also hardware prototype for PFC circuit. This section is organized as follows: Firstly, we will compare the proposed TAM with SEM, and then, we will compare the best TAM result presented in first section, SEM, and experimental measurement.

To evaluate the performance of different simulation methods and experimental measurements, simulation waveforms will be presented to provide visual comparison to the reader of the different methods. The waveform of TAM with different distortion methods will be compared with SEM and experimental measurement. Additionally, error of different distortion methods is compared by taking the difference of TAM methods with the ''reference'' waveform which are SEM current waveforms for Case II and experimental measurement current waveforms for Case III. For quantitative measure, peak-to-peak error and normalized root mean square error (NRMSE), as stated in Eq. 16, is used to show how closely matched are the TAM and the benchmark (SEM) simulation current waveform result, with the smallest number yielding the most accurate result. Additionally, current THD is also used for comparison, the TAM result with closest value to the benchmark yields the most accurate result.

$$NRMSE = \frac{1}{X_{rms,SEM}} \times \sqrt{\frac{1}{N}\sum_{i=1}^{N}(X_{i,\overline{SEM}} - X_{i,avg})^2} \quad (16)$$

A. CASE I

The first case is to study the simulation performance of VSC with a passive LC filter supplying a resistive load, as shown in Fig. 12.

Figs. 13 and 14 show the steady-state current waveform of the three different TAMs compared to SEM and also the error between TAMs and $\overline{SEM}$ (switching period current average of SEM), for $m_i = 0.125$ and $m_i = 0.5$, respectively. By visual analysis of the current waveform, the result of all TAM methods are consistent with SEM for both m_i. Nevertheless, one can see that the proposed 5L-DA model yields the smallest error. This becomes obvious when m_i becomes smaller, which

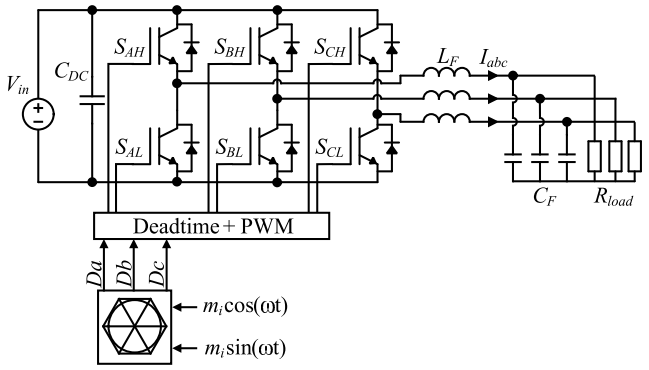

FIGURE 12. VSC with passive LC filter and resistive load.

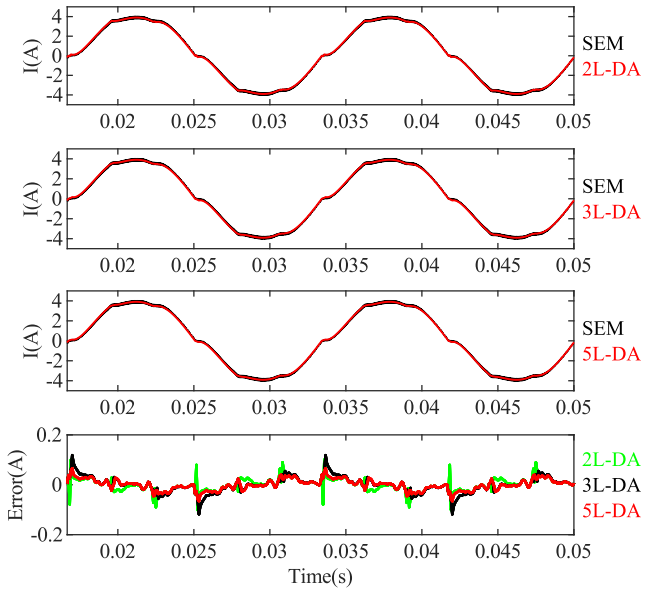

FIGURE 13. Phase current waveform at $m_i = 0.125$ with passive load for different TAM methods.

results in stronger zero crossing distortions. Fig. 14 shows that when $m_i = 0.5$, the three TAMs yield a smaller error. However, when $m_i = 0.125$ as shown in Fig. 12, the error for the 5L-DA is the smallest.

Table 3 provides the summary of simulation results that show 5L-DA simulation has the least peak-to-peak error and smallest NRMSE compared to 3L-DA and 2L-DA. The current THD of 5L-DA is slightly lower than that of 2L-DA at $m_i = 0.125$ and the same current THD at $m_i = 0.5$. In general, 5L-DA when used in passive load circuit has the best performance compared to other methods, although the difference is not significant.

B. CASE II

For the second test, the performance comparison was done using a grid-connected VSC circuit operating as an active rectifier with regulated output voltage and unity input power factor. As shown in, Fig. 15, PI controllers were used to regulate the output voltage by providing $I_{d,ref}$. The inner currents, converted to the synchronous reference frame by the

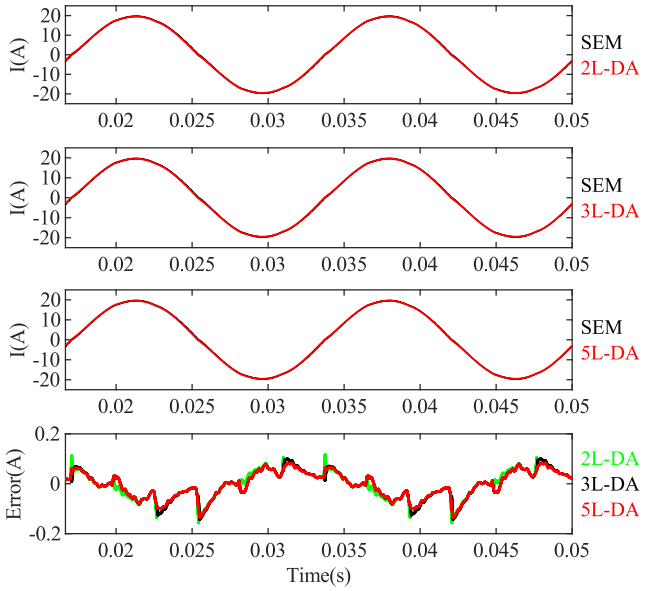

FIGURE 14. Phase current waveform at $m_i = 0.5$ with passive load for different TAM methods.

TABLE 3. Error summary of different TAM methods for passive load circuit simulations.

	Peak-to-Peak Error (A)	NMRSE(%)	THDi(%)
	$m_i = 0.125$, I_{SEM} (RMS = 2.8256 A and THDi = 7.064%)		
2L-DA	0.203	0.933	6.603
3L-DA	0.238	1.065	6.510
5L-DA	0.132	0.774	6.593
	$m_i = 0.5$, I_{SEM}(RMS = 13.918 A and THDi = 1.821%)		
2L-DA	0.274	0.407	1.646
3L-DA	0.244	0.398	1.633
5L-DA	0.219	0.377	1.646

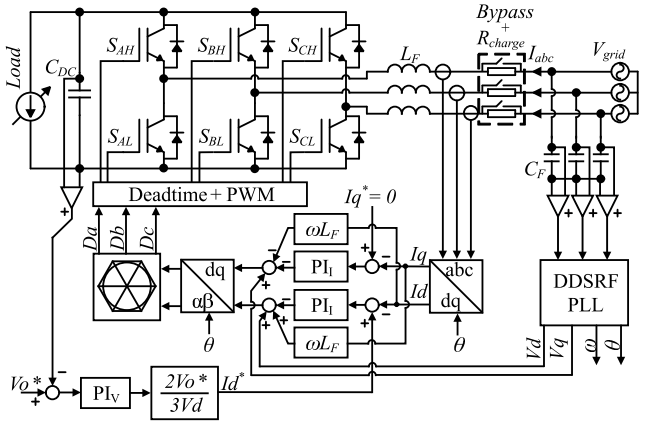

FIGURE 15. PFC circuit with synchronous reference frame current controller.

Park transform, which are regulated by the PI controllers. The phase angle required by the Park transform and its inverse was obtained using the double decoupled synchronous reference frame PLL (DDSRF-PLL) [12]. Various operating conditions, including step load increase and decrease, VSC start-up, and steady-state are investigated to justify the proposed model.

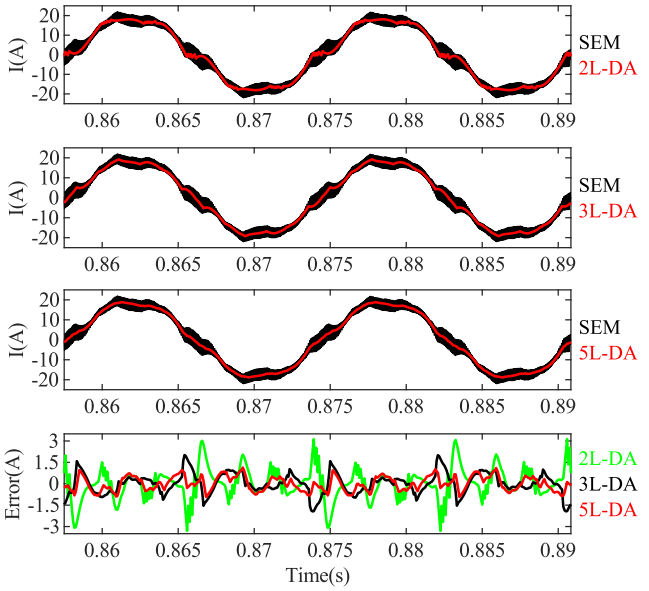

FIGURE 16. Phase current waveform at 5 kW load for different TAMs compared to SEM.

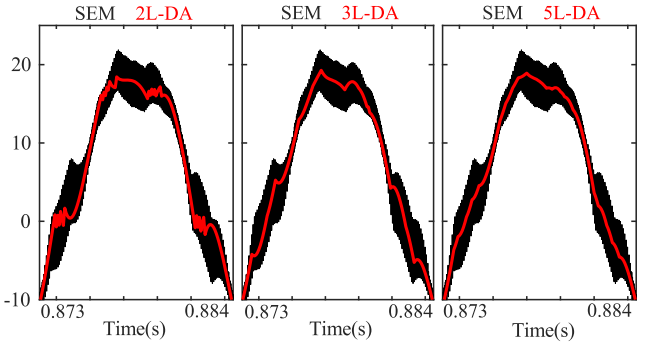

FIGURE 17. Phase current waveform at 5 kW load for different TAMs compared to SEM (zoomed from t = 0.873 s to t = 0.8845 s).

The steady-state current waveform is shown in Figs. 16 and 18 operating at 5 kW and 10 kW output power. Unlike Case I where the three TAM methods have very similar current waveforms, the three TAMs in this case yield different current waveforms especially at lower power output due to longer duration of the current within $\pm I_p$. For $P_{out} = 5$kW, the current waveform for 2L-DA shows around zero crossing (the detailed waveform is provided in Fig. 17) where current is clamped at zero for long time; for 3L-DA zero clamping no longer exists but some discontinuities are shown, the 5L-DA shows the smoothest zero crossing waveform. From the error plot, the 2L-DA shows very large error compared to 3L-DA, which is smaller, and 5L-DA is the smallest. Similar characteristics are also shown at the current waveforms at $P_{out} = 10$ kW, although the distortion is not as significant as current waveform at $P_{out} = 5$ kW.

Table 4 summarizes the simulation results, indicating that 5L-DA simulation now has significantly the lowest peak-to-peak error and NRMSE, 3L-DA with the larger error, and 2L-DA has the largest error. For current THD, 5L-DA

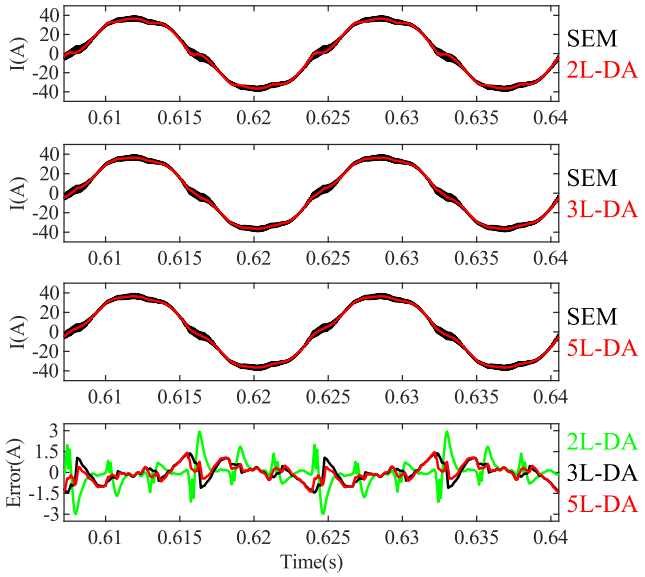

FIGURE 18. Phase current waveform at 10 kW load for different TAMs compared to SEM.

TABLE 4. Error summary of different TAM-PFC methods for PFC simulation.

	Peak-to-Peak Error (A)	NMRSE(%)	THDi(%)
	P_{out} = 5kW, I_{SEM} (RMS = 14.911 A and THDi = 9.503%)		
2L-DA	6.017	8.1372	13.268
3L-DA	3.953	5.3616	6.590
5L-DA	2.063	3.7349	7.463
	P_{out} = 10 kW, I_{SEM} (RMS = 27.717 A and THDi = 7.353%)		
2L-DA	5.951	3.2171	8.636
3L-DA	2.827	2.3669	6.317
5L-DA	2.761	2.0787	6.719

also exhibits the nearest THD value with SEM simulation. In this VSC simulation, 5L-DA shows best accuracy with very significant improvement over the existing methods.

C. CASE III

After comparing the simulation results on passive load and PFC circuits both at steady state, it can be concluded that 5L-DA shows the best result over 3L-DA and conventional 2L-DA. Thus, from hereby only 5L-DA simulation was used to compare with SEM for load transient and startup simulations.

Figs. 19 and 20 present the load transient output voltage, three-phase sinusoidal input current, and synchronous reference frame I_d and I_q waveforms under step load increase and decrease from 5kW to 10kW and vice-versa. All 5L-DA simulation waveforms match very closely, including I_d and I_q waveforms, under both transient simulations. The realistic I_d and I_q waveforms are well preserved by the 5L-DA, meaning one can directly visualize the controller behavior without using a SEM.

Simulation on VSC startup transient was conducted and its results are depicted in Fig. 21. The operation procedure of this simulation consists of three stages. The first is to pre-charge the output capacitor via pre-charge resistor to slowly bring

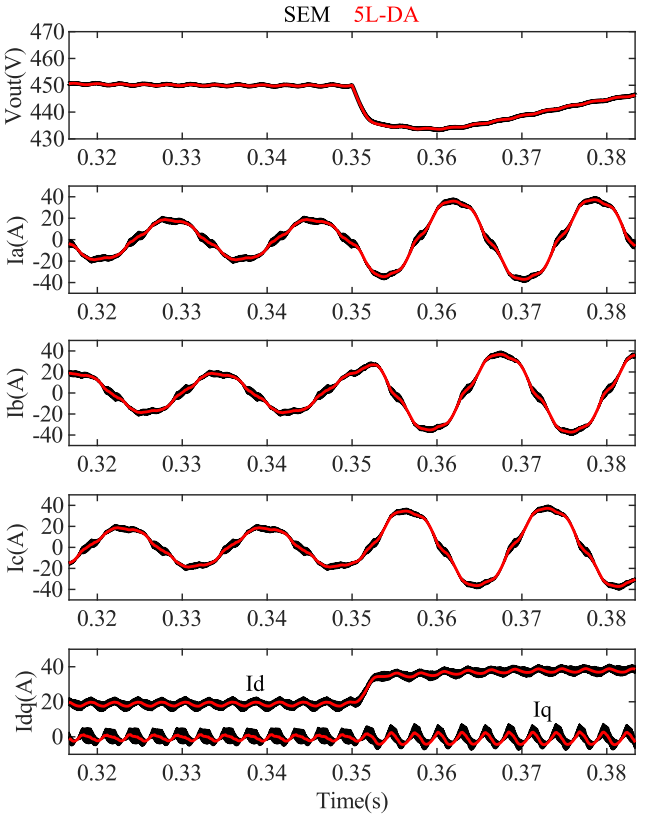

FIGURE 19. Phase current waveform at 10kW load for different TAMs compared to SEM.

the output voltage from zero to $\sqrt{2}V_{grid}$, where V_{grid} is the input line-to-line voltage. During the first stage, all IGBT switches are off and power resistor is connected in series with L_f to limit the current. Here in the second stage, the current is first limited to 20 A for soft-start and then at the third stage, the current limit is set to 60 A, allowing a rated current of 40 A to flow with some margin to allow for transient dynamic. Using this three-stage configuration, the output voltage can be brought to the nominal value at slower manner without causing excessive inrush current. The timing configuration at converter startup is 0.091 s for pre-charge, 0.05 s for second stage, and followed by normal operation at the third stage. Simulation waveform at start-up condition closely matches with the SEM simulation for the three different operation stages.

D. COMPUTATION PERFORMANCE OF TAM AND SEM SIMULATIONS

The main advantage of conducting simulation with TAM is its fast simulation capability. Note that it takes only 194 ms CPU time[1] for the proposed 5L-DA model to run for one second of the simulation time, while it takes 80.8 s for the SEM with a time step of 0.167 μs to accurately model the switching behavior of VSC. Hence, the 5L-DA model runs 400 times faster than the SEM.

[1] All the simulations were carried out using a desktop computer with CPU AMD Ryzen 5-3400G, 3.7 GHz base speed and 4.2 GHz boost speed, and 16 GB or RAM

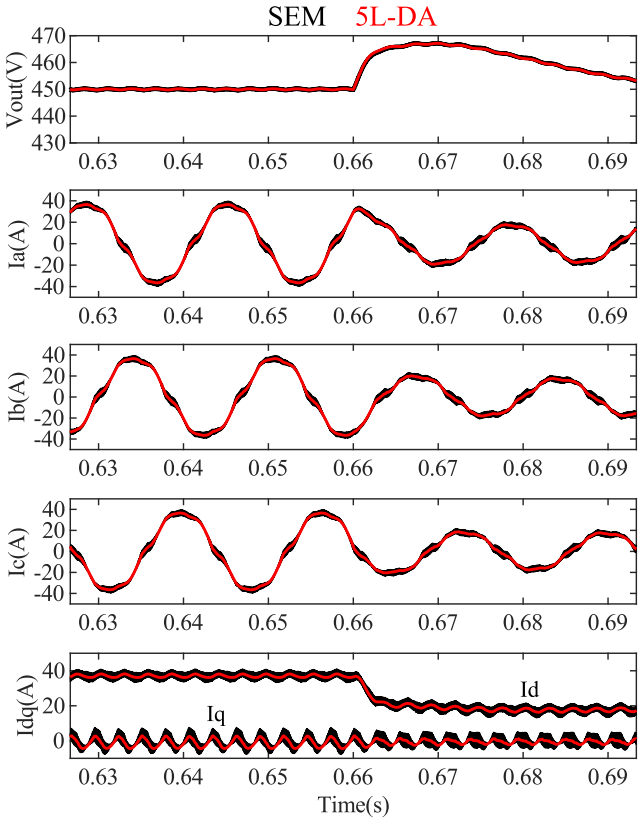

FIGURE 20. Phase current waveform at 10kW load for different TAMs compared to SEM.

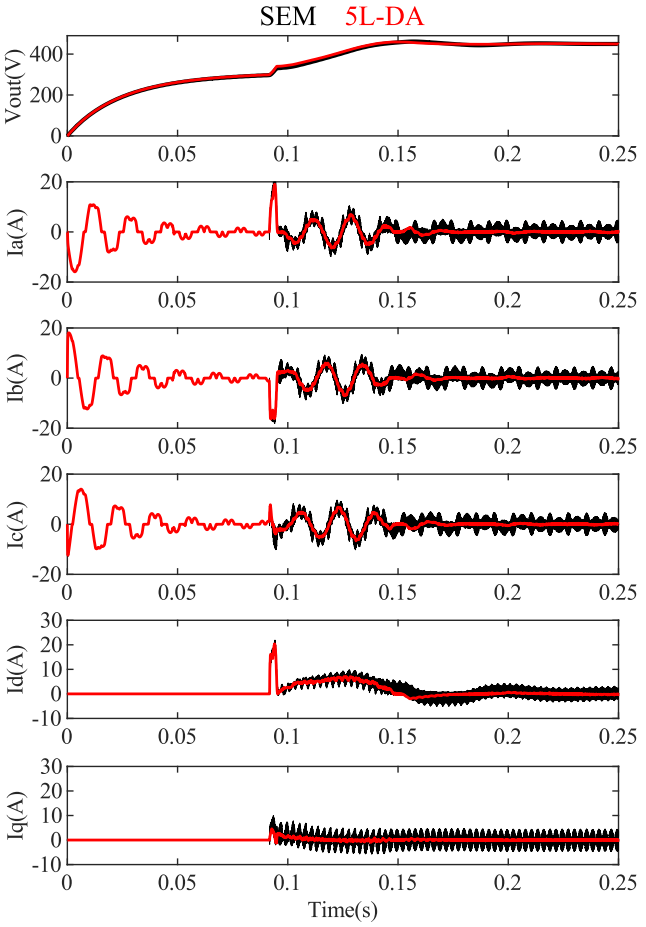

FIGURE 21. Converter startup waveform for SEM and 5L-DA.

The issue with detailed simulation using switching element model (SEM) on many of the simulation softwares are the simulation time does not scale up linearly with the number of circuit nodes, which often increase non-linearly depending on the solver used by the software. Additionally, when a circuit simulation contains non-linear element (such as switches and diodes), the simulator needs to update the circuit computation matrix multiple times within one switching period to ensure that the right condition is being simulated. These two conditions combined with long time constant and switching elements then resulting in very long computation time. The results of the proposed method are very satisfactory when compared with those from the experiment and simulation software. Essentially, all the low-order harmonics were well captured by the proposed method. Moreover, the simulation time is significantly smaller than that of the SEM. Consequently, the proposed method not only can effectively shorten the simulation time but also accelerate the converter control design process. The designer does not need to switch between TAM model to the SEM model to see the effect of the non-linearity and the related low-order harmonics problem.

E. COMPARISON OF EXPERIMENTAL MEASUREMENT AND SIMULATION (VSC AS ACTIVE RECTIFIER)

In this section, we will validate the proposed model experimentally. Fig. 22 shows the experimental setup for Fig. 15.

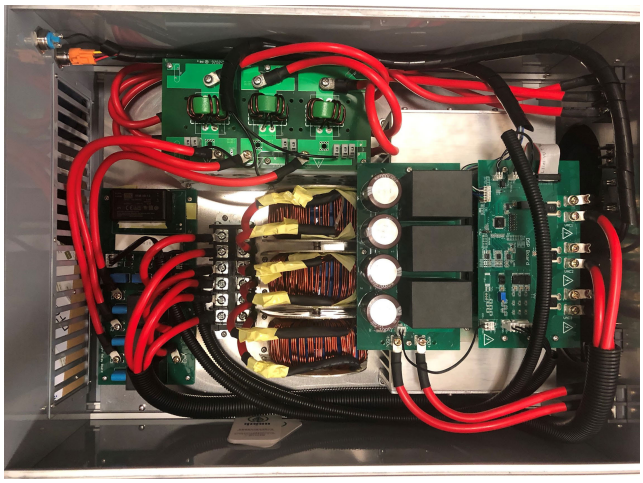

FIGURE 22. Hardware prototype of three phase VSC.

The controller was implemented using Texas Instruments TMS320F28035 (60MHz clock speed).

Figs. 23 and 24 show the steady-state waveforms for 5 kW and 10 kW loads. Both figures show that the waveforms of SEM closely match with those from experiment. The proposed 5L-DA model, though it does not exhibit the high frequency distortion caused by the switching ripple of SEM,

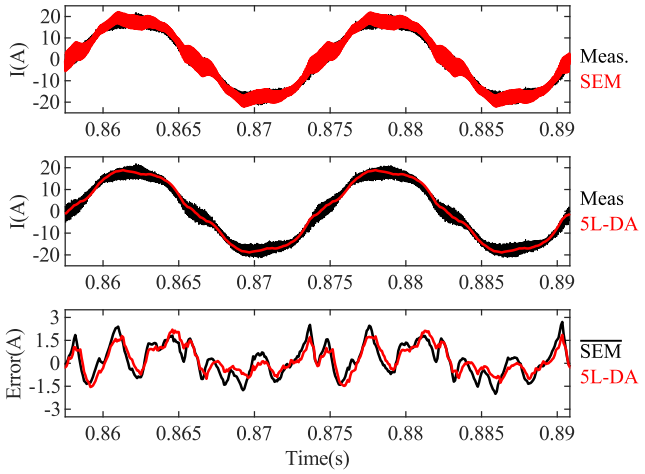

FIGURE 23. Phase current waveform at 5 kW load for 5L-DA and $\overline{SEM}$ compared to measurement waveform.

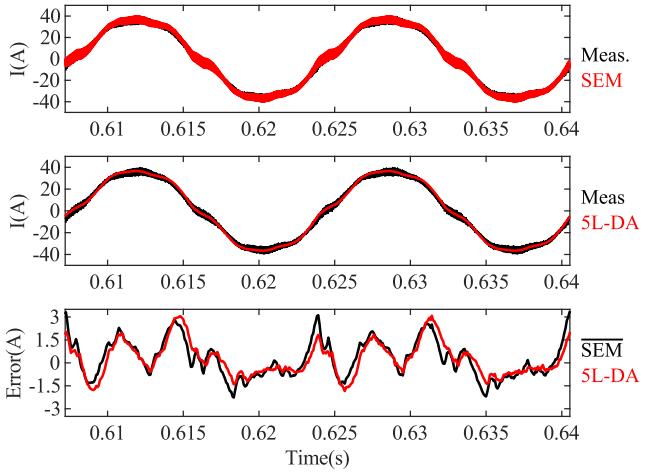

FIGURE 24. Phase current waveform at 10 kW load for 5L-DA and $\overline{SEM}$ compared to measurement waveform.

TABLE 5. Error summary of $\overline{SEM}$ and 5L-DA compared to measurement.

	Peak-to-Peak Error (A)	NMRSE(%)	THD(%)
	P_{out} = 5 kW, $I_{Meas.}$ (RMS = 12.906 A and THDi = 8.091%)		
$\overline{SEM}$	4.702	8.101	9.503
5L-DA	3.755	6.986	7.463
	P_{out} = 10 kW, $I_{Meas.}$(RMS = 27.717A and THDi = 5.768%)		
$\overline{SEM}$	5.579	4.808	7.353
5L-DA	4.922	4.346	6.719

reproduce the distortions caused by the dead-time and those of the low-order harmonics. Therefore the difference between 5L-DA and the actual hardware is very similar and consistent with that between SEM and experimental measurement.

Table 5 quantitatively compares the results of SEM and 5L-DA. The 5L-DA model have lower peak-to-peak error and NRMSE compared to SEM for both 5kW and 10kW operating condition. For the current THDs, the values predicted by the 5L-DA models are also very close to those obtained experimentally. In fact, the 5L-DA predicted that the THD increases when the load changed from 10 kW to 5 kW.

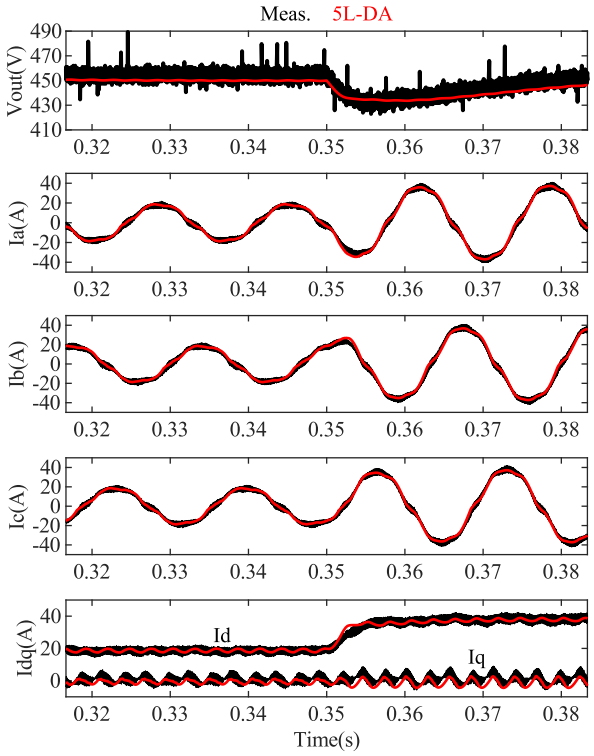

FIGURE 25. 5 kW to 10 kW load transient waveform for 5L-DA and experimental measurement.

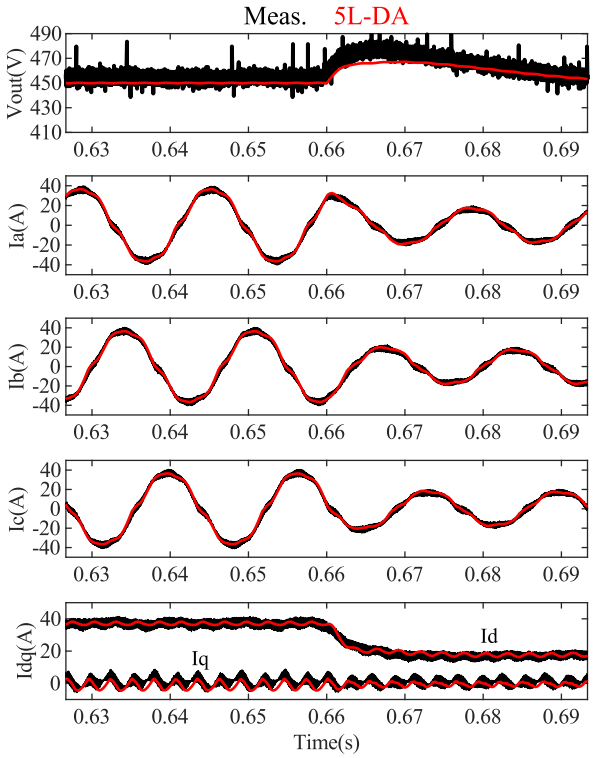

FIGURE 26. 10 kW to 5 kW load transient waveform for 5L-DA and measurement.

Figs. 25 and 26 show the voltage and current waveforms when the load is changed from 5kW to 10kW and vice versa. For both transient conditions, the 5L-DA can closely matches

the experiment. In particular, the proposed model captures well the moments of transients and accurately reproduce the current ripples of I_d and I_q. Some slight difference of the output voltage response, such as a slightly larger overshoot/undershoot and slight difference in V_{DC} recovery time as well as as a slightly lower I_d transient current is also observable. This to be expected due to some non-idealities from the hardware prototype which is not taken into account.

VI. CONCLUSION

This paper proposed an enhanced time-average model, which is able to account for the dead-time distortions and low-frequency harmonics of various operating conditions. It has been demonstrated that such a model is able to reproduce the zero-crossing distortions and low-order harmonics that a VSC produces. The proposed model takes only a fraction of second for simulation which is about 400 times faster than a detailed SEM model, and yet the results are as good as the SEM. In fact, as discussed in Section IV, in some cases the proposed model better resembles the actual VSC hardware as compared to SEM.

By taking the advantage of its very fast computation time, such a method serves as a viable alternative for simulation on large and and complex system with large time constant (long transient time) such as a wind farm, solar farm, or micro grid when the simulation involves multiple VSCs. Other potential applications are to use the proposed model to perform frequency response analysis or to run design optimization by sweeping design parameters, which requires multiple simulations, and the proposed model can also be a viable tool for handling such simulation demanding tasks.

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