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A Detailed Analytical Model of SiC MOSFETs for Bridge-Leg Configuration by Considering Staged Critical Parameters

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ABSTRACT The high operating voltage and switching speed of silicon carbide (SiC) MOSFETs have significant impacts on parasitic elements. This leads to a limitation in the performance of the devices. Especially in the bridge-leg configuration, the coupling of the parasitic elements, in the upper and lower bridge-legs, produces knock-on effects, which complicates the modeling development to reveal the underlying mechanisms. This paper presents a detailed piecewise linear analytical model for bridge-leg configured SiC MOSFETs, which takes into account their characteristics and all parasitic elements. The novelty of the proposed model lies in the fact that the critical parameters in each stage are distinguished flexibly and emphatically according to their influence weights to the corresponding main variables. Therefore, the complexity of the model which considers all parasitic elements is reduced but the critical impacts on the switching processes are carefully kept. The turn-on and turn-off processes are analyzed stage-by-stage in detail with the derived critical parameters equivalent circuits, and the mechanism underlying how each critical parameter influences the model is revealed individually. Furthermore, based on this model, the impact mechanisms and trends of the switching rate variation, the power loop attenuation oscillation, and the driver loop crosstalk phenomenon for different critical parameters are analyzed emphatically. Double pulse measurements with a 600 V/20A SiC MOSFETs based bridge-leg test circuit are used for the experimental verification of the accuracy of the model and the trends of the critical parameters' impacts.

INDEX TERMS Analytical model, bridge-leg, SiC MOSFET, critical parameters, impact mechanisms, staged.

NOMENCLATURE

C_{gsX}	Gate-source capacitance
C_{gdX}	Gate-drain capacitance
C_{dsX}	Drain-source capacitance
L_{gX_in}	Internal parasitic inductance of gate
L_{dX_in}	Internal parasitic inductance of drain
L_{sX_in}	Internal parasitic inductance of source
L_{gX_ex}	External parasitic inductance of gate
L_{dX_ex}	External parasitic inductance of drain
L_{sX_ex}	External parasitic inductance of source
L_{LOOP}	Parasitic inductances of power loop
R_{gX_in}	Internal gate driver resistance
R_{gX_ex}	External gate driver resistance
g_f	Transconductance of SiC MOSFET
D_{bX}	Antiparallel freewheeling diode of SiC MOSFET
Q_{RS}	Charge quantity of the minority carriers of antiparallel freewheeling diode
R_{gH_eq1}	Equivalent damping resistance of higher SiC MOSFET in Stage 4
R_{gL_eq1}	Equivalent damping resistance of lower SiC MOSFET in Stage 4
R_{gL_eq2}	Equivalent damping resistance of lower SiC MOSFET in Stage 6
R_{gH_eq2}	Equivalent damping resistance of higher SiC MOSFET in Stage 8
V_{DD}	DC input voltage
V_{GATE}	Driver supply voltage
V_{th}	Threshold voltage of SiC MOSFET
V_{miller}	Miller platform voltage
V_{gsX}	Gate-source voltage

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V_{dsX}	Drain-source voltage
V_{idsX}	Induced voltage on L_{sX}
V_{iddX}	Induced voltage on L_{dX}
i_{ch}	Channel current
i_{gX}	Driver current
i_{dX}	Drain current
I_{RR_PEAK}	Peak value of reverse recovery current
I_{RR_BV}	Value of reverse recovery current when minority carriers elicited
I_{LOAD}	Output load current

Note: the subscript "X" is represented as "H" and "L" refer to the higher SiC MOSFET and lower SiC MOSFET of bridge-leg configuration, respectively.

I. INTRODUCTION

Silicon carbide (SiC) MOSFETs are promising candidates for next-generation power devices. Compared with a silicon-based MOSFET, a SiC MOSFET has a number of advantages such as wider bandgap, lower on-state resistance, higher thermal conductivity, higher switching speed, and higher block voltage level [1]–[4]. However, along with these excellent characteristics comes, the impacts of its parasitic elements are significantly intensified during the fast switching process, which leads to many unfavorable factors that restrict the device's optimal performance. In a bridge-leg configuration, there are further knock-on effects such as switching oscillation of the power loop [5] and crosstalk phenomenon of the driver loop [6], [7] due to the coupling effects of the upper and lower devices [8]. Besides, the own characteristics of a SiC MOSFET can be also the key obstacles. A SiC MOSFET has a lower turn-on threshold voltage and negative breakdown voltage compared with a silicon-based MOSFET [9], and its gate-source parasitic capacitance is relatively small [10], which makes the driver loop more susceptible to the voltage coupling effects. These two factors contradict each other and reduce the reliability of the bridge-leg based on SiC MOSFETs, which could even result in misconducting [11]. Therefore, to take full advantage of SiC MOSFETs and avoid the obstacles, an accurate and detailed model is needed to evaluate the working processes and the impacts of different parameters for SiC MOSFETs operating in a bridge-leg configuration.

So far, there have been many studies summarizing various models, they can be classified into three categories: physics-based model, behavioral model, and analytical model. The physics-based model based on the carrier drift-diffusion motion equations provides the most detailed descriptions of the physical parameters of the device [12], [13]. But this model is too complex to be used to describe the bridge-leg switching processes at the circuit level. With the development of simulation software, more and more complete behavioral models are employed to describe the switching processes of different kinds of devices. These models are more suitable to analyze the responses of devices nested in a circuit. The commonly used simulation software such as PSpice and SABER provide plentiful and accurate device models that could adjust a series of key parameters and peripheral parasitic elements [14]. Some device manufacturers such as CREE also provide specific SPACE model libraries for their products to close to reality. In [15], the influences of temperature are also taken into account. The perfect behavioral models make it realistic and precise to analyze the switching processes of devices working in a circuit. However, they can only provide the response results of switching processes, but cannot reveal the underlying mechanism and the influences' trends of the parameters. Additionally, the specific behavioral model cannot be easily transplanted to other devices, which makes the analysis tedious. Analytical models are set up based on the mathematical of the loop equations [16]–[18]. For a nonlinear variation switching process of the device, the piecewise linear model is the most convenient and widely used analytical model, which divides the switching process into several linear stages according to the different variable responses and the equivalent circuit models are established in each stage [17], [19]. However, in order to maintain the accuracy of the calculation results, the equations need to consider as many details of the parasitic elements as possible. This inevitably increases the circuit number and the order of equations, which makes the model too complex and can only be solved by iteration methods [20], [21]. Thus, the numerical solutions obtained by such a model cannot fundamentally reveal the physical impacts of the parameters, and a great deal of calculations and comparisons with changed parameters is needed to reveal the impact trends. In this way, the analytical method is analogous to the behavior model. However, in order to simplify the equations and obtain the analytical solutions of the responses, some insignificant parameters are uniformly omitted, such omissions may cause errors or even overlook the impacts of certain parameters [11], [17], [22]. These two aspects become a dilemma of analytical models to evaluate complex circuits.

For both the behavioral model and analytical model, the accuracy of them depends on the precise descriptions of the devices' actual characteristics and the correlations of parasitic elements. However, there is no consistent conclusion on such correlations in the reported literature. This could lead to inaccuracies, error simplifications, and even opposite conclusions. For example, the literatures [23] and [24] believe that common source parasitic inductance can suppress the driver crosstalk phenomenon, while [21] and [25] conferred an opposite conclusion. Another critical influence comes from the reverse recovery process of the freewheeling diode. Although the reverse recovery characteristics of SiC MOSFETs are better than Si MOSFETs, it still exists due to the capacitance effect of the drain-source junction, but it is ignored in some studies [22], [26]. Moreover, the descriptions of the occurrence interval of the reverse recovery process are not consistent. The authors, in [27] and [28], report that the current peak of the reverse recovery process occurs during the drain-source voltage decrease stage whereas [17] claims that it occurs before the drain-source voltage decrease.

Literatures [11] and [29] shown that the drain-source voltage does not change during the reverse recovery current rising time, while the drain-source voltage builds up when the reverse recovery current decreases. These differences will lead to cumulative irregularities in the calculation results. There are different judgments for the division of the nonlinear parasitic capacitances, and the linearization method adopted determines the accuracy of capacitance value restoration. In [19], only the nonlinear characteristic of the gate-drain capacitance is considered in detail. The authors of [17] consider both gate-drain capacitance and drain-source capacitance have nonlinear characteristics, but simply divide them into large and small values according to the drain-source voltage. The literatures [30] and [31] consider that all parasitic capacitances of SiC MOSFETs have nonlinear characteristics. Particularly, [31] presents a comprehensive behavior model of the nonlinear characteristics of parasitic capacitances. To sum up, although these special characteristics greatly increase the complexity of the model designing, they are related to the accuracy of the switching responses and cannot be ignored. Furthermore, the upper and lower devices have the same number of parasitic elements for a bridge-leg, which makes the analysis even more cumbersome.

This paper proposes a detailed and accurate analytical model for SiC MOSFETs applied to bridge-leg configuration. The model comprehensively considers all parasitic elements and the special characteristics of the switching devices, including the nonlinear characteristics of the interelectrode parasitic capacitance, the transconductance of the channel current versus the gate-source voltage, and the reverse recovery processes of antiparallel freewheeling diodes. Further, on the basis of the piecewise linear model, the dominant elements and key variables of each switching stage are identified independently, and they are selected separately according to their influence weights on different variables of the driver loop and power loop. Non-critical parasitic elements and variables are flexibly excluded. Through these staged parameter optimizations, the complexity of modeling can be reduced while ensuring its accuracy. The dominant elements, that affect the main switching responses, and the key coupling variables are summarized as the staged critical parameters. The equivalent circuits based on the critical parameters of each stage are derived individually and the switching processes are described in detail. Moreover, based on the proposed model, the influence mechanisms and trends of the critical parameters on the current and voltage switching rates, the coupling effects of the bridge-leg, the oscillation of the power loop, and the crosstalk of the driver loop, can be analyzed in detail. They are vital features of the bridge-arm. A double pulse test circuit composed of 600V, 20A SiC MOSFETs is set up and experimental results are obtained to verify the accuracy of the proposed analytical model and the tendencies of the critical parameters' effect.

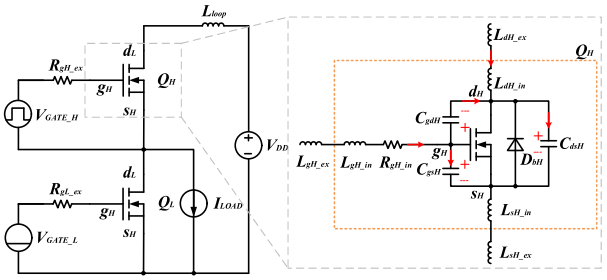

FIGURE 1. Equivalent circuit model of a bridge-leg configuration.

II. ANALYSIS OF STAGED SWITCHING PROCESS OF BRIDGE-LEG CONFIGURATION

In this section, the switching process of a bridge-leg configuration is introduced in detail. A double pulse test equivalent circuit based on SiC MOSFETs is established. Fig.1 displays the equivalent circuit model. The proposed model includes a DC input voltage V_{DD} modeled as a constant voltage source. The output current is considered as a constant current source. The SiC MOSFETs, Q_H and Q_L, are connected in series as the upper and lower switching devices of the bridge-leg, where their gates are connected to the gate drivers through the external driver resistances R_{gH_ex} and R_{gL_ex} respectively. The rise and fall times of the gate drivers' voltages are neglected in the analysis. In addition, the parasitic elements of the SiC MOSFETs are considered in the internal of the device packages and the external circuit traces. Taking Q_H as an example, the internal parasitic elements include interelectrode capacitances C_{gsH}, C_{gdH}, and C_{dsH}, parasitic inductances L_{gH_in}, L_{dH_in}, and L_{sH_in}, internal gate driver resistance R_{gH_in}, and the antiparallel freewheeling diode D_{bH}. The external parasitic elements are the stray inductances of the electrode pins and the circuit traces connected to the gate, source, and drain, which are represented by L_{gH_ex}, L_{dH_ex}, and L_{sH_ex}, respectively. As well, Q_L has the same structure. Indeed, there are extra stray inductances in the power loop lumped by L_{LOOP}, in order to facilitate the analysis, L_{LOOP} is lumped into L_{dH_ex} in the subsequent discussion, and $L_{gH} = L_{gH\_ex} + L_{gH\_in}$, $L_{dH} = L_{dH\_ex} + L_{dH\_in}$, $L_{sH} = L_{sH\_ex} + L_{sH\_in}$, that respectively denote the total gate, the drain, and the source inductances of Q_H. Q_L is modeled in the same way.

To ensure the consistency of the variables' response expressions in each stage, the reference direction of each vector variable in the equivalent circuit is uniformly specified. The currents flow into the gates are in the positive direction in Q_H and Q_L driver loops, and the current direction from drain to source is positive in the power loop. Fig. 2 illustrates the staged analytical turn-on and turn-off switching waveforms of Q_H and Q_L in sequence. According to the period of major variables' response change, the turn-on and turn-off switching processes are divided into eight stages. A thorough analysis of each stage is then presented stage-by-stage.

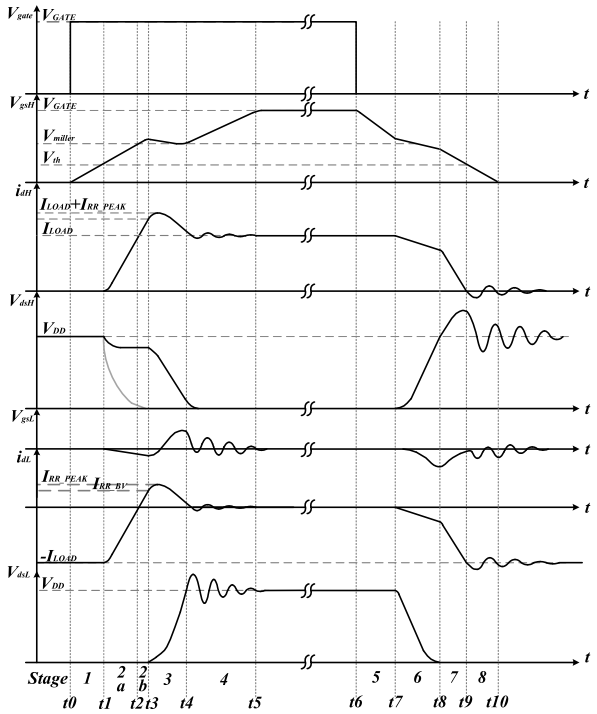

FIGURE 2. Analytical switching sequence of turn-on and turn-off stages.

A. TURN-ON SWITCHING TRANSITION

Before the gate signal of Q_H turns higher, Q_H and Q_L are in the cut-off state, the load current I_{LOAD} flows through the antiparallel freewheeling diode D_{bL} of Q_L, D_{bL}.

1) STAGE 1 (t0-t1) TURN-ON DELAY TIME

The gate signal of Q_H becomes high at V_{GATE}, and the gate current charges the input capacitances C_{gsH} and C_{gdH}. The gate-source voltage V_{gsH} starts to rise and the gate-drain voltage experiences a slight drop. Since V_{gsH} has not reached the threshold voltage V_{th}, Q_H remains cut-off, I_{LOAD} still circulates through D_{bL} and the voltage distribution of the bridge-leg power loop remains unchanged.

Due to the nonlinear characteristics of the interelectrode capacitances with respect to the drain-source voltage. And there is a high voltage applied to the drain-source of Q_H in this stage. The value of C_{gdH} stays at a minimum, which is much smaller than that of C_{gsH}. In general, the value of C_{gsH} is a hundredfold or more than C_{gdH} for SiC MOSFETs. Thus, the current flowing through C_{gdH} and the small voltage drop on the drain parasitic inductance L_{dH} can be neglected (the neglected parasitic element and circuits are represented by dashed lines in Fig. 3). The equivalent circuit of this stage is shown in Fig. 3, the circuit equations are established as

$$V_{gsH} = V_{gdH} + V_{dsH} \tag{1}$$

$$i_{gH} = C_{gsH}\frac{dV_{gsH}}{dt} \tag{2}$$

$$V_{GATE} = R_{gH}i_{gH} + \left(L_{gH} + L_{sH}\right)\frac{di_{gH}}{dt} + V_{gsH} \tag{3}$$

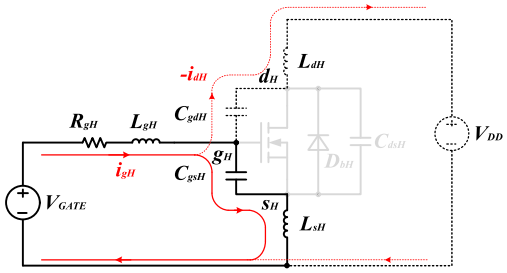

FIGURE 3. Equivalent circuit for Stage 1.

V_{gsH} is a step response of a second-order circuit, the equations can be obtained as shown in (4).

$$\left(L_{gH}+L_{sH}\right)C_{gsH}\frac{dV_{gsH}^2}{dt^2} + R_{gH}C_{gsH}\frac{dV_{gsH}}{dt} + V_{gsH} = V_{GATE} \tag{4}$$

And V_{gsH} can be solved as

$$V_{gsH} = V_{GATE} - \frac{V_{GATE}}{\tau_{bH1}-\tau_{aH1}} \times \left(\tau_{bH1}e^{-\tau_{aH1}\omega_{n\_H1}t} - \tau_{aH1}e^{-\tau_{bH1}\omega_{n\_H1}t}\right) \tag{5}$$

where $\tau_{aH1} = \xi_{H1} - \sqrt{\xi_{H1}^2 - 1}$, $\tau_{bH1} = \xi_{H1} + \sqrt{\xi_{H1}^2 - 1}$ and the characteristic parameters of the driver loop are

$$\omega_{n\_H1} = \frac{1}{\sqrt{\left(L_{gH}+L_{sH}\right)C_{gsH}}} \tag{6}$$

$$\xi_{H1} = \frac{R_{gH}}{2}\sqrt{\frac{C_{gsH}}{L_{gH}+L_{sH}}} \tag{7}$$

where ω_{n_H1} denote the natural frequency and ξ_{H1} denotes the damping coefficient.

2) STAGE 2 (t1-t3) Q_H CHANNEL CURRENT RISE TIME AND D_{bL} REVERSE RECOVERY CURRENT RISE TIME

When V_{gsH} exceeds V_{th}, Q_H starts conducting and its channel current i_{ch} increases from zero. At the same time, the freewheeling current of D_{bL} decreases from I_{LOAD} and drops to zero when i_{ch} reaches I_{LOAD}. Nevertheless, due to the reverse recovery characteristic, the reverse recovery current through D_{bL} increases until it approaches the maximum I_{RR_PEAK}, which is I_{RR_BV}, and i_{dH} rises to $I_{LOAD} + I_{RR\_BV}$. So, according to the direction of i_{dL}, this stage can be divided into two sub-stages.

3) STAGE 2 (t1-t2) Q_H CHANNEL CURRENT RISE TIME

In this stage, Q_H works in the saturation region and the channel current i_{ch} is controlled by V_{gsH}. Their relationship is given by:

$$i_{ch} = g_f\left(V_{gsH} - V_{th}\right) \tag{8}$$

where g_f is the transconductance coefficient of Q_H. The drain current i_{dH} can be expressed as follows:

$$i_{dH} = i_{ch} - C_{gdH}\frac{dV_{gdH}}{dt} + C_{dsH}\frac{dV_{dsH}}{dt} \tag{9}$$

g_f increases nonlinearly with the increase of V_{gsH} until it levels out slowly, and the rising rate of i_{ch} reaches

the maximum. Correlatively, the freewheeling current through D_{bL} decreases. These rapid varying currents generate induced voltages on L_{dH}, L_{sH}, L_{dL}, and L_{sL} in the power loop, which cause a slight drop on V_{dsH}. Thereby, the equation of the power loop can be expressed as

$$V_{DD} = V_{dsH} + (L_{dH} + L_{sH})\frac{di_{dH}}{dt} + L_{sH}\frac{di_{gH}}{dt} + (L_{dL} + L_{sL})\frac{d\,(i_{dH} - I_{LOAD})}{dt} \quad (10)$$

Same as Stage 1, V_{dsH} does not decrease significantly and C_{gdH} still stay around its minimum. So, most of driver current of Q_H continues to charge C_{gsH} and the influence of the current flowing through C_{gdH} can still be neglected. The equivalent circuit of this sub-stage is shown in Fig. 4a.

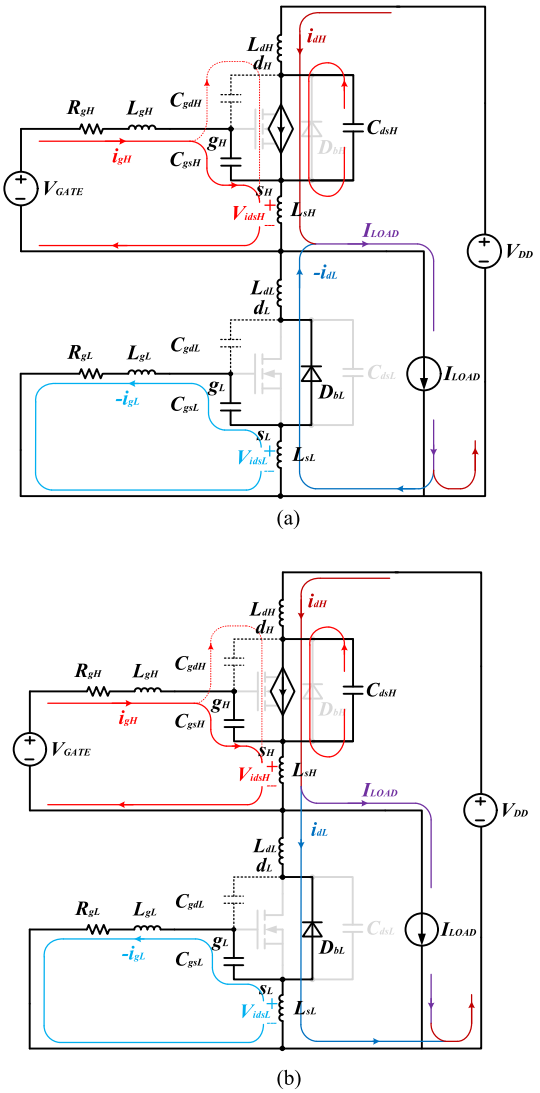

FIGURE 4. (a) Equivalent circuit for Stage 2a. (b) Equivalent circuit for Stage 2b.

The driver loop equation of Q_H can be expressed as

$$R_{gH}\,i_{gH} + \left(L_{gH} + L_{sH}\right)\frac{di_{gH}}{dt} + V_{idsH} + V_{gsH} = V_{GATE} \quad (11)$$

where V_{idsH} is the induced voltage on L_{sH} with i_{dH} increases.

$$V_{idsH} = L_{sH}\frac{di_{dH}}{dt} \quad (12)$$

When the rising rate of i_{dH} approaches its maximum, the induced voltages on L_{dH}, L_{sH}, L_{dL}, and L_{sL} remain constant. Thus, the power loop current can be considered as $i_{dH} = i_{ch}$. By combining (2) and (8)-(12), the driver loop equation of Q_H can be obtained as

$$V_{GATE} = \left(L_{gH} + L_{sH}\right)C_{gsH}\frac{d^2V_{gsH}}{dt^2} + \left(R_{gH}C_{gsH} + L_{sH}g_f\right)\frac{dV_{gsH}}{dt} + V_{gsH} \quad (13)$$

The characteristic parameters of this equation can be deduced as given below:

$$\omega_{n\_H2} = \frac{1}{\sqrt{\left(L_{gH} + L_{sH}\right)C_{gsL}}} \quad (14)$$

$$\xi_{H2} = \frac{R_{gH}}{2}\sqrt{\frac{C_{gsH}}{L_{gH} + L_{sH}}} + \frac{L_{sH}g_f}{2\sqrt{\left(L_{gH} + L_{sH}\right)C_{gsH}}} \quad (15)$$

Compared with Stage 1, the natural frequency of the driver loop is unaffected, but the damping coefficient increases with the influence of g_f.

At the same time, the induced voltage on L_{sL} increases, which will be superimposed on the driver loop of Q_L and causes a negative voltage response for V_{gsL}. The key equations can be listed as

$$V_{idsL} + V_{gsL} + R_{gL}i_{gL} + L_{gL}\frac{di_{gL}}{dt} = 0 \quad (16)$$

$$i_{gL} = C_{gsL}\frac{dV_{gsL}}{dt} \quad (17)$$

$$V_{idsL} = L_{sL}\frac{di_{dL}}{dt} \quad (18)$$

$$i_{dL} = i_{ch} - I_{LOAD} \quad (19)$$

where V_{idsL} is the induced voltage on L_{sL}. Combining with (8), (16)-(19), the driver loop equation of Q_L can be obtained as

$$L_{gL}C_{gsL}\frac{d^2V_{gsL}}{dt^2} + R_{gL}C_{gsL}\frac{dV_{gsL}}{dt} + V_{gsL} = -L_{sL}g_f\frac{dV_{gsH}}{dt} \quad (20)$$

4) STAGE 2 (t2-t3) D_{bL} REVERSE RECOVERY CURRENT RISE TIME

Once i_{dH} reaches I_{LOAD}, the current of D_{bL} drops to zero and the reverse recovery process starts. D_{bL} has a charge-storage effect and a great number of minority carriers accumulated at the interface of the PN junction during the previous freewheeling prosses. Thus, these minority carriers need to be elicited first and then a depletion layer can be formed. Thereafter, D_{bL} turns to the reverse-biased state and the blocking voltage starts to build up. In contrast to Stage 2a, the only difference is the direction of i_{dL}. The rising rate of i_{dL} keeps the same, the influences of i_{dH} and i_{dL} on the driver loop of upper and lower devices do not change, and

the voltage distribution of the power loop keeps stable. The equivalent circuit of this sub-stage is shown in Fig. 4b. When i_{dL} increases to I_{RR_BV}, the elicitation of minority carriers is completed. The time at which this happens is denoted as *t3*.

The charge quantity of the minority carriers Q_{RS} is determined by the diffusion capacitance of D_{bL}, the minority carriers' lifetime, the forward current, and the junction temperature. The value of diffusion capacitance C_{dbL} can be expressed as

$$C_{dbL} = \left(\frac{1}{2V_t}\right)\left(I_{p0}\tau_{p0} + I_{n0}\tau_{n0}\right) \tag{21}$$

where V_t is the forward voltage drop and it is usually assumed to be a constant. τ_{p0} and τ_{n0} are the minority carriers' lifetime, and I_{p0} and I_{n0} are the equivalent current of the P zone and N zone, respectively. In the macroscopic view, the output current can be expressed as $I_{LOAD} = I_{p0} + I_{n0}$. I_{RR_BV} and Q_{RS} can be expressed as

$$I_{RR\_BV} = \left.\frac{di_{dL}}{dt}\right|_{t=t2}(t3 - t2) \tag{22}$$

$$Q_{RS} = \frac{1}{2}I_{RR\_BV}\,(t3 - t2) \tag{23}$$

Therefore, the reverse recovery current can be obtained as

$$I_{RR\_BV} = \sqrt{2Q_{RS}g_f \left.\frac{dV_{gsH}}{dt}\right|_{t=t2}} \tag{24}$$

When i_{dL} reaches I_{RR_BV} at *t3*, it continues to rise at the same rate because of the parasitic inductances in the power loop, which can be considered as the initial condition of the blocking voltage building up in the next stage. The reverse recovery model of the independently packaged freewheeling diode applied in [17] and [20] is inadequate to describe the blocking voltage increase process. This is because the freewheeling diode is inverse paralleled with the SiC MOSFET, hence, all the parasitic capacitances need to be considered to evaluate the response of the blocking voltage increase.

5) STAGE 3 (t3-t4) VOLTAGE SWITCHING TIME

At *t3*, the blocking voltage of D_{bL} starts to increase, and the voltage of the bridge-leg begins to switch. The switching rate of the voltages is not only determined by the characteristic of the switching devices and the driver capability but also is restricted by the voltage dynamic equilibrium of the whole bridge-leg. This balance is maintained until V_{dsH} approaches zero and V_{dsL} increases to V_{DD}. The reverse recovery current of D_{bL} has the initial rising rate and continues to rise to I_{RR_PEAK} and then begins to decrease. It can be regarded as the initial condition for the voltage switching process. In addition, the interelectrode capacitances values change due to the nonlinear characteristics related to the drain-source voltage, which makes the voltage switching process more complicated.

More concretely, the drop rate of V_{dsH} is determined by two key factors. The first on is the characteristics of the driver loop, which is reflected in the maximum discharge current of C_{gdH}. It is restricted by the pull-up current of the driver module, the resistances and the parasitic inductances of the driver loop, the clamp limiting factor caused by V_{gsH}, and the current carrying capacity of the channel. The second one is the characteristics of the power loop, which is reflected in the discharge rate of C_{dsH}. It is restricted by the dynamic equilibrium of the power loop. The parasitic inductances of the power loop, the parasitic capacitances of Q_L, the load characteristic, and the initial rising rate of the reverse recovery current are all associated with the discharge rate of C_{dsH}. Overall, the drop rate of V_{dsH} is determined by the slower one of the discharge rates of C_{gdH} and C_{dsH}. They keep an equilibrium state on the whole. Therefore, the power loop and driver loop are mutually coupled, their equilibrium point and the influences to the voltage switching processes are different under different operating situations that should be distinguished.

If a perfect condition is provided by the channel of Q_H and the power loop, it could satisfy the rapid discharge current of C_{dsH}. This usually occurs with SiC MOSFETs operating in high-voltage, high-current switching situations. However, the resistance conditions of the driver loop are relatively stable and it limits the maximum discharge current of C_{gdH}. Thus, the state of the driver loop reaches the limiting condition more easily, and the decrease rate of V_{dsH} is dominated by the driver loop. On the contrary, in the situations of low input voltage, low output current, or the parasitic inductances are extremely large that hinders the fast switching of the bridge-leg, the discharge process of C_{gdH} would spend less time. The decrease rate of V_{dsH} is dominated by the power loop. Besides, V_{dsH} may drop to the on-state voltage directly because of the low V_{DD} and it is all distributed by the parasitic inductances of the power loop in Stage 2. The operation enters Stage 4 directly, as shown by the gray line in Fig. 2. SiC MOSFETs work smoothly on these slow switching, light load, or low-voltage conditions. Therefore, only the former conditions will be discussed in the following.

In this stage, most of i_{gH} turns to supply the discharge current of C_{gdH} and V_{gsH} remains stable basically due to the limitation of the saturation region. It causes a slight drop in V_{gsH} with i_{ch} declining from its maximum value. When i_{ch} closes to I_{LOAD}, V_{gsH} keeps steady at the miller platform voltage V_{miller}, which can be expressed as $V_{miller} = I_{LOAD}/g_f + V_{th}$. Thus, the current flowing through C_{gsH} decreases significantly and can be neglected. The reverse recovery current of D_{bL} starts to charge C_{dsL}, C_{gdL}, and C_{gsL}, accompanied by the blocking voltage building up. The equivalent circuit of this stage is shown in Fig. 5a.

In the process of V_{dsH} decrease, the currents flow through the channel of Q_H include the discharge current of C_{gdH} and C_{dsH}, the reverse recovery current, and the output current I_{LOAD}. These four currents make the channel carrying current reach the maximum value. The channel keeps saturated state and the restriction of the channel to the current can be passed on to the V_{gsH} clamp limiting factor of the driver loop. The discharge current of C_{dsH} only flows through the

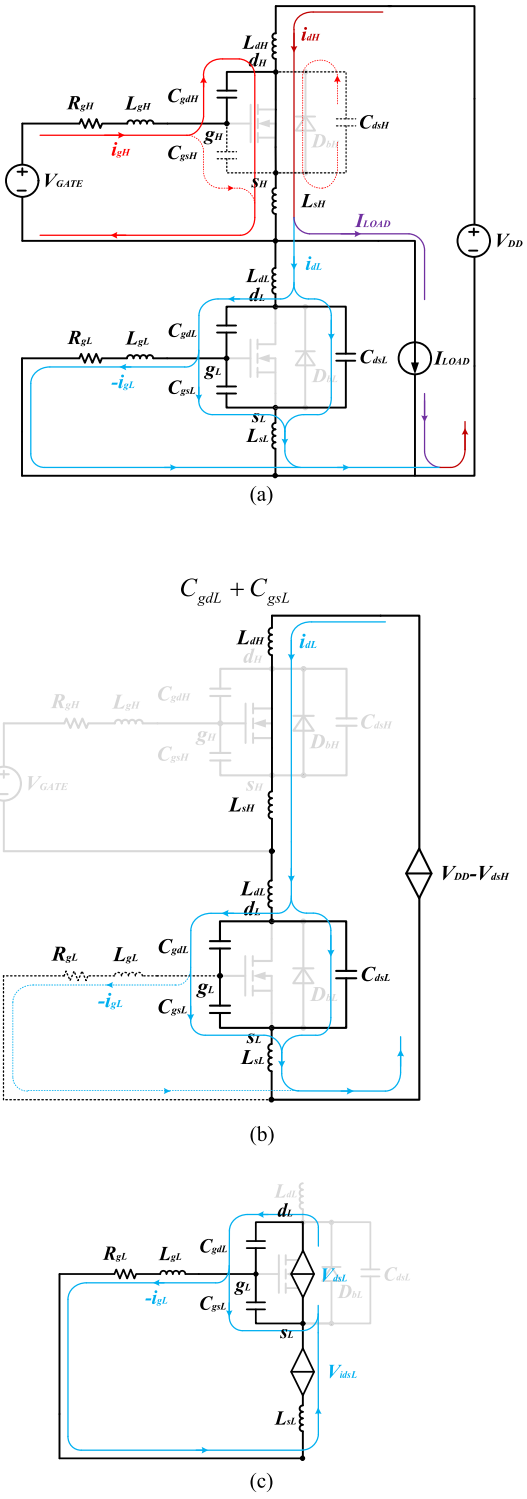

FIGURE 5. (a) Equivalent circuit for Stage 3. (b) Power loop equivalent circuit for Stage 3. (c) Driver loop of Q_L equivalent circuit for Stage 3.

channel, this process can be considered as an independent and passive response which is influenced by the decrease of V_{dsH}, C_{dsH} is not a critical element. The driver current of Q_H turns to the following expression:

$$i_{gH} = C_{gdH}\frac{dV_{gdH}}{dt} \tag{25}$$

The driver loop equation of Q_H can be established as

$$R_{gH}i_{gH} + \left(L_{gH} + L_{sH}\right)\frac{di_{gH}}{dt} + V_{gdH} + V_{idsH} = V_{GATE} \tag{26-I}$$

This equation is only appropriate to describe the transitional process of the driver loop from Stage 2b. The initial states of i_{gH}, di_{gH}/dt, and V_{idsH} should be considered. It is established based on i_{gH} supporting the discharge of C_{gdH} and the drain and source are regarded as an equipotential connection to avoid the voltage contradiction of C_{gdH} caused by the reference potential difference. When i_{gH} is clamped by the the driver loop saturation, it reaches the ceiling and the discharge rate of C_{gdH} reduces to zero, and the induced voltages on L_{gH} and L_{sH} causesd by i_{gH} can be neglected. The driver loop equation is given by

$$R_{gH}i_{gH} + V_{miller} + V_{idsH} = V_{GATE} \tag{26-II}$$

where V_{idsH} is the induced voltage on L_{sH} caused by i_{dH}, it turns to negative when i_{dH} starts to decrease, and V_{idsH} gradually diminishes with i_{dH} dropping to i_{LOAD}.

The drain-source voltage of Q_L (the blocking voltage of D_{bL}), V_{dsL}, increases. This process can be equivalent to a response of the whole parasitic capacitances of Q_L charged by the applied voltage V_{DD} - V_{dsH}, the charge current flowing through all the power loop parasitic inductances. The reverse recovery current only exists in the power loop initially. It is divided into two parts which flow through C_{gdL} and C_{dsL} respectively, and the C_{gdL} charging current is further divided by C_{gsL} and the driver loop of Q_L. The current flowing through the driver loop slowly increases from zero due to the relatively large impedance. It is too small and is not distributed naturally compared with the reverse recovery current that always exists in the power circuit. Therefore, the current in the driver loop of Q_L is not the dominant factor can be ignored when calculating the V_{dsL} response in this stage. The equivalent circuit of the power loop is shown in Fig. 5b and the power loop equations can be expressed as

$$\left(L_{dH}+L_{sH}+L_{dL}+L_{sL}\right)\frac{di_{dL}}{dt} + V_{dsL} + V_{dsH} = V_{DD} \tag{27}$$

$$i_{dL} = C_{XL}\frac{dV_{dsL}}{dt} \tag{28}$$

where

$$C_{XL} = \frac{C_{gdL}C_{gsL} + C_{gdL}C_{dsL} + C_{dsL}C_{gsL}}{C_{gdL} + C_{gsL}} \tag{29}$$

Combining (27)-(29) with (1), (12), (25), (26-II), the relationship between the power loop and the driver loop of Q_H can be linked by i_{dL}

$$V_{GATE} = R_{gH}C_{gdH}\left(L_{dH} + L_{sH} + L_{dL} + L_{sL}\right)\frac{d^2i_{dL}}{dt^2} + L_{sH}\frac{di_{dL}}{dt} + \frac{R_{gH}C_{gdH}}{C_{XL}}i_{dL} + V_{miller} \tag{30}$$

i_{dL} can be deducted as

$$i_{dL} = \frac{C_{XL}}{C_{gdH}R_{gH}}\left(V_{GATE} - V_{miller}\right) - \frac{\left(\tau_p - \tau_q\tau_{aH3}\right)}{\tau_r}e^{-\tau_{bH3}\omega_{n\_H3}(t-t3)} - \frac{\left(\tau_p - \tau_q\tau_{bH3}\right)}{\tau_r} \times e^{-\tau_{aH3}\omega_{n\_H3}(t-t3)} \quad (31)$$

where

$$\tau_{aH3} = \xi_{H3} - \sqrt{\xi_{H3}^2 - 1}, \quad \tau_{bH3} = \xi_{H3} + \sqrt{\xi_{H3}^2 - 1},$$
$$\tau_{bH3} = \xi_{H3} + \sqrt{\xi_{H3}^2 - 1},$$
$$\tau_r = C_{gdH}R_{gH}\omega_{n\_H3}\left(\tau_{bH3} - \tau_{aH3}\right),$$
$$\tau_p = C_{gdH}R_{gH}\left.di_{dL}/dt\right|_{t=t3},$$
$$\tau_q = \left(C_{XL}\left(V_{GATE} - V_{miller}\right) - C_{gdH}R_{gH}\left.i_{dL}\right|_{t=t3}\right)\omega_{n\_H3}.$$

The characteristic parameters are

$$\omega_{n\_H3} = \frac{1}{\sqrt{\left(L_{dH} + L_{sH} + L_{dL} + L_{sL}\right)C_{XL}}} \quad (32)$$

$$\xi_{H3} = \frac{L_{sH}}{2C_{gdH}R_{gH}}\sqrt{\frac{C_{XL}}{L_{dH} + L_{sH} + L_{dL} + L_{sL}}} \quad (33)$$

And V_{dsL} can be deducted as

$$V_{dsL} = \frac{1}{C_{XL}}\int_{t3}^{t} i_{dL}dt = \frac{\left(V_{GATE} - V_{miller}\right)}{C_{gdH}R_{gH}}(t - t3) - \frac{e^{-\tau_{aH3}\omega_{n\_H3}(t-t3)}}{C_{XL}\omega_{n\_H3}\tau_r\tau_{aH3}} \times \left(\tau_p - \tau_q\tau_{bH3}\right) + \frac{e^{-\tau_{bH3}\omega_{n\_H3}(t-t3)}}{C_{XL}\omega_{n\_H3}\tau_r\tau_{bH3}} \cdot \left(\tau_p - \tau_q\tau_{aH3}\right) \quad (34)$$

It must be noted that this equivalent model can only be employed to calculate the response of the power loop variables, the shunted current flowing through the driver loop hardly affects the V_{dsL} response. However, it plays a key role in the crosstalk response of the driver loop. From the perspective of the driver loop of QL. The fast-rising rate of V_{dsL} results in an increase in the displacement current of C_{gdL}, the current of the driver loop to increase from zero and the voltages on R_{gL} and L_{gL} cannot be ignored. Besides, the reverse recovery current flows through L_{sL} and causes induced voltage, V_{idsL}. These two voltages responses maintain a dynamic equilibrium at C_{gsL}, which causes fluctuations in V_{gsL}, known as the crosstalk phenomenon. The equivalent circuit is shown in Fig. 5c and the equation can be expressed as

$$V_{gsL} = V_{gdL} + V_{dsL} \quad (35)$$

$$V_{idsL} = L_{sL}\frac{di_{dL}}{dt} \quad (36)$$

$$i_{gL} = C_{gdL}\frac{dV_{gdL}}{dt} + C_{gsL}\frac{dV_{gsL}}{dt} \quad (37)$$

$$R_{gL}i_{gL} + L_{gL}\frac{di_{gL}}{dt} + V_{gsL} + V_{idsL} = 0 \quad (38)$$

Thus, V_{gsL} can be obtained as

$$L_{gL}\left(C_{gdL}+C_{gsL}\right)\frac{d^2V_{gsL}}{dt^2} + R_{gL}\left(C_{gdL}+C_{gsL}\right)\frac{dV_{gsL}}{dt} + V_{gsL} = \left(\frac{L_{gL}C_{gdL}}{C_{XL}} - L_{sL}\right)\frac{di_{dL}}{dt} + \frac{R_{gL}C_{gdL}}{C_{XL}}i_{dL} \quad (39)$$

The characteristic parameters of this equation can be deduced as

$$\omega_{n\_L3} = \frac{1}{\sqrt{L_{gL}\left(C_{gdL} + C_{gsL}\right)}} \quad (40)$$

$$\xi_{L3} = \frac{R_{gL}}{2}\sqrt{\frac{C_{gdL} + C_{gsL}}{L_{gL}}} \quad (41)$$

6) STAGE 4 (t4-t5) GATE REMAINING CHARGING TIME

When V_{dsH} reaches the on-state voltage, Q_H works in the ohmic region and i_{ch} is separated from the relationship with V_{gsH}. C_{gsH} and C_{gdH} start charging and V_{gsH} continues to rise until it reaches V_{GATE}. The equations of the driver loop of Q_H are the same as (11) and (12) in Stage 2, and i_{gH} can be expressed as

$$i_{gH} = \left(C_{gsH} + C_{gdH}\right)\frac{dV_{gsH}}{dt} \quad (42)$$

In this stage, V_{dsL} keeps the rising rate at *t4* and starts oscillating due to the parasitic inductances of the power loop and the parasitic capacitances of Q_L. The V_{gsH} increasing process for the driver loop of Q_H is a relatively independent response. But, when it is considered from the perspective of the power loop with Q_H turns on, the driver loop is equivalent to be in parallel with the common source parasitic inductance, L_{sH}. The equivalent circuit is shown in Fig. 6a.

The power loop forms a serial RLC second-order circuit. Many studies consider that the resistance is composed of the stray resistance of the power loop and the on-state resistances of the SiC MOSFETs. The sums of these resistances, however, are generally in the milliohm range. Actually, the damping attenuation of the V_{dsL} oscillation is determined by the equivalent impedance of the whole poor loop which includes the paralleled drivel loop of Q_H, as described in [32] and [33]. However, it should be noted that this damping effect does not occur ideally after Q_H is fully turned-on. The power loop will start RLC oscillating once Q_H breaks away from the saturation region. Therefore, the impedance of the driver loop of Q_H in this stage is expressed as

$$X_{gH} = R_{gH} + j\omega_{n\_P4}L_{gH} + \frac{1}{j\omega_{n\_P4}\left(C_{gsH} + C_{gdH}\right)} \quad (43)$$

where ω_{n_P4} is the oscillation frequency. The total equivalent impedance of the upper SiC MOSFET in the power loop is

$$X_H = \frac{X_{gH} \cdot j\omega_{n\_P4}L_{sH}}{X_{gH} + j\omega_{n\_P4}L_{sH}} \quad (44)$$

The equivalent damping resistance is determined by the ratio of the current that flows through R_{gH} and the total

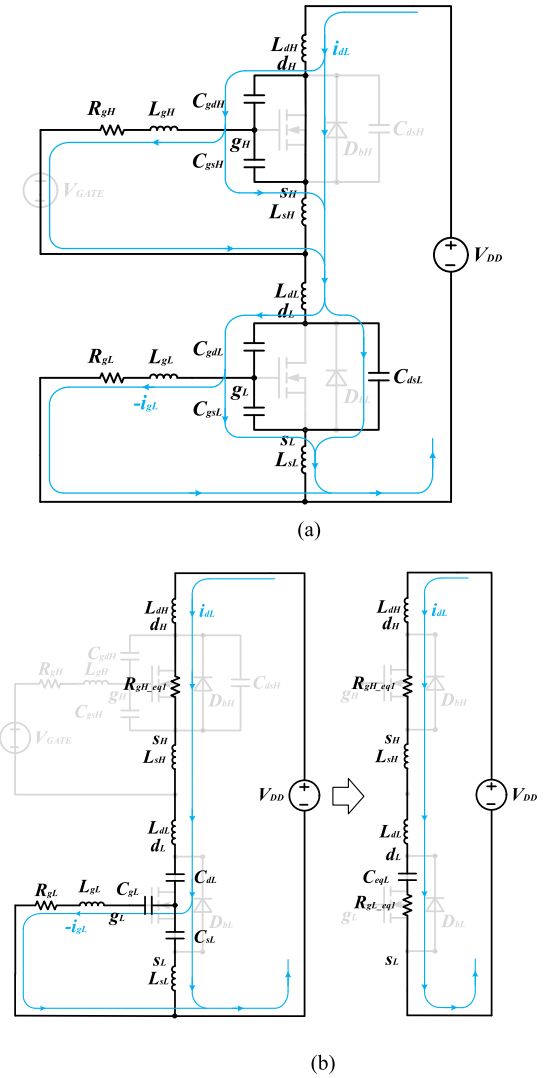

FIGURE 6. (a) Equivalent circuit for Stage 4. (b) Simplified equivalent circuit for Stage 4.

current of the power loop, and can be expressed as

$$R_{gH\_eq1} = R_{gH}\left(\frac{|X_H|}{|X_{gH}|}\right)^2 = R_{gH}\left(\left|\frac{j\omega_{n\_P4}L_{sH}}{X_{gH}+j\omega_{n\_P4}L_{sH}}\right|\right)^2 = R_{gH}\frac{\omega_{n\_P4}^2 L_{sH}^2}{R_{gH}^2+\left(\omega_{n\_P4}L_{gH}+\omega_{n\_P4}L_{sH}-\frac{1}{\omega_{n\_P4}(C_{gsH}+C_{gdH})}\right)^2} \tag{45}$$

As for the driver loop of Q_L, C_{gsL}, C_{gdL}, and C_{dsL} can be transformed into a Y connection, the driver loop is connected in parallel with the power loop from the central node as shown in Fig. 6b. The A-Y transformation is expressed as

$$\begin{cases} C_{gL} = C_{gsL} + C_{gdL} + C_{gsL}C_{gdL}/C_{dsL} \\ C_{sL} = C_{gsL} + C_{dsL} + C_{gsL}C_{dsL}/C_{gdL} \\ C_{dL} = C_{gdL} + C_{dsL} + C_{gdL}C_{dsL}/C_{gsL} \end{cases} \tag{46}$$

ω_{n_P4} is given by

$$\omega_{n\_P4} \approx \frac{1}{\sqrt{(L_{dH}+L_{sH}+L_{dL}+L_{sL})\,C_{eqL}}} \tag{47}$$

$$C_{eqL} = \frac{C_{dL}C_{sL}}{C_{dL}+C_{sL}} \tag{48}$$

The impedance of the driver loop of Q_L is expressed as

$$X_{gL} = R_{gL} + j\omega_{n\_P4}L_{gL} + \frac{1}{j\omega_{n\_P4}C_{gL}} \tag{49}$$

The impedance of the source branch is expressed as

$$X_{sL} = j\omega_{n\_P4}L_{sL} + \frac{1}{j\omega_{n\_P4}C_{sL}} \tag{50}$$

The total equivalent impedance of the lower SiC MOSFET in the power loop is

$$X_L = \frac{X_{gL}\cdot X_{sL}}{X_{gL}+X_{sL}} \tag{51}$$

The equivalent damping resistance is determined by the ratio of current flowing through R_{gL} and the total current of the power loop, which can be expressed as

$$R_{gL\_eq1} = R_{gL}\left(\frac{|X_L|}{|X_{gL}|}\right)^2 = R_{gL}\frac{\left(\omega_{n\_P4}L_{sL}-\frac{1}{\omega_{n\_P4}C_{sL}}\right)^2}{R_{gL}^2+\left(\omega_{n\_P4}L_{gL}-\frac{1}{\omega_{n\_P4}C_{gL}}+\omega_{n\_P4}L_{sL}-\frac{1}{\omega_{n\_P4}C_{sL}}\right)^2} \tag{52}$$

Therefore, the power loop is equivalent to a second-order circuit, as shown in the right-hand side of Fig. 6b. The total equivalent resistance is then calculated by (53) and the power loop equations can be modeled as

$$R_{eq1} = R_{gH\_eq1} + R_{dsH\_on} + R_{gL\_eq1} \tag{53}$$

$$V_{dsL} + R_{eq1}i_{dL} + (L_{dH}+L_{sH}+L_{dL}+L_{sL})\frac{di_{dL}}{dt} = V_{DD} \tag{54}$$

$$i_{dL} = C_{eqL}\frac{dV_{dsL}}{dt} \tag{55}$$

It is noteworthy that the A-Y transform for the driver loop of Q_L can be only applied in this full turn-on state because the currents of the driver loop and the power loop for Q_L transit into a natural distribution. While in Stage 3, the current distribution in the driver loop of Q_L builds up from zero, which is too small and not distributed naturally, it should be ignored.

The initial value of V_{dsL} is V_{DD} and the initial rising rate of V_{dsL} depends on the switching rate in Stage 3. The damping coefficient is obtained as

$$\xi_{P4} = \frac{R_{eq1}}{2}\sqrt{\frac{C_{eqL}}{L_{dH}+L_{sH}+L_{dL}+L_{sL}}} \tag{56}$$

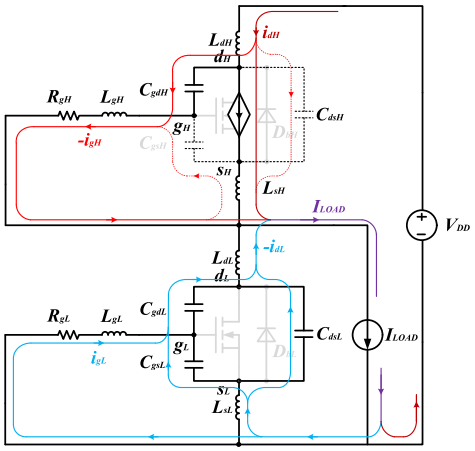

FIGURE 7. Equivalent circuit for Stage 6.

The response of V_{gsL} can still be described by the separate equivalent model for the driver loop of Q_L in stage 3. V_{gsL} will fluctuate due to the oscillations in the displacement current of C_{gdL} and the induced voltage over L_{sL}. The natural frequency and the damping coefficient of the driver loop of Q_L remain the same as those in Stage 3.

B. TURN-OFF SWITCHING TRANSITION

1) STAGE 5 (t6-t7) TURN-OFF DELAY TIME

When the gate signal of Q_H is set to zero, C_{gsH} and C_{gdH} start discharging through the driver loop, and V_{gsH} decreases. Q_H operates in the ohmic region until V_{gsH} drops to V_{miller}. i_{dH} keeps flowing through the channel of Q_H and remains unchanged. The driver loop equation of Q_H is given by (57), and i_{gH} is still expressed by (42). The characteristic parameters of the driver loop of Q_H keep the same as Stage 4.

$$V_{gsH} + R_{gH} i_{gH} + \left(L_{gH} + L_{sH}\right) \frac{di_{gH}}{dt} = 0 \tag{57}$$

2) STAGE 6 (t7-t8) VOLTAGE SWITCHING TIME

Q_H enters the saturation region at this stage and the channel resistance starts to increase. The load current continues to support through Q_H due to D_{bL} is still reverse-biased. V_{dsH} starts to rise and V_{dsL} decreases until it reaches the forward turn-on voltage of D_{bL}. C_{gdH} and C_{dsH} are charged, C_{gdL} and C_{dsL} are discharged, the displacement currents of these capacitances supply part of the load current and cause i_{ch} decreases to some extent.

Similar to the turn-on counterpart (Stage 3), almost all the current of the Q_H driver loop comes from the charging current of C_{gdH} and dominates the rising rate of V_{dsH}. The current flowing through C_{gsH} can be neglected. The equivalent circuit of this stage is shown in Fig. 7.

The charging process C_{gdH} can be established as

$$-R_{gH} i_{gH} - L_{gH} \frac{di_{gH}}{dt} - V_{gdH} + V_{iddH} = V_{DD} \tag{58}$$

$$V_{iddH} = L_{dH} \frac{di_{dL}}{dt} \tag{59}$$

where i_{gH} is same as (25), and V_{iddH} is the induced voltage of L_{dH} due to i_{dH} decreases.

When i_{gH} is clamped by the saturated state of the driver loop, the charge rate of C_{gdH} reaches the ceiling and the driver loop equation is given by

$$R_{gH} i_{gH} + V_{miller} + V_{idsH} = 0 \tag{60}$$

As for Q_L, the decrease of V_{dsL} is restricted by the dynamic equilibrium of the power loop. All the parasitic parameters of the power loop and the driver loop need to take into consideration. Same as Stage 4, C_{gsL}, C_{gdL}, and C_{dsL} can be transformed to Y connection and then the driver loop can be simplified to a second-order circuit. The equivalent damping resistance can be deduced as

$$\begin{aligned} R_{gL\_eq2} &= R_{gL} \left(\frac{|X_L|}{|X_{gL}|} \right)^2 \\ &= R_{gL} \frac{\left(\omega_{n\_P6} L_{sL} - \frac{1}{\omega_{n\_P6} C_{sL}} \right)^2}{R_{gL}^2 + \left(\omega_{n\_P6} L_{gL} - \frac{1}{\omega_{n\_P6} C_{gL}} + \omega_{n\_P6} L_{sL} - \frac{1}{\omega_{n\_P6} C_{sL}} \right)^2} \end{aligned} \tag{61}$$

where $\omega_{n\_P6} \approx 1/\sqrt{(L_{dL} + L_{sL})\, C_{eqL}}$, the equivalent power loop equation of Q_L can be modeled as

$$\begin{aligned} L_{dL} C_{eqL} \frac{d^2 V_{dsL}}{dt^2} + R_{gL\_eq2} C_{eqL} \frac{dV_{dsL}}{dt} + V_{dsL} \\ = V_{DD} - V_{dsH} - V_{idsH} - V_{iddH} \end{aligned} \tag{62}$$

$$i_{dL} = C_{eqL} \frac{dV_{dsL}}{dt} \tag{63}$$

Combining (58)-(63) with (1), (12), (25), the relationship between the power loop and the driver loop of Q_H can be linked by i_{dL}

$$\begin{aligned} R_{gH} C_{gdH} \left(L_{dH} + L_{sH} + L_{dL}\right) \frac{d^2 i_{dL}}{dt^2} \\ + \left(R_{gH} R_{gL\_eq2} C_{gdH} + L_{sH} \right) \frac{di_{dL}}{dt} \\ + \frac{R_{gH} C_{gdH}}{C_{eqL}} i_{dL} + V_{miller} = 0 \end{aligned} \tag{64}$$

In this stage, the initial value and rate of i_{dL} are zero, the characteristic parameters are

$$\omega_{n\_H6} = \frac{1}{\sqrt{\left(L_{dH} + L_{sH} + L_{dL}\right) C_{eqL}}} \tag{65}$$

$$\xi_{H6} = \frac{R_{gH} R_{gL\_eq2} C_{gdH} + L_{sH}}{2 C_{gdH} R_{gH}} \sqrt{\frac{C_{eqL}}{L_{dH} + L_{sH} + L_{dL}}} \tag{66}$$

Correspondingly, the V_{gsL} crosstalk response can also be described by the separate equivalent model of the driver loop in Stage 3. There is a negative crosstalk voltage response of V_{gsL} due to the rapid drop of V_{dsL}.

3) STAGE 7 (t8-t9) CURRENT SWITCHING TIME

After V_{dsL} reaches the forward voltage of D_{bL}, the current begins to divert from the channel of Q_H to D_{bL}. V_{dsH} keeps the rising rate at $t8$ and starts oscillating, which is coupled with the current switching process. When V_{dsH} reaches V_{DD}, the charge rate of C_{gdH} no longer dominants the rising rate of V_{dsH}, C_{gdH} is paralleled with C_{dsH} and is involved in the oscillating of the power loop. However, similar to Stage 2, C_{gdH} stays at a minimum due to the nonlinear characteristic. The displacement current of C_{gdH} is much smaller than the charge current of C_{dsH} and the discharge current of C_{gsH}, which exerts little influence on the power loop and can be neglected in this stage. The equivalent circuit of this stage is shown in Fig. 8.

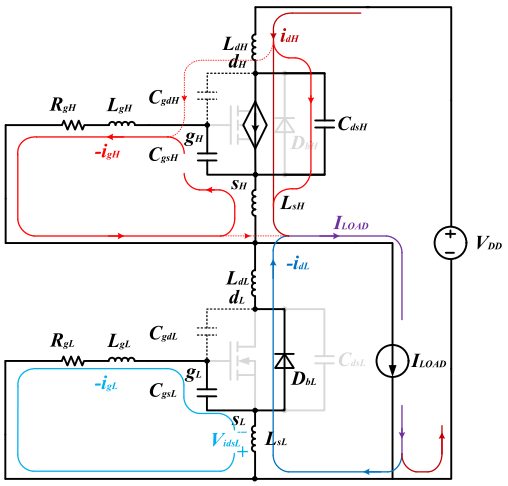

FIGURE 8. Equivalent circuit for Stage 7.

The driver loop of Q_H can be can be expressed as

$$R_{gH} i_{gH} + \left(L_{gH} + L_{sH}\right) \frac{di_{gH}}{dt} + V_{idsH} + V_{gsH} = 0 \quad (67)$$

where i_{gH} and V_{idsH} can be obtained from (2) and (12). Part of the drain current flowing through C_{dsH} dominates the oscillation of V_{dsH}. The remaining current flows through the channel, i_{dH} can be expressed as

$$i_{dH} = i_{ch} + C_{dsH} \frac{dV_{dsH}}{dt} \quad (68)$$

where i_{ch} is controlled by V_{gsH} which is given by (8).

The power loop can be established as

$$\left(L_{dH} + L_{sH} + L_{dL} + L_{sL}\right) \frac{di_{dH}}{dt} + L_{sH} \frac{di_{gH}}{dt} + V_{dsH} = V_{DD} \quad (69)$$

With the increase of the freewheeling current of D_{bL}, a negative induced voltage on L_{sL} is superimposed on the driver loop of Q_L. The equations of the driver loop are the same as Stage 2. Since the direction of the increasing freewheeling current is negative, a positive gate-source voltage fluctuation is induced in this stage.

4) STAGE 8 (t9-t10) V_{gsH} REMAINING DECREASING TIME

When the load current flows entirely through D_{bL}, Q_H is completely shut down and V_{gsH} decreases to zero, while the voltage and current of the power loop keep oscillation. Due to Q_H breaks away from the saturation region, all the parasitic capacitances of Q_H are involved in the oscillation in this stage. The equivalent circuit is shown in Fig. 9a.

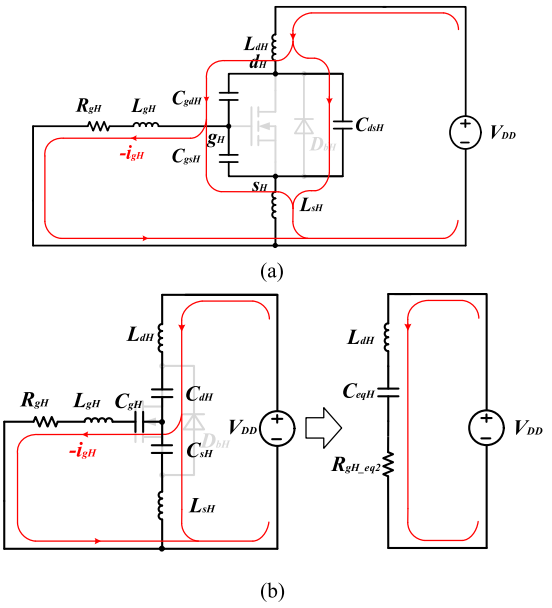

FIGURE 9. (a) Equivalent circuit for Stage 8. (b) Simplified equivalent circuit for Stage 8.

Similar to the state of Q_L in Stage 4, the paralleled driver loop of Q_H has a restrained effect on the oscillation. C_{gsH}, C_{gdH}, and C_{dsH} could be transformed to Y connection, which is given by (70) and the simplified equivalent circuit is shown in Fig. 9b.

$$\begin{cases} C_{gH} = C_{gsH} + C_{gdH} + C_{gsH} C_{gdH} / C_{dsH} \\ C_{sH} = C_{gsH} + C_{dsH} + C_{gsH} C_{dsH} / C_{gdH} \\ C_{dH} = C_{gdH} + C_{dsH} + C_{gdH} C_{dsH} / C_{gsH} \end{cases} \quad (70)$$

The equivalent damping resistance can be deducted as

$$\begin{aligned} R_{gH\_eq2} &= R_{gH} \left(\frac{|X_H|}{|X_{gH}|} \right)^2 \\ &= R_{gH} \frac{\left(\omega_{n\_P8} L_{sH} - \frac{1}{\omega_{n\_P8} C_{sH}} \right)^2}{R_{gH}^2 + \left(\omega_{n\_P8} L_{gH} - \frac{1}{\omega_{n\_P8} C_{gH}} + \omega_{n\_P8} L_{sH} - \frac{1}{\omega_{n\_P8} C_{sH}} \right)^2} \end{aligned} \quad (71)$$

where $\omega_{n\_P8} = 1/\sqrt{\left(L_{dH} + L_{sH}\right) C_{eqH}}$, and $C_{eqH} = C_{dL} C_{sL} / \left(C_{dL} + C_{sL}\right)$.

The power loop equations can be expressed as

$$V_{DD} = L_{dH} C_{eqH} \frac{d^2 V_{dsH}}{dt^2} + R_{gH\_eq2} C_{eqH} \frac{dV_{dsH}}{dt} + V_{dsH} \quad (72)$$

The characteristic parameters are

$$\omega_{n\_H8} = \frac{1}{\sqrt{C_{eqH} L_{dH}}} \tag{73}$$

$$\xi_{H8} = \frac{R_{gH\_eq2}}{2} \sqrt{\frac{C_{eqH}}{L_{dH}}} \tag{74}$$

This stage will extend until V_{dsH} stabilizes at V_{DD} and this process may spend more time than that V_{gsH} decreases to zero.

TABLE 1. The critical parameters in each stage and their effects.

stage	Main variable	Critical parameter		Omit parameter
		Parasitic element	Variable	
2	V_{gsH}	L_{sH}, R_{gH}, C_{gsH}	di_{dH}/dt	C_{gdH}
	di_{dH}/dt	--	g_f, V_{gsH}	C_{gdH}
	V_{dsH}	L_{dH}, L_{sH}, L_{dL}, L_{sL}	di_{dH}/dt	--
	V_{gsL}	L_{sH}	di_{dH}/dt	C_{gdL}
	I_{RR_BV}	Q_{SR}	$di_{dH}/dt\|_{t=t2}$	--
3	i_{dL}	C_{gdH}, R_{gH}, L_{sH}, C_{XL}	V_{miller}, I_{RR_BV}, $di_{dH}/dt\|_{t=t3}$	C_{gsH}, C_{dsH}, L_{gH}, L_{sH}, di_{gH}/dt, R_{gL}, L_{gL}
	dV_{dsL}/dt	C_{XL}	i_{dL}	
	V_{gsL}	R_{gL} L_{sH} C_{gdL}	di_{dH}/dt dV_{dsL}/dt	--
4	V_{dsL}	R_{gH_eq1}, R_{gL_eq1}, C_{XL}	$dV_{dsL}/dt\|_{t=t4}$	--
6	i_{dL}	C_{gdH}, R_{gH}, L_{sH}, C_{eqL}, R_{gL_eq2}	--	C_{gsH}, C_{dsH}, L_{gH}, L_{sH}, di_{gH}/dt
	dV_{dsL}/dt	C_{eqL}	i_{dL}	
	V_{gsL}	R_{gL} L_{sH} C_{gdL}	di_{dH}/dt dV_{dsL}/dt	--
7	V_{gsH}	L_{sH}, R_{gH}, C_{gsH}	di_{dH}/dt	C_{gdH}
	di_{dH}/dt	-- C_{dsH}	g_f, V_{gsH} dV_{dsH}/dt	C_{gdH}
	V_{dsH}	L_{dH}, L_{sH}, L_{dL}, L_{sL}	di_{dH}/dt, $dV_{dsH}/dt\|_{t=t8}$	C_{gdH}
	V_{gsL}	L_{sH}	di_{dH}/dt	C_{gdL}
8	V_{dsH}	C_{eqH}, R_{gH_eq2}	$dV_{dsL}/dt\|_{t=t9}$	--

Summarily, based on the preceding discussion, the critical parameters separately discussed of each stage and their effects on the main variables are summarized in Table 1.

III. EFFECTS OF CRITICAL PARAMETERS ON THE SWITCHING PERFORMANCE

Based on the derived model, the correlations between the main variable responses and the parameters in each stage are thoroughly analyzed. The influence mechanism and coupling effects of the critical parameters are clarified. Therefore, the influence trends can undergo further analysis to distinguish the effect weights of the critical parameters in each stage. A 600V/20A double pulse test circuit is built. The bridge-configuration is composed of the SiC MOSFETs, C2M0080120D, from Wolfspeed corporation. All the analytical calculation circuit parameters and the value of parasitic elements are based on this real circuit configuration within reasonable ranges, the switching process can be simulated by

TABLE 2. Fixed parameter setup.

Component	Parameter	Value	Parameter	Value
Power circuit	V_{DD}	600V	L_{dH_ex}+ L_{dL_ex}	5.5nH
	I_{DD}	20A	L_{LOOP}	50nH
	V_{GATE}	20V	R_{LOOP}	120mΩ
Upper and lower SiC MOSFET (C2M0080120D)	V_{th}	3.3V	Q_{RS}	26nC
	R_{gH_ex}	8.2Ω	R_{gL_ex}	8.2Ω
	R_{gH_in}	3.9Ω	R_{gL_in}	3.9Ω
	L_{gH_in}	1.1nH	L_{gL_in}	1.3nH
	L_{gH_ex}	2.6nH	L_{gL_ex}	2.7nH
	L_{sH_in}	1.3nH	L_{sL_in}	1.3nH
	L_{sH_ex}	3.7nH	L_{sL_ex}	3.4nH
	L_{dH_in}	1.2nH	L_{dL_in}	1.1nH

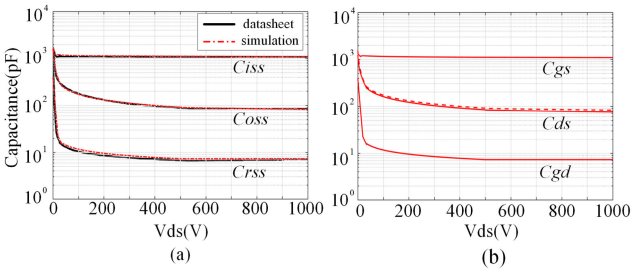

FIGURE 10. Nonlinear capacitance curves. (a) Comparison between the data from datasheet and the simulation. (b) interelectrode capacitances calculated by the simulation.

MATLAB calculations stage-by-stage. The initial and fixed parameters of the circuit model are listed in Table 2.

To ensure the accuracy of calculations, the nonlinear parameters should be described accurately. The datasheet of SiC MOSFET provides the curves of the input capacitance C_{iss}, the output capacitance C_{oss}, and the reverse transfer capacitance C_{rss} versus the drain-source voltage V_{ds}. According to the method provided in [19], [30], and [34], the nonlinearity of the capacitance can be piecewise fitted by (75), and the interelectrode capacitances can be obtained by (76) based on the datasheet.

$$C = C_{jo} \left(1 + \frac{V_{ds}}{V_j}\right)^{-m} \tag{75}$$

where C_{jo} is the capacitance value when $V_{ds} = 0$, V_j is the built-in voltage, m is the capacitance gradient factor. They can be adjusted according to the range of V_{ds}.

$$\begin{cases} C_{iss} = C_{gs} + C_{gd} \\ C_{oss} = C_{ds} + C_{gd} \\ C_{rss} = C_{gd} \end{cases} \tag{76}$$

Fig.10(a) shows the fitted capacitance curves compared with the datasheet. The interelectrode capacitance curves are shown in Fig.10(b). Since C_{gs} and C_{ds} are much larger than C_{gd}, the interelectrode capacitances curves are almost same as the parasitic capacitances' curves provided in the datasheet.

The transconductance g_f represents the transfer current capability of the channel. The datasheet provides the curve of the transfer characteristic, the nonlinear increase of i_{ch} could be piecewise fitted by (77).

$$i_{ch} = k_1 \left(V_{gs} - V_{th}\right)^n + k_2 \tag{77}$$

where k_1, k_2, and n are parameters of the transconductance and can be adjusted according to the value range of V_{gs}. Fig. 11(a) shows a comparison between the transconductance characteristic curve provided by the datasheet and the piecewise fitting result. Thus, the nonlinear curve of g_f can be obtained, which is shown in Fig.11(b). Notice that g_f becomes gentle when the rate of i_{ch} reaches the maximum.

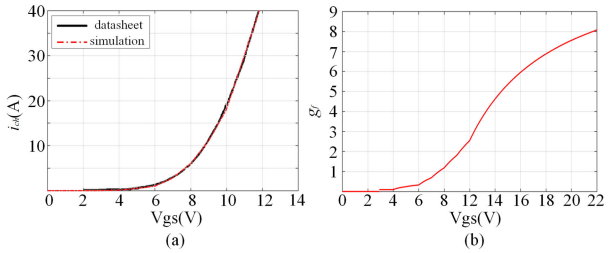

FIGURE 11. Nonlinear capacitance curves. (a) Comparison between the data from datasheet and the simulation. (b) interelectrode capacitances calculated by the simulation.

The piecewise fitting model of the interelectrode capacitances and g_f can be invoked as independent computing units based on the values of V_{dsH}, V_{dsL}, and V_{gsH} to obtain the precise values in every discrete computing period of MATLAB.

In order to compare the importance of different parameters in terms of their influences in the same stage, the original parameters of the model are referred to as the basic values. These basic values are varied by uniformly multiplying themselves by 1.5, 2, and 2.5 in this paper. Because of the nonlinear characteristics of interelectrode capacitances, the minimum values of the capacitances are used as the basic values.

A. CURRENT SWITCHING RATE

The current switching processes occur in Stage 2 and Stage 7, where Q_H works in the saturation region. In Stage 2a, the rising rate of i_{ch} is determined by the response of V_{gsH} and g_f. According to (15), the damping coefficient ξ_{H2} increases with the increases in R_{gH} and C_{gsH}, which reduces the slew rates of V_{gsH}. Fig. 12 (a) and (b) presents the turn-on analytical waveforms of V_{gsH} and i_{dH} with increased R_{gH} and C_{gsH}. L_{gH} also can reduce ξ_{H2}, but it has a lesser effect in comparison with C_{gsH}, L_{sH}, and R_{gH}. The analytical waveforms of V_{gsH} and i_{dH} are shown in Fig.12(c). It emerges that, a significant difference in the rising response of V_{gsH} and $i_{d\mathrm{H}}$ appears when L_{gH} increases over twenty times. The nonlinear growth of g_f promotes the increase of i_{dH}. According to (8), (11), and (12), when the rising rate of i_{dH} increases, the induced voltage on L_{sH} provides a negative feedback to the driver loop, which weakens V_{gsH} build-up, and the driver loop keeps its equilibrium state (13). (15) reveals that L_{sH} and g_f could

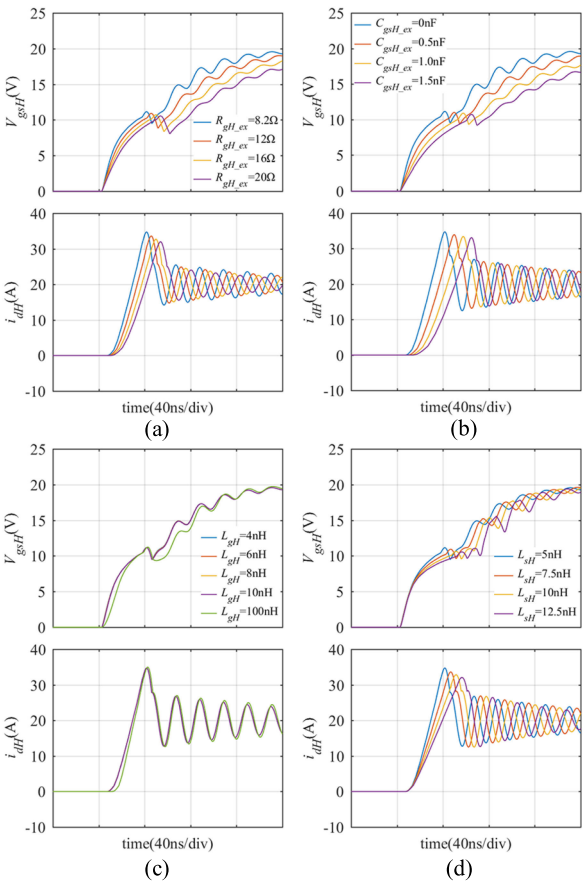

FIGURE 12. Analytical turn-on switching waveform of V_{gsH} and i_{dH} showing the effect of (a) Q_H driver resistance. (b) Q_H gate-source capacitance. (c) Q_H gate inductance. (d) Q_H source inductance.

increase ξ_{H2}, which decreases the response speed of V_{gsH}. Thus, it is noteworthy that although g_f ostensibly increases the rising rate of i_{dH}, it strengthens the negative feedback that restricts the rising rate of V_{gsH}, which in turn restrains the growth of g_f. As a result, the rising rate of i_{dH} will reach and be limited at its maximum. This effect will be more obvious with a larger L_{sH}. The analytical switching waveforms with varying L_{sH} are shown in Fig. 12(d). In Stage 2b, the reverse recovery current flows through D_{bL}. The rising rate of i_{dH} stays the same as that in Stage 2a. It is because the equilibrium state of the driver loop remains unchanged.

Fig. 13(a), (b), and (c) show the turn-off analytical switching waveforms of V_{gsH} and i_{dH}. Similar to the turn-on counterpart, the slew rate of i_{dH} decreases with larger R_{gH}, C_{gsH}, and L_{gH}. L_{sH} still provides a negative feedback to the driver loop. However, a portion of the drain current already starts switching in the voltage switching process (charging the parasitic capacitances C_{gdH} and C_{dsH} in Stage 6), which shunts the channel current i_{ch}. In Stage 7, this phenomenon will continue with the oscillation of V_{dsH}. The decrease rate of the shunted current through C_{dsH} depends on the characteristic of the power loop, which is determined by all the parasitic inductances of the bridge-leg according to (69), while L_{sH} hardly

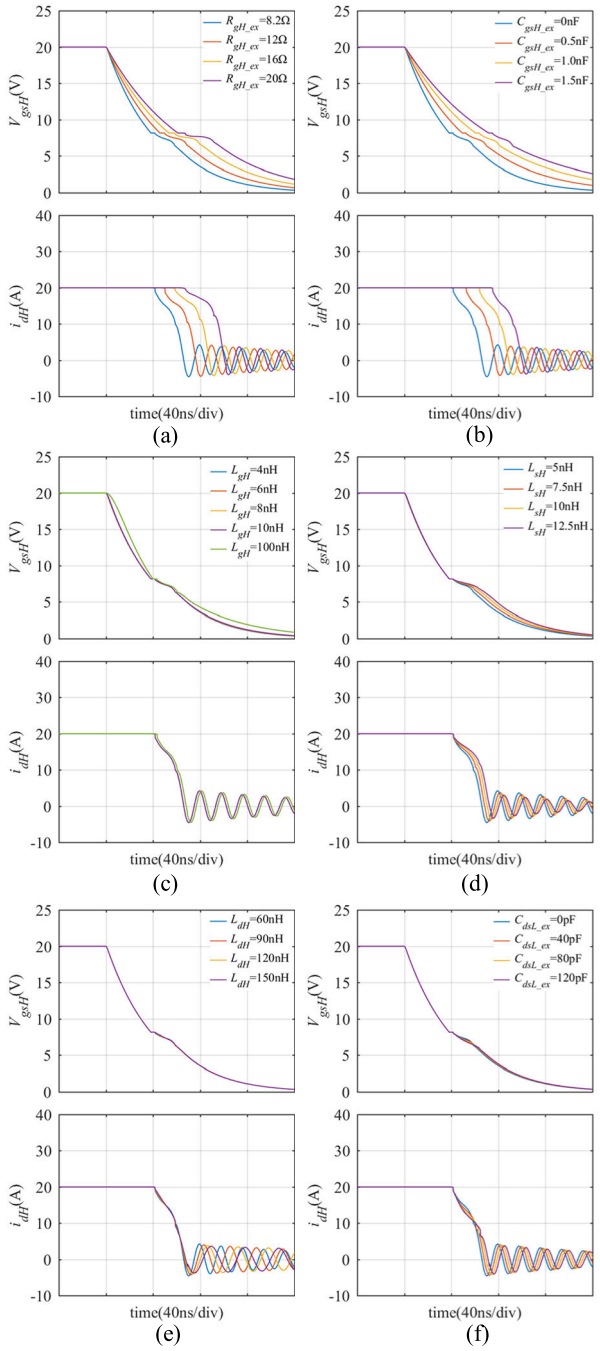

FIGURE 13. Analytical turn-off switching waveform of V_{gsH} and i_{dH} showing the effect of (a) Q_H driver resistance. (b) Q_H gate-source capacitance. (c) Q_H gate inductance. (d) Q_H source inductance. (e) parasitic inductances of the power loop. (f) Q_L drain-source capacitance.

changes the rate of the current through C_{dsH}. Thus, it can be considered as the shunted current through C_{dsH} weakens the negative feedback effect of L_{sH}, and i_{dH} is less controlled by the driver loop. Further, because of the shunted current through C_{dsH}, i_{ch} is smaller than I_{LOAD} at the beginning of Stage 7 and V_{gsH} has a lower value, which cause g_f to be smaller. The channel current i_{ch} decreases faster compared

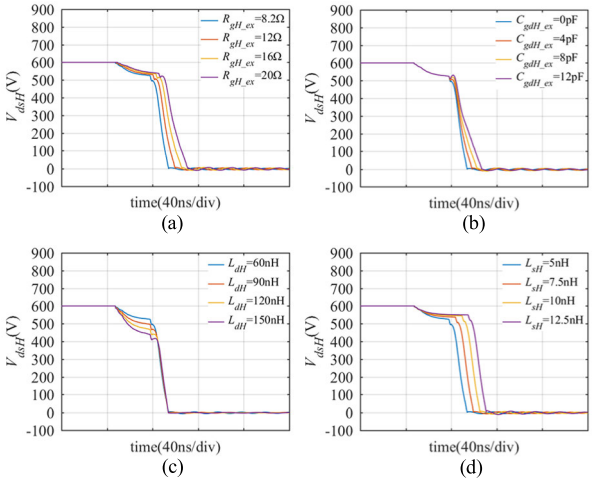

FIGURE 14. Analytical turn-on switching waveform of V_{dsH} showing the effect of (a) Q_H driver resistance. (b) Q_H gate-drain capacitance. (c) parasitic inductances of the power loop. (d) Q_H source inductance.

with the turn-on process in Stage 2. The turn-off analytical switching waveforms of V_{gsH} and i_{dH} with varying L_{sH} are shown in Fig. 13 (d). To compare Fig. 13 (d) with Fig. 12(d), the maximum rate of i_{dH} in the turn-off stage is faster than that in the turn-on stage. When L_{sH} increases, the variation tendency of the decrease rate of i_{dH} is less noticeable than it is in the turn-on stage. With the increase of the parasitic inductances of the power loop, the oscillation frequency drops, which causes the slew rate of i_{dH} to decrease, as shown in Fig.13(e). The increase in C_{dsH} extends its discharging time and increases the i_{dH} drop in Stage 6, and it has a limited effect on the current switching rate in Stage 7, as shown in Fig.13(f).

B. VOLTAGE SWITCHING RATE

The voltage switching processes occur in Stages 2, 3, and 6. In Stage 2, the rapid current switching of the power loop causes the induced voltages over the parasitic inductances and V_{dsH} to drop from V_{DD}. This voltage drop is determined by the value of the parasitic inductances and the rising rate of the drain currents. Fig. 14 (a), and (d) illustrate that the increase in R_{gH} and L_{sH} diminishes the amplitude of V_{dsH} drop, which is essentially because of the confined rising rate of i_{dH}. In Fig. 14 (c), the increase in L_{dH} raises the amplitude of V_{dsH} drop because voltage over it is higher.

In Stage 3, the decrease rate of V_{dsH} depends on the discharging speed of C_{gdH}. The discharging current is clamped by the state of the power loop, which is directly determined by R_{gH}, C_{gdH} and the value of V_{miller}. Besides, the reverse recovery current (drain current of Q_L) decreases in this stage, it charges the parasitic capacitances of Q_L depending on its initial state and influences the voltage switching responses indirectly.

It can be derived from the responses of the power loop, (31)-(34), that although the increases in R_{gH} and C_{gdH} could reduce the damping coefficient ξ_{H3}, however, they still exist

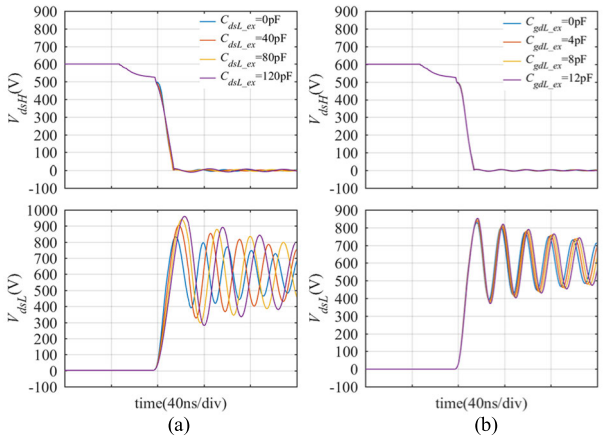

FIGURE 15. Analytical turn-on switching waveform of V_{dsL} and V_{dsL} showing the effect of (a) Q_L drain-source capacitance. (b) Q_L gate-drain capacitance.

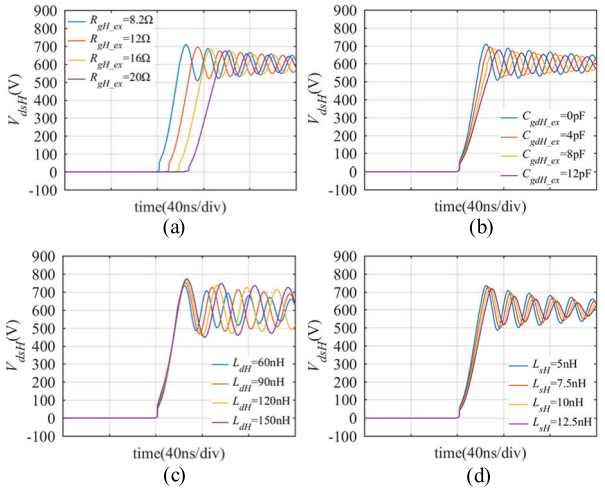

FIGURE 16. Analytical turn-off switching waveform of V_{dsH} showing the effect of (a) Q_H driver resistance. (b) Q_H gate-drain capacitance. (c) parasitic inductances of the power loop. (d) Q_H source inductance.

in the steady-state components of (31) and (34). This indicates that R_{gH} and C_{gd}H diminish i_{dL} and prolong the voltage switching time. Fig. 14 (a) and (b) illustrate the turn-on analytical switching waveforms of V_{dsH} with varying R_{gH} and C_{gdH}. The increase in parasitic inductances of the power loop (L_{dH}, L_{dL}, and L_{sL}) lead to ξ_{H3} and ω_{n_H3} decrease, which could aggravate the oscillations of i_{dL} and V_{dsL} in the next stage. Only the increase in L_{sH} results in a larger ξ_{H3}, which could slow down the slew rate of i_{dL} and reduce I_{RR_PEAK}. The turn-on analytical switching waveforms of V_{dsH} with varying L_{dH} and L_{sH} are shown in Fig. 14 (c) and (d).

Similarly, the increase in the equivalent capacitance of Q_L, C_{XL}, changes the characteristics of the power loop (ξ_{H3} increased and ω_{n_H3} decreased), but does not affect the voltage switching rate. In (31), the increase in C_{XL} directly causes the steady-state components of i_{dL} to increase, whereas it does not exist in the steady-state components of V_{dsL} in (34). C_{XL} is definitively determined by C_{dsL}. It is because that C_{gdL} is in series with C_{gsL}, especially C_{gdL} is less than C_{gsL} and C_{dsL} in one or two orders of magnitude, which hardly changes the value of C_{XL}. As shown in Fig. 10, C_{XL} is depicted by a dotted line which is almost near C_{dsL}. Fig. 15 presents the turn-on analytical waveforms of V_{dsH} and V_{dsL} with varying C_{dsL} and C_{gdL}.

In the voltage switching process, a non-negligible factor is the nonlinear characteristics of the interelectrode capacitances, especially the gate-drain capacitances, which significantly increase with the decrease of the drain-source voltage. In Stage 3, these changes increase ω_{n_H3} and decrease ξ_{H3}, which can accelerate the switching rate gradually.

To sum up, in the turn-on process, the voltage switching rate is determined by the clamped current of the driver loop of Q_H, the initial state of the reverse recovery current, the characteristics of the power loop, and the nonlinear characteristics of the interelectrode capacitances. It is the most complex switching process which involves numerous closely related parameters.

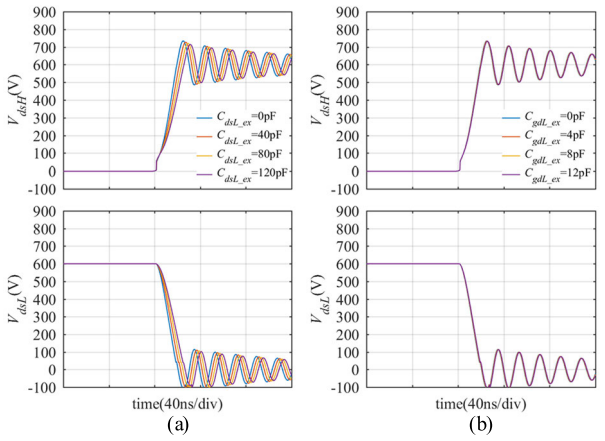

FIGURE 17. Analytical turn-off switching waveform of V_{dsL} and V_{dsL} showing the effect of (a) Q_L drain-source capacitance. (b) Q_L gate-drain capacitance.

In Stage 6, the restrictive conditions are the same as those in Stage 3. Fig. 16 displays the turn-off analytical switching waveforms of V_{dsH} with varying R_{gH}, C_{gdH}, L_{dH}, and L_{sH}. However, the initial values and rates of the charging currents of Q_H and the discharging currents of Q_L are zero, which prolong the switching time. Therefore, the voltage switching rate in this stage is lower than that in Stage 3 even under the same parasitic element conditions.

The increase in the parasitic capacitances of Q_L also increases the damping coefficient ξ_{H6}. The difference in the voltage slew rate is more noticeable than in the turn-on process. Fig. 17 presents the turn-off analytical switching waveforms of V_{dsH} and V_{dsL} with varying C_{dsL} and C_{gdL}.

Based on the current and voltage switching, fast slew rates serve as critical parameters that further exert knock-on effects on the switching process of the bridge-leg. The most significant impacts are the oscillations of the power loop and crosstalk phenomenon of the driver loop.

C. OSCILLATIONS IN THE POWER LOOP

The oscillations in the power loop occur in Stage 4, 7 and 8. In Stage 4, V_{dsL} reaches V_{DD} and keeps the rising rate from Stage 3, which can be regarded as the initial state of the power loop oscillation. According to (47) and (56), the oscillation intensifies with the decrease in C_{eqL} and the increase in the parasitic inductances of the power loop. The literature [33] reveals that the equivalent resistance R_{gH_eq1} has nonmonotonic relations with R_{gH} and L_{sH}, and the same trend is also true for R_{gL_eq1}. While it only considers the optimum value of driver resistance for taking the maximum of equivalent resistance to suppress the oscillation. The value of R_{gH_eq1} considered varying R_{gH} and L_{sH} is further presented in Fig. 18. It can be found that the maximum values of R_{gH_eq1} exist in the range of R_{gH} is less than 3.7Ω. However, the internal gate resistance of a SiC MOSFET is usually beyond this range. Thus, R_{gH_eq1} only decreases with the increase in R_{gH}. While R_{gH_eq1} is positively correlated with L_{sH}. Equally, the same result can be derived for R_{gL_eq1} according to (52).

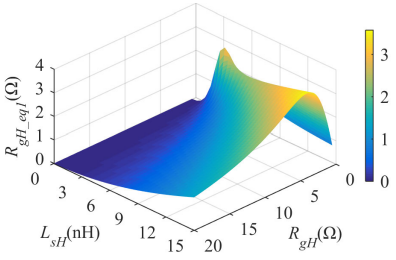

FIGURE 18. Equivalent resistance of Q_H with varied R_{gH} and L_{sH} in Stage 4.

Therefore, to suppress the oscillation, R_{gH} should decrease and L_{sH} should increase. Combined with the analysis of part B, the increases in R_{gH} and L_{sH} can reduce the initial rising rate of V_{dsL}, which could restrict the oscillation fundamentally. Thus, the increase in L_{sH} suppresses oscillation amplitude and shortens the oscillation time, whereas the increase in R_{gH} prolong the oscillation time. Fig. 19 illustrates the turn-on analytical oscillation waveforms of V_{dsL} with various L_{sH} and R_{gH}.

In Stage 7, the oscillation of the power loop is accompanied by the current switching process. The decrease in the channel current i_{ch} causes negative induced voltages across L_{dH} and L_{sH}, which are superimposed on the oscillation circuit (L_{dH} and L_{sH} - C_{dsH}). This factor increases the V_{dsH} amplitude of the initial oscillation. Combining the analyses of parts A and B, the increases in R_{gH}, C_{gsH}, C_{gdH}, and L_{sH} reduce the initial rising rate of V_{dsH} or the decrease rate of i_{ch}, which diminish the amplitude of V_{dsH}. While the increase in L_{dH} aggravates the oscillation amplitude. These trends are predicted by the analytical waveform in Fig. 16.

In Stage 8, Q_H is completely shut down. Similar to the state of Q_L in Stage 4, the trend of equivalent resistance R_{gH_eq2} can be obtained as shown in Fig. 20, where the gray translucent surface is R_{gH_eq1} in Stage 4. It shows that

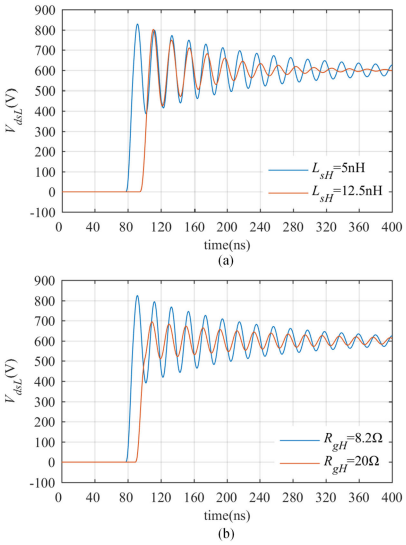

FIGURE 19. Analytical turn-on oscillation waveform of V_{dsL} showing the effect of (a) Q_H source inductance. (b) Q_H driver resistance.

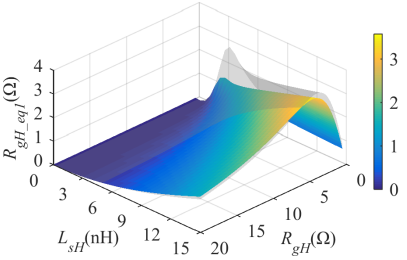

FIGURE 20. Equivalent resistance of Q_H with varied R_{gH} and L_{sH} in Stage 8.

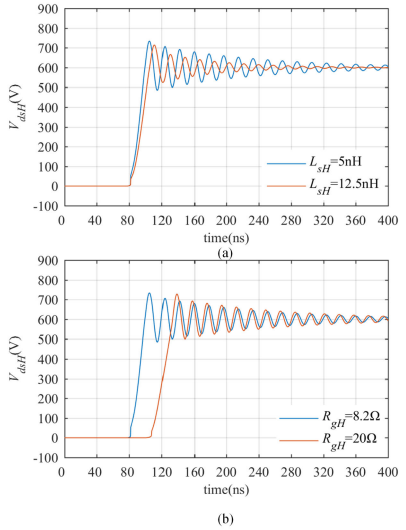

FIGURE 21. Analytical turn-off oscillation waveform of V_{dsH} showing the effect of (a) Q_H source inductance. (b) Q_H driver resistance.

R_{gH_eq2} has the same variation trend as varying R_{gH} and L_{sH} in Stage 4. Fig. 21 illustrates the turn-off analytical oscillation waveforms of V_{dsH} with varying L_{sH} and R_{gH}.

D. CROSSTALK OF THE DRIVER LOOP

During the turn-on and turn-off processes of Q_H, the crosstalk phenomenon occurs at the driver loop of Q_L and lasts almost throughout the whole switching process.

In Stage 2, a positive induced voltage of L_{sL} is superimposed on the driver loop of Q_L due to the rapid decrease of the current through L_{sL}, which induces a negative voltage fluctuation on V_{gsH}. In Stage 3, there are two factors impact the crosstalk, on the one hand, with the decrease of the reverse recovery current, the induced voltage over L_{sL} turns negative and induces a positive voltage fluctuation on V_{gsL}. On the other hand, the displacement current flows through C_{gdL} and is then shunted by C_{gsL} and the driver loop, which can also induce a positive pulse on V_{gsL}. The voltage on R_{gL} and L_{gL} achieves equilibrium with the sum of V_{gsL} and the induced voltage of L_{sL}, which satisfies equation (39). (39) illustrates that the fluctuation of V_{gsL} is positively correlated with the value and the slew rate of i_{dL}, where the value of i_{dL} reflects the rising rate of V_{dsL}.

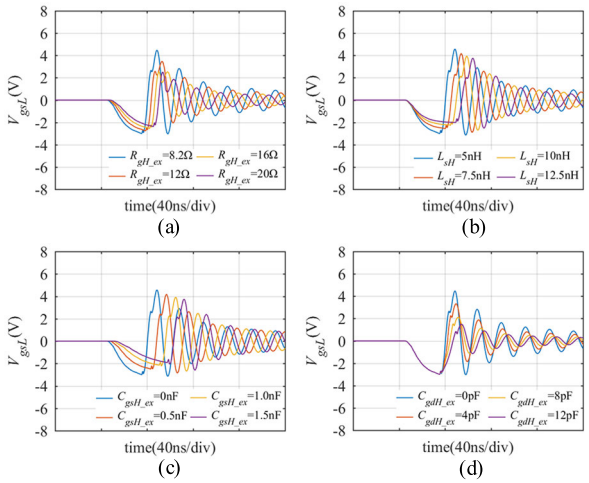

FIGURE 22. Analytical turn-on crosstalk waveform of V_{gsL} showing the effect of (a) Q_H driver resistance. (b) Q_H source inductance. (c) Q_H gate-source capacitance. (d) Q_H gate-drain capacitance.

Fig. 22 presents the analytical turn-on waveforms of V_{gsL} with varied elements that have obvious effects on the voltage or current switching rate. It is discovered that the elements related to the voltage switching rate, such as R_{gH} and C_{gdH}, have much more effects on the V_{gsL} positive crosstalk voltage, and the elements related to the current switching rate, such as L_{sH} and C_{gsH}, have relatively fewer effects on the crosstalk voltage, as they can only indirectly affect the current slew rate by changing the initial rate of the reverse recovery current at *t3*.

For C_{gdL} and L_{sL}, their increase will aggravate the effects of the two factors and intensify the positive fluctuation of V_{gsL}. Fig. 23 presents the analytical waveforms of V_{gsL} with the effects of varying C_{gdL} and L_{sL}. Combined with the earlier analysis, larger L_{sL} causes greater negative voltage fluctuations of V_{gsL} in Stage 2, and the crosstalk phenomenon is more serious overall.

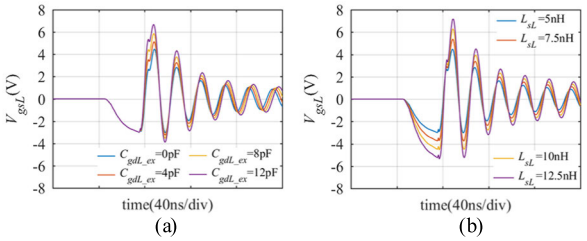

FIGURE 23. Analytical turn-on crosstalk waveform of V_{gsL} showing the effect of (a) Q_L gate-drain capacitance. (b) Q_L source inductance.

However, the impedance of the driver loop of Q_L itself has the opposite effects on these two factors. For the displacement current of C_{gdL}, the driver loop and C_{gsL} are equivalent to be in parallel. The increase in the impedance of the driver loop will promote a positive fluctuation of V_{gsL}. For the induced voltage of L_{sL}, the driver loop and C_{gsL} are equivalent to be in series. So, the increase in the impedance of the driver loop suppresses the positive fluctuation of V_{gsL}. According to (39), a larger R_{gL} increases the voltage formed by the displacement current of C_{gdL} flowing through the driver loop, which is shown in the right-hand side of the equation. Nevertheless, a larger R_{gL} also increases the damping coefficient ξ_{L3} of the driver loop in (41), which slows down the rising rate of V_{gsL}. Given the above reasoning, the influence of the driver loop impedance on the amplitude of the V_{gsL} is inconclusive.

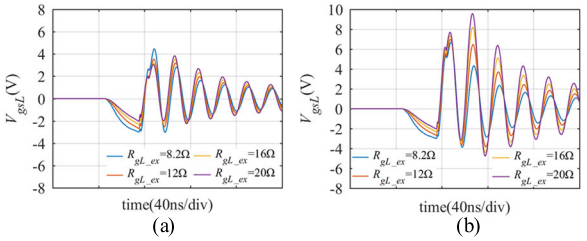

FIGURE 24. Analytical turn-on crosstalk waveform of V_{gsL} showing the effect of R_{gL} with (a) C_{gdL_ex} = 0pF. (b) C_{gdL_ex} = 8pF.

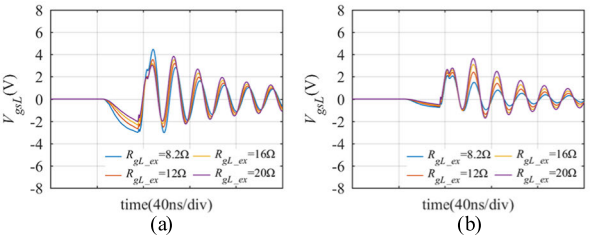

FIGURE 25. Analytical turn-on crosstalk waveform of V_{gsL} showing the effect of R_{gL} with (a) L_{sL} = 5nH. (b) L_{sL} = 2nH.

Fig. 24 presents the analytical waveforms of V_{gsL} with the effects of varied R_{gL} when external C_{gdL_ex} is paralleled or not. It reveals that with an increase in R_{gL}, the positive fluctuation of V_{gsL} will decrease if no external C_{gdL_ex} is paralleled, and will increase if C_{gdL_ex} = 8pF. Fig. 25 presents the analytical waveforms of V_{gsL} with the effects of varied R_{gL}, whether L_{sL} is reduced or not. Fig. 25 reveals that with an increase in R_{gL}, the positive fluctuation of V_{gsL} will decrease if L_{sL} keeps at 5nH, and will increase if L_{sL} is 2nH.

It can be concluded, that the positive fluctuations of V_{gsL} essentially depend on the balance of the displacement current of C_{gdL} and the induced voltage on L_{sL} acting on the driver loop. The variation of the impedance of the driver loop will change the balance point. Besides, it is noteworthy that the nonlinear characteristics of parasitic capacitances aggravate the crosstalk due to ξ_{L3} decreases and ω_{n_L3} increases.

In Stage 4, the driver loop is affected by the same factors as in Stage 3. The oscillations of V_{dsL} cause the currents through C_{gdL} and L_{sL} to oscillate, which leads to the oscillations of V_{gsL}.

During the turn-off process, the voltage and current switching rates affect the negative fluctuation amplitude of V_{gsL}. Fig. 26 shows the analytical turn-off crosstalk waveforms of V_{gsL} with varied elements that have obvious effects on the voltage or current switching rate. Similar to the turn-on process, the elements related to the voltage switching rate have much more effects on the negative amplitude of V_{gsL}.

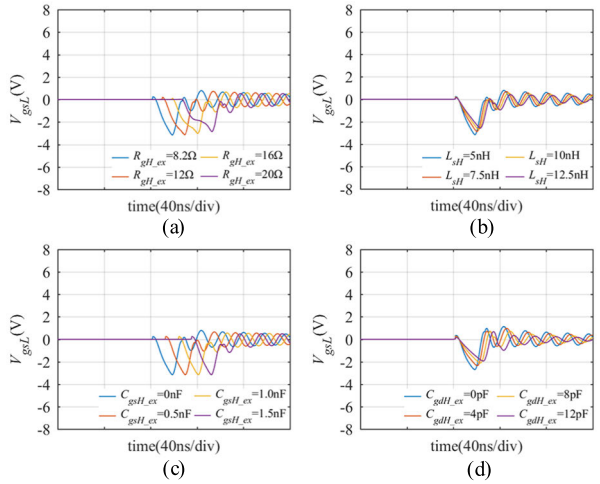

FIGURE 26. Analytical turn-off crosstalk waveform of V_{gsL} showing the effect of (a) Q_H driver resistance. (b) Q_H source inductance. (c) Q_H gate-drain capacitance. (d) Q_H gate-drain capacitance.

In the turn-off process, the voltage and current switching sequence is reversed. Therefore, the response of Q_L is different from that in the turn-on process. In Stage 6, the voltage starts to switch first, V_{dsL} decreases and the displacement current of C_{gdL} induces negative fluctuation in V_{gsL}. While there is no initial current when V_{dsL} decreases and i_{dL} starts to increase reversely from zero. It still causes negative induced voltage over L_{sL}, which could induce a positive fluctuation trend in V_{gsL}. These two factors produce opposite effects on the response of V_{gsL}. Thus, the increase in C_{gdL} promotes the negative fluctuation of V_{gsL}, while the increase in L_{sL} suppresses the fluctuation as shown in Fig. 27.

Therefore, the impedance of the driver loop of Q_L has the same effect on the two factors in Stage 6, which is different from the turn-on process. Fig.28 presents the analytical waveforms of V_{gsL} with the effects of varied R_{gL} when external C_{gdL_ex} is paralleled or not. Fig. 29 shows the analytical waveforms of V_{gsL} with the effects of varied R_{gL} when L_{sL}

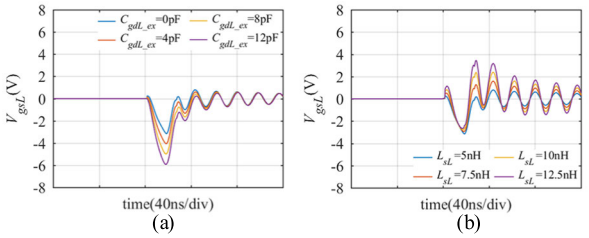

FIGURE 27. Analytical turn-off crosstalk waveform of V_{gsL} showing the effect of (a) Q_L gate-drain capacitance. (b) Q_L source inductance.

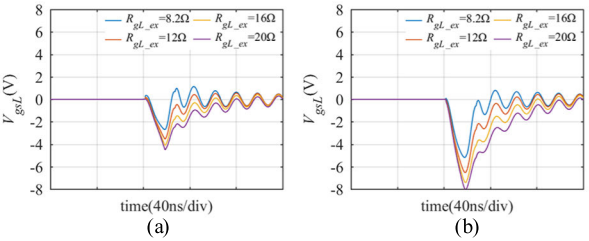

FIGURE 28. Analytical turn-off crosstalk waveform of V_{gsL} showing the effect of R_{gL} with (a) C_{gdL_ex} = 0pF. (b) C_{gdL_ex} = 8pF.

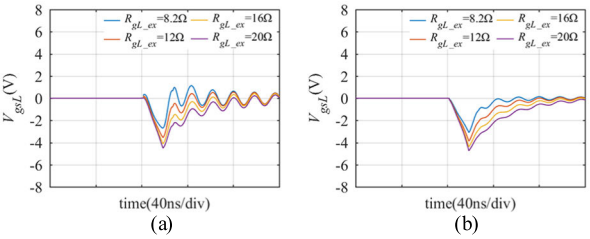

FIGURE 29. Analytical turn-off crosstalk waveform of V_{gsL} showing the effect of R_{gL} with (a) L_{sL} = 5nH. (b) L_{sL} = 2nH.

is reduced or not. Combining Fig. 28 with Fig. 29, it can be deduced that the increase in R_{gL} aggravates the negative fluctuation amplitude of V_{gsL} no matter how C_{gdL} and L_{sL} change.

In Stage 7, D_{bL} starts to conduct, the displacement current of C_{gdL} drops to zero and the reverse rising rate of i_{dL} increases, which causes a larger negative induced voltage on L_{sL}. These factors induce a positive fluctuation in V_{gsL} based on Stage 6. If L_{sL} is large, a positive crosstalk voltage may appear, as the comparison shown in Fig. 29, while R_{gL} helps to suppress the upward voltage fluctuation.

IV. EXPERIMENTAL VERIFICATION

The bridge-leg test circuit has been designed for the experimental evaluation of the proposed analytical model. Fig. 30 shows the photograph of the test platform. Two SiC MOSFETs form the bridge-leg structure, and a 20 μH ferrite-core inductor is connected in parallel with the lower SiC MOSFET as the load inductor. The test circuit is fed by 600 V DC supply voltage, multiple groups of capacitances are connected in parallel with the input end to ensure the stability of the support DC voltage. The DC loop was designed to minimize the parasitic inductances. The external pins of the devices and the connecting leads of the power loop is

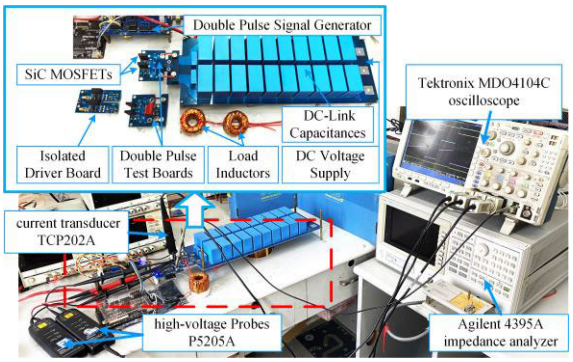

FIGURE 30. Photograph of the double pulse test platform.

measured by an Agilent 4395A impedance analyzer, the internal pins of the devices and the printed circuit board PCB layout is implemented by finite-element analysis of ANSYS Q3D [35]. The measurement and extraction results are listed in TABLE 2.

A high speed high current gate driver IXDN409 is selected to provide sufficient gate driver capability. The gate driver resistances of upper and lower transistors are chosen as 8.2Ω, which could maintain an appropriate switching speed to present the different switching stages of the bridge-leg. Since there is no any crosstalk suppression method in the experiment, in order to prevent spurious trigger of Q_L, the negative driver voltage level of the lower SiC MOSFET is set at −4V, this negative voltage bias does not have a significant effect on the responses of crosstalk voltage.

The measurement system should have enough bandwidth to acquire trustworthy experimental results. Power loop switching voltage is measured by high-voltage differential probes: P5205A (1300 V/100 MHz). The gate driver voltage of Q_L is measured by voltage probes: TPP0101 (300 V/100 MHz). The drain current is measured by a current transducer: TCP202A (30A peak/50MHz). These switching waveforms were carried out with the Tektronix MDO4104C, 1GHz oscilloscope. It should be noted that the delay time between the current probe and the voltage probe is 11.5ns displayed on the oscilloscope, which should set delay compensation to eliminate the deviation.

Double pulse test results are compared with the analytical results shown as follows. Particularly, in order to facilitate the comparison of crosstalk fluctuation amplitude, the −4V of the experimental V_{gsL} coordinates and the 0V of the analytical $V_{gs}L$ coordinates are set as the same reference position. Fig. 31 shows the turn-on and turn off switch waveforms.

To verify the model under different voltages, double pulse test results when DC voltage is 400V while other test conditions remain unchanged are shown in Fig. 32.

To verify the model under different load currents, moving the double pulse trigger signal position to change the load current, double pulse test results when the load current is 10A while other test conditions are not changed are shown in Fig. 33.

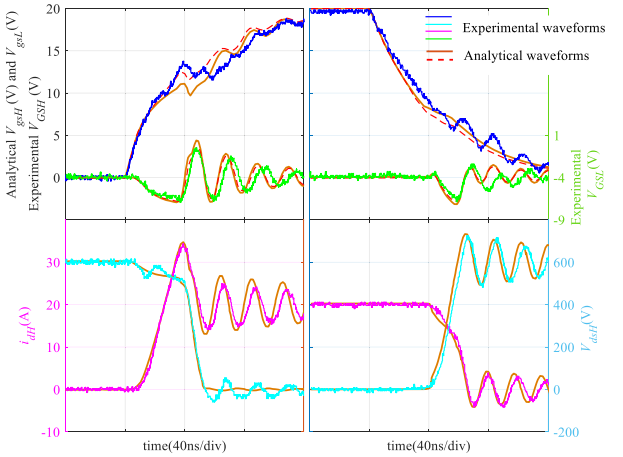

FIGURE 31. Comparison of experiment and analytical waveforms @600V/20A. Left: turn-on waveforms, right: turn-off waveforms: V_{gsH} and V_{gsL} (5V/div), V_{dsH} (200V/div), I_{dH} (10A/div), and t (40ns/div).

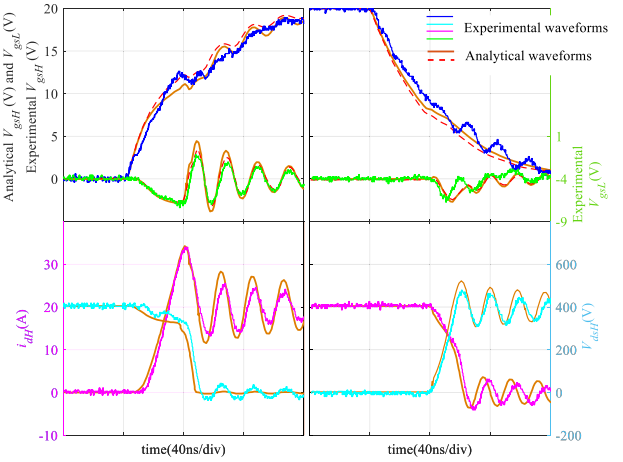

FIGURE 32. Comparison of experiment and analytical waveforms @400V/20A. Left: turn-on waveforms, right: turn-off waveforms: V_{gsH} and V_{gsL} (5V/div), V_{dsH} (200V/div), I_{dH} (10A/div), and t (40ns/div).

It can be seen from Figs. 31 to 33 the analytical results match test results very well. The proposed analytical model can correctly represent the switching transient waveforms in terms of the voltage slope, the current slope, reverse recovery current, oscillation of the power loop, and the crosstalk of the driver loop.

In practice, the voltage measurement probes can only be connected between the external terminals, the internal voltages of parasitic elements are included in the measurement values. The gate-source voltages between the external package nodes are expressed by V_{GSH} and V_{GSL}, their relationships with the internal voltages are given by equations (78) and (79). The analytical waveforms of V_{GSH} and V_{GSL} are depicted in red dashed curves in Figs. 31 to 33.

$$V_{GSH} = V_{gsH} + R_{gH\_in} i_{gH} + \left(L_{gH\_in} + L_{sH\_in}\right) \frac{di_{gH}}{dt} + L_{sH\_in} \frac{di_{dH}}{dt} \tag{78}$$

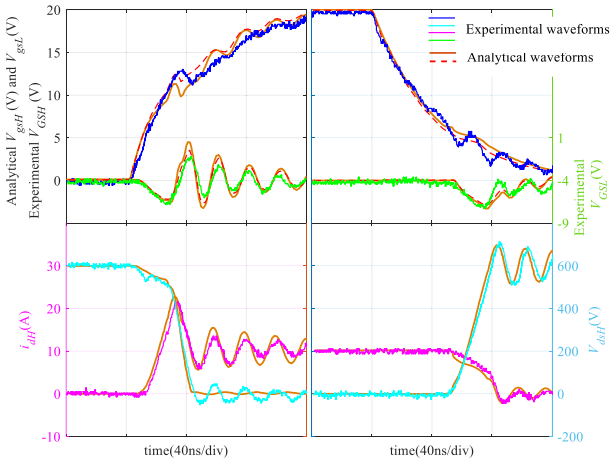

FIGURE 33. Comparison of experiment and analytical waveforms @600V/10A. Left: turn-on waveforms, right: turn-off waveforms: V_{gsH} and V_{gsL} (5V/div), V_{dsH} (200V/div), I_{dH} (10A/div), and t (40ns/div).

$$V_{GSL} = V_{gsL} + R_{gL\_in} i_{gL} + \left(L_{gL\_in} + L_{sL\_in}\right) \frac{di_{gL}}{dt} + L_{sL\_in} \frac{di_{dL}}{dt} \tag{79}$$

Thus, for the driver loop of Q_H, the measured value of the gate-source voltage is larger than the calculated values in the turn-on process, while smaller in the turn-off process. Similarly, since the gate and source internal parasitic elements of Q_L share part of the gate-source voltage, the measured value of gate-source voltage is smaller than the calculated value during the turn-on and turn-off process. The crosstalk phenomena by experimental measurements can therefore be compared with the analytical waveforms of V_{GSL} and V_{gsL} in Figs. 31 to 33.

In the power loop, the measured V_{dsH} includes the induced voltages of L_{dH_in} and L_{sH_in}, this internal parasitic inductance forms an LC circuit with the drain-source capacitances, which causes the measured V_{dsH} has fluctuations with the voltage drop in Stage 2 and the more obvious oscillation in Stage 4.

The oscillation frequency and oscillation attenuation amplitude of the voltage and current provided by the experimental results are slightly larger than those of the proposed analytical model. During the voltage switching process (Stage 3 and Stage 6), there is a deviation between the calculation results and the actual response curve of drain current. It is because of the difference of the nonlinear capacitances model with the actual capacitances value and the measurement deviation of parasitic inductances of the power loop. These deviations are inevitable but the variation trend can still be correctly inferred.

Next, a series of experimental results be provided to verify the trends of the switching speed, the duration and amplitude of power loop oscillation, and the magnitude of the crosstalk voltage under the influence of critical parameters. The adjustment rules of each element are the same as in section III.

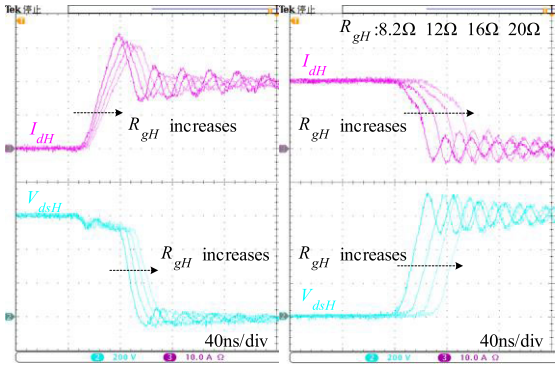

FIGURE 34. Experimental switching waveform of i_{dH} and V_{dsH} showing the effect of R_{gH}. Left: turn-on, right: turn-off.

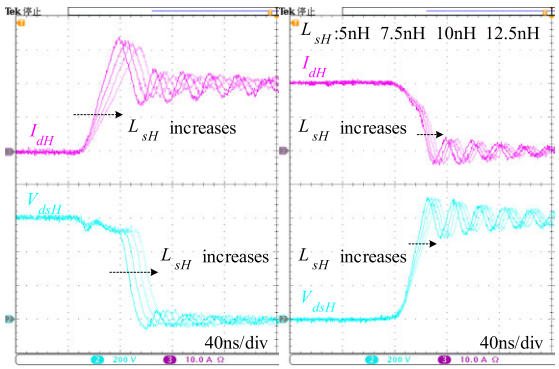

FIGURE 35. Experimental switching waveform of i_{dH} and V_{dsH} showing the effect of L_{sH}. Left: turn-on, right: turn-off.

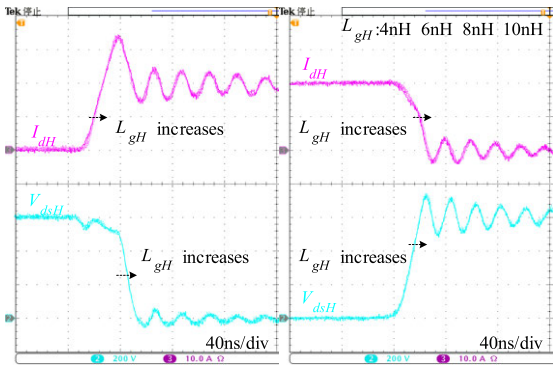

FIGURE 36. Experimental switching waveform of i_{dH} and V_{dsH} showing the effect of L_{gH}. Left: turn-on, right: turn-off.

The switching waveforms with the varied elements are superimposed on one capture window of the oscilloscope.

Figs. 34-41 display the experimental switching waveforms of i_{dH} and V_{dsH} under the influence of the elements of the driver loop of Q_H and the power loop respectively.

Fig. 34 and Fig. 35 show the experimental waveforms of i_{dH} and V_{dsH} with varying R_{gH} and L_{sH} respectively, both of them have influences on the current and voltage switching rate. The current slew rate decreases in the turn-on and turn-off processes with the increase in R_{gH}. L_{sH} has the same obvious influence on the current slew rate in the

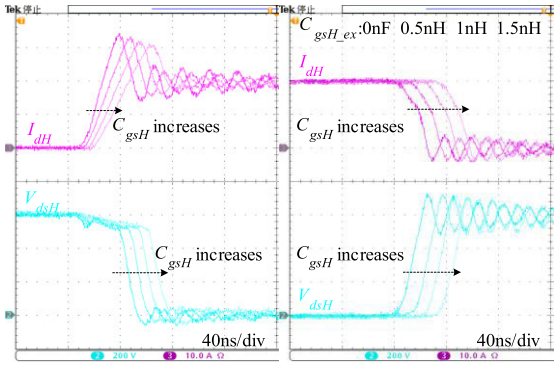

FIGURE 37. Experimental switching waveform of i_{dH} and V_{dsH} showing the effect of C_{gsH}. Left: turn-on, right: turn-off.

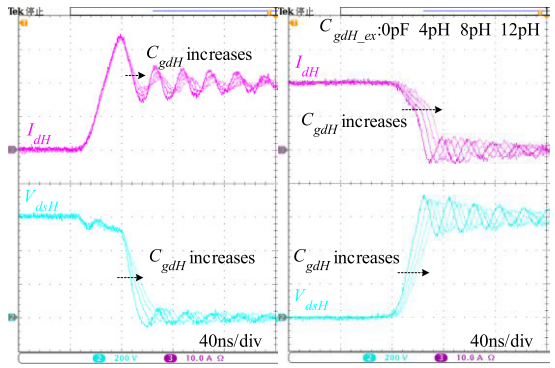

FIGURE 38. Experimental switching waveform of i_{dH} and V_{dsH} showing the effect of C_{gdH}. Left: turn-on, right: turn-off.

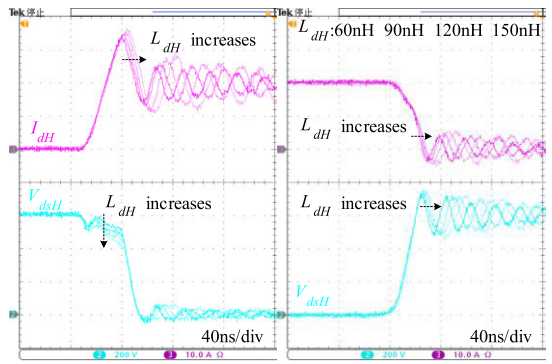

FIGURE 39. Experimental switching waveform of i_{dH} and V_{dsH} showing the effect of L_{dH}. Left: turn-on, right: turn-off.

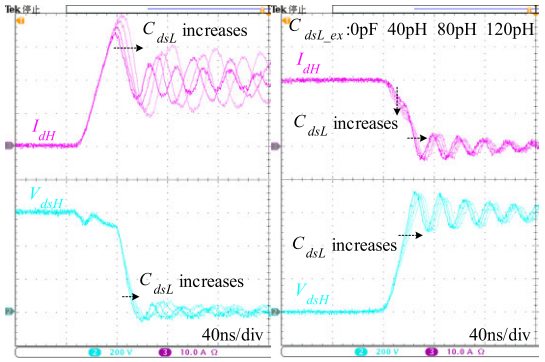

FIGURE 40. Experimental switching waveform of i_{dH} and V_{dsH} showing the effect of C_{dsL}. Left: turn-on, right: turn-off.

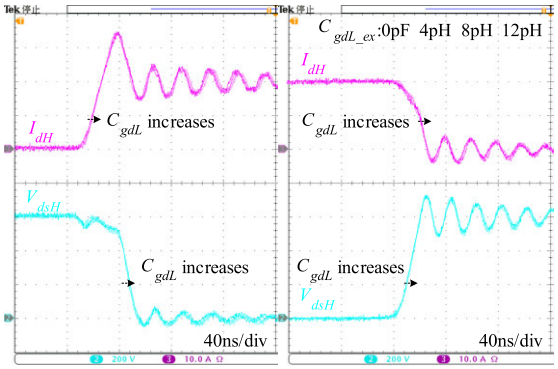

FIGURE 41. Experimental switching waveform of i_{dH} and V_{dsH} showing the effect of C_{gdL}. Left: turn-on, right: turn-off.

turn-on process, while its influence is smaller in the turn-off process, which shows the same characteristics as Fig. 12 and Fig. 13 predicted. The change range of the voltage slew rates with varied L_{sH} is relatively small, which confirms the explanation in section III.

As shown in Fig. 36, The turn-on and turn-off experimental switching waveforms with different L_{gH} are the same as the analytical model prediction, which shows little change in the switching rate.

The experimental current and voltage switching waveforms under the influence of C_{gsH} are shown in Fig. 37, the current slew rate decreases significantly with the increase in C_{gsH} during both the turn-on and turn-off process, while the voltage slew rates are barely changed. Fig. 38 displays the experimental switching waveforms under the influence of C_{gdH}, which shows the voltage slew rate was reduced significantly with the increase of C_{gdH}, while the current slew rate has almost no change. These trends are consistent with the analytical model prediction for the impacts of critical elements in the different stages.

Same as the model setting rules, all the power loop parasitic inductances are denoted by L_{dH}. The experimental waveforms under the influence of the power loop parasitic inductances are depicted in Fig. 39, which illustrate that the increase in L_{dH} aggravates the amplitude of the reverse recovery current overshoot and the amplitude of the oscillation, but they have no significant effect on the current and voltage switching rate during the turn-on process, and it slightly restrains the current slew rate during the turn-off process, these phenomena confirm the analysis of section III.

Fig. 40 and Fig. 41 show the experimental waveforms under the influence of C_{dsL} and C_{gdL}. It can be seen that only C_{dsL} causes obvious changes in the current and voltage oscillation, which are consistent with the analytical results. Compare Fig. 39 and Fig 40, the increase in C_{dsL} has the same effect on current and voltage as L_{dH} during the turn-on process. However, in the turn-off process, the increase in C_{dsL} reduces the voltage switching rate and causes a greater current

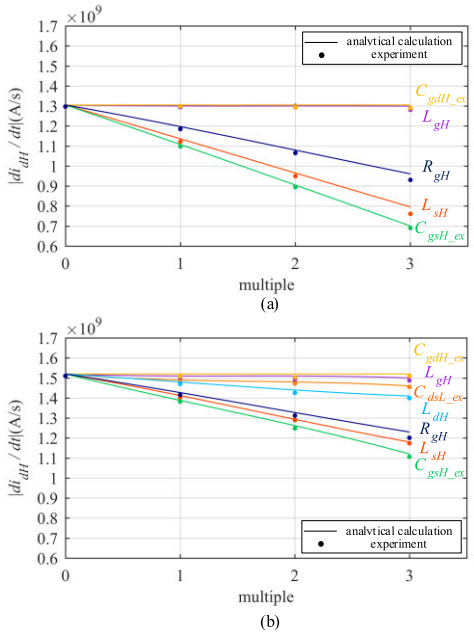

FIGURE 42. Variation trend of i_{dH} switching rate with different elements effect. (a) turn-on. (b) turn-off.

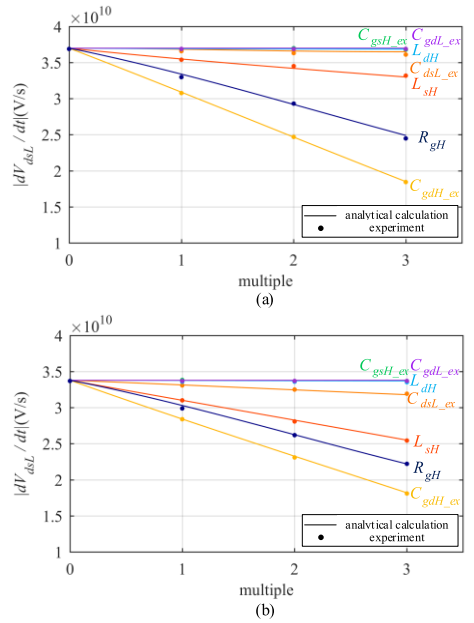

FIGURE 43. Variation trend of V_{dsH} switching rate with different elements effect. (a) turn-on. (b) turn-off.

drop in Stage 6. While after the voltage switching process, C_{dsL} is short-circuited and it does not affect the oscillating characteristics.

Summarizing the influence of all these key elements on the current and voltage switching rate, the comparisons of the influence trends with different elements obtained from experiments and analytical calculations are illustrated in Fig. 42 and Fig. 43 respectively. Fig. 42 illustrates that the elements that have obvious effects on the current switching

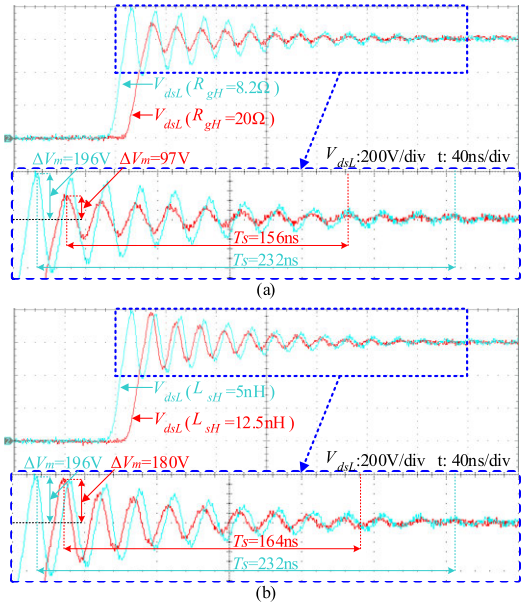

FIGURE 44. The turn-on oscillation experimental waveforms of V_{dsL} showing the effect of R_{gH} and L_{sH}.

rate are C_{gsH}, L_{sH}, and R_{gH} in sequence, the parasitic inductances of the power loop and C_{dsL} also have influences on the current slew rate in the turn-off process. Fig. 43 illustrates that the elements that have obvious effects on the voltage switching rate are C_{gdH}, R_{gH}, and L_{sH} in sequence. Overall, the current switching rate in the turn-off process is generally faster than the turn-on process under the same conditions, while the voltage switching rate is just the opposite. Moreover, combining these two figures, it is shown that the effects of the driver loop elements on the variation ranges of current and voltage switching rate in the turn-on process are more obvious than those in the turn-off process.

With the transition of the stages, the parasitic inductances and the equivalent parasitic capacitances in the power loop cause oscillations, the increase in these elements aggravates the amplitude of the oscillation, which has been verified in the previous experimental waveforms as shown in Fig. 39 and Fig. 40.

Fig. 44 compares the turn-on experimental oscillation waveforms of V_{dsL} with R_{gH} and L_{sH} increases, and Fig. 45 compares the turn-off experimental oscillation waveforms of V_{dsH} with R_{gH} and L_{sH} increased.

In Fig. 44 and Fig. 45, the amplitude of the maximum peak value of V_{dsL} and V_{dsH} exceeding V_{DD} is marked as ΔV_m, the duration from the maximum peak value of V_{dsL} and V_{dsH} to the oscillation amplitude within 5% V_{DD} is T_s. Since the increase in R_{gH} and L_{sH} slows down the initial rate of the voltage, introduce $\lambda = T_s / \Delta V_m$ as the oscillation duration coefficient, the larger λ indicates the longer relative duration of the oscillation. The results are listed in Table 3.

As shown in Table 3, in the turn-on process, although the increase in R_{gH} can reduce the maximum peak value of V_{dsL} increases from 196V to 97V and the oscillation

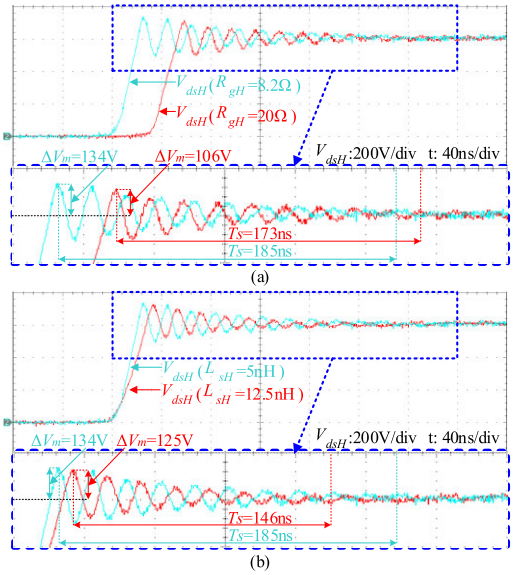

FIGURE 45. The turn-off oscillation experimental waveforms of V_{dsL} showing the effect of R_{gH} and L_{sH}.

TABLE 3. Turn-on V_{dsL} and turn-off V_{dsH} oscillation characteristics with R_{gH} and L_{sH} regulated.

Test conditions			Initial state	R_{gH} increased	L_{sH} increased
Adjusted components		R_{gH} (Ω)	8.2	20	8.2
		L_{sH} (nH)	5	5	12.5
Turn on	Parameters	R_{gH_eq1} (Ω)	0.432	0.179	2.126
		ξ	0.031	0.023	0.084
	V_{dsL} Response	ΔV_m (V)	196	97	180
		overshoot	32.7%	16.2%	30%
		T_s (ns)	232	156	164
		λ (ns/V)	1.18	1.61	0.91
Turn off	Parameters	R_{gH_eq2} (Ω)	0.431	0.181	2.215
		ξ	0.028	0.023	0.062
	V_{dsH} Response	ΔV_m (V)	134	106	125
		overshoot	22.3%	17.6%	21%
		T_s (ns)	185	173	146
		λ (ns/V)	1.38	1.63	1.17

duration drops from 219ns to 166ns, the damping coefficient ξ decreases from 0.031 to 0.023 and λ increases from 1.18 to 1.61, which indicates that the relative duration of the oscillation is prolonged with the increase in R_{gH}. The increase in L_{sH} reduces the maximum peak value of V_{dsL} and also causes ξ increase from 0.031 to 0.084, λ decreases to 0.91. Thus, the relative duration of the oscillation is shortened significantly. Similarly, in the turn-off process, the increase in R_{gH} prolongs the relative duration of the V_{dsH} oscillation, λ increases from 1.38 to 1.63; the increase in L_{sH} shortens the relative duration of the V_{dsH} oscillation with λ decreases

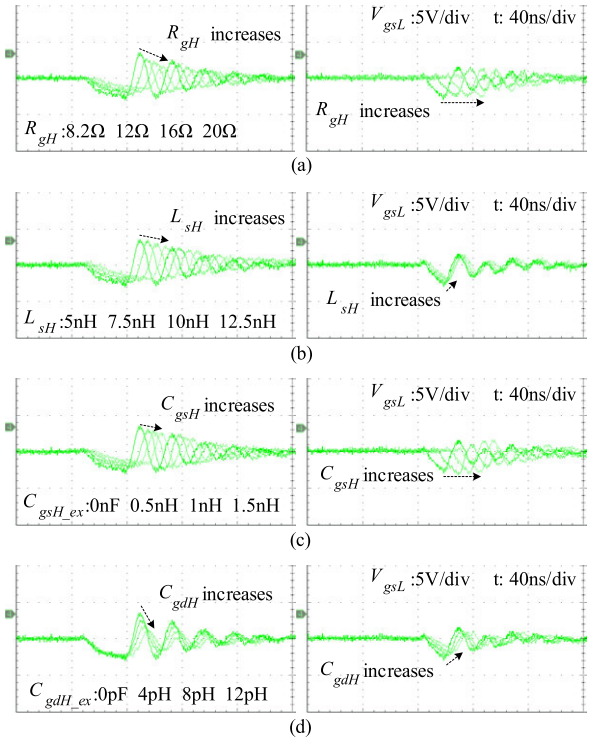

FIGURE 46. Experimental crosstalk waveform of V_{gsL} showing the effect of (a) Q_H driver resistance. (b) Q_H source inductance. (c) Q_H gate-source capacitance. (d) Q_H gate-drain capacitance. Left: turn-on, right: turn-off.

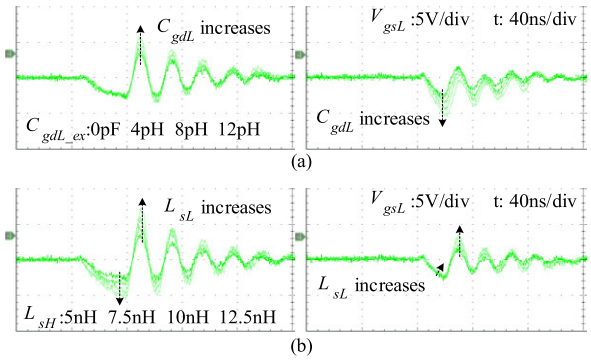

FIGURE 47. Experimental crosstalk waveform of V_{gsL} showing the effect of (a) Q_L gate-drain capacitance. (b) Q_L source inductance. Left: turn-on, right: turn-off.

to 1.17. This series of experiment results verify the analytical model prediction.

Fig. 46 displays the experimental waveforms of V_{gsL} under the influence of R_{gH}, L_{sH}, C_{gsH}, and C_{gdH}. Obviously, the increase in R_{gH} and C_{gdH} restrain the amplitude of the crosstalk voltage, while L_{sH} and C_{gsH} have relatively small impacts on the crosstalk voltage. These results are consistent with the analytical model shown in Fig. 22.

The experimental waveforms of V_{gsL} under the influence of C_{gdL} and L_{sL} are depicted in Fig. 47. In the turn-on process, both of them aggravate the amplitude of the crosstalk voltage. While in the turn-off process, it can be seen that the increase in C_{gdL} intensifies the negative crosstalk voltage,

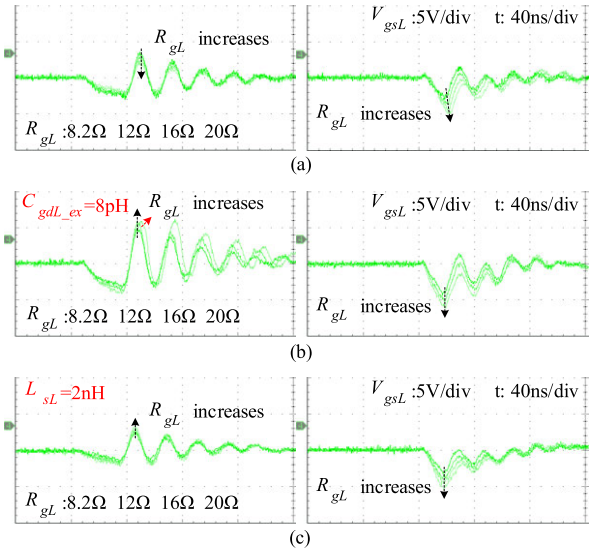

FIGURE 48. Experimental crosstalk waveform of V_{gsL} showing the effect of Q_L gate resistance increase with (a) C_{gdL_ex} = 0pF, L_{sL} = 5nH. (b) C_{gdL_ex} = 8pF, L_{sL} = 5nH. (c) C_{gdL_ex} = 0pF, L_{sL} = 2nH. Left: turn-on, right: turn-off.

the increase in L_{sL} restrains the negative crosstalk voltage, which agrees with the analytical switching waveforms shown in Fig. 23 and Fig. 27.

The experimental crosstalk waveforms under the influence of R_{gL} are depicted in Fig. 48. The crosstalk voltage waveforms with the default parasitic parameter settings are shown in Fig. 48(a), the increase in R_{gL} restrains the positive fluctuation of V_{gsL}. Fig. 48(b) shows the experimental waveforms of V_{gsL} with external C_{gdL_ex} paralleled, instead, the increase in R_{gL} aggravates the amplitude of the crosstalk voltage. It should be noticed that when R_{gL} increases to 12Ω, Q_L has a spurious turn-on phenomenon, the amplitude and the oscillation frequency of the crosstalk voltage are changed. Fig. 48(c) shows the experimental waveforms of V_{gsL} with L_{sL} decreases to 2nH, it is discovered that the crosstalk voltage is significantly reduced, but the increase in R_{gL} aggravates the amplitude of the crosstalk voltage. Fig. 48 also illustrates that the increase in R_{gL} aggravates the negative amplitude of V_{gsL} no matter how C_{gdL} and L_{sL} change in the turn-off process. All these results concluded from the combined comparison of the three experiments are consistent with the analytical model prediction.

V. CONCLUSION

A detailed and accurate circuit-level analytical model for a bridge-leg configuration based on SiC MOSFETs is proposed in this paper. Clear piecewise linear turn-on and turn-off switching processes are presented in detail and the critical parameters that have dominating effects on the variable switching responses in each switching stage are identified flexibly and independently. The influence mechanisms of these staged critical parameters on the main switching variables are analyzed in detail. Based on this model, the impacts of the critical parameters on the switching speed, the knock-on effects on the oscillation of the power loop, and the crosstalk of the driver loop are further studied, which are the important features of a bridge-leg. The influence degrees and trends of these staged critical parameters on the switching processes are derived and compared. The switching waveforms in a bridge-leg, which consists of 1200 V/ 20A SiC MOSFETs are measured and compared with the analytical results. The proposed model shows are successfully verified by experimental measurements and the influences of the critical parameters on the switching performance are successfully verified. The proposed model can be employed in the design and development of the power converters based on SiC MOSFETs bridge configurations to evaluate their operational performances, stability, and reliability for high power and/or high frequency applications.

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