IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received January 7, 2021, accepted January 27, 2021, date of publication February 2, 2021, date of current version February 9, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3056151

Research on Negative Bias Temperature Instability Effects Under the Coupling of Total Ionizing Dose Irradiation for PDSOI MOSFETs

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This work was supported in part by the National Natural Science Foundation of China under Grant 61704031 and Grant 12075065, and in part by the Guangdong Basic and Applied Basic Research Foundation under Grant 2019A1515012213.

ABSTRACT The degradation mechanisms for pMOSFETs from a 130 nm partially-depleted silicon on insulator (PDSOI) technology under the combined effects of total ionizing dose (TID) and negative bias temperature instability (NBTI) are investigated. The TID and NBTI related degradations show an opposite trend as gate oxide scaling, which implies the different traps are activated during irradiation and NBTI stress. The radiation-induced traps can affect the NBTI effect of pMOSFET, especially for the ON bias irradiation. The irradiated I/O pMOSFET shows a smaller threshold voltage shift than the un-irradiated device under the same NBTI stress at the early stress stage. It may be contributed to the enhanced Fowler-Nordheim electron injection during NBTI stressing after ON bias irradiation. But the irradiation also increases the time exponent n from 0.11 to 0.13 for Core pMOSFETs and from 0.18 to 0.20 for I/O devices. It means that the NBTI degradations become worse after ON bias irradiation in a long time scale. This phenomenon is attributed to the change of trap characteristics caused by irradiation. As a result, the NBTI lifetime of Core device is reduced by nearly three orders of magnitude and the lifetime of I/O device is reduced by five times after ON bias irradiation at the rated operating voltage.

INDEX TERMS MOSFET, negative bias temperature instability, silicon on insulator, total ionizing dose effect.

I. INTRODUCTION

Silicon-on-insulator (SOI) technology has become attractive for space application due to the natural advantage on single event effect hardening [1], [2]. But the SOI MOSFET still suffer from total ionizing dose (TID) effect as operating in radiation harsh environment [3]–[5]. The ionizing radiation can produce electron-hole pairs in the oxide of MOSFET. Then the electrons with higher mobility move out of the oxide layer rapidly under the applied electric field, while the holes migrate slowly to the Si/SiO_2 interface through the localized state. Finally, some of the holes are trapped by deep level traps near the interface and become positive oxide trapped charges. During the processes of hole transport and capture, the released hydrogen or H^+ will break the Si-H bones at the Si/SiO_2 interface and the interface traps are formed [4]. It is interesting to note that although the mechanisms of trap formation are different, both TID and NBTI will produce interface traps and oxide trap charges in the gate oxide of MOSFET, resulting in similar parameter degradations [6]–[8].

The mechanisms of TID effects and NBTI effects for SOI devices have been systematically studied [9]–[12]. However, the degradation mechanisms of SOI devices under the combined effect of TID and NBTI have not been well studied. It is doubt whether these two effects will interact. There are still great disputes on the formation mechanism of NBTI defects under the coupling of ionizing radiation, as well as the correlation and interaction of defects produced by these two different effects. The performance degradations of SOI MOSFETs under the dual stresses of irradiation and reliability may be different from that under single stress. This is

The associate editor coordinating the review of this manuscript and approving it for publication was Jiajie Fan.

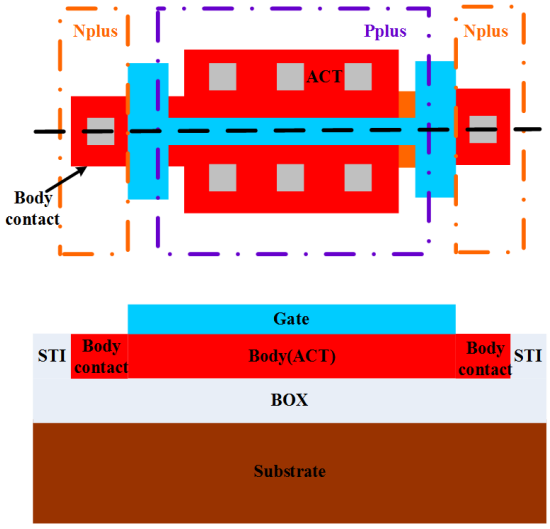

FIGURE 1. Structure of the H-gate PDSOI pMOSFETs used in our experiments.

important for the long-term service devices in space, since these devices are confronted with the double risks of radiation damage and stress aging.

In this work, the NBTI effects of Core and input/output (I/O) devices from a 130 nm partially-depleted (PD) SOI technology with and without TID irradiation are investigated. The NBTI induced degradations are compared for the devices with and without TID irradiation. Then the influences of different bias irradiations on NBTI lifetime are clarified. Finally, the energy distributions of NBTI-induced traps are extracted for the un-irradiated and irradiated devices to show the correlation of TID and NBTI-induced traps in gate oxide.

II. EXPERIMENTAL DETAILS

The Core and I/O PDSOI pMOSFETs with 100 nm top silicon film and 145 nm buried oxide are chosen as experimental samples. The structure of the pMOSFETs are shown in Fig. 1. An H-shape gate is used for body contact. The operating voltages (VDD) of Core and I/O devices are 1.2 V and 3.3 V, respectively. The width-length-ratios are 10 μm/0.13 μm for Core device and 10 μm/0.3 μm for I/O device. These two different kinds of devices also have different gate oxide processes. The gate oxide of Core device is formation in NO at 750°C to a thickness of 2 nm, while the 7 nm gate oxide of I/O device is fabricated by wet oxidation.

The irradiation experiments were conducted with ^{60}Co γ-ray at Peking University. The chosen dose rate was 50 rad(Si)/s. During radiation exposure, the pMOSFETs were under three different biases which were corresponding to the three common operating states in digital circuit, as shown in Tab. 1 [13]. All the devices were irradiated up to 500 krad(Si). Before and after irradiation, the *I-V* characteristics of the pMOSFETs were tested by Agilent B1500 semiconductor parameter analyzer. Then the irradiated devices were applied NBTI stress. In addition, the same devices without irradiation were selected and applied with the same NBTI stress for comparison.

TABLE 1. Three different bias conditions for PMOSFETs during irradiation.

Bias condition	Gate	Drain	Source	Body
ON	-VDD	0	0	0
OFF	0	-VDD	0	0
TG	0	-VDD	-VDD	0

TABLE 2. NBTI stress induced threshold voltage shift for core and I/O devices with and without irradiation.

Sample	Threshold voltage, V_{th}(V)	Threshold voltage shift, ΔV_{th}(mV)
#1	-0.367	
#1 after NBTI	-0.483	-116
#2	-0.366	
#2 after NBTI	-0.467	-101
#3	-0.679	
#3 after NBTI	-0.760	-80.6
#4	-0.697	
#4 after NBTI	-0.771	-74.2

The NBTI lifetimes were extracted using the voltage step stress (VSS) technique [14] for both the irradiated and un-irradiated devices, as illustrated in our previous works [15]. For the Core device, it was first stressed at $V_{gs} = -2.1$ V for 1000 s at room temperature, then at -2.4 V for another 1000 s. And so on until the stress voltage reached -3.9 V. For I/O device, it was stressed from $V_{gs} = -4.5$ V to $V_{gs} = -7.5$ V with a -0.5 V interval. The threshold voltage shifts were extracted by on-the-fly (OTF) method [16] at 5 s, 10 s, 16 s, 25 s, 40 s, 63 s, 100 s, 160 s, 250 s, 400 s, 630 s and 1000 s in each stress segment. The complete transfer characteristic curve was measured after the whole stress processes. Since the high temperature will enhance the annealing of the radiation induced traps in gate oxide, all the following NBTI experiments were conducted at room temperature. This is different from the typical NBTI stress condition, so the obtained effects can be also considered as negative bias instability.

III. RESULTS ANS DISCUSSIONS

A. NBTI EFFECTS COUPLED BY TID IRRADIATION IN PDSOI PMOSFET

Fig. 2 compares the transfer characteristics and transconductance characteristics of pMOSFETs with and without irradiation before and after NBTI stress. The original Core and I/O pMOSFETs without irradiation are labeled as sample #1 and #3, respectively. The Core and I/O devices after irradiation are labeled as samples #2 and #4, respectively. The NBTI stress-induced threshold voltage shifts of all the samples are extracted from the complete I_d-V_g curve and shown in Tab. 2. The threshold voltages of the pMOSFETs are defined as the gate voltage corresponding to the drain current of $|(W/L) \times 10^{-7}|$ A. It is worth to note that the threshold voltage shifts do not include the contribution of fast recovery traps, since part of the NBTI degradations are relaxed as stress voltage removing [17], [18].

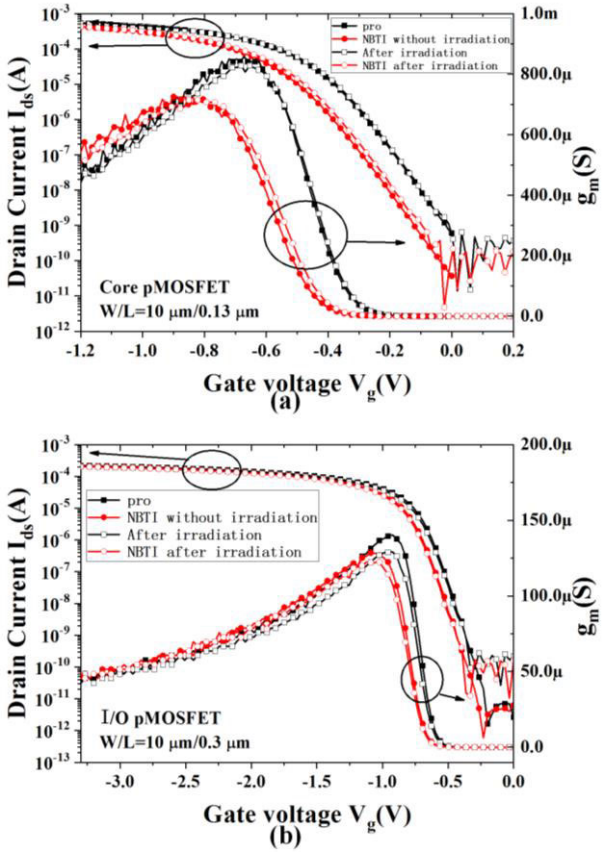

FIGURE 2. Comparisons of NBTI induced transfer and transconductance characteristics degradation for devices with and without irradiation. (a) Core pMOSFET. (b) I/O pMOSFET. Irradiation bias condition: ON bias. Test condition: $V_{drain} = -0.1$ V, $V_{source} = V_{body} = 0$ V.

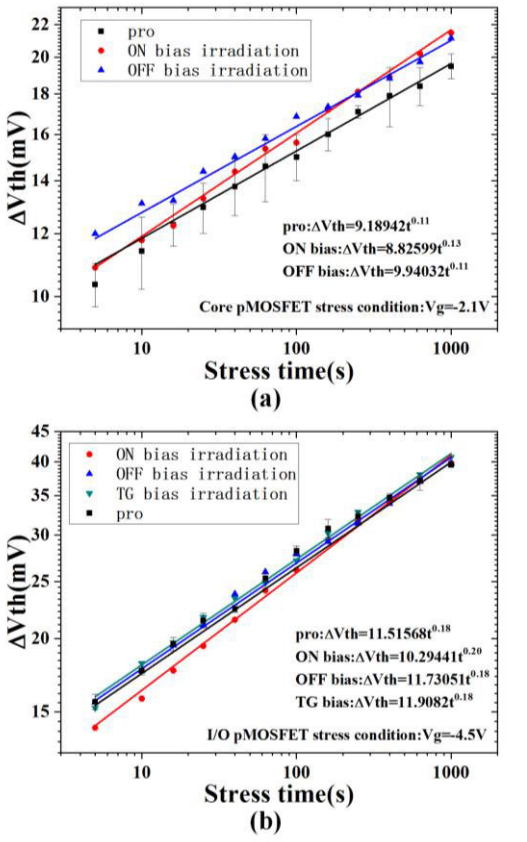

FIGURE 3. Threshold voltage shift as a function of stress time for pMOSFETs with and without irradiation during NBTI stressing. (a) Core pMOSFET. (b) I/O pMOSFET.

The radiation-induced threshold voltage shifts and transconductance degradations can be ignored for Core device, which is benefit from the thin gate oxide. While the NBTI stress induced threshold voltage shift and transconductance degradation can reach −116 mV and ∼14.7% respectively. For I/O pMOSFET, a more obvious degradation is observed after irradiation due to the relatively thick gate oxide. A −17.8 mV negative shift of threshold voltage and 8.0% g_m peak degradation are observed for I/O pMOSFET after irradiation. The radiation-induced effective trap density is extracted to be 5.49×10^{10} cm^{-2}. The NBTI stress-induced threshold voltage shifts and transconductance peak decreases are −80.6 mV and 8.4% respectively for un-irradiated I/O pMOSFET. The observed threshold voltage shift is contributed to positively charged oxide trapped charge and interface traps after irradiation and NBTI stress in pMOSFET [19]. The transconductance degradation is mainly result from the interface traps or interface-like traps, which is related to the increase of the effective Coulombic scattering [20]. It seems that TID and NBTI related degradations shows an opposite trend as gate oxide scaling, which implies the different traps are activated during TID irradiation and NBTI stress. The oxide trapped charges dominate the TID degradations. Since the radiation-induced oxide trap is proportional to the oxide thickness and the oxide trapped charge can be neutralized by the electron tunneling from polysilicon and channel in thin oxide, barely no degradation is observed after irradiation for Core device. The interface traps dominant the NBTI degradation. So even though the oxide is rather thin, a significant degradation is also observed for Core device.

The NBTI stress-induced threshold voltage shift (absolute value) for irradiated device is slightly lower than that for un-irradiated one. The NBTI-induced threshold voltage shift is −101 mV for irradiated Core pMOSFET. The observed threshold voltage shifts and transconductance degradations are −74.2 mV and 5.2% for irradiated I/O pMOSFET.

Fig. 3 shows the threshold voltage shift as a function of stress time for pMOSFETs with and without irradiation during NBTI stressing. The NBTI-induced threshold voltage shifts ΔV_{th} for the un-irradiated devices are the average value of three different samples. The threshold voltages in this figure are obtained by the OTF method to minimize the recovery and the threshold voltage shifts are absolute values. ΔV_{th} abides by a time power law with time exponents equate to 0.11 and 0.18 for Core and I/O devices without irradiation respectively. The ON bias irradiation results in the increase of time exponent to 0.13 and 0.20 for Core and I/O devices, respectively. It means the NBTI degradation

become worse after ON bias irradiation in a long time scale. But the threshold voltage shift of I/O pMOSFET with ON bias irradiation is smaller than that the device without irradiation at the early stress stage, as shown in Fig. 3. While for the devices under OFF and TG bias irradiation, the time exponent remains unchanged. The NBTI stress-induced threshold voltage shifts are only slightly increased compared with the un-irradiated device. This is consistent with the previous report that the worst-case degradations are exhibited by pMOSFET with thermal oxide irradiated and stressed in the ON condition [21].

The NBTI-induced traps have the same precursors as the TID-induced traps [22], [23]. There are neutron oxygen vacancies (i.e. Si-Si bond) close to the Si/SiO_2 interface due to the out-diffusion of oxygen in oxide and lattice mismatch, which can act as trap precursors for NBTI stress and irradiation [24]. During irradiation, the oxygen vacancies are activated as E' centers by trapping holes (or losing electron) and become positively charged. The E' center can act as switching trap, i.e. it can recapture and emit electron. During ON bias irradiation, the electron can tunnel from poly-gate to the E' centers, since the gate oxide is thin for the experimental devices. Then the E' centers activated by irradiation can become neutral dipole states as recapturing the tunneling electron which can easily lose an electron. For Core device, all the E' centers remain neutral due to the ultra-thin gate oxide, so no degradations are observed after irradiation.

According to the above discussions, the differences between irradiated and un-irradiated devices are that the Si-Si bonds become neutral E' centers. The Si-Si bond precursors usually lie about 1 eV below the silicon valence band edge, and the energy level is up inside the silicon bandgap when it becomes E' center [25]. It means that the charging/discharging barrier of E' center is lower than the barrier of Si-Si bond precursors. Then the neutral E' centers lose electron easier than the Si-Si bond precursors during the NBTI stress process and become positively charged. The positive E' center could act as a catalyst for the de-passivation of interface dangling bonds (i.e. P_b centers) by the migration of hydrogen to the newly formed dangling bonds at the positive E' center based on the two-stage model [26]. So it can be concluded that the ON bias irradiation may accelerate the activation of P_b centers in the NBTI stress process, then lead to $|\Delta V_{th}|$ increases with stress time faster. So the NBTI degradations is worse after irradiation in a long time scale. The greatest impact on subsequent NBTI testing for ON bias irradiation may be explained by the fact that more E' centers are in neutral dipole states for ON bias than the other bias conditions due to the negative gate bias.

In particular, the radiation induced E' center is more inclined to locate near the poly-gate/oxide interface for the device with ON bias irradiation. During the NBTI testing process, the high stress voltage is sufficient to induce Fowler-Nordheim (FN) carrier injection [27]. The FN electron injection from poly-gate can neutralized the NBTI stress-induced positive trapped charge. The trap centers near the poly-gate

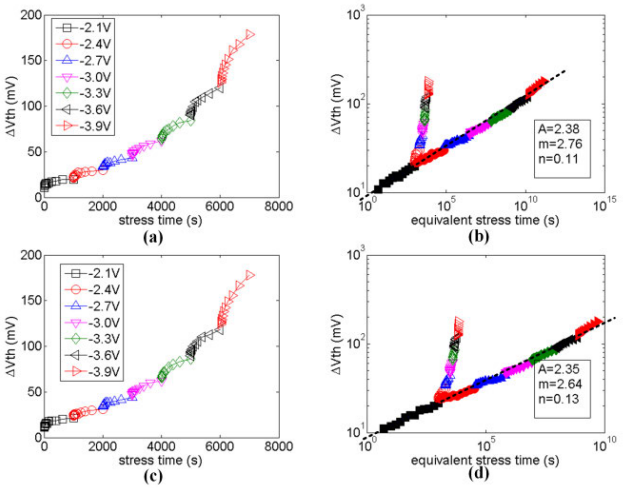

FIGURE 4. Measured threshold voltage shifts as a function of time during NBTI stress process using VSS method for Core pMOSFETs (a) without and (c) with irradiation. The extraction of power law parameters for (b) un-irradiated and (d) irradiated Core pMOSFET.

will reduce the barrier height of FN injection, this may explain the smaller $|\Delta V_{th}|$ at the early stage of NBTI stress for the ON bias irradiated I/O devices.

Fig. 4 shows the measured threshold voltage shifts as a function of time during NBTI stress process by using VSS method for Core pMOSFETs without and with irradiation. In the first stress segment, the NBTI stress-induced threshold voltages follow a power law and can be expressed as [28]:

$$|\Delta V_{th}| = A \cdot V_{gt}^{m} \cdot t^{n} \tag{1}$$

where A is a fitting constant, $V_{gt} = V_g\text{-}V_{th}$ is the overdrive gate voltage during NBTI stress, m is the stress voltage exponent, and n is the time exponent. Then the time exponent n can be extracted by the power fitting of measured threshold voltage shifts, as shown in Fig. 3. In the following stress segments, ΔV_{th} increases more rapidly due to the higher stress voltage. The basic principle of VSS method is assumed that NBTI-induced ΔV_{th} under gradually increasing stress voltages in a shorter time can be equivalent to ΔV_{th} under a single lower stress voltage in a longer effective time with a constant time exponent, i.e.

$$t_{eff} = \left(\frac{V_{high}}{V_{low}}\right)^{m/n} \cdot t \tag{2}$$

Based on (2), the effective stress time corresponding to a higher stress voltage is a function of parameter m. Only by choosing the correct m, the ΔV_{th} under the gradually increasing stress voltages versus effective stress time will follow the same power law as the first stress segment. Then voltage exponent parameter m is determined. Fig. 4 (b) and (d) shows the extracted parameter values for un-irradiated and irradiated Core pMOSFETs, respectively. Similarly, the extracted parameter values for I/O pMOSFETs are: $A = 0.26$ and $m = 2.88$ for un-irradiated device; $A = 0.26$ and $m = 2.74$ for irradiated one. Then NBTI lifetime as a function of operating voltages can be calculated by setting the failure criterion as

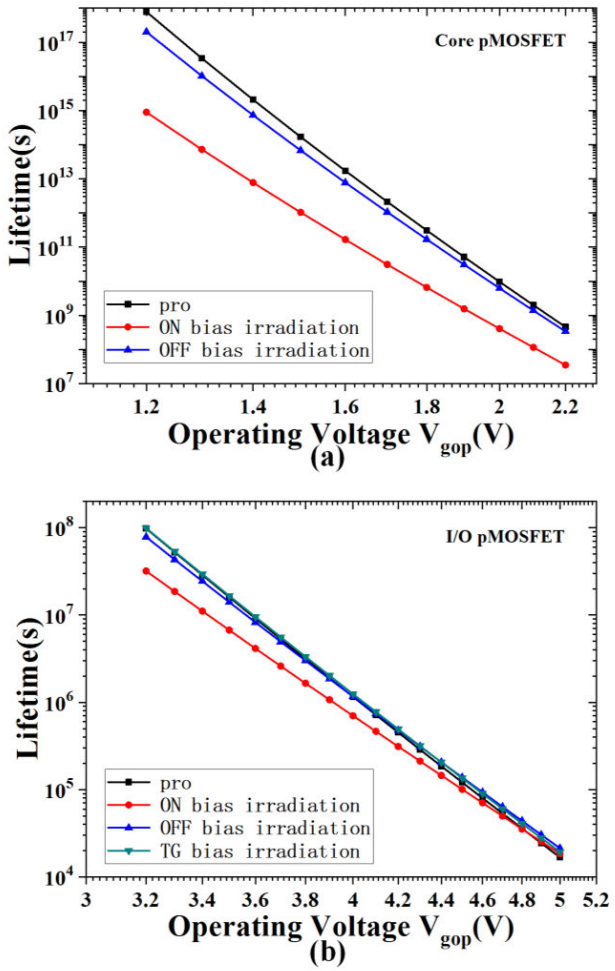

FIGURE 5. Influence of TID irradiation on NBTI life time for (a) Core and (b) I/O pMOSFETs.

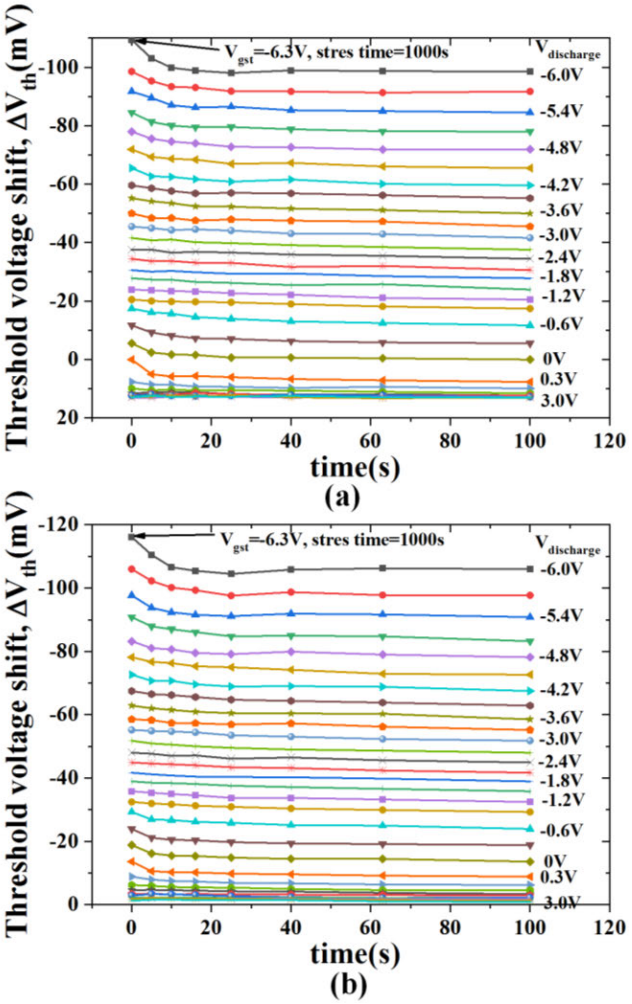

FIGURE 6. Discharging processes under the gradually increase gate voltage for I/O pMOSFETs (a) without and (b) with irradiation. The device was firstly stressed at $V_{gst} = -6.3$ V for 1000 s. Then the discharging is monitor against time.

$|\Delta V_{th}| = 100$ mV for devices with and without irradiation, as shown in Fig. 5. It can be seen that the OFF and TG bias irradiation only slightly affect the NBTI lifetime. While the NBTI lifetime of the pMOSFET after ON bias irradiation is obviously lower than the device without irradiation. The NBTI lifetime is nearly three orders of magnitude lower for the Core device and is five times lower for the I/O device after ON bias irradiation at the rated operating voltage.

B. INFLUENCE OF TID IRRADIATION ON THE NBTI TRAP CHARACTERISTICS IN GATE OXIDE

Fig. 6 shows the discharging process of the NBTI stress-induced recoverable defects for un-irradiated and irradiated I/O pMOSFETs. The devices are firstly stressed at $V_{gst} = -6.3$ V under room temperature for 1000 s. Then the gate voltage $V_{discharge}$ gradually changes from -6 V to 3V at a constant interval $\Delta V_g = 0.3$ V. OTF method is used to evaluate the ΔV_{th} at the stress phase and each discharging phase. ΔV_{th} reaches -116.1 mV and -109.4 mV for irradiated and un-irradiated device respectively after the -6.3 V stress phase. As $|V_g|$ lowers down to $V_{discharge} = -6$ V, $|\Delta V_{th}|$ starts to decrease due to the discharging of the recoverable traps. As discharging time increases, ΔV_{th} gradually becomes stable, and a flat region is reached after 25 s, indicating all the recoverable traps have been discharged. After discharging for 100 s, $V_{discharge}$ keeps dropping and the similar $\Delta V_{th} \sim$ discharging time curve is observed.

By plotting the ΔV_{th} value in the end of the discharging time against the corresponding gate voltage $V_{discharge}$, ΔV_{th} profile against V_g can be obtained, as shown in Fig. 7 (a). The test results of the irradiated and un-irradiated I/O pMOSFET are obtained respectively. It is worth to note that all the traps are recoverable for the un-irradiated device, but not for the irradiated device. All the NBTI stress-induced traps are recovered after discharging at $V_{discharge} = 0$ V, while ΔV_{th} remains -13.6 mV after the same discharging processes. It implies the trap characteristics have been changed by the irradiation.

The detailed energy distributions of the positive charges built up during NBT stress for the irradiated and un-irradiated

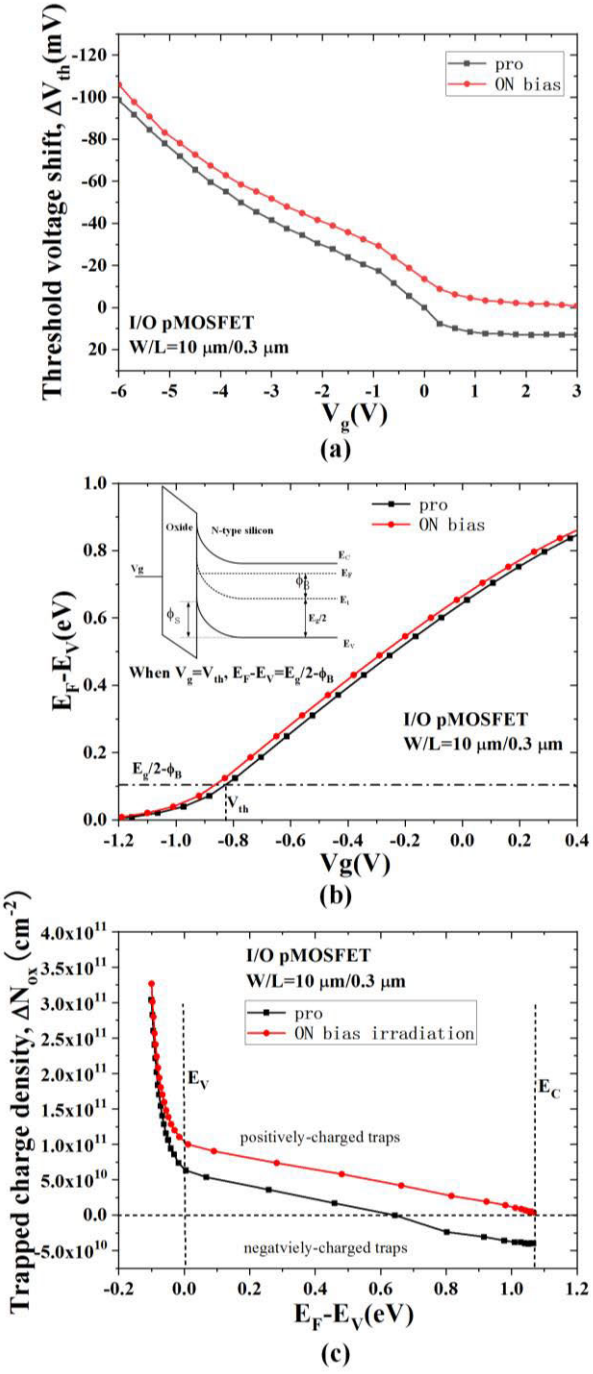

FIGURE 7. (a) Threshold voltage shift ΔV_{th} as a function of $V_{discharge}$ at discharge time=100 s. (b) Fermi energy level position as a function of V_g at the gate oxide/silicon interface for I/O pMOSFETs before and after ON bias irradiation. (c) Energy distribution of the built-up traps during NBTI stress for the I/O pMOSFETs.

I/O pMOSFETs can be obtained from Fig. 7 (a) using the method in [29]. Firstly, $\Delta V_{th} \sim V_g$ curve needs to be converted to trap density against energy level E_F-E_V. The effective trap density induced by NBTI stress in the gate oxide ΔN_{ox} can be calculated from ΔV_{th},

$$\Delta N_{ox} = \frac{-\Delta V_{th}\varepsilon_{ox}}{qt_{ox}} \tag{3}$$

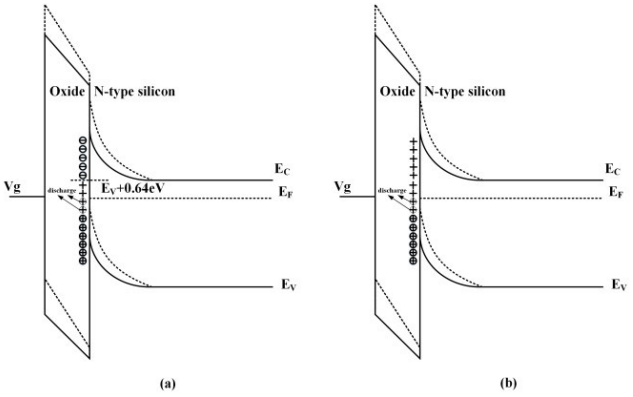

FIGURE 8. Energy band diagram of the traps distribution for (a) un-irradiated and (b) irradiated I/O pMOSFETs. The dash lines of energy band represent the situation with a high gate voltage (absolute value).

The position of Fermi energy level relative to valence band, i.e. E_F-E_V, at the gate oxide/silicon interface can be calculated as a function of V_g for I/O pMOSFET without stress by the Silvaco TCAD simulations [30]. It accounts for the real body doping and gate oxide thickness during simulations. The process parameters are obtained from foundry. Since the threshold voltages become different for irradiated and un-irradiated devices after −6.3 V NBTI stress, which will lead to different $(E_F$-$E_V) \sim V_g$ relation. Then $(E_F$-$E_V) \sim V_g$ curve from TCAD simulation should be adjusted properly to fit the threshold voltage of irradiated and un-irradiated devices after NBT stress (as shown in Fig. 7 (b)) using

$$E_F - E_V = \frac{E_g}{2} - \phi_B, \quad when\ V_g = V_{th} \tag{4}$$

where E_g is the bandgap of silicon, ϕ_B is the different between mid-bandgap energy level and Fermi energy level in the body and $E_g/2 - \phi_B = 0.104$ for our device. By converting ΔV_{th} to effective trap density ΔN_{ox} and converting V_g to Fermi energy level position E_F-E_V at the gate oxide/silicon interface, the accumulated trap density distribution is obtained and shown in Fig. 7 (c).

Fig. 8 (a) shows energy band diagram of the traps distribution after NBTI stress for un-irradiated I/O pMOSFET. The NBTI stress leads to net donor-like traps distributing below $E_V + 0.64$ eV and net acceptor-like traps above $E_V + 0.64$ eV. Assuming all the traps above E_F are empty and below E_F are filled by electron. At a higher gate bias (absolute value), as E_F-E_V < 0.64 eV, both the donor-like traps below E_F and acceptor-like traps above $E_V + 0.64$ eV are electrically neutral. While the donor-like traps between $E_F \sim E_V + 0.64$ loss electrons (i.e. trap holes) and become positively charged. These traps lead to the negative shift of the threshold voltage. When the gate bias become smaller, the energy band near the interface moving down, some of the positively-charged traps move below E_F. They are filled by the electron again and become electrically neutral, which results in the recovery of the threshold voltage. With the further decrease of gate voltage, as E_F-E_V > 0.64 eV, all the donor-like traps become

neutral and the acceptor-like traps between $E_V + 0.64$ eV $\sim E_F$ are negatively charged. This can explain the positive shift of threshold voltage observed in Fig. 7 (a) at $V_{discharge} = 0.3$ V. For the irradiated I/O pMOSFET, there are only net donor-like traps but no acceptor-like traps distributing at the whole bandgap region after NBTI stress. So no positive shift of threshold voltage is observed during the recovery process. The traps above E_F can become positively charged and result in the negative shift of the threshold voltage after NBTI stress. The density of the donor-like traps is higher in irradiated device than the un-irradiated one, which corresponding to more serious NBTI degradations. This is consistent with the NBTI stress test results in Section A.

IV. CONCLUSION

The NBTI effects of 130 nm PDSOI pMOSFETs with and without irradiation are studied. The radiation-induced degradations are not obvious due to the thin gate oxide, but it can significantly affect the NBTI effect of the pMOSFETs. The NBTI stress-induced threshold voltage shifts follows a power law with stress time for both the un-irradiated and irradiated devices. While the time exponents increase from 0.11 and 0.18 to 0.13 and 0.20 for Core and I/O device respectively after ON bias irradiation. It means that the ON bias irradiation will enhance the NBTI degradations in a long time scale, which is finally manifested as the decrease of NBTI lifetime for Core and I/O pMOSFETs after irradiation. It is worth to note that the NBTI stress-induced threshold voltage shift in I/O pMOSFET with irradiation is smaller than that in device without irradiation at the early stress stage. It may be explained by the enhanced Fowler-Nordheim carrier injection from poly-gate due to the traps buildup near poly-gate/oxide interface after ON bias irradiation.

The energy distributions of traps induced by NBTI stress are also extracted. There are both donor-like and acceptor-like traps located in the bandgap for the un-irradiated device. But there are only donor-like traps distributing at the whole bandgap region. It implies that the trap types and states have been altered by the irradiation. The density of the donor-like traps is higher in irradiated device than the un-irradiated one, which is corresponding to more serious NBTI degradations. It is a great challenge to ensure that SOI devices still have high NBTI reliability after TID irradiation.

ACKNOWLEDGMENT

The authors are indebted to the Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences for providing the experimental samples.

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