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Switching Time Delay Optimization for "SiC+Si" Hybrid Device in a Phase-Leg Configuration

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ABSTRACT Compared to SiC MOSFET, the switching loss of Si IGBT is much higher due to its slow switching speed and tail current. Si IGBT/SiC MOSFET hybrid switch device can reach to optimal performance with low static and dynamic loss, which can improve the current capacity of SiC devices and reduce the power loss of Si IGBT based converters. With the separated gate control signals, the switching moments of the two devices can be controlled independently to ensure Si IGBT under zero-voltage switching (ZVS) conditions. This measurement tends to reduce the switching loss of Si IGBT. However, the switching time delay between these two devices has significant impacts on its power loss. In this paper, the switching time delay optimization method is proposed to minimize the power loss of the hybrid switch. The static and dynamic characteristics of Si IGBT/SiC MOSFET hybrid-paralleled switch are studied, and a generalized power loss model for hybrid switch is developed. The influence of switching time delay on the characteristics of hybrid switch is analyzed and verified through double pulse tests in a phase-leg configuration. The experimental results show that the optimal turn-on delay time is that the two devices turn on at the same time and the turn-on loss can be reduced by about 73% compared with the solely Si IGBT and by about 52% compared with the solely SiC MOSFET. While the optimal turn-off sequence is that the Si IGBT turns off ahead of the SiC MOSFET. Under the proposed optimal turn-off delay time of the hybrid switch, the turn-off loss is reduced by about 61.4%. This optimization strategy is used in a Buck converter to verify the superiority of the SiC/Si hybrid switch and the optimal switching sequence. Simulation results show that the optimal switching sequence is consistent with theoretical analysis, and the efficiency is improved by 2.5% compared with Buck converter using solely Si IGBT.

INDEX TERMS Si IGBT/SiC MOSFET, hybrid switch, power loss model, switching time delay, double pulse tests.

I. NOMENCLATURE

a	The current ratio flowing through Si IGBT and SiC MOSFET.
E_{c_MOS}	Conduction loss of SiC MOSFET.
E_{c_IGBT}	Conduction loss of Si IGBT.
E_{on}	Turn-on loss of the hybrid switch.
$E_{hard\_on\_MOS}$	Hard-switching-on loss of the SiC MOSFET.
$E_{hard\_on\_IGBT}$	Hard-switching-on loss of the Si IGBT.
$\Delta E_{con\_MOS\_on}$	Additional conduction loss of SiC MOSFET in T_{on_delay}.
$\Delta E_{con\_IGBT\_on}$	Additional conduction loss of Si IGBT in T_{on_delay}.
$E_{s\_on\_MOS}$	Turn-on loss of the SiC MOSFET in T_{on_delay} when $T_{on\_delay} \geq 0$ and $T_{on\_delay} \leq T_{on\_MOS}$.
$E_{s\_on\_Hybrid}$	Turn-on loss of the hybrid switch after T_{on_delay} when T_{on_delay} is shorter than the turn-on time of Si IGBT or SiC MOSFET.
$E_{s\_on\_IGBT}$	Turn-on loss of the Si IGBT in T_{on_delay} when $T_{on\_delay}<0$ and $\lvert T_{on\_delay}\rvert \leq T_{on\_IGBT}$.

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$E_{\text{hard\_off\_MOS}}$	Hard-turn-off loss of the SiC MOSFET.
$\Delta E_{\text{con\_MOS\_off}}$	Additional conduction loss of SiC MOSFET in $T_{\text{off\_delay}}$.
$E_{\text{hard\_off\_IGBT}}$	Hard-switching-off loss of the Si IGBT.
$E_{\text{off\_IGBT1}}$	The zero-state response of turn-off loss caused by undertake the blocking voltage.
$E_{\text{res\_off}}$	The inherent loss of IGBT when turned off.
$E_{\text{off\_IGBT2}}$	The zero-input response of turn-off loss caused by removing inherent plasma.
E_{off}	Turn-off loss of the hybrid switch.
$E_{\text{off\_delay}}$	Turn-off loss of the hybrid switch considering the additional conduction loss.
i_{C}	Forward current flowing through Si IGBT.
i_{D}	Forward current flowing through SiC MOSFET.
i_{L}	Forward current flowing through hybrid switch.
I_{O}	Load current when hybrid switch working at static state.
I_{b}	The critical forward current when Si IGBT begins to conduct current.
I_{L0}	The load current when it is distributed evenly in the two devices of the hybrid switch.
k	The curve slope ratio of Si IGBT and SiC MOSFET.
$R_{\text{CE(on)}}$	On-resistance of Si IGBT.
$R_{\text{DS(on)}}$	On-resistance of SiC MOSFET.
T_{on}	Total turn-on time of the hybrid switch.
T_{con}	Conduction time of hybrid switch.
$T_{\text{on\_MOS}}$	Turn-on switching time of SiC MOSFET.
$T_{\text{on\_IGBT}}$	Turn-on switching time of Si IGBT.
$T_{\text{off\_MOS}}$	Turn-off switching time of SiC MOSFET.
$T_{\text{off\_IGBT}}$	Turn-off switching time of Si IGBT.
$T_{\text{on\_delay}}$	Turn-on delay time.
$T_{\text{off\_delay}}$	Turn-off delay time.
τ_0	The lifetime of the IGBT.
τ	The exponential time constant for the dependency of the IGBT's turn-off loss.
v_{CE}	Forward voltage of Si IGBT.
v_{DS}	Forward voltage of SiC MOSFET.
v_{GS}	Gate-source voltage of SiC MOSFET.
v_{GE}	Gate-emitter voltage of Si IGBT.
V_{F}	Forward voltage of hybrid switch.
V_{T0}	Inherent turn-on voltage drop of Si IGBT.

II. INTRODUCTION

In the past few decades, silicon (Si) IGBT has been widely used in high-power applications for its low forward voltage drop and high current capability. However, due to the inherent limitations of Si material, such as narrow band gap, low thermal conductivity and low critical breakdown electric field, it is challenging for Si-based power devices to meet the requirements of next-generation power electronic applications. Recently, SiC power devices have attracted attentions due to its superior properties [1], [2]. For example, SiC MOSFET is increasingly adopted for its reduced switching loss, and the power density and efficiency of the converter can be further improved.

However, due to the low short-circuit withstand capability [3], high cost of the material and its fabrication [4], the applications of SiC power devices are limited, and the current rating of SiC MOSFET is still not competitive compared with Si IGBT. Therefore, a Si IGBT/SiC MOSFET hybrid switch concept was proposed to make fully use of Si IGBT benefits in conduction characteristics and SiC MOSFET benefits in switching characteristics [5]–[8]. The gate control signals of SiC MOSFET and Si IGBT are controlled separately so that the SiC MOSFET is responsible for facilitating hard switching process of the hybrid switch and the Si IGBT is zero-voltage switched. This measurement helps to reduce switching loss, especially the turn-off switching loss caused by turn-off current tail of the IGBT [9].

In recent years, some studies on Si IGBT and SiC MOSFET hybrid paralleled switch has been done and was reported to achieve optimized efficiency [10]–[18]. [10]–[12] compared the performance and cost of hybrid switches composed of SiC MOSFET and Si IGBT with different current ratings. The comparison shows that hybrid switches with equivalent rated current are more costly than single Si IGBT solution. Therefore, a cost-effective solution was proposed by using high-current Si IGBT as main switch and low-current SiC MOSFET as auxiliary switch. In [13], [14], the 6.5 kV Si IGBT and SiC MOSFET hybrid switch for high voltage applications and the hybrid switch was proved to be efficient in efficiency improvement. The results show that, the total loss of high-voltage hybrid devices is reduced by about 35% compared with single-device solutions. In [15]–[18], the current distribution between the Si IGBT and SiC MOSFET inside the hybrid switch was studied. It is shown that the hybrid parallel switch has lower switching loss and oscillation compared with all-Si IGBT and all-SiC MOSFET switches.

In an ideal condition, SiC MOSFET firstly turns on and turns off later, which can realize ZVS of the IGBT, and the switching energy of the IGBT is ignored. As a matter of fact, the switching-off characteristic of the IGBT is special [19] and this makes the actual switching characteristics of the hybrid switch more complicated. When SiC MOSFET is turned off, there is a current spike in IGBT which may lead to additional power loss. Setting a turn-off delay time can decrease the power loss in IGBT but will introduce more power loss in SiC MOSFET. The turn-on and turn-off delay time significantly affects the switching performance and efficiency of the hybrid switch. Therefore, the switching delay time needs to be optimized to minimize the total turn-off losses in the hybrid switch since the turn-on switching loss of the SiC MOSFET within time $T_{\text{off\_delay}}$ might be larger than the reduced turn-off loss of the Si IGBT. Some studies on the switching time delay have already been done these years. [20], [21] have conducted a certain degree of research on the switching timing of hybrid parallel switches, and a gate

drive signal dynamic adjustment strategy for the inverter was proposed. [22]–[24] studied the relationship between switching delay time and switching power loss but the selection of an appropriate delay time is not mentioned. [25]–[27] conducted research on the characteristics of Si/SiC hybrid devices. Starting from the performance of the hybrid device converter, the influence of the hybrid device gate drive control strategy on the characteristics of the hybrid device is analyzed. However, the previous study on the characteristics and power loss of the hybrid device is quite simple. The principle of switching-delay-time selection for ''SiC+Si'' hybrid device is still insufficient, either.

To bridge such a research gap, this paper presents two original contributions that distinguish our work from existing literature. First, a generic power loss calculation model is established according to the conduction characteristics of the hybrid switch. Second, the relationship between the power loss of the hybrid switch and the switching time delay is revealed and an optimized switching time delay method is proposed. The phase-leg configuration is one of the most commonly used power circuit structure in power electronic converters. The structures include single-phase half-bridge, full-bridge, three-phase and multi-phase bridge circuits, covering various types of converters. For simplicity, we studied the phase-leg configuration and conducted some experiments to give more guidance on real applications, such as electric vehicle application.

The following sections of this paper are organized as follows. Section II summarizes the output characteristics of SiC MOSFET, Si IGBT and the SiC/Si hybrid switch. In Section III, the power loss model of the hybrid switch device is developed, and influence of the switching delay time on the power loss of the hybrid switch device is analyzed. In Section IV, the optimal switching delay time of the hybrid switch device is verified through the double pulse test experiments. In Section V, simulations are carried out on a Buck converter to verify the superiority of the SiC/Si hybrid switch with the optimal switching sequence, and finally conclusions are drawn in Section VI.

III. CONDUCTION CHARACTERISTICS OF "SIC+SI" HYBRID DEVICES

The hybrid switch proposed in this paper is composed of a Si IGBT with a high current rating and a SiC MOSFET with a low current rating and Fig.1 shows the configuration of the hybrid switch. The number of SiC MOSFET and Si IGBT are depended on the load current.

In [11], the hybrid switch can work safely and reliably under most operating conditions when the SiC/Si current ratio is as low as 1:5. The smaller this ratio is, the less safely the hybrid device works. By contrast, the lager ratio results in the higher cost of the hybrid switch. Therefore, a compromise is made between the reliability and the capital cost. In the following study, C2M0160120D (SiC MOSFET, CREE) and IKW25N120T2 (Si IGBT, Infineon) are used for hybrid-parallel connection. The SiC/Si current ratio is 1:2.27,

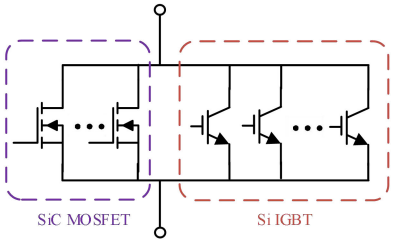

FIGURE 1. "SiC+Si" hybrid switch configuration.

which is acceptable according to previous study, showing an excellent cost performance. Table 1 shows the related parameters and the test conditions of the conduction characteristics.

TABLE 1. Parameters of SIC devices and SI IGBT evaluated.

Device	SiC MOSFET	Si IGBT
Part No.	C2M0160120D	IKW25N120T2
Voltage Rating/V	1200	1200
Current Rating (25°C)/A	18	50
$R_{DS(on)}$(25°C)/mΩ	160	-
$V_{CE(SAT)}$(25°C)/V	-	1.7

The conduction characteristics are tested at room temperature of 25 °C and the testing conditions are listed in Table 2. The experimental set up are all the same in this study. Fig. 2 compares the output characteristic curves of the Si IGBT, SiC MOSFET and hybrid switch of these two devices. Under light load conditions, due to the inherent turn-on voltage drop V_{T0} in Si IGBT, the turn-on switching loss is larger than SiC MOSFET. Under heavy load conditions, Si IGBT has lower conduction power losses compared with SiC MOSFET. The output characteristics of the hybrid switch is the combination of the Si IGBT and SiC MOSFET. As shown in Fig. 2, at small load current, the output characteristic of the hybrid switch is close to that of the SiC MOSFET and the conduction loss of the hybrid switch is smaller compared with using Si IGBT alone; while at large load current, the output characteristic curve of the hybrid switch is close to that of the Si IGBT and the conduction loss of the hybrid switch is smaller compared with using SiC MOSFET alone. Therefore, the conduction loss of the hybrid switch is significantly reduced under light load and heavy load conditions.

TABLE 2. Testing conditions of the conduction characteristics.

Device	SiC MOSFET	Si IGBT
Ambient temperature/°C	25	25
External Gate Resister/Ω	5	5
Drive Voltage/V	20/–4	15/–8.7

Fig. 3 illustrates the current distribution between Si IGBT and SiC MOSFET. When load current $i_L < 5$ A, the load current only flows through the SiC MOSFET; When 5 A$< i_L <$ 18 A, part of the load current starts to flow

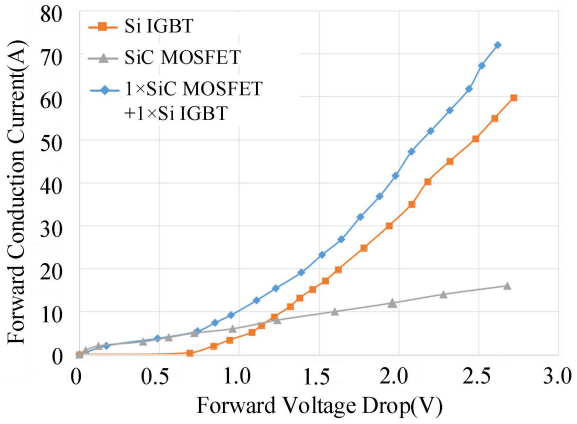

FIGURE 2. Output characteristic of Si IGBT, SiC MOSFET and hybrid switch.

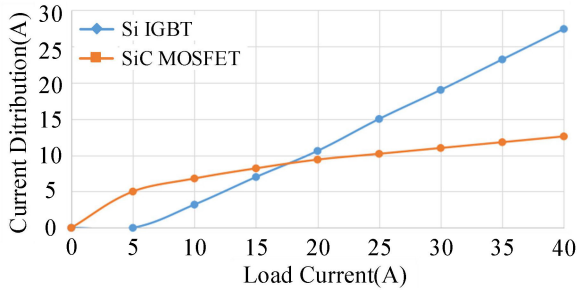

FIGURE 3. Current distribution of hybrid device.

through the Si IGBT, and it increases faster than that of the SiC MOSFET; When $i_L = 18$ A, the current flowing through the IGBT and SiC MOSFET is distributed evenly; When $i_L > 18$ A, the current flowing through the IGBT starts to be more than the current flowing through the SiC MOSFET. With the increase of load current, current flowing through SiC MOSFET and current flowing through Si IGBT increase almost linearly. The curve slope ratio of Si IGBT and SiC MOSFET is defined as k, one can get $k = 6.5$ according to the on-resistance of Si IGBT and SiC MOSFET. The current distribution of the hybrid switch depends on these two devices and the load current. With the increase of load current and k, Si IGBT undertakes more load current.

IV. POWER LOSS MODEL OF HYBRID DEVICES

To improve the efficiency of the phase-leg converters, the characteristics of Si/SiC hybrid switch is studied, and the power loss model of Si/SiC hybrid switch is established. To make calculation more accurate, the time period should be defined more precisely. According to different switching sequences, SiC MOSFET can be turned on and off with the sequence of leading or lagging behind Si IGBT. As shown in Fig. 4, we can get four gate control patterns for hybrid paralleled devices. The conduction time T_{con} and switching time T_{on} and T_{off} are marked in Fig. 4. G1 is the gate drive signal of the SiC MOSFET, and G2 is the gate drive signal

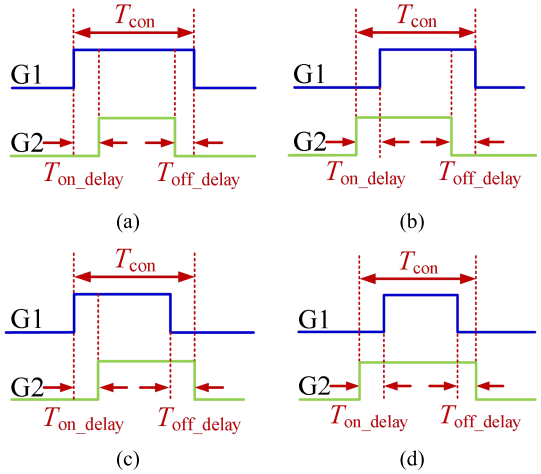

FIGURE 4. Different gate control patterns of hybrid switch. (a) Pattern I. (b) Pattern II. (c) Pattern III. (d) Pattern IV.

of the Si IGBT. Conduction time T_{con} and switching delay times T_{on_delay} and T_{off_delay} are labeled in Fig. 4. T_{on_delay} and T_{off_delay} are included in T_{con} since the hybrid switch is conducting during this period. The additional conduction loss in switching delay time will be discussed when we analyse the switching characteristics later.

A. CONDUCTION LOSS MODEL

A conduction model of the paralleled hybrid device under the steady state is shown in Fig. 5. The internal parasitic capacitance and inductance are ignored for simplicity. The forward voltage v_{DS} is the same as v_{CE}. The current distribution varies according to the output characteristics of the paralleled devices. The Si IGBT is equivalent to the series connection of on-resistance $R_{CE(on)}$ and a constant voltage source V_{T0}, while the SiC MOSFET can be simplified to an on-resistance $R_{DS(on)}$. Therefore, the current sharing of the paralleled devices depends on their on-resistances and on-threshold voltage levels of the Si IGBT and SiC MOSFET.

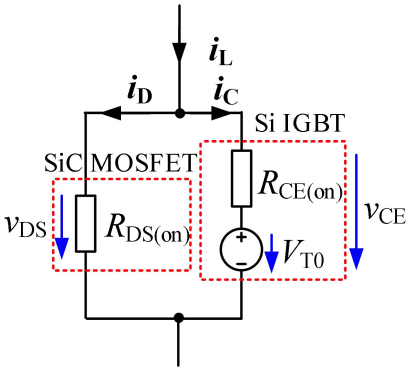

FIGURE 5. Steady-state model of hybrid parallel devices.

As shown in Fig. 5, the steady-state current flowing through the Si IGBT and SiC MOSFET can be expressed as:

$$i_C = \frac{i_L \cdot R_{DS(on)} - V_{T0}}{R_{DS(on)} + R_{CE(on)}} \quad (1)$$

$$i_D = \frac{i_L \cdot R_{CE(on)} + V_{T0}}{R_{DS(on)} + R_{CE(on)}} \quad (2)$$

Due to the turn-on threshold voltage of IGBT, there will be no current flowing through Si IGBT if i_L is too small, for the forward voltage is less than V_{T0}. Therefore, the current flowing through the SiC MOSFET and/or Si IGBT depends on the load current levels. The critical forward current I_b can be described as:

$$I_b = \frac{V_{T0}}{R_{DS(on)}} \quad (3)$$

If the overall forward current of the hybrid current is smaller than I_b, the forward voltage drop of the hybrid switch is lower than V_{T0}, the load current i_L will flow through the SiC MOSFET only. If the overall forward current is larger than I_b, both devices will undertake the forward current. When current flows in both Si IGBT and SiC MOSFET, the ratio of the current flowing in Si IGBT and SiC MOSFET can be defined as:

$$a = \frac{i_C}{i_D} = \frac{i_L \cdot R_{DS(on)} - V_{T0}}{i_L \cdot R_{CE(on)} + V_{T0}} \quad (4)$$

When the forward current is evenly distributed in Si IGBT and SiC MOSFET, we can get $a = 1$. If $a < 1$, SiC MOSFET undertakes most forward current; If $a > 1$, Si IGBT undertakes most forward current. I_{L0} is the load current when it is distributed evenly in the two devices of the hybrid switch and it can be derived as (5).

$$I_{L0} = \frac{2V_{T0}}{R_{DS(on)} + R_{CE(on)}} \quad (5)$$

One can get $I_{L0} = 18$ A in Fig. 2.

In one switching period, the conduction energies of Si IGBT and SiC MOSFET can be expressed as:

$$E_{c\_MOS} = \begin{cases} I_O^2 \cdot R_{DS(on)} \cdot T_{con}, & I_O \le I_b \\ \frac{I_O^2}{(1+a)^2} \cdot R_{DS(on)} \cdot T_{con}, & I_O > I_b \end{cases} \quad (6)$$

$$E_{c\_IGBT} = \begin{cases} 0, & I_O \le I_b \\ \left(\frac{a^2 I_O^2}{(1+a)^2} \cdot R_{CE(on)} + \frac{a I_O}{(1+a)} \cdot V_{T0} \right) \cdot T_{con}, & I_O > I_b \end{cases} \quad (7)$$

B. SWITCHING LOSS MODEL

As shown in Fig.4, in pattern I, the SiC MOSFET turns on before and turns off after the Si IGBT. During the switching delay time, the SiC MOSFET undertakes all forward current for a short time, and the IGBT achieves ZVS turn-on. In pattern II, the SiC MOSFET turns on and off after the Si IGBT. The SiC MOSFET is ZVS turn-on and IGBT is ZVS turn-off. In pattern III and IV, IGBT is turned off later than the SiC MOSFET. Si IGBT undertakes all forward current which leads to more conduction loss in these patterns. Moreover, the hard turn-off of Si IGBT leads to more switching loss. Therefore, turning off Si IGBT later than SiC MOSFET is no use decreasing power loss. In this study, pattern III and IV are not considered due to large hard-switching-off loss of IGBT.

1) TURN-ON LOSS

The switching characteristics of the hybrid switch under different turn-on time delay levels are different. The delay time of the turn-on gate signals between the SiC MOSFET and the Si IGBT is defined as T_{on_delay}. When T_{on_delay} is greater than zero, the SiC MOSFET is turned on ahead of the Si IGBT. When T_{on_delay} is less than zero, it means that the SiC MOSFET is turned on lagging behind the Si IGBT. Similarly, the hard-switching-on time of SiC MOSFET is defined as T_{on_MOS} and the hard-switching-on time of Si IGBT is T_{on_IGBT}. The following four cases are analyzed.

① $T_{on\_delay} \ge 0$ and $T_{on\_delay} > T_{on\_MOS}$

The turn-on process of hybrid switch when $T_{on\_delay} > T_{on\_MOS}$ is shown in Fig. 6. When the Si IGBT is ZVS turn-on and its turn-on loss is almost zero. The turn-on loss of the hybrid switch is all provided by the SiC MOSFET, which is equal to the hard-switching-on loss of the SiC MOSFET.

$$E_{on} = E_{hard\_on\_MOS} = \int_0^{T_{on\_MOS}} i_D(t) \cdot v_{DS}(t) dt \quad (8)$$

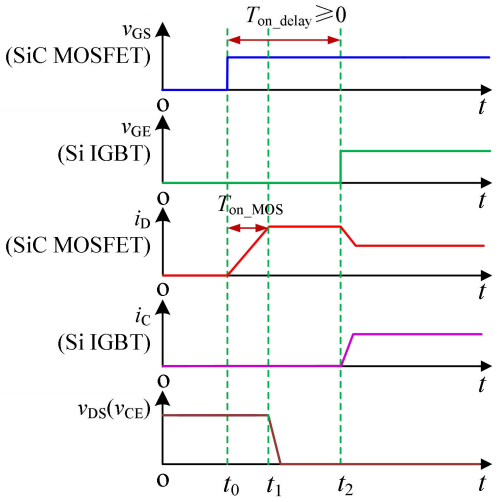

FIGURE 6. Turn-on process when $T_{on\_delay} > T_{on\_MOS}$.

When the SiC MOSFET is fully turned on, the Si IGBT is still off and all load current flows through the SiC MOSFET during time interval T_{on_delay}. As analyzed in Section II, the hybrid switch produces some conduction loss. It is more than the conduction loss when both devices participate in the switching-on transient. The additional conduction loss is defined as $\Delta E_{con\_MOS\_on}$ which is the integration value of the conduction loss between only SiC MOSFET and the hybrid

switch during T_{on_delay}. It can be expressed as:

$$\Delta E_{con\_MOS\_on} = \int_{T_{on\_MOS}}^{T_{on\_delay}} I_O \cdot (V_{DS} - V_F)dt = I_O \cdot (V_{DS} - V_F) \cdot (T_{on\_delay} - T_{on\_MOS}) \quad (9)$$

where V_{DS} is the voltage drop of the SiC MOSFET during the turn-off delay time, and V_F is the voltage drop of the hybrid parallel switch when SiC MOSFET and Si IGBT are both turned on, and I_O is the load current. We can see that the additional conduction loss increases with the increase of the turn-on time delay.

② $T_{on\_delay} \geq 0$ and $T_{on\_delay} \leq T_{on\_MOS}$

The turn-on process of hybrid switch is shown in Fig. 7. When the Si IGBT is turned on, the current flowing in the SiC MOSFET has not risen to the load current I_O. Therefore, the Si IGBT has to undertake part of the load current and generate turn-on loss during its turn-on period. At this time, the Si IGBT cannot achieve ZVS turn-on. The turn-on loss of the hybrid switch consists of two parts: the turn-on loss caused by SiC MOSFET during T_{on_delay}, and the turn-on loss caused by both SiC MOSFET and Si IGBT after T_{on_delay} and before the hybrid switch is fully turned on. The turn-on loss expression of the hybrid switch under this condition can be described as:

$$E_{on} = E_{s\_on\_MOS} + E_{s\_on\_Hybrid} = \int_0^{T_{on\_delay}} i_D(t) \cdot v_{DS}dt + \int_{T_{on\_delay}}^{T_{on}} (i_D(t) + i_C(t)) \cdot v_F dt \quad (10)$$

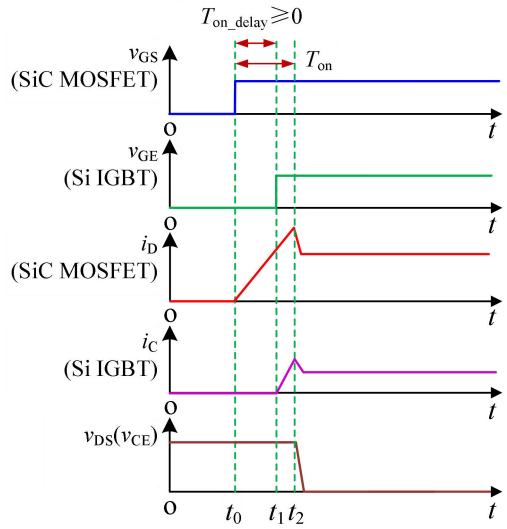

FIGURE 7. Turn-on process when $T_{on\_delay} \leq T_{on\_MOS}$.

where T_{on} is the time period from SiC MOSFET begins to turn on to the hybrid switch is completely turned on, v_F is the voltage drop of the hybrid switch. Under this condition, the turn-on loss of the hybrid switch only includes the respective turn-on losses of SiC MOSFET and Si IGBT.

③ $T_{on\_delay} < 0$ and $|T_{on\_delay}| \leq T_{on\_IGBT}$

This working condition is similar to condition ②, Si IGBT and SiC MOSFET jointly participate in the turn-on process, and there is no additional conduction loss during T_{on_delay}. When the SiC MOSFET is turned on, the current flowing in the Si IGBT has not yet risen to the load current. Therefore, the SiC MOSFET has to undertake part of the load current and generate some of the turn-on losses. Under this working condition, the turn-on loss of the hybrid switch includes two parts: the turn-on loss caused by the Si IGBT during T_{on_delay}, and the turn-on loss caused by both SiC MOSFET and Si IGBT after T_{on_delay} and before the hybrid switch is fully turned on. The turn-on loss expression of the hybrid switch under this condition can be shown as:

$$E_{on} = E_{s\_on\_IGBT} + E_{s\_on\_Hybrid} = \int_0^{T_{on\_delay}} i_C(t) \cdot v_{CE}dt + \int_{T_{on\_delay}}^{T_{on}} (i_D(t) + i_C(t)) \cdot v_F dt \quad (11)$$

④ $T_{on\_delay} < 0$ and $|T_{on\_delay}| > T_{on\_IGBT}$

When the turn-on delay time T_{on_delay} is greater than the Si IGBT hard-switching-on time T_{on_IGBT}, the SiC MOSFET in the hybrid device is in the ZVS turn-on state, and its turn-on loss is zero. At this time, the turn-on loss of the hybrid device is the hard-switching-on loss of the Si IGBT which is defined as $E_{hard\_on\_IGBT}$. Moreover, when the hybrid device is fully turned on, the Si IGBT will undertake the full load current, resulting in additional conduction loss ΔE_{con_IGBT}. Therefore, the turn-on loss and additional conduction loss of the hybrid device under this operating condition can be expressed as:

$$\Delta E_{con\_IGBT\_on} = \int_{T_{on\_IGBT}}^{T_{on\_delay}} I_O \cdot (V_{CE} - V_F)dt = I_O \cdot (V_{CE} - V_F) \cdot (T_{on\_delay} - T_{on\_IGBT}) \quad (12)$$

$$E_{on} = E_{hard\_on\_IGBT} = \int_0^{T_{on\_IGBT}} i_C(t) \cdot v_{CE}(t)dt \quad (13)$$

Under the traditional switching-on strategy, the SiC MOSFET is turned on ahead of the Si IGBT so that the Si IGBT can realize the ZVS turn-on, but it will result in the additional conduction loss of the SiC MOSFET. With inappropriate time delay, even more conduction loss will be introduced in during the turn-on time delay. If we take additional conduction loss into consideration, the turn-on loss of the hybrid switch can be approximately expressed as (14), as shown at the bottom of the next page.

When $T_{on\_delay} = 0$, E_{s_on} can be expressed as (15).

$$E_{on}\big|_{T_{on\_delay}=0} = \int_0^{T_{on}} (i_D(t) + i_C(t)) \cdot v_F(t)dt \quad (15)$$

where T_{on} is the time period from Si IGBT begins to turn on to the hybrid switch is completely turned on.

It is obvious that E_{s_on} is the smallest when $T_{on\_delay} = 0$, which means each device should turn on at the same time

to reduce the switch-on loss. Therefore, setting reasonable turn-on time delay is very important to achieve ZVS turn-on for Si IGBT or SiC MOSFET. However, the additional conduction loss will be increased and even greater than the total power loss of the hybrid switch.

2) TURN-OFF LOSS

The turn-off process of hybrid switch will be analyzed is shown in Fig. 8. During the turn-off time delay, the SiC MOSFET is still conducting while the Si IGBT is turned off, the voltage drop of the hybrid switch is the forward voltage of the SiC MOSFET. Therefore, the zero-voltage switching-off of the Si IGBT can be realized. The turn-off power loss caused by tail current of the Si IGBT can be reduced significantly. The turn-off loss of the SiC MOSFET is equal to its hard-switching-off loss, which can be expressed as:

$$E_{\text{off\_MOS}} = \int_{T_{\text{off\_delay}}}^{T_{\text{off\_delay}}+T_{\text{off\_MOS}}} i_{\text{D}}(t) \cdot v_{\text{DS}}(t)\text{d}t \tag{16}$$

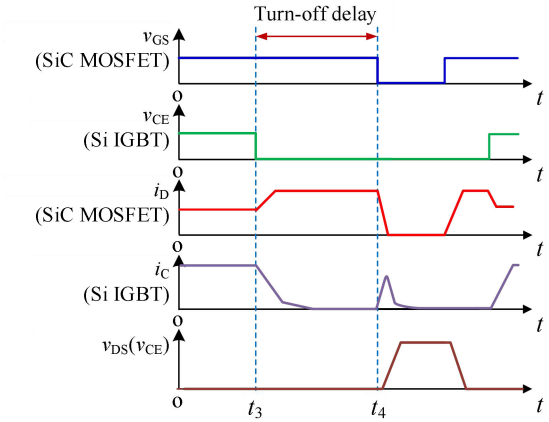

FIGURE 8. Turn-off process.

When the DC bus voltage and load current are constant, switching-off loss of the SiC MOSET is only related to the device itself. During the turn-off delay time, SiC MOSFET undertakes the full load current, the hybrid switch will produce more conduction loss than both devices are conducting. The additional conduction loss is defined as $\Delta E_{\text{con\_MOS\_off}}$ which can be derived as (17)

$$\begin{aligned}\Delta E_{\text{con\_MOS\_off}} &= \int_0^{T_{\text{off\_delay}}} I_{\text{O}} \cdot (V_{\text{DS}} - V_{\text{F}})\text{d}t \\ &= I_{\text{O}} \cdot (V_{\text{DS}} - V_{\text{F}}) \cdot (T_{\text{off\_delay}} - T_{\text{off\_MOS}})\end{aligned} \tag{17}$$

We can see that the additional conduction loss increases gradually with the increase of the turn-off delay time. A longer turn-off delay time will cause a larger $\Delta E_{\text{con\_MOS\_off}}$.

The IGBT is ZVS-off without undertaking the high voltage since the SiC MOSFET is still conducted during the short turn-off delay time. When the SiC MOSFET is turned off, the Si IGBT carriers have not fully recombined, and a current spike is generated, which results in a power loss of the IGBT. The large amount of stored charge in the drift region of the IGBT decreases exponentially due to the minority carrier recombination during the gate turn-off delay time [28]. The stored charge is proportional to the current [29], therefore, the turn-off loss of the Si IGBT displays an exponentially decrease with the increase of delay time. The turn-off loss caused by stored charge can be considered as the sum of a zero-state response and a zero-input response. The zero-state response caused by undertaking the blocking voltage and removing stored charge can be expressed as:

$$E_{\text{off\_IGBT1}} = E_{\text{hard\_off\_IGBT}} \cdot e^{-T_{\text{off\_delay}}/\tau_0} \tag{18}$$

where τ_0 is the lifetime of the IGBT. $E_{\text{hard\_off\_IGBT}}$ is the hard-switching-off loss of the IGBT at a certain forward current, which can be expressed as:

$$E_{\text{hard\_off\_IGBT}} = \int_0^{T_{\text{off\_IGBT}}} i_{\text{C}}(t) \cdot v_{\text{CE}}(t)\text{d}t \tag{19}$$

The other part of IGBT turn-off loss is caused by removing inherent plasma [30]. The zero-input response is related to the residual turn-off switching loss of the IGBT which is mainly influenced by the DC-link voltage and has nothing to do with the turn-off delay time. Therefore, the zero-input response can be expressed as:

$$E_{\text{off\_IGBT2}} = E_{\text{res\_off}} \cdot (1 - e^{-T_{\text{off\_delay}}/\tau_0}) \tag{20}$$

where $E_{\text{res\_off}}$ is the residual turn-off switching loss of the IGBT.

$$E_{\text{s\_on}} = \begin{cases} \int_0^{T_{\text{on\_MOS}}} i_{\text{D}}(t) \cdot v_{\text{DS}}(t)\text{d}t + I_{\text{O}} \cdot (V_{\text{DS}} - V_{\text{F}}) \cdot (T_{\text{on\_delay}} - T_{\text{on\_MOS}}), T_{\text{on\_delay}} > 0, T_{\text{on\_delay}} > T_{\text{on\_MOS}} \\ \int_0^{T_{\text{on\_delay}}} i_{\text{D}}(t) \cdot v_{\text{DS}}(t)\text{d}t + \int_{T_{\text{on\_delay}}}^{T_{\text{on}}} (i_{\text{C}}(t) + i_{\text{D}}(t)) \cdot v_{\text{F}}(t)\text{d}t, T_{\text{on\_delay}} > 0, T_{\text{on\_delay}} < T_{\text{on\_MOS}} \\ \int_{T_{\text{on\_delay}}}^{0} i_{\text{C}}(t) \cdot v_{\text{CE}}(t)\text{d}t + \int_{-T_{\text{on}}}^{T_{\text{on\_delay}}} (i_{\text{C}}(t) + i_{\text{D}}(t)) \cdot v_{\text{F}}(t)\text{d}t, T_{\text{on\_delay}} < 0, -T_{\text{on\_delay}} < T_{\text{on\_IGBT}} \\ \int_0^{T_{\text{on\_IGBT}}} i_{\text{C}}(t) \cdot v_{\text{CE}}(t)\text{d}t + I_{\text{O}} \cdot (V_{\text{CE}} - V_{\text{F}}) \cdot (-T_{\text{on\_delay}} - T_{\text{on\_IGBT}}), T_{\text{on\_delay}} < 0, -T_{\text{on\_delay}} > T_{\text{on\_IGBT}} \end{cases} \tag{14}$$

The turn-off loss of IGBT can be expressed as:

$$E_{\text{off\_IGBT}} = (E_{\text{hard\_off\_IGBT}} - E_{\text{res\_off}}) \cdot e^{-\tau \cdot T_{\text{off\_delay}}} + E_{\text{res\_off}} \tag{21}$$

where $\tau = 1/\tau_0$, which is the exponential time constant for the dependency of the IGBT's switching off loss on the gate turn-off delay time. Therefore, when $T_{\text{off\_delay}} = 0$, the Si IGBT is in the hard turn-off state, and the residual loss of the IGBT is the hard-switching-off loss under the steady-state. When $T_{\text{off\_delay}}$ is large enough, since the minority carriers in the drift region disappear after the recombination process, the residual loss of the Si IGBT is basically stable. When the SiC MOSFET is turned off and the hybrid device undertakes the bus voltage again, the parasitic capacitance charging of the Si IGBT itself will also produce a current spike, resulting in some residual losses.

In summary, the turn-off loss of the hybrid switch when the Si IGBT is turned-off ahead of the SiC MOSFET can be expressed as:

$$E_{\text{off}} = E_{\text{off\_MOS}} + E_{\text{off\_IGBT}} \tag{22}$$

Therefore, setting reasonable turn-off delay time is very important. If $T_{\text{off\_delay}}$ is too short, the loss caused by the current spike of the IGBT is large, and zero-voltage switching cannot be effectively realized. However, if the turn-off delay time is too long, the excessive additional conduction loss of SiC MOSFET may lead to more power loss as well. It can be seen that the turn-off delay time of the hybrid switch has a great influence on its switching loss. With the consideration of $\Delta E_{\text{con\_MOS\_off}}$, the total switching loss affected by $T_{\text{off\_delay}}$ can be described as:

$$E_{\text{off\_delay}} = E_{\text{off\_MOS}} + \Delta E_{\text{con\_MOS\_off}} + E_{\text{off\_IGBT}} \tag{23}$$

From (16) and (17) we can see that the total turn-off loss of SiC MOSFET is increasing linearly, and its increasing speed is the difference of the conduction loss of hybrid switch and SiC MOSFET with the value of $(V_{\text{DS}} - V_{\text{F}}) \cdot I_{\text{O}}$. The $E_{\text{off\_IGBT}}$ decreases exponentially, therefore its decreasing speed is getting slower with $T_{\text{off\_delay}}$. If $T_{\text{off\_delay}}$ is large enough, the decreasing speed of $E_{\text{off\_IGBT}}$ is nearly zero. Therefore, there must be one optimal $T_{\text{off\_delay}}$ where the $E_{\text{off\_delay}}$ is minimized. When the derivatives of $\Delta E_{\text{con\_MOS\_off}}$ and $E_{\text{off\_IGBT}}$ have same value, the $E_{\text{off\_delay}}$ is smallest. So the optimal turn-off delay time $T_{\text{off\_delay\_optimal}}$ can be described as:

$$T_{\text{off\_delay\_optimal}} = \frac{1}{\tau} \ln \frac{(V_{\text{DS}} - V_{\text{F}}) \cdot I_{\text{O}}}{(E_{\text{off\_hard\_IGBT}} - E_{\text{res\_off}}) \cdot \tau} \tag{24}$$

With the increase of $T_{\text{off\_delay}}$, before $T_{\text{off\_delay\_optimal}}$, the decreasing speed of $\Delta E_{\text{off\_IGBT}}$ is larger than the increasing speed of $\Delta E_{\text{con\_MOS\_off}}$, therefore the $E_{\text{off\_delay}}$ is decreasing during this period. Once $T_{\text{off\_delay}}$ is larger than $T_{\text{off\_delay\_optimal}}$, the $E_{\text{off\_delay}}$ begins to increase.

The essential parameters to calculate the optimal turn-off time delay is shown in Table 3. These parameters are obtained from the static characteristics measured in Part.II and the double pulse test of the Si IGBT and SiC MOSFET.

TABLE 3. Essential Parameters of The Optimal Turn-off Time Delay.

parameter	value
V_{DS}/V	6.5
V_{F}/V	1.7
I_{O}/A	30
τ/μs^{-1}	1.194
$E_{\text{off\_hard\_IGBT}}$/mJ	1.303
E_{res}/mJ	0.038

Therefore, according to equation (24), the theoretical $T_{\text{off\_delay\_optimal}}$ is calculated as 1.98 μs.

V. SWITCHING DELAY TIME OPTIMIZATION FOR POWER LOSS REDUCTION

A better dynamic performance of hybrid switch includes high switching speed, low switching loss, low settling time, low overshoot, and slight oscillation. These characteristics are influenced by varies factors such as the design of driving circuit and the layout of circuit. In this study, we mainly focus on power loss reduction, and verify the optimal gate signal sequence by minimizing the power loss of hybrid switch. According to the previous analysis, the optimal switching sequence for the hybrid switch is Si IGBT and SiC MOSFET turn on synchronously; Si IGBT turns off ahead of SiC MOSFET for $T_{\text{off\_delay\_optimal}}$ shown in (24). To verify the optimal switching sequence, a double pulse test in an inductive clamped circuit was performed for the evaluation of the switching performance of the hybrid switch, as shown in Fig. 9. The STM32 single-chip microcomputer is used to generate the dual-pulse gate drive signal for the two discrete devices in hybrid switch. The driving board of each device is discrete. The V_{GS} of Si IGBT and SiC MOSFET are $+20\text{V}/-4\text{V}$ and $+15\text{V}/-8.7\text{V}$ respectively. The turn-on delay time of Si IGBT varies from 0.2 μs ahead of the SiC MOSFET to 0.2 μs lag behind the SiC MOSFET; the turn-off delay time of SiC MOSFET varies from 0 μs to 4 μs lagging behind Si IGBT. The working conditions of the circuit are listed in Table 4.

TABLE 4. Testing Conditions of Double Pulse Test.

parameter	value
DC bus voltage	600 V
Load current	30 A
Load inductor value	600 µH
Bypassing capacitor value	110 µF

A. TURN-ON DELAY TIME

Fig. 11 shows the turn-on waveforms under different Si IGBT turn-on delay times when $T_{\text{on\_delay}} \geq 0$ and $T_{\text{on\_delay}} > T_{\text{on\_MOS}}$. When the turn-on delay time is long enough, all load current is flowing through the SiC MOSFET at the moment

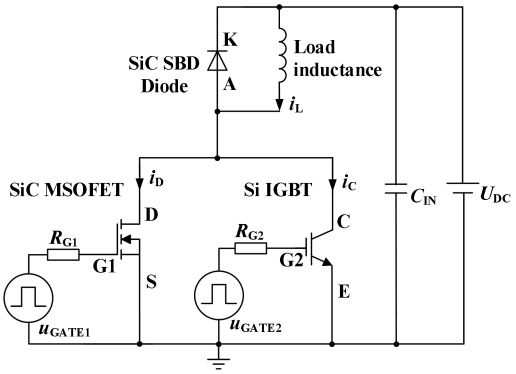

FIGURE 9. Schematic of the test platform.

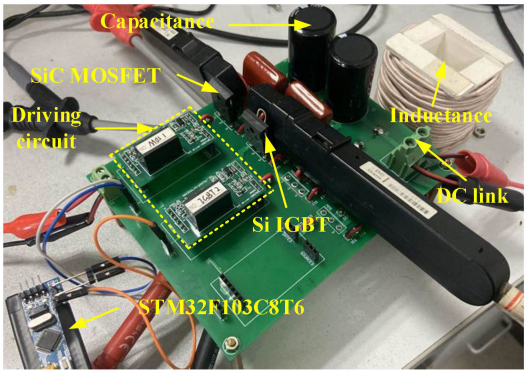

FIGURE 10. Experimental setup.

the hybrid device is turned on. When i_D rises to I_O, due to the reverse recovery current of the diode, i_D continues to rise, a small current spike appears. After the reverse recovery current of the diode reaches its peak value, forward voltage of the hybrid switch begins to rise, and the voltage on C_{GC} and C_{CE} will quickly drop to almost zero. The discharge current on C_{CE} creates a reverse current flowing through the Si IGBT, and this reverse current will be superimposed on the turn-on current of the SiC MOSFET. Once IGBT is turned on, the load current starts to commutate from the SiC MOSFET to the IGBT and gradually reaches the steady state.

Fig. 12 shows the turn-on process under different Si IGBT turn-on delay times when $T_{on\_delay} \geq 0$ and $T_{on\_delay} \leq T_{on\_MOS}$. Under this condition, when the Si IGBT is turned on, the current flowing through the SiC MOSFET has not yet risen to the load current, so the Si IGBT also has to undertake part of the load current and generate turn-on losses. During the T_{on_delay}, the SiC MOSFET turns on firstly, and the current is gradually commutated from the freewheeling diode to the channel of SiC MOSFET. At the end of T_{on_delay}, i_D has not risen to I_O, the load current starts to flow into the Si IGBT at this time, i_C begins to rise and i_D continues rising. When $i_D + i_C = I_O$, the current in the diode drops to 0, but due to its reverse recovery characteristics, i_C and i_D will continue increasing until the diode reverse recovery current reaches its peak value. At this moment, v_{DS} begins to drop. When v_{DS}

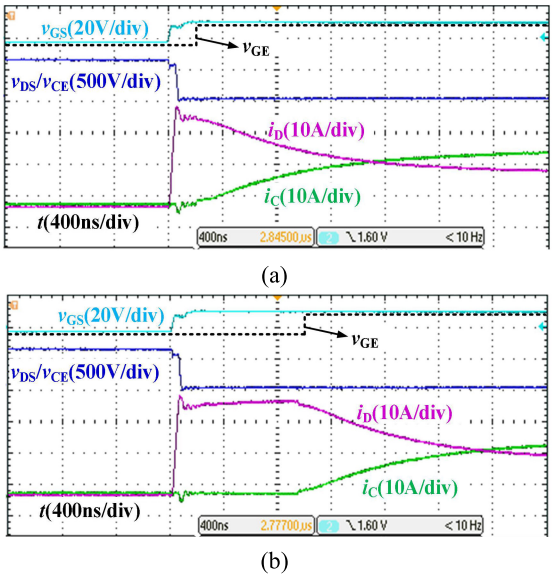

FIGURE 11. Turn-on process of hybrid switch when $T_{on\_delay} \geq 0$ and $T_{on\_delay} > T_{on\_MOS}$. (a) $T_{on_delay} = 0.1\mu$s. (b) $T_{on_delay} = 1\mu$s.

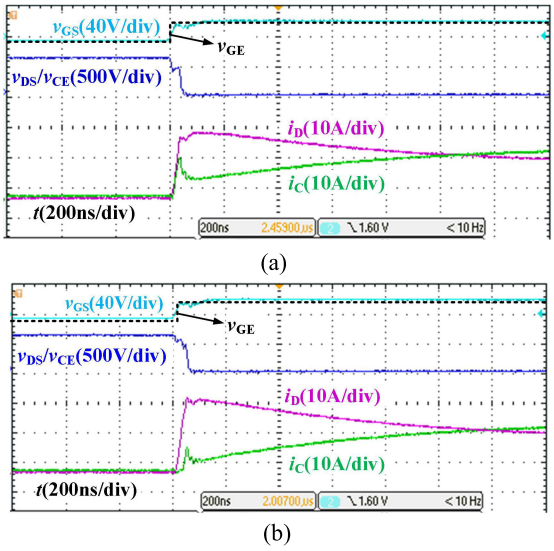

FIGURE 12. Turn-on process of hybrid switch when $T_{on\_delay} \geq 0$ and $T_{on\_delay} \leq T_{on\_MOS}$. (a) $T_{on\_delay} = 0$. (b) $T_{on\_delay} = 20$ ns.

drops to the conduction voltage of the hybrid switch, the turn-on process basically ends. i_C and i_D in the hybrid switch are redistributed until it reaches a steady state.

Fig. 13 shows the turn-on waveforms under different Si IGBT turn-on delay times when $T_{on\_delay} < 0$ and $|T_{on\_delay}| \leq T_{on\_IGBT}$. The operating principle of the device switching on is similar to the working condition that when $T_{on\_delay} \geq 0$ and $T_{on\_delay} \leq T_{on\_MOS}$. At the moment SiC MOSFET is turned on, the current flowing through the Si IGBT has not yet risen to the load current, the hybrid switch is not fully turned on, both devices take part in the load current conduction during turn-off transient process.

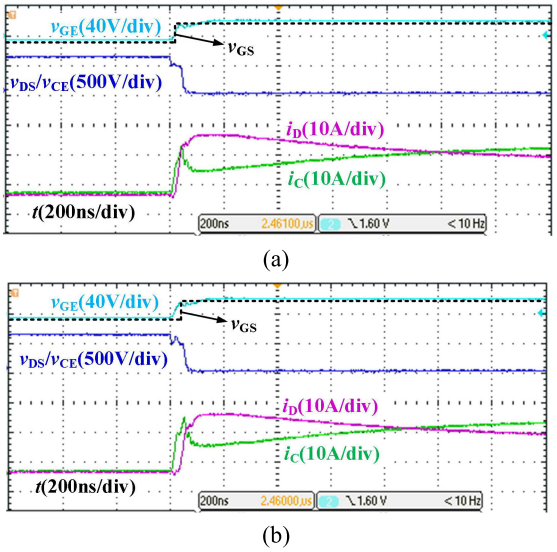

FIGURE 13. Turn-on process of hybrid switch when $T_{on\_delay} \geq 0$ and $|T_{on\_delay}| \leq T_{on\_IGBT}$. (a) $T_{on\_delay} = -20$ ns. (b) $T_{on\_delay} = -40$ ns.

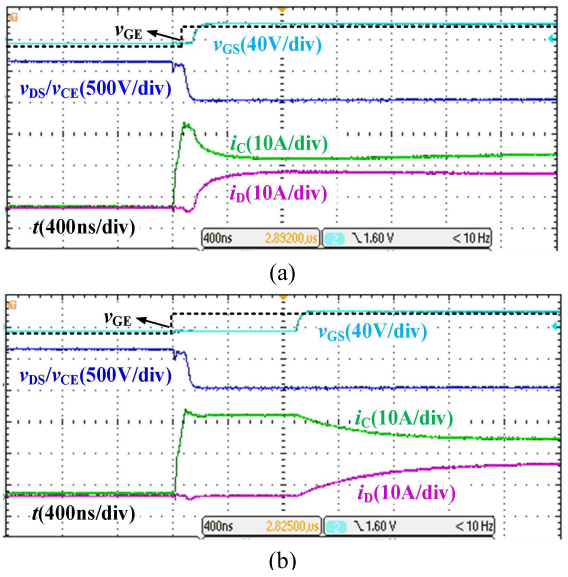

FIGURE 14. Turn-on process of hybrid switch when $T_{on\_delay} < 0$ and $|T_{on\_delay}| > T_{on\_IGBT}$. (a) $T_{on_delay} = -0.2\mu$s. (b) $T_{on_delay} = -1\mu$s.

Fig. 14 shows the turn-on waveforms under different turn-on delay times when $T_{on\_delay} < 0$ and $|T_{on\_delay}| > T_{on\_IGBT}$. The operating principle is similar to the working condition $T_{on\_delay} > 0$ and $T_{on\_delay} > T_{on\_MOS}$. When the SiC MOSFET is turned on, the Si IGBT has been fully turned on, and the SiC MOSFET can achieve ZVS turn-on. In this process, the IGBT is in a hard turn-on state and undertakes all turn-on losses of the hybrid switch. While the SiC MOSFET can achieve ZVS turn-on, and its turn-on switching loss is almost zero. SiC MOSFET has no additional conduction loss as well.

Fig. 15 shows the relationship between the turn-on switching loss E_{on} of the hybrid switch and the turn-on delay time T_{on_delay}. As the turn-on delay time is shortened from -0.2 μs to -0.1 μs, the Si IGBT is turned on ahead of SiC MOSFET, the turn-on switching loss of the Si IGBT remains unchanged. During this period, the turn-on switching loss is all composed of the hard-switching-on loss of Si IGBT, which is about 1.05 mJ. When the turn-on delay time is shortened from -0.1μs to 0, the turn-on switching loss of Si IGBT is significantly reduced. The turn-on loss of SiC MOSFET increases slightly at the same time, therefore the total turn-on switching loss of the hybrid switch decreases. When the T_{on_delay} is 0, the total turn-on loss of the hybrid switch is the smallest, which is about 0.28 mJ. When the turn-on delay becomes greater than zero, the Si IGBT is turned on lagging behind SiC MOSFET. As the turn-on delay time increases from 0 to 0.08 μs, the turn-on switching loss of the Si IGBT continues to decrease, but the decreasing speed is getting lower. The turn-on loss of the SiC MOSFET continues to increase, the total turn-on loss of the hybrid switch increases as well. After 0.08 μs, the turn-on loss of the hybrid switch remains basically unchanged. At this time, the total turn-on loss equals to the hard-switching-on loss of SiC MOSFET,

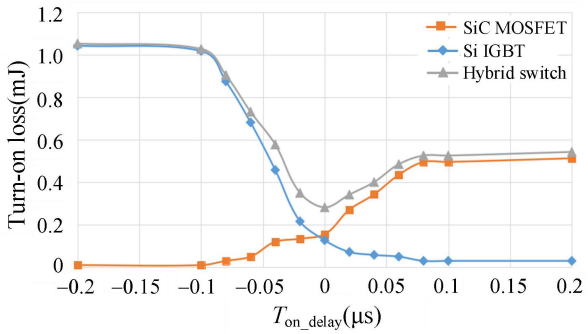

FIGURE 15. Turn-on switching losses of the hybrid switch as a function of T_{on_delay}.

whose value is about 0.58 mJ. Therefore, the lowest turn-on switching loss appears when Si IGBT and SiC MOSFET are turned on synchronously, and the turn-on switching loss can be decreased for about 73% compared with using Si IGBT only and about 52% compared with using SiC MOSFET only.

When the absolute value of the delay time T_{on_delay} of the gate signal is small, the load current has not been fully commutated to the hybrid switch at the end of the T_{on_delay}. Therefore, after the period of turn-on delay time ends, both devices participate in the turn-on process. The di/dt of the hybrid switch is the sum of the di/dt of these two devices, which is larger than that of either device. When the load current is constant, if the time when both devices participate in the turn-on process is longer, the total switching-on time will be shorter, and the turn-on loss of the hybrid switch will be less. Fig.16 shows how the di/dt of the hybrid switch changes with T_{on_delay}. When the T_{on_delay} is less than -0.1μs, the di/dt of the hybrid switch is only about 0.34 A/ns, which is the same as the switching on speed of the Si IGBT; when

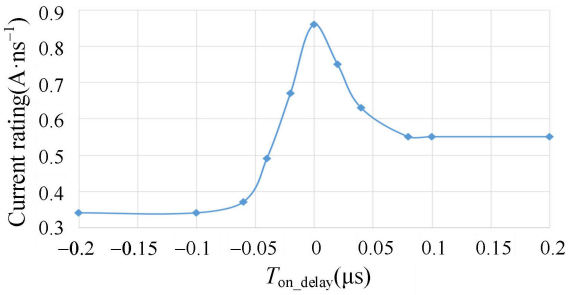

FIGURE 16. Relationship between current rating of hybrid switch and T_{on_delay}.

the T_{on_delay} is greater than 0.08 μs, the di/dt of the hybrid switch is about 0.56 A/ns, which is the same as the switching on speed of the SiC MOSFET, and it is about 65% faster than the turn-on speed of the Si IGBT. When the T_{on_delay} is zero, the di/dt of the hybrid switch is 0.86 A/ns, which is about the sum of the turn-on speeds of Si IGBT and SiC MOSFET. It is almost 153% higher than that of Si IGBT. Therefore, for the hybrid switch, the optimal turn-on sequence is that the two devices are turned on at the same time, that is, the optimal turn-on delay is zero.

B. TURN-OFF DELAY TIME

The testing condition of turn-off process is the same as that of turn-on process. Fig.17 shows the turn-off process of a hybrid switch with turn-off delay times of 0.1 μs, 0.4μs, 1.0μs and 2.0 μs, respectively. When v_{GE} becomes low level, the current in the Si IGBT is firstly reduced to almost zero, achieving ZVS turn-off. However, due to the internal structure of each device in the hybrid switch, Si IGBT will generate a current spike at the moment when SiC MOSFET is turned off. This current spike causes the Si IGBT to generate turn-off losses. With the increase of T_{off_delay}, its peak value gradually decreases. The SiC MOSFET undertakes a hard-switching-off process.

The internal structure of Si IGBT is equivalent to a cascade of MOSFET and a BJT. When the Si IGBT is turned off, the MOSFET channel is quickly turned off, and i_C quickly drops to zero. In the turn-off delay time, the SiC MOSFET undertakes all the load current, and the forward voltage of the hybrid device is the same as that of the SiC MOSFET. Therefore, the residual carriers in the internal drift region of the Si IGBT can only disappear by the recombination process and the compound speed changes exponentially. When the SiC MOSFET is turned off, v_{DS} will quickly rise to the DC bus voltage. If the recombination of the residual carriers in the Si IGBT is not completed within the T_{off_delay} time, then the minority carriers in the Si IGBT need to withstand the high dv/dt during the turn-off process of the SiC MOSFET, resulting in a high rate of carriers extraction. This causes a turn-off current spike of the Si IGBT. Fig. 18 shows the relationship between the turn-off current spike and the turn-off delay time under different turn-off gate resistance $R_{G(ext)}$. The change

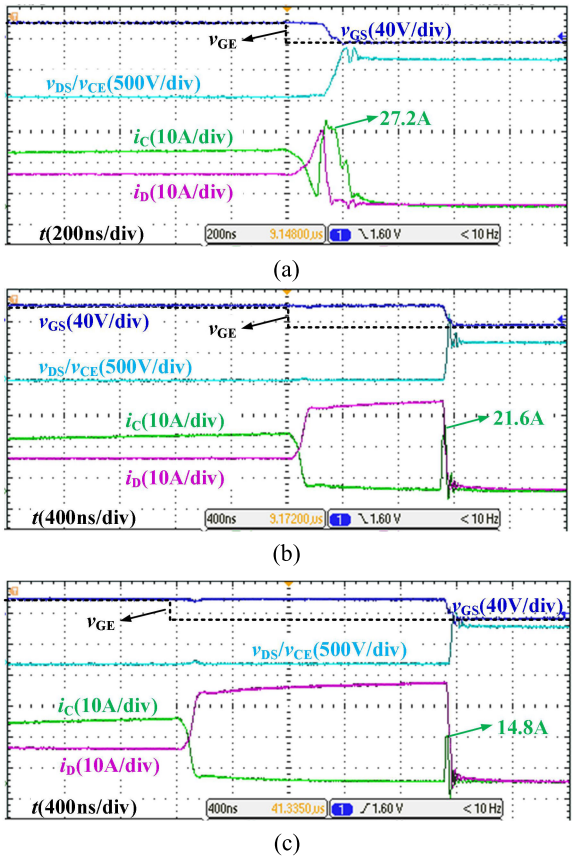

FIGURE 17. Relationship between current rating of hybrid switch and T_{off_delay}. (a) $T_{off_delay} = 0.1\,\mu$s. (b) $T_{off_delay} = 1\,\mu$s. (c) $T_{off_delay} = 2\,\mu$s.

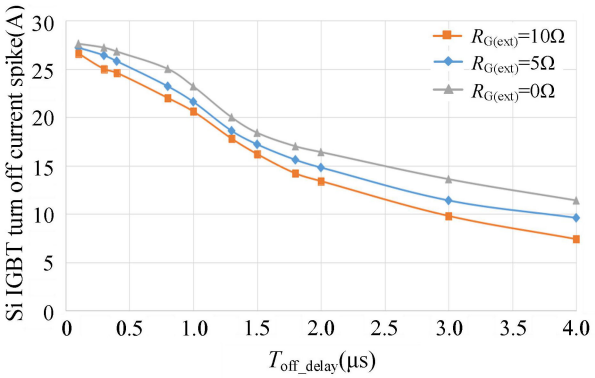

FIGURE 18. Relationship between the turn-off current spike of Si IGBT and turn-off delay time under different $R_{G(ext)}$.

of $R_{G(ext)}$ also results in the change of dv_{DS}/dt during the turn-off process.

Table 5. shows the turn-off dv_{DS}/dt corresponding to different $R_{G(ext)}$. From Fig. 18 we can intuitively see that the turn-off current spike of Si IGBT varies with the changes in dv_{DS}/dt. With the $R_{G(ext)}$ increases, dv_{DS}/dt gradually decreases, the turn-off speed of SiC MOSFET becomes slower, and the carrier extraction speed of Si IGBT becomes slower, so the peak value of the turn-off current spike

TABLE 5. Variation Ratio of V_{DS} Under Different External Gate Resister.

External gate resister $R_{G(ext)}/\Omega$	dv_{DS}/dt (V/ns)
0	44.09
5	38.13
10	32.72

of Si IGBT decreases as well. When dv_{DS}/dt is constant, the current spike of Si IGBT decreases with the increase of T_{off_delay}. The longer T_{off_delay} will lead to the better completion of the IGBT carrier recombination. The current spike formed after the extraction of carrier is also smaller. When $T_{off\_delay} = 0.1\mu s$, the IGBT turn-off current peak value $I_{peak} = 27.2$ A, which is very close to the load current value. When $T_{off\_delay} = 2.0\mu s$, $I_{peak} = 14.8$ A, which drops for about 45.6% compared with $T_{off\_delay} = 0.1\mu s$.

Fig. 19 shows the relationship between the turn-off switching loss of the Si IGBT and turn-off delay time T_{off_delay}. For Si IGBT, the turn-off switching loss is caused by its turn-off current spikes when the SiC MOSFET is turned off. This residual loss decays exponentially as the T_{off_delay} increases. The turn-off switching loss of Si IGBT decreases exponentially with the increase of T_{off_delay}. With the increase of gate resistances $R_{G(ext)}$, the turn-off switching loss increases when the T_{off_delay} is short, especially when T_{off_delay} is less than $1\mu s$. When T_{off_delay} is more than $1\mu s$, the difference of the switching loss can be ignored. Although the IGBT current spike decreases with the increase of the $R_{G(ext)}$, the switching speed decreases as well, which leads to a larger switching loss.

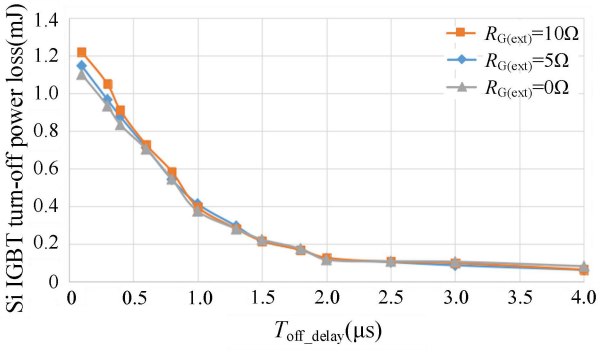

FIGURE 19. Relationship between the turn-off loss of Si IGBT and turn-off delay time under different $R_{G(ext)}$.

The turn-off loss of the SiC MOSFET mainly contains the hard-switching-off loss. However, the additional conduction loss must be taken into consideration since T_{off_delay} may cause additional conduction power loss. When T_{off_delay} is too long, additional conduction loss leads to more total loss of the hybrid switch. Fig. 20 shows the relationship between power loss of the SiC MOSFET and T_{off_delay}. During the turn-off process, the power loss of the SiC MOSFET consists of two parts: additional conduction

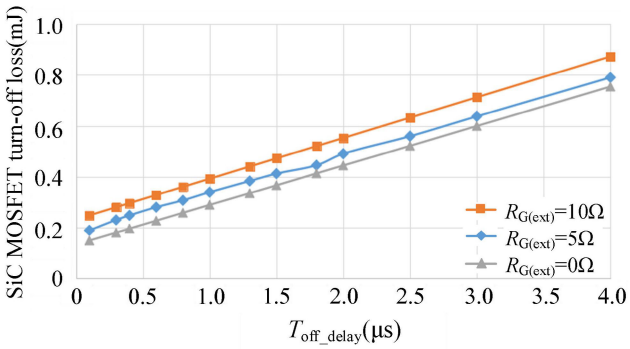

FIGURE 20. Relationship between the turn-off loss of SiC MOSFET and turn-off delay time under different $R_{G(ext)}$.

loss and hard-switching-off loss. Additional conduction loss increases with turn-off delay time, while hard-switching-off loss is constant, so the turn-off loss of SiC MOSFET increases linearly with T_{off_delay} increases.

Fig. 21 shows the relationship between the total turn-off loss of hybrid switch and the turn-off delay time T_{off_delay} when the gate resistance is 5 Ω. The curve of hybrid switch is the sum of Si IGBT and SiC MOSFET power loss curves. The total turn-off loss of the hybrid switch decreases first and then increases. The minimum turn-off loss point can be found when T_{off_delay} changes. When the turn-off loss of the hybrid switch is minimum, the corresponding T_{off_delay} is the optimal turn-off delay time. Clearly, $T_{off\_delay\_optimized} = 2.0\mu s$. This value is quite close to the theoretical $T_{off\_delay\_optimized}$ (1.98 μs) obtained in Part.III. Therefore, the feasibility of the power loss model is verified. This means that when the SiC MOSFET lags behind the Si IGBT by about 2.0 μs, the total turn-off poloss of the hybrid parallel switch is the smallest, and E_{off_min} is about 0.54 mJ, which is about 61.4% reduction compared with using pure Si IGBT as the switching device.

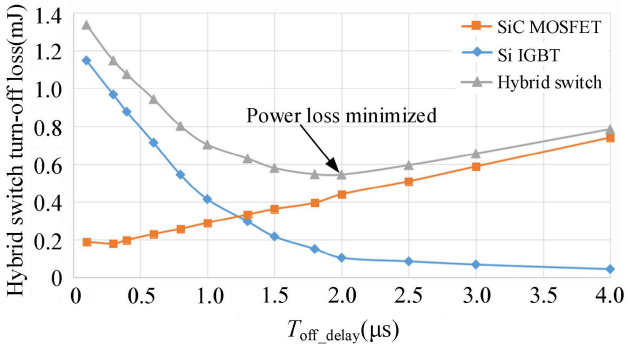

FIGURE 21. Relationship between the turn-off loss of the hybrid device and the turn-off delay time when $R_{G(ext)}$ is 5Ω.

Fig. 22 shows the relationship between the power loss of the hybrid switch and T_{off_delay} with different gate resistor. With the increase of the external gate resistor, the turn-off switching loss of the hybrid switch increases slightly.

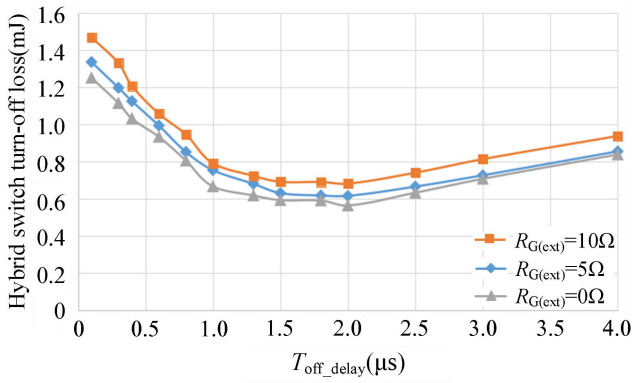

FIGURE 22. Relationship between the turn-off loss of the hybrid device and the turn-off delay time under different $R_{G(ext)}$.

However, the external gate resistor changes, the switching off energy firstly decreases and then increases. The lowest power loss always appears when $T_{off\_delay\_optimized}$ is 2.0 μs.

VI. PERFORMANCE EVALUATION

To verify the superiority of the SiC/Si hybrid switch with the optimal switching sequence, simulations are carried out in LTSpice. A hybrid-switch based Buck converter, shown as Fig. 23, is built and tested to verify the conversion efficiency improvement by using optimized switching time delay. The C2M0160120D and IKW25N120T2 are selected to constitute the hybrid device. The parameters are tabulated in Table 6.

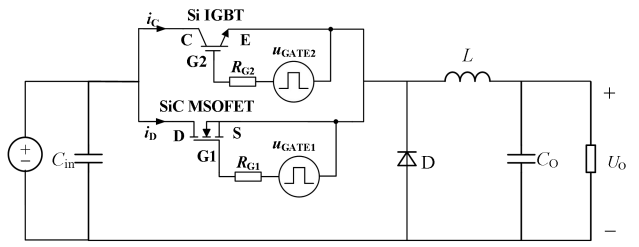

FIGURE 23. Schematic of hybrid-switch based Buck converter.

TABLE 6. Testing conditions of buck converter.

parameter	Value
DC bus voltage	400 V
Switching frequency	50 kHz
Turn-on delay time of Si IGBT	0 μs
Turn-off delay time of SiC MOSFET	2 μs
Rated load power	4 kW
Rated output voltage	120 V

Fig. 24 shows the relationship between the turn-off delay time of Si IGBT and the efficiency of the converter. When T_{off_delay} is quite low, the efficiency is low because of the large switching loss of IGBT. When T_{off_delay} is 2.2μs, the efficiency is the highest, which is about 95.4%.

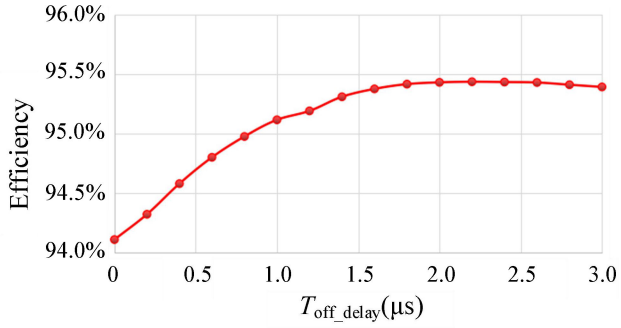

FIGURE 24. Schematic of hybrid-switch based Buck converter.

When T_{off_delay} continues increasing, the efficiency begins to decrease because of the increasing additional conduction loss of the SiC MOSFET.

Fig. 25 shows the relationship between the turn-on delay time of Si IGBT and the efficiency of the converter. It can be seen clearly that when Si IGBT and SiC MOSFET are turned on synchronously, the converter has the highest efficiency.

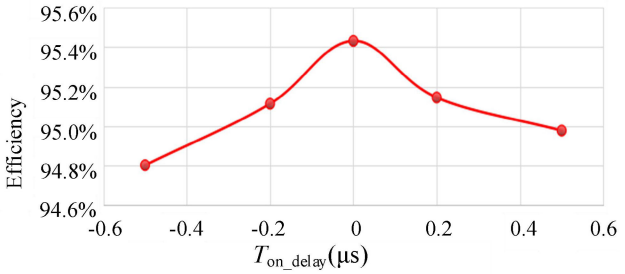

FIGURE 25. Schematic of hybrid-switch based Buck converter.

The comparison of the efficiency between hybrid-switch based converter and pure Si IGBT based converter is shown in Fig. 26. Five load operating points, namely, 20%, 40%, 60%, 80%, and 100% are simulated. The turn-on delay time is set to be 0 s, the duty cycle of SiC MOSFET is 0.3, and the Si IGBT is turned-off 2 μs earlier than SiC MOSFET. The efficiency is increased by 7.5% at 20% load condition, and by 2.5% at full load condition. Therefore, using hybrid

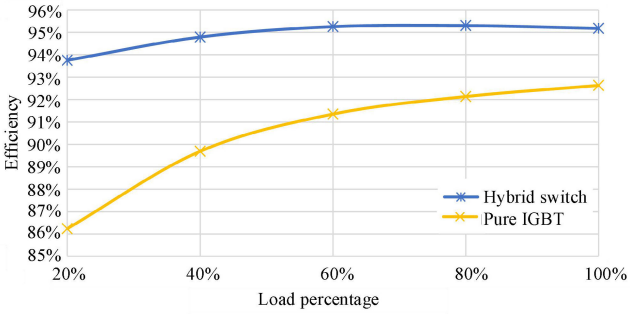

FIGURE 26. Schematic of hybrid-switch based Buck converter.

switch with the optimized switching sequence can significantly improve the efficiency of the Buck converter.

VII. CONCLUSION

In this paper, a generic power loss calculation model is established according to the conduction characteristics of the hybrid switch, and then an optimized timing sequence of hybrid parallel switch is studied. Based on the power loss calculation model, the optimal turn-on sequence is that Si IGBT and SiC MOSFET are turned on at the same time. By contrast, the optimal turn-off sequence is Si IGBT turns off ahead of SiC MOSFET, and the optimal turn-off delay time can be calculated according to the power loss model. Therefore, in the case study, Si IGBT is turned off before SiC MOSFET for about 2 μs. The switching characteristics of hybrid parallel switches working on this switching sequence are analyzed both theoretically and experimentally.

A. TURN-ON DELAY TIME

The turn-on switching loss is the smallest when Si IGBT and SiC MOSFET are turned on at the same time. The experiment compared the total power loss when Si IGBT turned on ahead of and lag behind SiC MOSFET with different turn-on delay time. Since the switching on speed of the hybrid parallel switch is the fastest, the switching loss is the smallest. It is not necessary to additionally set a turn-on delay time of the Si IGBT lagging turn-on. When Si IGBT and SiC MOSFET are turned on synchronously, the turn-on switching loss can be decreased for about 73% compared with using Si IGBT only and about 52% compared with using SiC MOSFET only.

B. TURN-OFF DELAY TIME

During the turn-off process, when the Si IGBT is turned off ahead of the SiC MOSFET, there is still a current spike in the Si IGBT due to carrier extraction at the moment the SiC MOSFET is turned off. This will cause additional turn-off loss on the Si IGBT. The Si IGBT current peak value and turn-off loss value decrease with the increase of turn-off delay. During the turn-off delay time, the turn-on loss of SiC MOSFET increases with the increase of turn-off delay time. Therefore, the switching off power loss of the hybrid switch firstly decreases and then increases with the increase of turn-off delay time. A short turn-off delay time can efficiently help decrease the power loss of the hybrid switch, but it cannot be too long. For the hybrid switch mentioned in this paper, the optimal turn-off delay is 2 μs, and the $E_{\text{off\_min}}$ is decreased about 61.4% than using pure Si IGBT as the switching device.

C. VERIFICATION ON BUCK CONVERTER

The simulation results show that the optimized switching gate sequence is improved to be efficient in decreasing the power loss of the hybrid switch and improving the efficiency of the converter. With the optimal switching time delay, the efficiency of the Buck converter is significantly improved for about 2.5% at full load and 7.5% at 20% load. Therefore, the switching sequence strategy is instructive in designing a converter based on SiC/Si hybrid switch.

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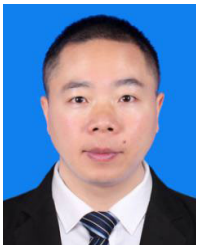

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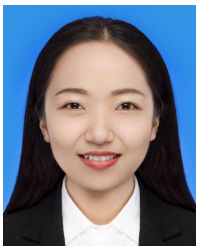

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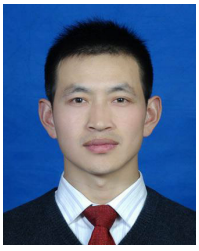

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