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Switched-Capacitor High Voltage Gain Z-Source Converter With Common Ground and Reduced Passive Component

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ABSTRACT Conventional dc-dc Boost converter has limited boost capacity, and its power device suffers high voltage stress. A novel Z-source based dc-dc boost converter featured with high step-up capability and low device voltage stress is proposed in this paper. The proposed topology can also provide a common ground for input and output, which is lacking in the traditional Z-source topology. Compared with other high step-up topologies, the proposed converter can achieve higher voltage gain under the same duty ratio and maintain low voltage stresses on the switch and diode. Moreover, there are fewer passive components in the proposed structure than in other structures. The steady-state analysis for the continuous conduction mode and discontinuous conduction mode is also provided in this manuscript. Finally, a prototype circuit with 40V-60V input voltage, 400V output voltage and 200W output power is implemented in the laboratory. Experiment results confirm the analysis and the features of the proposed converter.

INDEX TERMS DC-DC converter, impedance network, high step-up, switched-capacitor.

I. INTRODUCTION

Step-up dc-dc converters have been used for many applications, such as photovoltaic (PV) generation systems, fuel cells, electric vehicles and LED lighting systems [1]–[4]. In some applications, a high voltage gain is often required. Theoretically, the conventional dc-dc boost converter can provide a high voltage conversion ratio under an extremely high duty cycle. However, the power device suffers high voltage stress, which will cause a serious reverse-recovery problem [5]. Moreover, the current ripple is increased under such a high duty ratio, which will cause the saturation of the inductance. As a result, conventional dc-dc boost converter is unlikely to be used in applications where the voltage conversion ratio is more than 5 times.

Transformer-isolated converters can provide a high voltage gain by adjusting the turn ratio of the transformer [6]. And they have higher reliability and safety than non-isolated converters. However, the switches in this type of converters may suffer extremely high voltage spikes due to leakage inductance of the transformer. To resolve this problem, a resistance-capacitance-diode (RCD) [7] cell is often required, which will cause extra loss and decrease efficiency. Another solution is the active-clamped circuit [8], it can suppress the voltage spike without increasing power loss. However, one more power switch is required, the cost and control complexity are also increased. Moreover, the transformer-isolated converters are subject to the increasing manufacturing costs.

Nonisolated step-up dc-dc converters can be generalized as the coupled-inductor based type [9] and noncoupled-inductor based type [10]–[14]. The coupled-inductor converters can achieve high step-up voltage gain and minimize the voltage stress on the power switch. However, compared to other structures, the converter is relatively bulky. Also, the problems mentioned in the isolated topologies also exist for this type of converter. Various boost techniques without a coupled-inductor have been proposed. The focus of the studies include super-lift [10], switched-inductor and switched-capacitor [11], [12], cascade techniques [13], and impedance network [14], [15].

By integrating multiple voltage-lift cells, the super-lift technique can improve the voltage gain geometrically. However, the voltage stress of the switch is increased as voltage gain increases. Besides, the current spike for charging the capacitors is also increased, which will deteriorate the efficiency and limit its boost capacity in practice.

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Switched-inductor and active switched-inductor structures can charge the inductors in parallel and then discharge them in series to obtain a higher voltage gain. The proposed structure is amenable to many other structures [16], [17]. Unfortunately, the input current has become discontinuous. Besides, the voltage stresses on the semiconductors are also increased. Considering the switched-capacitor structure, in order to obtain a high voltage gain, the cascaded topology with multiple switched-capacitor cells is often required [18], so the number of capacitors and diodes is increased. A higher voltage gain can also be obtained through the two cascaded boost converters. But an additional power switch is required. To reduce circuit complexity and cost, the two switches are integrated into one in [19], named quadratic boost. But the voltage stresses on the switch and output diode are still high. And the current ripple of the inductors is not decreased significantly.

Compared with other structures, Z-source converter and quasi-Z-source converter can provide a high voltage gain with fewer components. Also, the current ripple of the inductor is reduced because of the lower operating duty ratio. Impedance network based converters have the capability of overcoming the limitations of conventional dc-dc converters. However, the traditional Z-source dc-dc converter lacks a common ground for input and output [20]. And the voltage stress of the power device is relatively high. In this paper, A novel Z-source based dc-dc boost converter featured with high step-up capability and low device voltage stress is proposed. The proposed topology can also provide a common ground for input and output, which makes it more suitable for some applications. The rest of this paper is constructed as follows. The structure of the proposed converter and circuit operation mode are present in Section II. Steady-state characteristics are analyzed in Section III. The non-ideal element analysis is given in Section IV. The extension of the proposed topology is present in Section V. Then, a comprehensive comparison between the proposed converter and other structures is shown in Section VI. Simulation and experimental results will be provided to examine the features of the converter in Section VII. The last part is the conclusions in Section VIII.

II. OPERATING MODE OF THE PROPOSED CONVERTER

The circuit topology of the proposed converter is shown in Fig.1, which contains one Z-source network (L_1-C_{Z1}-L_2-C_{Z2}), and one switched-capacitor cell (D_1-S_1-D_2-S_2-C_1). Switches S_1 and S_2 are controlled simultaneously by the same drive signal. Additionally, the proposed converter comprises an input diode D_i, an output diode D_o, and a capacitor C_o.

The operating principles of continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are analyzed in this section. In the following analysis, the following assumptions are assumed.

1) All the capacitors are large enough. Thus, the voltage of the capacitors is considered as constant in one switching period.

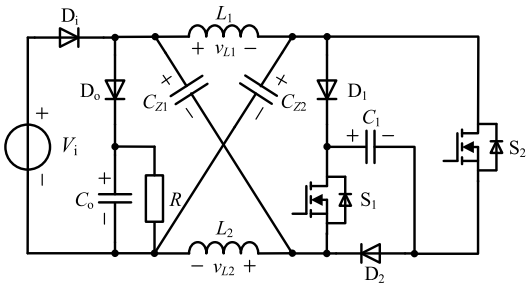


FIGURE 1. Circuit topology of the proposed converter.

2) The power devices are ideal, and the parasitic elements are neglected.
3) Considering the symmetries of the topologies, inductors L_1 and L_2 possess the same level of inductance.

A. CCM OPERATION

There are two operating modes in CCM operation. Fig. 3(a) shows some typical waveforms during CCM operation.

Mode 1 [t_0-t_1]: S_1, S_2 and D_o are turned on, diodes D_i, D_1 and D_2 are reverse biased by V_o-V_i, V_{C1} and V_{C1}, respectively. The current flow path is shown in Fig. 2(a). $L_1$is charged by C_{Z1} and C_1, L_2 is charged by C_{Z2} and C_1. Meanwhile, C_{Z1}, C_{Z2} and C_1 are connected in series to charge the load R and C_o. According to KVL, equations (1) and (2) are obtained.

$$\begin{cases} v_{L1} = V_{C1} + V_{CZ1} \\ v_{L2} = V_{C1} + V_{CZ2} \end{cases} \tag{1}$$

$$V_o = V_{C1} + V_{CZ1} + V_{CZ2} \tag{2}$$

Mode 2 [t_1-t_2]: The switches are turned off. Diodes D_i, D_1 and D_2 are turned on. D_o is reverse biased by V_o-V_i. The current flow path is shown in Fig. 2(b). C_{Z1} is charged by V_i and L_2, C_{Z2} is charged by V_i and L_1. Also, C_1 is charged by V_i, L_1 and L_2. Output voltage is maintained by C_o. According to KVL, the following relationships are obtained

$$\begin{cases} v_{L1} = V_i - V_{CZ2} \\ v_{L2} = V_i - V_{CZ1} \end{cases} \tag{3}$$

$$V_{C1} = V_{CZ1} + V_{CZ2} - V_i \tag{4}$$

B. DCM OPERATION

There are three operating modes in DCM operation. Fig. 3(b) shows some typical waveforms during DCM operation.

Mode 1 [t_0-t_1]: The equivalent circuit is the same as that of CCM operation. Equations (1) and (2) still apply at this stage. Assuming that $L_1 = L_2 = L$, the variation of the inductor current during this time interval can be calculated as

$$\begin{cases} \Delta i_{L1} = \dfrac{(V_{CZ1} + V_{C1})}{L} DT_S \\ \Delta i_{L2} = \dfrac{(V_{CZ2} + V_{C1})}{L} DT_S \end{cases} \tag{5}$$

Mode 2 [t_1-t_2]: The current flow path is the same as that of CCM operation. Equations (3) and (4) still apply at this stage. Mode 2 ends when the inductor current is decreased to zero at t_2.

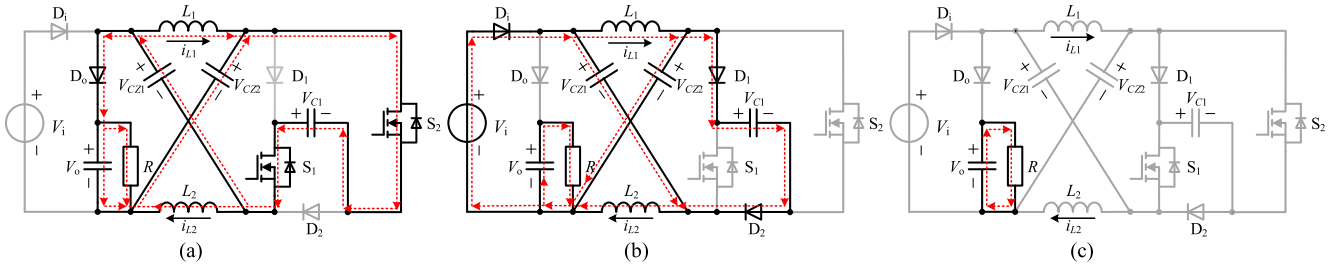


FIGURE 2. Current flow path of the proposed converter within each mode. (a) Mode 1 in CCM and DCM. (b) Mode 2 in CCM and DCM. (c) Mode 3 in DCM.

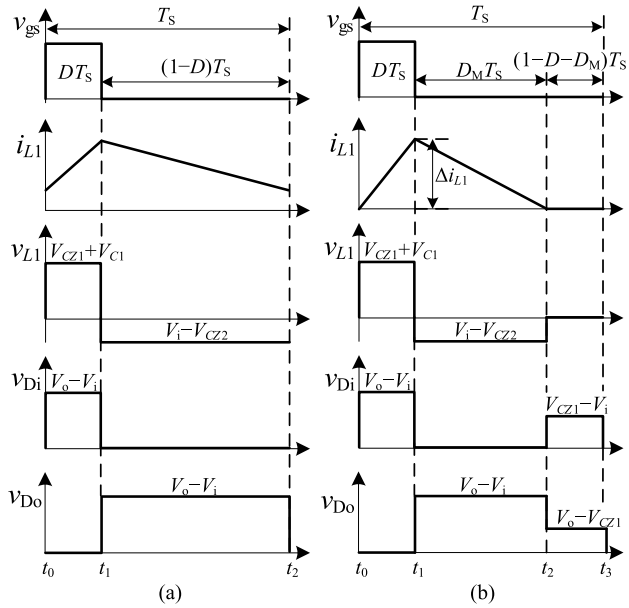


FIGURE 3. Theoretical waveforms of the proposed converter. (a) Typical waveforms in CCM. (b) Typical waveforms in DCM.

Mode 3 [t_2-t_3]: During this time interval, switches and all diodes are turned off. The output voltage is maintained by C_o. The equivalent circuit is shown in Fig. 2(c). This mode ends when switches are turned on at t_3, which is the beginning of the next switching period.

III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

A. CCM OPERATION

Assuming that $T_0 = DT_S$ is the interval of mode 1 in a switching cycle T_S, where D is the duty cycle of the switch, $T_1 = (1-D)T_S$ is the interval of mode 2 in a switching cycle T_S. By applying the voltage–second balance principle to the inductors, equations (6), (7) and (8) are formulated as

$$\int_0^{DT_S} (V_{C1} + V_{CZ1}) + \int_{DT_S}^{T_S} (V_i - V_{CZ2}) = 0 \tag{6}$$

$$\int_0^{DT_S} (V_{C1} + V_{CZ2}) + \int_{DT_S}^{T_S} (V_i - V_{CZ1}) = 0 \tag{7}$$

$$V_{CZ1} = V_{CZ2} \tag{8}$$

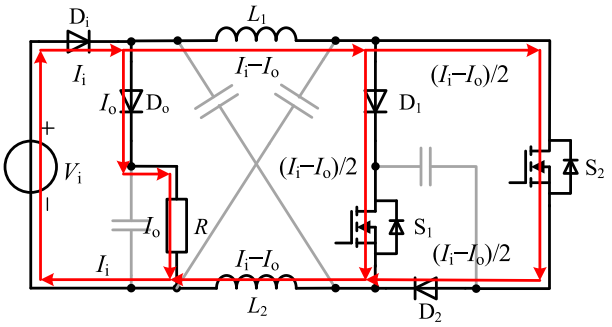


FIGURE 4. Average current equivalent circuit of the proposed converter.

Combine (6), (7) and (8) with (2), (4), the voltage across the capacitors and the voltage gain G are calculated by

$$V_{CZ1} = V_{CZ2} = \frac{1-2D}{1-4D} V_i \tag{9}$$

$$V_{C1} = \frac{1}{1-4D} V_i \tag{10}$$

$$G = \frac{V_o}{V_i} = \frac{3-4D}{1-4D} \tag{11}$$

The average currents of the input and output are expressed by I_i and I_o respectively, then the current transfer function of the proposed converter is given by

$$G_I = \frac{I_o}{I_i} = \frac{1-4D}{3-4D} \tag{12}$$

By applying the above-calculated voltage relationships in the steady state, the voltage stresses on the switch and diodes can be calculated. The following relationships show the voltage stresses on the diodes (cathode to anode) and switches (drain to source).

$$V_{S1} = V_{S2} = \frac{1}{1-4D} V_i \tag{13}$$

$$V_{D1} = V_{D2} = \frac{1}{1-4D} V_i \tag{14}$$

$$V_{Di} = V_{Do} = \frac{2}{1-4D} V_i \tag{15}$$

The average currents of the inductors are expressed by I_{L1}, and I_{L2}, respectively, the average currents of D_i, D_o, D_1 and D_2 are expressed by I_{Di}, I_{Do}, I_{D1} and I_{D2}, respectively. And the average currents of switches are expressed by I_{S1} and I_{S2}. According to the charge balance of the capacitors, Fig. 4 can be depicted. From Fig.4, the following equations

can be obtained.

$$I_{Di} = I_i \tag{16}$$
$$I_{Do} = I_o \tag{17}$$
$$I_{L1} = I_{L2} = I_i - I_o \tag{18}$$
$$I_{S1} = I_{S2} = I_{D1} = I_{D2} = \frac{I_i - I_o}{2} \tag{19}$$

B. DCM OPERATION

Assuming that $T_1 = DT_S$ is the interval of mode 1 in a switching cycle T_S. $T_2 = D_M T_S$ is the interval of mode 2. Then the time interval corresponding to mode 3 is $T_3 = (1 - D - D_M)T_S$. In terms of the voltage-second of the inductors in a whole switching cycle, the capacitor voltages, as well as the output voltage V_o, can be obtained from (1)-(4), as

$$V_{CZ1} = V_{CZ2} = \frac{D_M - D}{D_M - 3D} V_i \tag{20}$$
$$V_{C1} = \frac{D_M + D}{D_M - 3D} V_i \tag{21}$$
$$G = \frac{V_o}{V_i} = \frac{3D_M - D}{D_M - 3D} \tag{22}$$

According to the charging balance of the capacitors, the average currents of the inductors is given by (23). From Fig.3(b) and (5), the average current of the inductors can be rewritten as (24). Based on (22), D_M can be rewritten as (25)

$$I_{L1} = I_{L2} = \frac{2D_M + 2D}{D_M - 3D} \cdot \frac{V_o}{R} \tag{23}$$
$$I_{L1} = I_{L2} = \frac{D_M D\,(D_M + D)}{D_M - 3D} \cdot \frac{V_i T_S}{L} \tag{24}$$
$$D_M = \frac{D\,(3G - 1)}{G - 3} \tag{25}$$

From (23)-(25), the duty cycle D is derived as

$$D = \sqrt{\frac{2G\,(G - 3)}{3G - 1} \cdot \frac{L}{RT_S}} \tag{26}$$

Then, a dimensionless parameter is defined as

$$\tau = \frac{L}{RT_S} \tag{27}$$

Substituting (27) into (26), the voltage gain G is given by

$$G = \frac{\sqrt{9D^4 + 28\tau D^2 + 36\tau^2} + 3D^2 + 6\tau}{4\tau} \tag{28}$$

The curve of the voltage gain is shown in Fig. 5. When the proposed converter is operated in DCM operation, the voltage gain will increase as τ decreases.

C. EXTERNAL CHARACTERISTIC OF THE PROPOSED CONVERTER

If the converter is operating under the boundary condition of CCM and DCM. The voltage gain of DCM operation is

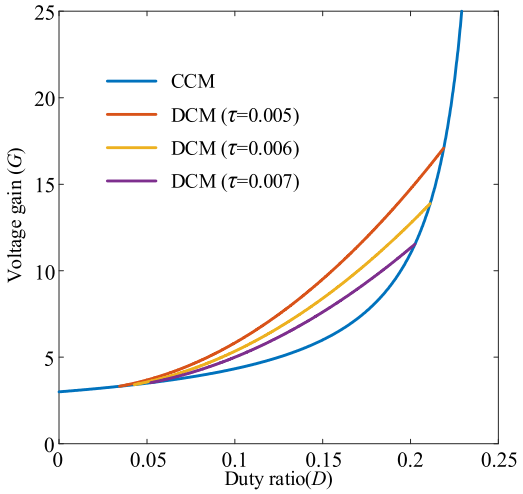


FIGURE 5. Voltage-gain versus duty ratio at DCM operation under various τ and at CCM operation.

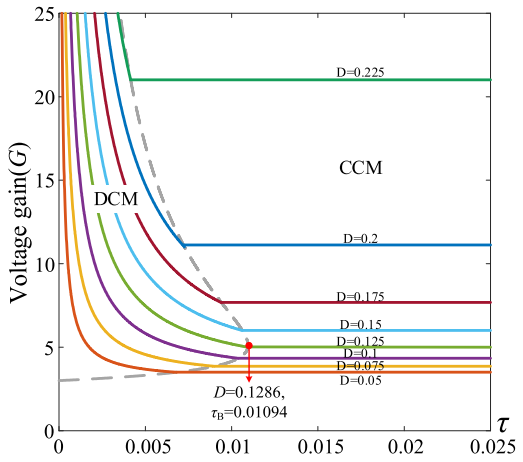


FIGURE 6. External characteristic of the proposed converter.

the same as that of CCM operation. According to (26), the boundary constant τ_B can be obtained as

$$\tau_B = \frac{(G - 3)\,(3G - 1)}{2G\,(4G - 4)^2} \tag{29}$$

Combine (29) with (28), the external characteristic of the proposed converter is depicted in Fig. 6. The proposed converter will be more likely to work in DCM operation when $D = 0.1286$.

IV. NONIDEAL ELEMENT ANALYSIS OF THE PROPOSED CONVERTER

The parasitic parameters of all elements are ignored in the above analysis. Actually, the losses of each component could influence the efficiency and boost ability of the proposed converter. In this section, the effect of nonideal element is analyzed, and the efficiency and nonideal voltage gain expressions are also calculated.

Assuming that the equivalent series resistors of the capacitors are r_C, the forward voltage drops of the diodes are V_D and V_{D1}, the on-resistances of the switches are r_S, the dc

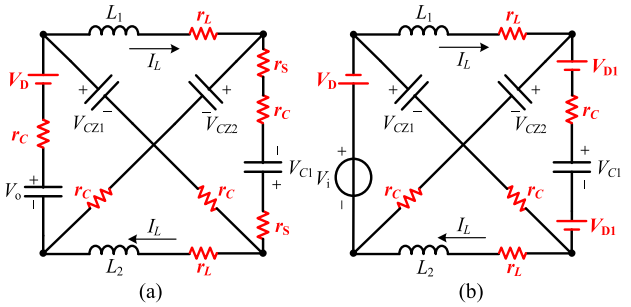


FIGURE 7. Equivalent current loops when considering the parasitic parameters. (a) Switches are turned on. (b) Switches are turned off.

resistances of the inductors are r_L, Fig. 7 shows the equivalent current loops of the proposed converter working in CCM operation.

A. POWER LOSS OF THE PROPOSED CONVERTER

The conduction loss of the power switch is mainly related to the on-resistance and the root-mean-square (RMS) value of the current. The current through the switch can be expressed by

$$i_S = \begin{cases} 2I_i - 2I_o + \dfrac{I_o}{D} & 0 \le t \le DT_S \\ 0 & DT_S \le t \le T_S \end{cases} \tag{30}$$

According to (12) and (30), the conduction loss of the switch can be calculated as

$$P_{rs} = \frac{2I_o^2 r_S}{D^2 (1-4D)^2} = P_o \cdot \frac{2r_S}{D^2 (1-4D)^2 R} \tag{31}$$

The switch-on loss can be calculated by linearizing the currents and voltages of the switches when they are changing their states [30], as

$$P_{son} = f_s \int_0^{t_{on}} \frac{I_S t}{t_{on}} \times \frac{V_S (t_{on} - t)}{t_{on}} dt = \frac{1}{6} f_s V_S I_S t_{on} \tag{32}$$

where the V_S is the voltage stress on the switch before it is turned on, I_S is the current through the switch after it is turned on, f_S is the switching frequency, t_{on} is the turn-on delay of the switch. Similarly, the switch-off loss for the switch can be calculated by

$$P_{soff} = \frac{1}{6} V_S I_S t_{off} f_S \tag{33}$$

where t_{off} is the turn-off delay of the switch. Consequently, the switching loss can be obtained by

$$P_{ss} = 2\left(P_{son} + P_{soff}\right) = P_o \cdot \frac{f_S \left(t_{on} + t_{off}\right)}{3\,(3-4D)\,D\,(1-4D)} \tag{34}$$

Therefore, the total power loss in the main switches can be calculated as follows

$$P_S = P_o \cdot \left(\frac{2r_S}{D^2 (1-4D)^2 R} + \frac{f_S \left(t_{on} + t_{off}\right)}{3D\,(3-4D)\,(1-4D)} \right) \tag{35}$$

The losses of the diodes depend on the magnitude of the current flow and their forward voltage drops. Therefore, the currents of diode D_1 and diode D_2 can be expressed by

$$i_{D1} = i_{D2} = \begin{cases} 0 & 0 \le t \le DT_S \\ \dfrac{I_i - I_o}{2\,(1-D)} & DT_S \le t \le T_S \end{cases} \tag{36}$$

The power loss associated with the forward voltage drop V_{D1} is expressed by

$$P_{D1} = P_{D2} = \frac{1}{1-4D} I_o V_{D1} \tag{37}$$

Similarly, the power loss of diodes D_i and D_o can be calculated as

$$P_{Di} = \frac{3-4D}{1-4D} I_o V_D \tag{38}$$

$$P_{Do} = I_o V_D \tag{39}$$

The total power loss in the diodes is obtained by

$$P_D = \frac{P_o}{V_o} \cdot \left(\frac{4-8D}{1-4D} V_D + \frac{2}{1-4D} V_{D1} \right) \tag{40}$$

The main loss of the inductors in the PWM converter is the conduction loss. According to (18), the average currents of the inductors are given by

$$I_{L1} = I_{L2} = \frac{2}{1-4D} I_o \tag{41}$$

The power losses of inductors can be calculated as

$$P_L = P_{L1} + P_{L2} = P_o \cdot \frac{8r_L}{(1-4D)^2 R} \tag{42}$$

The power losses of the capacitors depend on the equivalent series resistance of the capacitors and root-mean-square (RMS) value of the currents. According to the charging balance of the capacitors, the currents passing through the capacitors can be approximated by

$$i_{CZ1,CZ2} = \begin{cases} -\dfrac{1-2D}{D\,(1-4D)} I_o & 0 \le t \le DT_S \\ \dfrac{1-2D}{(1-D)\,(1-4D)} I_o & DT_S \le t \le T_S \end{cases} \tag{43}$$

$$i_{C1} = \begin{cases} -\dfrac{I_o}{D\,(1-4D)} & 0 \le t \le DT_S \\ \dfrac{I_o}{(1-D)\,(1-4D)} & DT_S \le t \le T_S \end{cases} \tag{44}$$

$$i_{Co} = \begin{cases} -\dfrac{1-D}{D} I_o & 0 \le t \le DT_S \\ I_o & DT_S \le t \le T_S \end{cases} \tag{45}$$

From (43)-(45), the power losses of the capacitors can be obtained, as

$$P_{CZ1} = P_{CZ2} = P_o \cdot \frac{(1-2D)^2 r_C}{D\,(1-D)\,(1-4D)^2 R} \tag{46}$$

$$P_{C1} = P_o \cdot \frac{r_C}{D\,(1-D)\,(1-4D)^2 R} \tag{47}$$

$$P_{Co} = P_o \cdot \frac{(1-D)\,r_C}{DR} \tag{48}$$

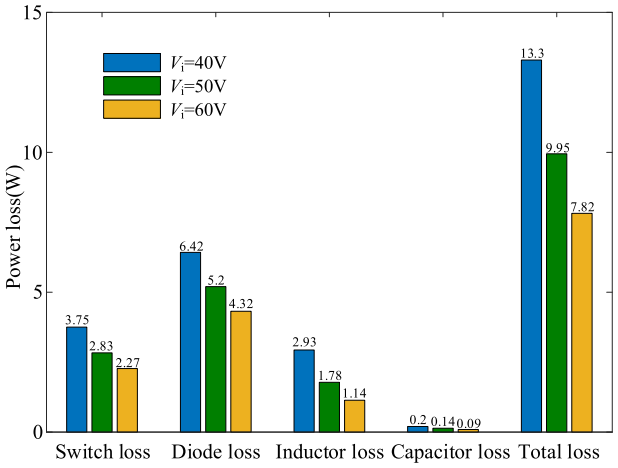


FIGURE 8. Calculated power loss of the proposed converter under $P_o = 200W$ and $V_o = 400V$.

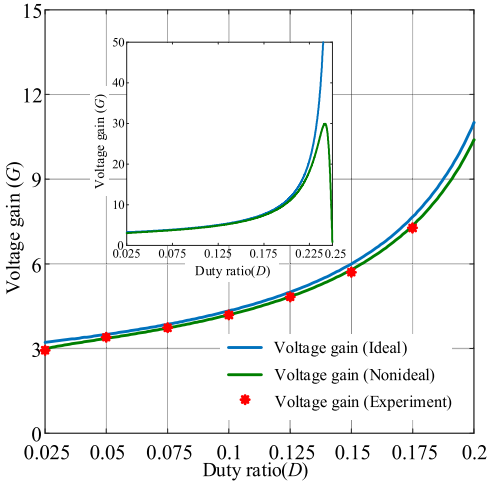


FIGURE 9. Voltage gain under different conditions.

From (46)-(48), the total power losses of the capacitors in the proposed converter can be obtained, as

$$P_C = P_o \cdot \frac{\left[(1-2D)^2 + 1 + (1-D)^2 (1-4D)^2\right] r_C}{D(1-D)(1-4D)^2 R} \tag{49}$$

We assume that the proposed converter is operated in CCM operation, the power loss considering the nominal specifications and selected components (shown in table 4) are calculated, which is shown in Fig. 8. It can be seen the diode loss accounts for the greatest proportion of the power loss, followed by the switch loss and inductor loss. This analysis proves that the overall efficiency can be improved by optimizing parasitic parameters.

B. EFFICIENCY AND NONIDEAL VOLTAGE GAIN OF THE PROPOSED CONVERTER

The proposed converter efficiency η is calculated as

$$\begin{aligned}\eta &= \frac{P_o}{P_i} = \frac{P_o}{P_S + P_L + P_C + P_D + P_o} = \frac{1}{1+\lambda} \\ \lambda &= \frac{2r_S}{D^2(1-4D)^2 R} + \frac{f_S\left(t_{on} + t_{off}\right)}{3D(3-4D)(1-4D)} \\ &\quad + \frac{4-8D}{1-4D} \cdot \frac{V_D}{V_o} + \frac{2}{1-4D} \cdot \frac{V_{D1}}{V_o} + \frac{8r_L}{(1-4D)^2 R} \\ &\quad + \frac{\left[(1-2D)^2 + 1 + (1-D)^2 (1-4D)^2\right] r_C}{D(1-D)(1-4D)^2 R}\end{aligned} \tag{50}$$

The voltage conversion ratio considering the parasitic parameters will be decreased unexpectedly. But the current transfer function is true for ideal and nonideal conditions. Thus, the nonideal voltage gain can be calculated as

$$G_{(nonideal)} = \frac{V_o}{V_i} = \frac{I_i}{I_o}\eta = \frac{3-4D}{1-4D} \cdot \frac{1}{\lambda + 1} \tag{51}$$

The voltage gain considering the nominal specifications and selected components is shown in Fig.9. It can be seen the proposed converter can maintain a high boost capacity when G < 20, and the measured voltage gain for experiment match well with the theoretical analysis.

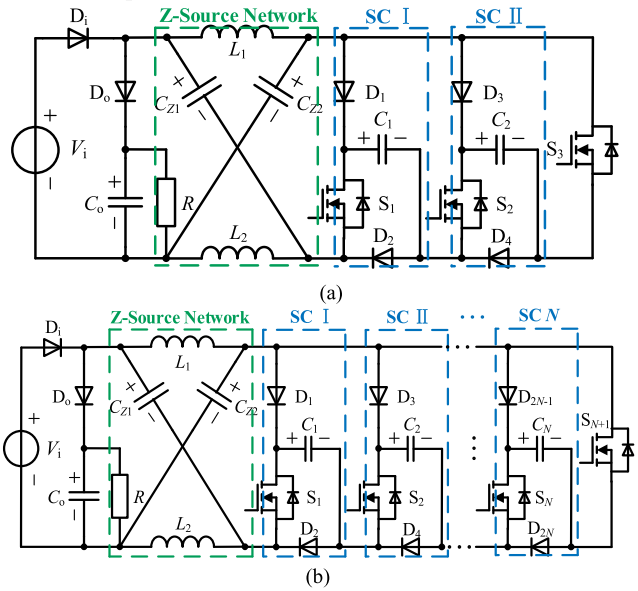


FIGURE 10. Cascaded topology. (a) Proposed converter with two switched-capacitor cells. (b) Proposed converter with N switched-capacitor cells.

V. EXTENSION OF THE PROPOSED CONVERTER

The cascaded topology is proposed in this section, which is obtained by cascading the multiple switched-capacitor (SC) cells, as shown in Fig.10. It can be seen that the advantage of common ground for input and output is still retained. Similarly, some necessary relationships can be obtained by using the same analytical method present in Section III, which is summarized in table 1. Since there are 4 diodes, 4 capacitors, 2 switches and 2 inductors in the basic structure, it is expected that there are $2N+2$ diodes, $N+2$ capacitors, $N+1$ switches

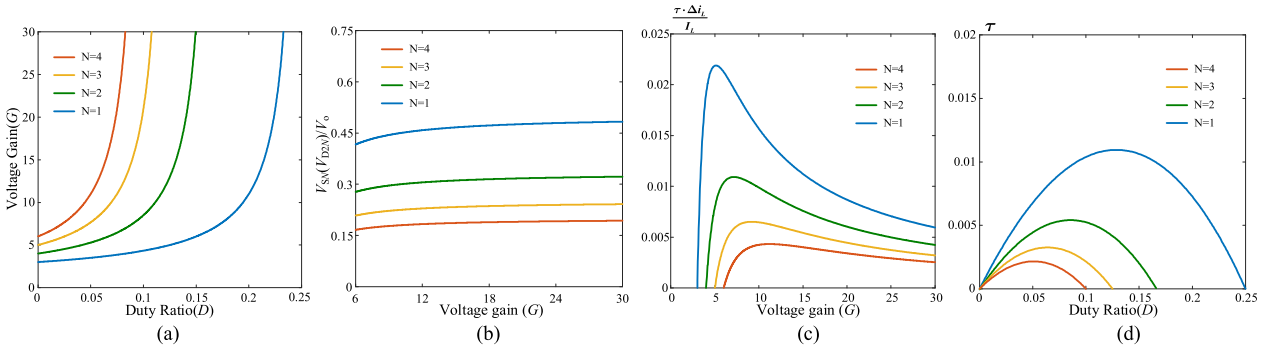


FIGURE 11. Characteristics of the cascaded structure. (a) Voltage gain. (b) Voltage stress on semiconductors. (c) Current ripple of the inductors. (d) Boundary conditions.

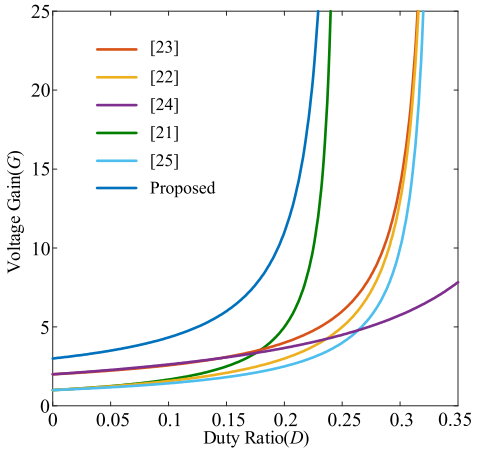


FIGURE 12. Voltage gain comparison between the proposed and other quasi-Z-source based dc-dc converters.

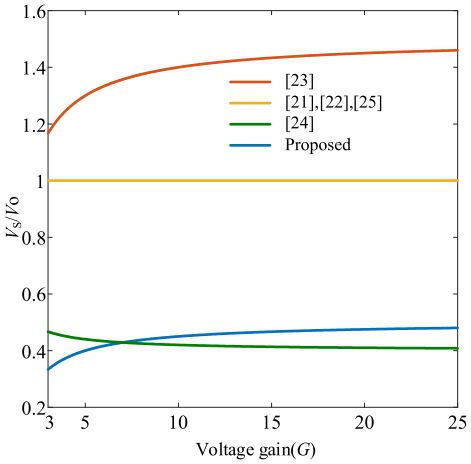


FIGURE 13. Voltage stress comparison between the proposed and other quasi-Z-source based dc-dc converters.

and 2 inductors in the topology with N switched-capacitor cells.

According to table 1, the average current of diodes and switches is decreased when increasing the number of SC cells. To give a graphical presentation, Fig. 11 is depicted, in which voltage gain, device voltage stress, current ripple of the inductors and boundary conditions are present to illustrate the characteristics of the cascaded topology. It can be seen even a small duty ratio of the switch will achieve a high voltage gain, and the current ripple of the inductors as well as the voltage stresses of most switches and diodes are reduced under the same output condition. What's more, the proposed converter will be less likely to work in DCM operation when adding the extra stages.

VI. COMPARISON

A comprehensive comparison between the proposed and other structures is provided in this section. The comparison is performed on their boost factors, device voltage stress, the number of devices and so on, as shown in table 2.

Boost ability is an important index to evaluate converter performance. To provide a graphical comparison of the voltage gains, Fig. 12 is illustrated. The proposed converter can achieve the highest voltage gain under the same duty ratio. Moreover, fewer capacitors and inductors are employed, making smaller size and higher power density.

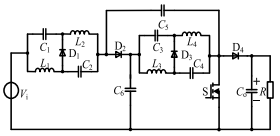
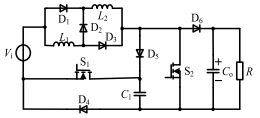
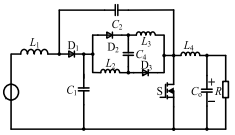
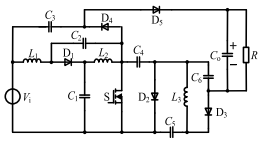
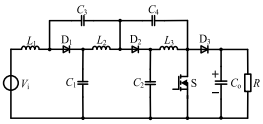
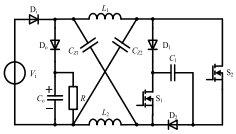
Another issue is the voltage stresses on the semiconductors. It can be seen from Fig. 13 that although the converter proposed in [21], [22] and [25] can achieve high voltage gain in theory, the device voltage stress is equal to the output voltage. And in [23], it exceeds the output voltage. The extremely high voltage stress will increase the probability of failure. Also, devices with high voltage ratings tend to have poor performance, which will lead to high cost, high power loss and low efficiency. It can be seen the proposed converter can provide the same output voltage with lower device voltage stress, so devices with low on-state loss can be employed to improve the overall efficiency.

In addition, a common ground for input and output are required in some applications. Otherwise, the lack of common ground may generate common-mode leakage current, which will decrease system reliability and lead to serious electromagnetic interference problem [30]. The proposed converter can provide a common ground for input and output, as shown in Fig. 14. Therefore, the common-mode leakage current can be greatly reduced by short-circuiting capacitor C_{GND}. Compared with the converters proposed in [22] and [24], the proposed converter is more competitive in this respect.

TABLE 1. Performance index of the proposed converter with N SC cells.

Index	Value	Index	Value
Voltage gain in CCM	$G=\frac{N+2-(2N+2)D}{1-(2N+2)D}$	V_{D1}, $V_{D3}...V_{D(2N-1)}$	$\frac{N+1-(n+1)/2}{1-(2N+2)D}V_i$ $[n(subscript)=1,3,5,...2N-1]$
V_{CZ1}, V_{CZ2}	$\frac{1-(N+1)D}{1-(2N+2)D}V_i$	I_{D1}, I_{D3} ...$I_{D(2N-1)}$	$\frac{I_i-I_o}{N+1}$
V_{C1}, $V_{C2}...V_{CN}$	$\frac{1}{1-(2N+2)D}V_i$	V_{D2}, $V_{D4}...V_{D(2N)}$	$\frac{1}{1-(2N+2)D}V_i$
V_{Di}, V_{Do}	$\frac{N+1}{1-(2N+2)D}V_i$	I_{D2}, I_{D4} ...$I_{D(2N)}$	$\left(N+1-\frac{n}{2}\right)\frac{I_i-I_o}{N+1}$ $[n(subscript)=2,4,6,...2N]$
V_{S1}, $V_{S2}...V_{SN}$	$\frac{1}{1-(2N+2)D}V_i$	Current ripple of the inductor in CCM	$\Delta i_L=\frac{(N+1)(1-D)V_iDT_S}{(1-2ND-2D)L}$
I_{S1}, $I_{S2}...I_{SN}$	$\frac{I_i-I_o}{N+1}$	Boundary conditions between CCM and DCM	$\tau_B=\frac{D(1-D)(1-2D-2ND)}{2(N+2-2D-2ND)}$

TABLE 2. Comparison between the proposed and other existing high step-up dc-dc converters.

Ref.	Structures	Voltage gain	Components	Voltage stresses on switches and diodes	Advantages and disadvantages
[21]		$G=\frac{1}{1-4D}$	4 Diodes 1 Switch 4 Inductors 7 Capacitors	$V_S=V_o$ $V_{D1,D2,D3,D4}=V_o$	√ Improved voltage gain √ Common ground for input and output ○ Relatively high voltage stress on components × Discontinuous input current × Many passive components
[22]		$G=\frac{1+D}{1-3D}$	6 Diodes 2 Switch 2 Inductors 2 Capacitors	$V_{S1,S2,D4,D5,D6}=V_o$ $V_{D1,D3}=\frac{G-1}{2G}V_o$ $V_{D2}=\frac{G+1}{G}V_o$	√ Improved voltage gain √ Reduced passive components ○ Relatively high voltage stress on components × Discontinuous input current × Lack of common ground for input and output
[23]		$G=\frac{2-2D}{1-3D}$	3 Diodes 1 Switch 4 Inductors 4 Capacitors	$V_S=\frac{3G-2}{2G}V_o$ $V_{D1}=\frac{3G-2}{2G}V_o$ $V_{D2,D3}=\frac{G}{2}V_o$	√ Improved voltage gain √ Common ground for input and output √ Smoother output voltage √ Continuous input current ○ Reduced passive components × Extremely high voltage stress on components
[24]		$G=\frac{2+D}{1-2D}$	5 Diodes 1 Switch 3 inductors 7 Capacitors	$V_S=\frac{2G+1}{5G}V_o$ $V_{D1,D2,D3}=\frac{2G+1}{5G}V_o$ $V_{D4,D5}=\frac{2G+1}{5G}V_o$	√ Low voltage stresses on components √ Extra stages can be added to get higher voltage gain ○ Not a significant improvement in voltage gain × Lack of common ground for input and output × Many passive components × Discontinuous input current
[25]		$G=\frac{1}{1-3D}$	3 Diodes 1 Switch 3 Inductors 5 Capacitors	$V_S=V_o$ $V_{D1,D2,D3}=V_o$	√ Improved voltage gain √ Extra stages can be added to get higher voltage gain √ Common ground for input and output √ Continuous input current ○ Relatively high voltage stress on components ○ Reduced passive components
Fig.2		$G=\frac{3-4D}{1-4D}$	4 Diodes 2 Switches 2 Inductors 4 Capacitors	$V_{S1,S2}=\frac{G-1}{2G}V_o$ $V_{D1,D2}=\frac{G-1}{2G}V_o$ $V_{Di,Do}=\frac{G-1}{G}V_o$	√ Improved voltage gain √ Extra stages can be added to get higher voltage gain √ Common ground for input and output √ Reduced passive components √ Low voltage stresses on components × Initial current spike on D_i, D_o,S_1 and S_2. × Discontinuous input current

The drawback of the proposed converter should also be pointed out. The main drawback is that the input current of the proposed converter is discontinuous, so a relatively large input filter is required. Another drawback is that inrush

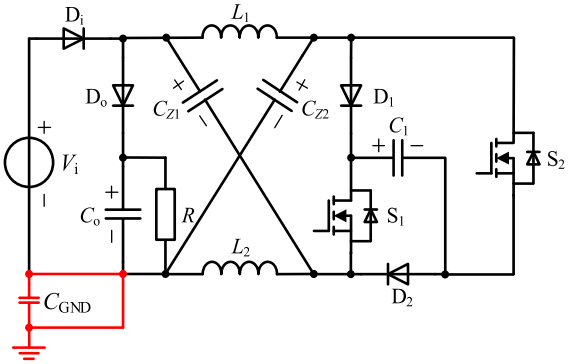


FIGURE 14. Equivalent circuit considering parasitic capacitance to ground.

current exists at startup, which may cause damage to the power device.

VII. SIMULATION AND EXPERIMENT VERIFICATIONS

A. DESIGN OF INDUCTANCE AND CAPACITANCE

We assume that the maximum allowed current ripple of the inductance is $x_L\%$ and the proposed converter works in CCM operation. Considering the cascaded topologies, the inductors L_1 and L_2 can be designed as

$$L_1 = L_2 = \frac{v_L dt}{di_L} = \frac{D\,(1-D)\,(1-2D-2ND)\,RT_S}{(N+2-2ND-2D)\,x_L\%} \tag{52}$$

where $dt = DT_S$ is the time interval when the switches are turned on, and $di_L = x_L\%I_L$ is the variation of the inductor current during this time interval. If the converter is designed to operate in DCM, the following equation can be obtained.

$$L_1 = L_2 < \frac{D\,(1-D)\,(1-2D-2ND)\,RT_S}{2\,(N+2-2D-2ND)} \tag{53}$$

Then, taking the $x_C\%$ peak-to-peak capacitor voltage ripple into consideration, the capacitance C_o can be designed as

$$C_o = i_C \frac{dt}{dv_C} = \frac{(1-D)\,T_S}{x_C\%R} \tag{54}$$

where $dt = DT_S$ is the time interval when the switches are turned off, and $dv_C = x_C\%V_C$ is the voltage ripple of C_o. Similarly, other capacitors can be designed as

$$C_{Z1} = C_{Z2} = C_1 = \cdots C_N = \frac{(N+2-2ND-2D)\,T_S}{x_C\%\,(1-2ND-2D)\,R} \tag{55}$$

B. DESIGN GUIDELINE FOR CONTROLLERS

A small signal model is established to study the dynamic characteristics of the converter and provide reference for the design of the controller. The small signal model is derived from the average state-space model. The inductor current i_{L1}, i_{L2} and capacitor voltage v_{C1}, v_{C2}, v_{C1}, and v_{Co} are selected as the basic variables. Since the capacitors are charged and discharged in parallel, the equivalent series resistance (ESR) of the capacitors cannot be ignored in the following analysis. We assume the ESR of the capacitors is r_C and the ESR of the inductance is r_L. The generalized state-space equations for CCM operation are given by

$$\begin{aligned} \frac{d\boldsymbol{x}}{dt} &= \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \\ \boldsymbol{x} &= \begin{bmatrix} i_{L1} & i_{L2} & v_{CZ1} & v_{CZ2} & v_{C1} & v_{Co} \end{bmatrix}^{\mathrm{T}} \\ \boldsymbol{u} &= [v_i]^{\mathrm{T}} \end{aligned} \tag{56}$$

In mode 1, equation (57) can be obtained.

$$\begin{cases} i_{CZ2} = i_{L1} + i_{CZ1} - i_{L2} \\ i_{C1} = i_{CZ1} - i_{L2} \\ i_{Co} = -i_{CZ1} - i_{L1} - \dfrac{v_{Co} + r_C i_{Co}}{R} \\ v_{Co} + r_C i_{Co} - v_{CZ2} - i_{CZ2} r_C \\ \qquad = v_{CZ1} + v_{C1} + (i_{CZ1} + i_{C1})\, r_C \end{cases} \tag{57}$$

Based on (57), equation (58) can be derived, as shown at the bottom of the next page. Similarly, in mode 2, equations (59) can be obtained.

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = -\left(\dfrac{2}{3}r_C + r_L\right) i_{L1} + \dfrac{1}{3} r_C i_{L2} + \dfrac{1}{3} v_{CZ1} \\ \qquad - \dfrac{2}{3} v_{CZ2} - \dfrac{1}{3} v_{C1} + \dfrac{2}{3} v_i \\ L_2 \dfrac{di_{L2}}{dt} = \dfrac{1}{3} r_C i_{L1} - \left(\dfrac{2}{3}r_C + r_L\right) i_{L2} - \dfrac{2}{3} v_{CZ1} \\ \qquad + \dfrac{1}{3} v_{CZ2} - \dfrac{1}{3} v_{C1} + \dfrac{2}{3} v_i \\ C_{Z1} \dfrac{dv_{CZ1}}{dt} = -\dfrac{1}{3} i_{L1} + \dfrac{2}{3} i_{L2} - \dfrac{1}{3r_C} v_{CZ1} - \dfrac{1}{3r_C} v_{CZ2} \\ \qquad + \dfrac{1}{3r_C} v_{C1} + \dfrac{1}{3r_C} v_i \\ C_{Z2} \dfrac{dv_{CZ2}}{dt} = \dfrac{2}{3} i_{L1} - \dfrac{1}{3} i_{L2} - \dfrac{1}{3r_C} v_{CZ1} - \dfrac{1}{3r_C} v_{CZ2} \\ \qquad + \dfrac{1}{3r_C} v_{C1} + \dfrac{1}{3r_C} v_i \\ C_1 \dfrac{dv_{C1}}{dt} = \dfrac{1}{3} i_{L1} + \dfrac{1}{3} i_{L2} + \dfrac{1}{3r_C} v_{CZ1} + \dfrac{1}{3r_C} v_{CZ2} \\ \qquad - \dfrac{1}{3r_C} v_{C1} - \dfrac{1}{3r_C} v_i \\ C_o \dfrac{dv_{Co}}{dt} = -\dfrac{v_{Co}}{R + r_C} \end{cases} \tag{59}$$

The control to output capacitor voltage v_{Co} open-loop transfer function by considering $\widehat{v_i} = 0$ is derived, the obtained values of the poles are $P_1 = -20477$, $P_2 = -1058$, P_3, $P_4 = -3.06 \pm 237\mathrm{i}$, and the zeros are obtained as $Z_1 = -73009$, $Z_2 = -2732$, $Z_3 = 2057$. The corresponding Bode plot is shown in Fig. 15. The above analysis proves that the system is a non-minimum phase system, which is similar to the traditional Boost converter and Buck-Boost converter. Besides, all poles are located on the left half of the S-domain, so the proposed converter is proved to be stable.

C. SIMULATION RESULTS

A lossless model was established in PSIM to examine the voltage gain and boundary conditions of CCM and DCM. Subsequently, a principle prototype was established in the

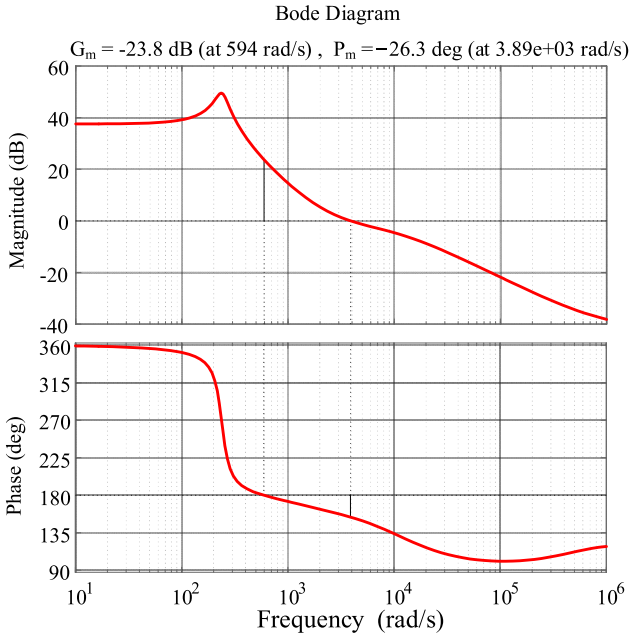


FIGURE 15. Open-loop Bode diagram from control to output voltage.

laboratory to verify theoretical analysis and boosting capabilities. The selected parameters are shown in table 3. And the principle prototype is shown in Fig. 17.

According to the boundary conditions (equation (29)), it can be inferred that under the selected parameters, the converter will first work in CCM and then in DCM as the inductance value decreases. We assume that the operational duty cycle $D = 0.1$ and the load resistance $R = 800\Omega$, if the proposed converter is operated under boundary conditions, the corresponding boundary constant τ_B and inductance value L_B are calculated as $\tau_B = 0.0104$ and $L_B = 332\mu$H.

Fig. 16(a) shows the typical simulation waveforms with $L = 1$mH. It is clear that the proposed converter works in CCM operation, and the voltage gain is consistent with the theoretical analysis and is only related to the duty cycle D.

Fig. 16(b) shows the typical simulation waveforms with $L = 332\mu$H. The simulation results show that the average current of the inductor is equal to half of its current ripple and the converter is operated under the boundary condition of CCM and DCM.

Fig. 16(c) shows the typical simulation waveforms with $L = 100\mu$H. It can be seen the proposed converter is operated in DCM operation, and the dimensionless constant τ is calculated as $\tau = 0.00313$. According to (28), the voltage gain can be calculated as $G_{DCM} = 7.589$. It can be seen the simulation results match well with the theoretical analysis. Consequently, the correctness of the theoretical analysis has been verified.

D. EXPERIMENT RESULTS

An experimental prototype was built to verify the theoretical analysis and the boosting capability of the proposed converter. The parameters for experiment are shown in table 3.

Fig. 18 shows some typical waveforms in CCM operation when $V_i = 40$V. The experimental duty cycle is 0.197, which is basically in line with the theoretical calculation value($D \approx 0.194$). The voltage across C_{Z1} is 106V, the

$$
\begin{cases}
L_1\dfrac{di_{L1}}{dt} = -\left(r_L + \dfrac{(4R+2r_C)\,r_C}{4R+3r_C}\right)i_{L1} + \dfrac{r_C^2}{4R+3r_C}i_{L2} + \dfrac{2R+r_C}{4R+3r_C}v_{CZ1} - \dfrac{2R+2r_C}{4R+3r_C}v_{CZ2} + \dfrac{2R+r_C}{4R+3r_C}v_{C1} \\
\qquad + \dfrac{2R}{4R+3r_C}v_{Co} \\
L_2\dfrac{di_{L2}}{dt} = \dfrac{r_C^2}{4R+3r_C}i_{L1} - \left(r_L + \dfrac{(4R+2r_C)\,r_c}{4R+3r_C}\right)i_{L2} - \dfrac{2R+2r_C}{4R+3r_C}v_{CZ1} + \dfrac{2R+r_C}{4R+3r_C}v_{CZ2} + \dfrac{2R+r_C}{4R+3r_C}v_{C1} \\
\qquad + \dfrac{2R}{4R+3r_C}v_{Co} \\
C_{Z1}\dfrac{dv_{CZ1}}{dt} = -\dfrac{2R+r_C}{4R+3r_C}i_{L1} + \dfrac{2R+2r_C}{4R+3r_C}i_{L2} - \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{CZ1} - \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{CZ2} - \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{C1} \\
\qquad + \dfrac{R}{(4R+3r_C)\,r_C}v_{Co} \\
C_{Z2}\dfrac{dv_{CZ2}}{dt} = \dfrac{2R+2r_C}{4R+3r_C}i_{L1} - \dfrac{2R+r_C}{4R+3r_C}i_{L2} - \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{CZ1} - \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{CZ2} - \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{C1} \\
\qquad + \dfrac{R}{(4R+3r_C)\,r_C}v_{Co} \\
C_1\dfrac{dv_{C1}}{dt} = -\dfrac{2R+r_C}{4R+3r_C}i_{L1} - \dfrac{2R+r_C}{4R+3r_C}i_{L2} - \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{CZ1} - \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{CZ2} - \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{C1} \\
\qquad + \dfrac{R}{(4R+3r_C)\,r_C}v_{Co} \\
C_o\dfrac{dv_{Co}}{dt} = -\dfrac{2R+2r_C}{4R+3r_C}i_{L1} - \dfrac{2R+2r_C}{4R+3r_C}i_{L2} + \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{CZ1} + \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{CZ2} + \dfrac{R+r_C}{(4R+3r_C)\,r_C}v_{C1} \\
\qquad - \dfrac{R^2+5Rr_C+3r_C^2}{(4R+3r_C)\,(R+r_C)\,r_C}v_{Co}
\end{cases}
\tag{58}
$$

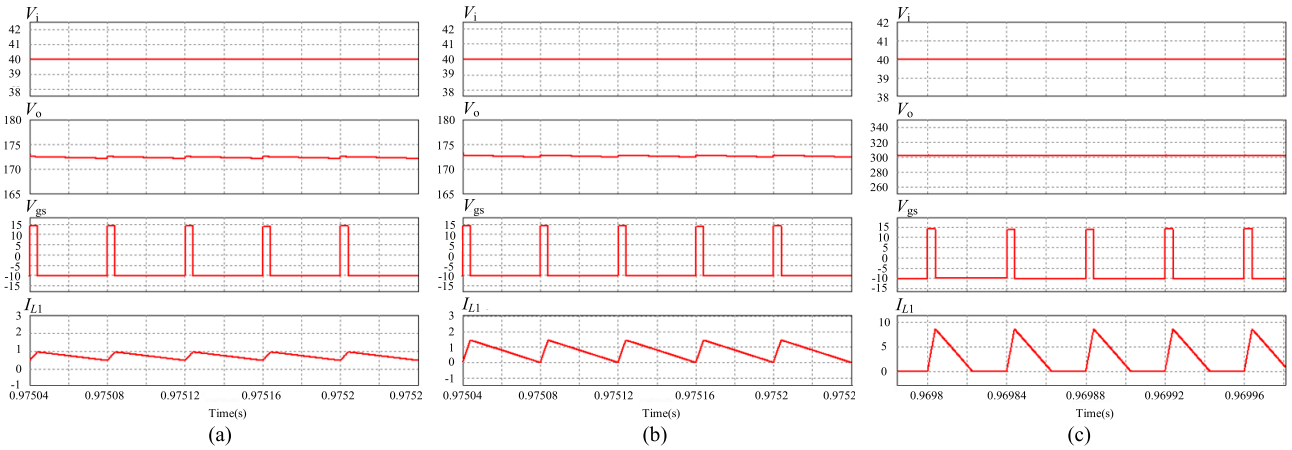


FIGURE 16. Simulation results of the proposed converter with $V_i = 40V$.

TABLE 3. Specifications of devices for simulation and experiment.

Parameter	Value/Part Number
Input voltage V_i	40V-60V
Maximum output voltage V_o	400V
Maximum output power	200W
Switching frequency f_s	25kHZ
MOSFET S_1/S_2	SUG90090E
Diodes D_i/D_o	DPG60C400HB
Diodes D_1/D_2	APT60S20BG
Capacitors $C_{Z1}/C_{Z2}/C_1/C_o$	22μF
Inductors L_1/L_2	1mH (CCM)/100μH (DCM)

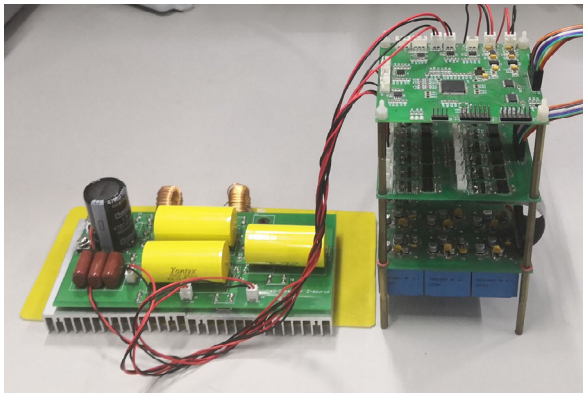


FIGURE 17. Principle prototype and its control circuit.

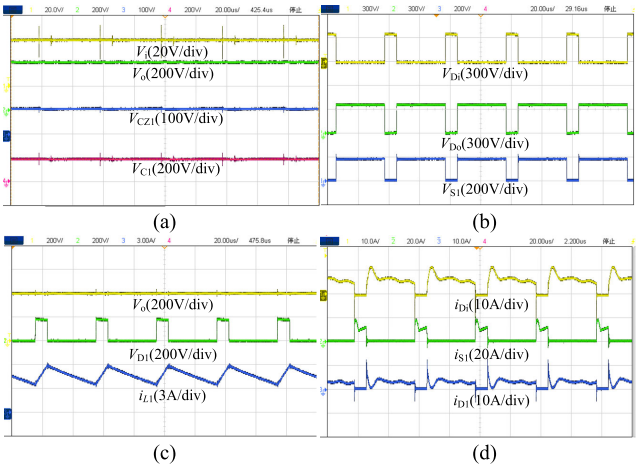


FIGURE 18. Experiment results of the proposed converter with $V_i = 40V$ in CCM operation. (a)Input voltage V_i, output voltage V_o, capacitor voltage V_{CZ1} and V_{C1}. (b) Voltage stresses on power semiconductors. V_{Di}. V_{Do}, V_{S1}. (c) V_o, V_{D1}, i_{L1}. (d) Current of diodes and switch, i_{Di}, i_{S1}, i_{D1}.

TABLE 4. Voltage gain and efficiency of CCM and DCM.

Duty ratio	Data category	CCM operation	DCM operation
0.05	Voltage gain	3.22	3.63
	Efficiency	92.0%	88.5%
0.075	Voltage gain	3.58	4.98
	Efficiency	92.8%	90%
0.1	Voltage gain	4.03	6.77
	Efficiency	93.2%	89.2%

voltage across C_1 is 188V, the voltage stresses across switch S and diodes D_i, D_o and D_1 are 188V, 360V, 360V and 188V, respectively. The current stresses of the power semiconductors are shown in Fig.18(d), the average current of D_i, S_1, and D_1 are 5.27A, 2.33A, and 2.39A respectively. Besides, the experiment results for $V_i = 60V$ are shown in Fig.19. Considering the power loss of the converter, the theoretical analysis is proved to be correct.

Fig. 20 and Fig. 21 show the typical voltage and current waveforms in DCM operation. It can be seen the proposed converter has three modes in each high frequency cycle. In mode 3, the inductor current drops to zero. In addition, the inductor current has a relatively low sinusoidal pulsation at this mode, which is caused by the resonance between the inductors and the junction capacitance of the power semiconductors. It is worth mentioning that this resonance will not occur in either mode 1 or mode 2. Because it is suppressed by a complete capacitor loop in these two modes.

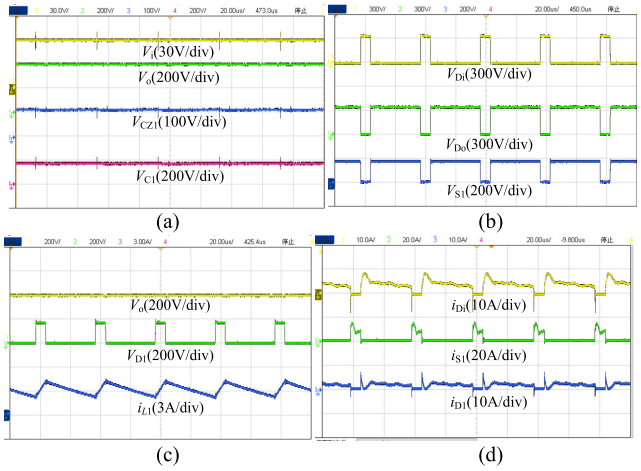


FIGURE 19. Experiment results of the proposed converter with $V_i = 60$V in CCM operation. (a) Input voltage V_i, output voltage V_o, capacitor voltage V_{CZ1} and V_{C1}. (b) Voltage stresses on power semiconductors. V_{Di}. V_{Do}, V_{S1}. (c) V_o, V_{D1}, i_{L1}. (d) Current of diodes and switch, i_{Di}, i_{S1}, i_{D1}.

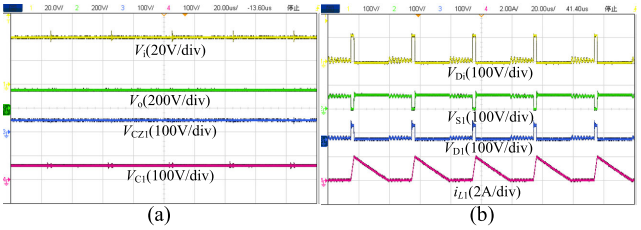


FIGURE 20. Experiment results of the proposed converter with $D = 0.05$ in DCM operation. (a)Input voltage V_i, output voltage V_o, capacitor voltage V_{CZ1} and V_{C1}. (b) V_{Di}. V_{S1}, V_{D1}, and i_{L1}.

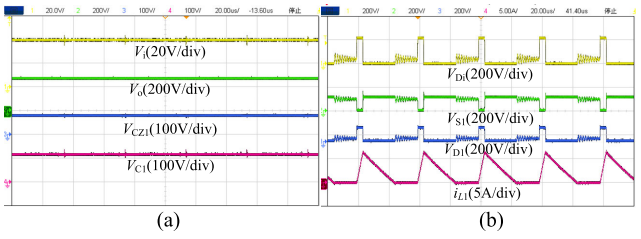


FIGURE 21. Experiment results of the proposed converter with $D = 0.1$ in DCM operation. (a) Input voltage V_i, output voltage V_o, capacitor voltage V_{CZ1} and V_{C1}. (b) V_{Di}. V_{S1}, V_{D1}, and i_{L1}.

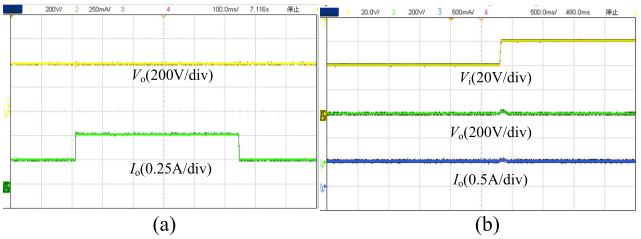


FIGURE 22. Key waveforms in the dynamic state with load change. (a) Experiment waveform for load resistance mutation. (b) Experiment waveform for input voltage mutation.

The comparison of voltage gain and efficiency between CCM and DCM is given in table 4. The converter can provide higher voltage gain in DCM operation. However, due to the larger current ripple and higher current root mean square value, the efficiency is relatively low. Fig. 22 shows the dynamic performance of the converter. It can be seen that the converter can maintain good stability when the load resistance changes or input voltage changes.

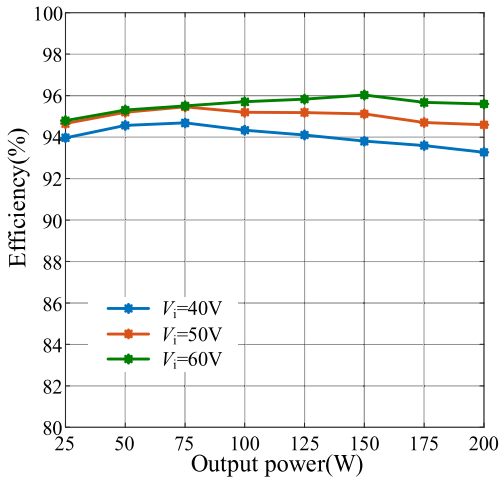


FIGURE 23. Measured efficiency curves of the proposed converter.

The efficiency curve of the experimental prototype at $V_o = 400$V is shown in Fig. 23. It can be seen the efficiency is improved when increasing input voltage. Compared with the transformer or coupled-inductor based converters proposed in [27]–[29], the proposed converter can achieve higher efficiency with the same voltage gain.

VIII. CONCLUSION

This paper has proposed a novel high step-up dc-dc converter. The proposed structure can achieve high voltage gain and maintain low voltage stress on the semiconductors.

Circuit operation principles, analysis, and necessary relationships were presented. Considering the result, the voltage gain will increase when the proposed converter is operated in DCM operation.

The cascaded topology was proposed in Section V, some desirable features exist in the cascaded topology, such as higher voltage gain, lower device voltage stress and lower current ripple of the inductors.

A comparison between the proposed and other structures was also provided. Considering the results, the superiority of the proposed converter to other converters is confirmed.

Finally, simulation and experimental results have verified the characteristics and theoretical analysis. Consider the advantages of the proposed converter such as high step-up capacity, low device voltage stress, common ground for input and output and reduced passive components, it could be a suitable choice for uninterruptible power supply systems, electric vehicles, and LED lighting systems, where high voltage gain is often required.

REFERENCES

[1] D. Vinnikov and I. Roasto, "Quasi-Z-source-based isolated DC/DC converters for distributed power generation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 192–201, Jan. 2011.

[2] W. Qian, H. Cha, F. Z. Peng, and L. M. Tolbert, "55-kW variable 3X DC-DC converter for plug-in hybrid electric vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1668–1678, Apr. 2012.
[3] Z. Zhang, O. C. Thomsen, M. A. E. Andersen, J. D. Schmidt, and H. R. Nielsen, "Analysis and design of Bi-directional DC-DC converter in extended run time DC UPS system based on fuel cell and supercapacitor," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2009, pp. 714–719.
[4] X. Xu and X. Wu, "High dimming ratio LED driver with fast transient boost converter," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 4192–4195.
[5] D. C. Lu, K. W. Cheng, and Y. S. Lee, "A single-switch continuous-conduction-mode boost converter with reduced reverse-recovery and switching losses," *IEEE Trans. Ind. Electron.*, vol. 50, no. 4, pp. 767–776, Aug. 2003.
[6] D. Chen and H. Zeng, "A buck type multi-input distributed generation system with parallel-timesharing power supply," *IEEE Access*, vol. 8, pp. 79958–79968, 2020.
[7] S. J. Finney, B. W. Williams, and T. C. Green, "RCD snubber revisited," *IEEE Trans. Ind. Appl.*, vol. 32, no. 1, pp. 155–160, Jan./Feb. 1996.
[8] D. Chen, J. Jiang, Y. Qiu, J. Zhang, and F. Huang, "Single-stage three-phase current-source photovoltaic grid-connected inverter high voltage transmission ratio," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7591–7601, Oct. 2017.
[9] Y. Hsieh, J. Chen, T. Liang, and L. Yang, "Novel high step-up DC-DC converter with coupled-inductor and switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 998–1007, Feb. 2012.
[10] F. Lin Luo and H. Ye, "Positive output super-lift converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 105–113, Jan. 2003.
[11] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC–DC PWM converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.
[12] L.-S. Yang, T.-J. Liang, and J.-F. Chen, "Transformerless DC–DC converters with high step-up voltage gain," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3144–3152, Aug. 2009.
[13] T. Zhao, X. Zhang, W. Mao, F. Wang, J. Xu, and Y. Gu, "A modified hybrid modulation strategy for suppressing DC voltage fluctuation of cascaded H-bridge photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3932–3941, May 2018.
[14] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.
[15] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 2008, pp. 2743–2749.
[16] Y. Tang, D. Fu, T. Wang, and Z. Xu, "Hybrid switched-inductor converters for high step-up conversion," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1480–1490, Mar. 2015.
[17] M. A. Salvador, J. M. de Andrade, T. B. Lazzarin, and R. F. Coelho, "Non-isolated high-step-up DC–DC converter derived from switched-inductors and switched-capacitors," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8506–8516, Oct. 2020.
[18] R. Stala, Z. Waradzyn, A. Penczek, A. Mondzik, and A. Skała, "A switched-capacitor DC–DC converter with variable number of voltage gains and fault-tolerant operation," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3435–3445, May 2019.
[19] Y. Ye and K. W. Eric Cheng, "Quadratic boost converter with low buffer capacitor stress," *IET Power Electron.*, vol. 7, no. 5, pp. 1162–1170, May 2014.
[20] J. Zhang and J. Ge, "Analysis of Z-source DC-DC converter in discontinuous current mode," in *Proc. Asia–Pacific Power Energy Eng. Conf.*, 2010, pp. 1–4.
[21] H. Shen, B. Zhang, and D. Qiu, "Hybrid Z-source boost DC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 310–319, Jan. 2017.
[22] A.-V. Ho, T.-W. Chun, and H.-G. Kim, "Extended boost active-switched-capacitor/switched-inductor quasi-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5681–5690, Oct. 2015.
[23] T. Takiguchi and H. Koizumi, "Quasi-Z-source DC-DC converter with voltage-lift technique," in *Proc. IEEE 39th Annu. Conf. Ind. Electron. Soc.*, Nov. 2013, pp. 1191–1196.
[24] M. M. Haji-Esmaeili, E. Babaei, and M. Sabahi, "High step-up quasi-Z source DC–DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10563–10571, Dec. 2018.
[25] D. Vinnikov, I. Roasto, R. Strzelecki, and M. Adamowicz, "Step-up DC/DC converters with cascaded quasi-Z-source network," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3727–3736, Oct. 2012.
[26] T. Zhao, X. Zhang, M. Wang, W. Mao, M. Ma, F. Wang, and X. Wang, "Analysis and suppression of resonant current envelope ripple of LLC converter in cascaded modular PV solid state transformer," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Apr. 20, 2020, doi: 10.1109/JESTPE.2020.2988989.
[27] S. A. Gorji, M. Ektesabi, and J. Zheng, "Isolated switched-boost push–pull DC–DC converter for step-up applications," *IEEE Power Electron Lett.*, vol. 53, no. 3, pp. 177–179, Feb. 2017.
[28] M. Nguyen, Y. Lim, J. Choi, and G. Cho, "Isolated high step-up DC–DC converter based on quasi-switched-boost network," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7553–7562, Dec. 2016.
[29] H. Liu, J. Wang, and Y. Ji, "A novel high-step-up coupled-inductor DC–DC converter with reduced power device voltage stress," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1941–1948, Sep. 2019.
[30] T. Zhao, X. Zhang, W. Mao, F. Wang, J. Xu, Y. Gu, and X. Wang, "An optimized third harmonic compensation strategy for single-phase cascaded H-bridge photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 8635–8645, Nov. 2018.

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