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A New Hybrid Zeta-Boost Converter With Active Quad Switched Inductor for High Voltage Gain

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ABSTRACT For renewable sources application like smart grids, microgrids, etc. high voltage gain converter becomes a fundamental unit. In this article, a new hybrid circuit of zeta and boost converter based on active-quad-switched-inductor (AQSL) is proposed. The discontinuous input current in classical zeta circuit determines the less consumption of input source. However, the proposed hybrid zeta-boost converter provides a higher voltage gain with continuous input and output currents. It achieves higher voltage gain devoid of the high-frequency transformer, and multiple stages of diode and capacitor circuit. The mode of operation, boundary region, and non-ideal model of the proposed converter are presented. Design consideration and a comparison study with recent circuits are provided. The design circuitry of the proposed converter investigated and the functionality of the suggested circuit is validated.

INDEX TERMS Active-quad-switched-inductor, boost circuit, high voltage gain, hybrid configuration, zeta circuit.

I. INTRODUCTION

Nowadays, DC-DC converter circuits are gaining more popularity in the renewable energy system [1]; since the basic boost converter circuits does not provide expected characteristics in terms of voltage gain [2]. Conventional converters appear inappropriate for high voltage gain applications as an increment in duty ratio leads to the degradation in performance of converter in the form of rising conduction losses, decimating the voltage gain and its performance. The high voltage across switches that causes the need for high rating switches, further increasing the power losses [3]. Isolated DC-DC converters introduced to overcome these disadvantages of conventional converters for delivering high output voltage [4]. Nonetheless, high voltage spike causes the use of energy recycle techniques, non-dissipative snubber circuit, high-frequency transformer, and clamping techniques to decrease the voltage spike and stress [5]. Therefore, the circuit is costly and large in volume due to the supplementary circuit which decreases its efficiency. Therefore, the non-isolated circuits are becoming an attractive solution compared to isolated configurations [6]. In coupled inductor based converter, weith the variation in turn ratio of a coupled inductor, high output voltage can be generated. However, the coupled inductor converters suffer the problems of leakage inductances, voltage spikes, etc. [7]. Non-coupled inductor DC-DC converter includes multilevel converters [8], utilization of boost converter with switching capacitor network [9], switching inductor network [10], XY converter family [11], cascaded converter [12], quadratic converter [13], Luo converter [14], and voltage multiplier based converter [15], [16]. Switched capacitor converters can provide high voltage gain reliant on capacitors units in the switched capacitor cell [17]. However, switched capacitor converters have disadvantages of pulsating input current and poor voltage regulation. Switched inductor passive cells

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have been applied to enhance the output voltage [18], [19]. Lower current rating of the inductor is one advantage of switched inductor based converters. The active switch voltage stress is the major disadvantages of the structure. The switched capacitor-inductor passive cell combines the features of the switched capacitor and switched inductor converters, but the input current is discontinuous [10], [19]. The XY converter family also provides high voltage gain; however, discontinuous input current, switch voltage, and capacitor stack is a major drawback [11]. Cascading of several converters increases the voltage gain compared to the conventional converter, but complexity and cost increase as several components increases [12]. The quadratic converter can somehow lessen the problems of cascade circuits by adopting a single switch but required high voltage and current rating devices [13]. Luo converters provide high voltage, but topological complexity, cost, volume, and losses increase at the same time [14], [17]. Capacitor–diode voltage multiplier cell-based converters are a useful approach to increase voltage gain with increased efficiency and reliability in combination with classical converter topologies [15]. However, the number of capacitors and diodes increase, and also current snubber is needed to decrease *di/dt*. Also, the size and cost of converter increases [20].

This article proposes a new hybrid converter based on zeta converter, boost converter, an active-quad-switched-inductor (AQSL) structure for high voltage gain. The main features of the suggested converter are 1) voltage gain is high without using multiplier circuitry, 2) continuous input current, 3) low current rating inductor, 4) low voltage/current rating devices. Section II describes the proposed converter configuration and operation. The non-ideality characteristics of the proposed converter are examined in section III and comparison is given section IV. The performance of the designed prototype of the proposed converter is discussed in Section V. The article is concluded in section VI.

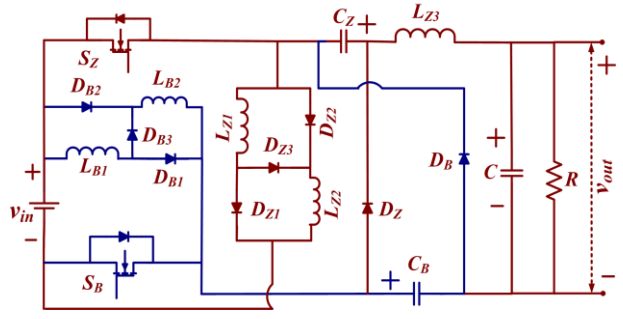

FIGURE 1. Hybrid zeta-boost converter.

II. HYBRID ZETA BOOST CONVERTER

Fig. 1 depicts the proposed circuit of the converter. The circuit is designed by combining zeta and boost converter, active quad switched-inductor (AQSL). The AQSL network contains diodes D_{Z1}, D_{Z2}, and D_{Z3}, inductors L_{Z1} and L_{Z2}, and switch S_Z for zeta converter; and diodes D_{B1}, D_{B2}, and D_{B3}, and inductors L_{B1} and L_{B2}, and switch S_B for the boost converter. The switch S_Z of zeta converters is connected at the positive polarity of the input supply, and switch S_B of the boost converter is connected at the negative polarity of the input supply. The diodes D_B and D_Z operate complimentary to the switches; and inductor L_{Z3} and capacitor C act as a low pass LC filter connected between the AQSL network and load.

A. CONTINUOUS CONDUCTION MODE

The equivalent circuit for different modes is illustrated in Fig. 2. The converter operates in two modes, one when switches S_B and S_Z are turned ON and another when switches S_B and S_Z are turned OFF. Fig. 3 shows the typical waveforms when the circuit operates in ON and OFF modes.

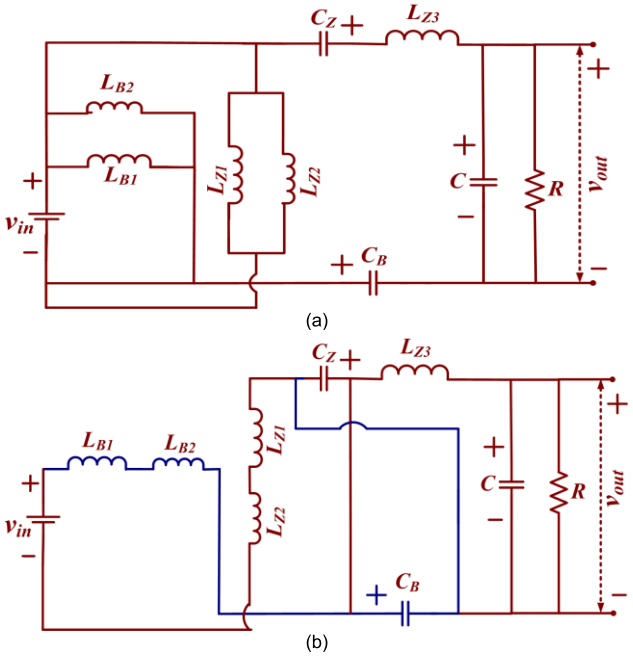

FIGURE 2. Equivalent circuitry of proposed hybrid zeta-boost converter (a) ON mode, (b) OFF mode.

1) MODE-1 ($t_0 < t < t_1$)

The proposed converter operates in this mode when switches S_B and S_Z are turned ON simultaneously. During this mode, the input source charged the inductors L_{B1}, L_{B2}, L_{Z1} and L_{Z2} in parallel and inductor L_{Z3} charged by input source and capacitors C_Z and C_B. The diodes D_{B1}, D_{B2}, D_{z1} and D_{z2} are forward bias, and diodes D_{B3}, D_{Z3}, D_B and D_Z are reversed bias. The inductors voltages are,

$$V_{LB1,on} = V_{LB2,on} = V_{LZ1,on} = V_{LZ2,on} = V_{in} \quad (1)$$

$$V_{LZ3,on} = V_{in} + V_{CZ} + V_{CB} - V_{out} \quad (2)$$

where V_{in} and V_{out} are voltage at the input and output terminal; $V_{LB1,on}$, $V_{LB2,on}$, $V_{LZ1,on}$, $V_{LZ2,on}$, and $V_{LZ3,on}$ are

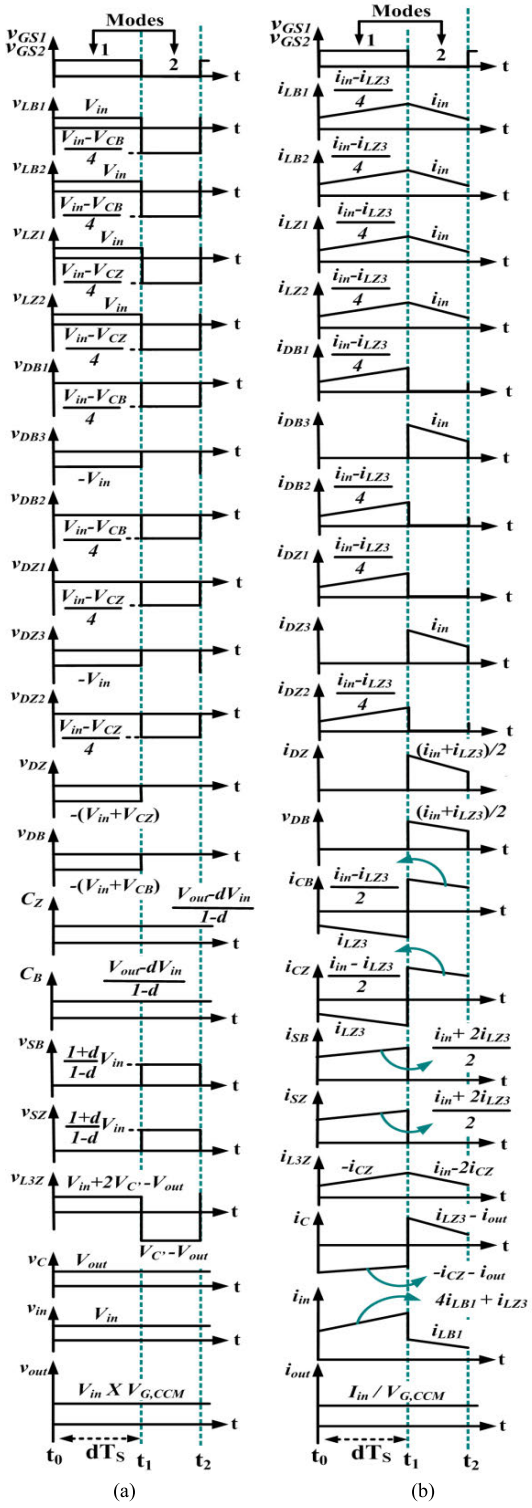

FIGURE 3. Typical characteristics of proposed converters in CCM operation.

the voltage across inductors L_{B1}, L_{B2}, L_{Z1}, L_{Z2} and L_{Z3} in mode-1, V_{CZ} is capacitor C_Z voltage, V_{CB} is capacitor C_B voltage. The input current is,

$$i_{in,on} = i_{LB1,on} + i_{LB2,on} + i_{LZ1,on} + i_{LZ2,on} + i_{LZ3,on} \quad (3)$$

where $i_{in,on}$ is current through input terminal mode-1; $i_{LB1,on}$, $i_{LB2,on}$, $i_{LZ1,on}$, $i_{LZ2,on}$, and $i_{LZ3,on}$ are the current through inductors L_{B1}, L_{B2}, L_{Z1}, L_{Z2} and L_{Z3} in mode-1,respectively. The current through capacitors C_Z, C_B, and C are obtained as,

$$i_{CZ,on} = -i_{LZ3,on}; \quad i_{CB,on} = -i_{LZ3,on} \quad (4)$$

$$i_{C,on} = i_{LZ3,on} - \frac{V_{out}}{R} \quad (5)$$

where $i_{CZ,on}$, $i_{CB,on}$, and $i_{C,on}$ are the current through capacitors C_Z, C_B, and C in mode-1, respectively. The current through diodes D_{Z1}, D_{Z2}, D_{B1}, and D_{B2} are obtained as,

$$i_{DZ1,on} = i_{LZ1,on}; \quad i_{DZ2,on} = i_{LZ2,on}; \; i_{DZ3,on} = 0 \quad (6)$$

$$i_{DB1,on} = i_{LB1,on}; \quad i_{DB2,on} = i_{LB2,on}; \; i_{DB3,on} = 0 \quad (7)$$

$$i_{DB,on} = 0; \quad i_{DZ,on} = 0 \quad (8)$$

where $i_{DZ1,on}$, $i_{DZ2,on}$, and $i_{DZ3,on}$ are current through diodes D_{Z1}, D_{Z2}, and D_{Z3} in mode-1, respectively; $i_{DB1,on}$, $i_{DB2,on}$, and $i_{DB3,on}$ are current through diodes D_{B1}, D_{B2}, and D_{B3} in mode-1, respectively; $i_{DZ,on}$ and $i_{DB,on}$ are current through diodes D_Z and D_B in mode-1, respectively.

2) MODE-2 ($t_1 < t < t_2$)

During this mode, switches are turned OFF and the inductors L_{B1}, L_{B2}, L_{Z1} and L_{Z2} are discharged in series. The input voltage source and inductors L_{B1}, L_{B2}, L_{Z1} and L_{Z2} provides energy to capacitors C_Z and C_B. The capacitors C_Z and C_B are charged in parallel. Also, the inductors L_{B1}, L_{B2}, L_{Z1}, L_{Z2}, and L_{Z3} provides energy to R and C. The diodes D_{B1}, D_{B2}, D_{Z1}, and D_{Z2} are reversed bias, and diodes D_{B3} and D_{Z3}, D_B and D_Z are forward bias. The inductor voltages are,

$$V_{LB1,off} = V_{LB2,off} = V_{LZ1,off} = V_{LZ2,off} = \frac{V_{in} - V_{CZ}}{4} = \frac{V_{in} - V_{CB}}{4} \quad (9)$$

$$V_{LZ3,off} = V_{CZ} - V_{out} = V_{CB} - V_{out} \quad (10)$$

where $V_{LB1,off}$, $V_{LB2,off}$, $V_{LZ1,off}$, $V_{LZ2,off}$, and $V_{LZ3,off}$ are the voltage across inductors L_{B1}, L_{B2}, L_{Z1}, L_{Z2} and L_{Z3} in mode-2, respectively. The current through capacitors C_Z, C_B, and C are obtained as,

$$i_{CZ,off} = \frac{i_{in,off} - i_{LZ3,off}}{2}, \quad i_{CB,off} = \frac{i_{in,off} - i_{LZ3,off}}{2} \quad (11)$$

$$i_{C,off} = i_{LZ3,off} - \frac{V_{out}}{R} \quad (12)$$

where $i_{CZ,off}$, $i_{CB,off}$, and $i_{C,off}$ are the current through capacitors C_Z, C_B, and C in mode-2, respectively. The current through diodes D_{Z1}, D_{Z2}, D_{B1}, and D_{B2} are obtained as,

$$i_{DZ1,off} = 0; \quad i_{DZ2,off} = 0; \; i_{DZ3,off} = i_{LZ1,off} = i_{LZ2,off} \quad (13)$$

$$i_{DB1,off} = 0; \quad i_{DB2,off} = 0; \; i_{DB3,off} = i_{LB1,off} = i_{LB2,off} \quad (14)$$

$$i_{DB,on} = \frac{i_{in,off} + i_{LZ3,off}}{2}; \quad i_{DZ,on} = \frac{i_{in,off} + i_{LZ3,off}}{2} \quad (15)$$

The voltage across intermediate capacitor C_Z and C_B are as follows,

$$V_{C'} = V_{CZ} = V_{CB} \tag{16}$$

As the average voltage across an inductor is null in steady-state, the following expression can be obtained,

$$\begin{aligned}\langle v_{LB1}\rangle &= \langle v_{LB2}\rangle = \langle v_{LZ1}\rangle = \langle v_{LZ2}\rangle \\ &= V_{in}d + \left(\frac{V_{in} - V_{C'}}{4}\right)(1-d) = 0 \end{aligned} \tag{17}$$

$$\langle v_{LZ3}\rangle = (V_{in} + 2V_{C'} - V_{out})\,d + (V_{C'} - V_{out})\,(1-d) = 0 \tag{18}$$

where d is the duty cycle. From (18), an expression for voltage $V_{C'}$ i.e. the voltage across capacitors C_Z or C_B is obtained as follows,

$$V_{C'} = \frac{V_{out} - V_{in}d}{1+d} = \frac{1+3d}{1-d}V_{in} \tag{19}$$

Using (17) and (19), the voltage gain is obtained as follows,

$$V_{M,CCM} = \frac{V_{out}}{V_{in}} = \frac{1+5d+2d^2}{1-d} \tag{20}$$

where, $V_{M,CCM}$ is the CCM voltage gain. Fig. 4 shows the plot of voltage across capacitor C_Z and C_B i.e. $V_{C'}$ and voltage gain with variation in duty cycle and observed that the voltage ratio can be obtained by selecting appropriate duty cycle.

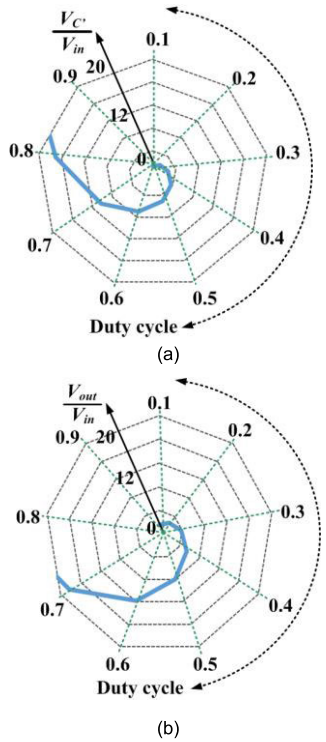

FIGURE 4. Plots (a) Ratio of capacitor voltage and input voltage versus duty cycle, (b) Voltage gain versus duty cycle.

When the inductances are unequal the current profile of the inductors are different. Hence, the operating modes of the converter are quite different when the inductances are unequal. However, the voltage gain of the converter is the same as the situation when the inductances are equal [21], [22].

B. DISCONTINUOUS CONDUCTION MODE

The typical waveforms for discontinuous conduction mode are shown in Fig. 5.

1) MODE-1 ($t_0 < t < t_1$)

The equivalent circuit is shown in Fig. 2(a). The maximum value of inductors L_{Z1}, L_{Z2}, L_{B1}, L_{B2}, and L_{Z3} currents are obtained as follows,

$$I_{LZ1,\max} = \frac{V_{in}d}{f_s L_{Z1}} + I_{LZ1,\min} \tag{21}$$

$$I_{LZ2,\max} = \frac{V_{in}d}{f_s L_{Z2}} + I_{LZ2,\min} \tag{22}$$

$$I_{LB1,\max} = \frac{V_{in}d}{f_s L_{B1}} + I_{LB1,\min} \tag{23}$$

$$I_{LB2,\max} = \frac{V_{in}d}{f_s L_{B2}} + I_{LB2,\min} \tag{24}$$

$$I_{LZ3,\max} = \frac{(V_{in} + V_{CZ} + V_{CB} - V_{out})\,d}{f_s L_{Z3}} + I_{LZ3,\min} \tag{25}$$

where, $I_{LZ1,max}$, $I_{LZ2,max}$, $I_{LB1,max}$, $I_{LB2,max}$, and $I_{LZ3,max}$ are the maximum value of current through inductors L_{Z1}, L_{Z2}, L_{B1}, L_{B2}, and L_{Z3} respectively; $I_{LZ1,min}$, $I_{LZ2,min}$, $I_{LB1,min}$, $I_{LB2,min}$, and $I_{LZ3,min}$ are the minimum values of current through inductors L_{Z1}, L_{Z2}, L_{B1}, L_{B2}, and L_{Z3}, respectively.

2) MODE-2 ($t_1 < t < t_2$)

The equivalent circuit is shown in Fig. 2(b). Let's assume, when $t_2 = dT_S + d_x T_S$, the diodes D_Z, D_B, D_{B2}, D_{Z2}, and inductors L_{Z1}, L_{Z2}, L_{B1}, L_{B2}, and L_{Z3} current reached to zero. The minimum value of inductor L_{Z1}, L_{Z2}, L_{B1}, L_{B2}, and L_{Z3} currents are obtained as follows,

$$I_{LZ1,\min} = \frac{(V_{in} - V_{CZ})\,d_x}{4f_s L_{Z1}} + I_{LZ1,\max} = 0 \tag{26}$$

$$I_{LZ2,\min} = \frac{(V_{in} - V_{CZ})\,d_x}{4f_s L_{Z2}} + I_{LZ2,\max} = 0 \tag{27}$$

$$I_{LB1,\min} = \frac{(V_{in} - V_{CB})\,d_x}{4f_s L_{B1}} + I_{LB1,\max} = 0 \tag{28}$$

$$I_{LB2,\min} = \frac{(V_{in} - V_{CB})\,d_x}{4f_s L_{B2}} + I_{LB2,\max} = 0 \tag{29}$$

$$I_{LZ3,\min} = \frac{(V_{CB} - V_{out})\,d_x}{f_s L_{Z3}} + I_{LZ3,\max} = 0 \tag{30}$$

3) MODE-3 ($t_2 < t < t_3$)

For this period, the current through the diodes becomes zero and the converter circuitry is illustrated in Fig. 6. The inductors L_{Z1}, L_{Z2}, L_{B1}, L_{B2}, and L_{Z3} currents are obtained as follows,

$$I_{LZ1,\min} = I_{LZ2,\min} = 0 \tag{31}$$

$$I_{LB1,\min} = I_{LB23,\min} = 0 \tag{32}$$

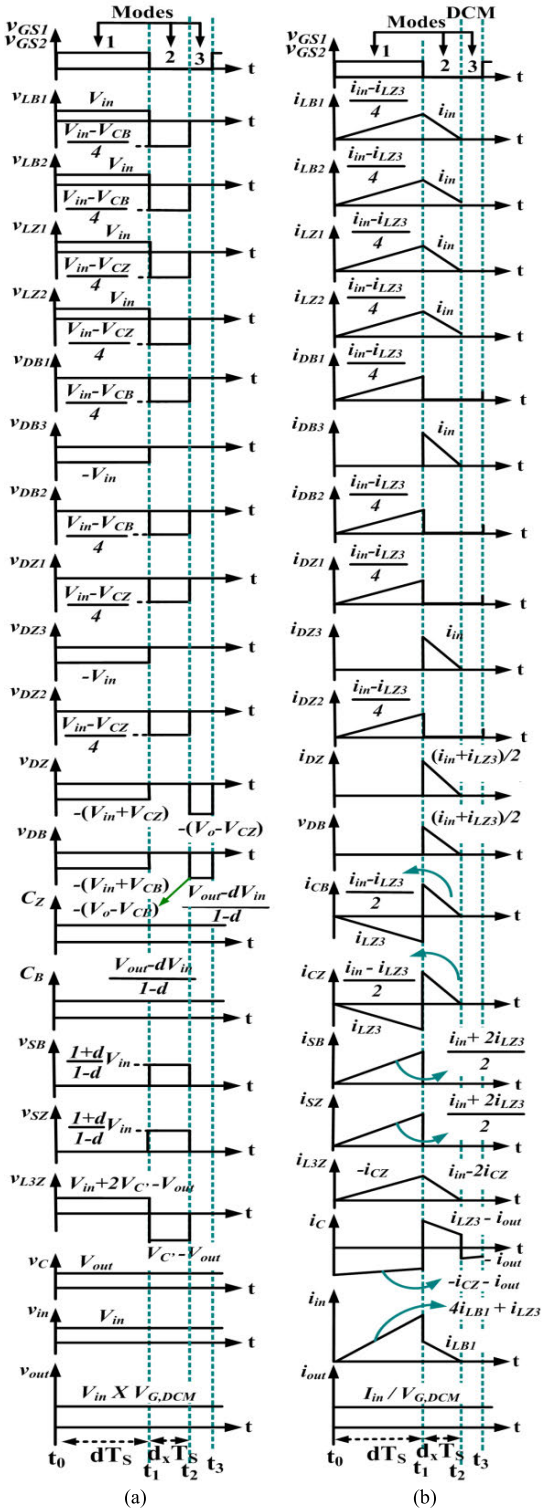

FIGURE 5. Typical Characteristics of proposed converters in DCM operation.

$$I_{LZ3,\min} = 0 \tag{33}$$

The current through capacitor C_Z and C_B for time period (t_2 to t_3) is as follows,

$$i_{CZ} = i_{CB} = 0 \tag{34}$$

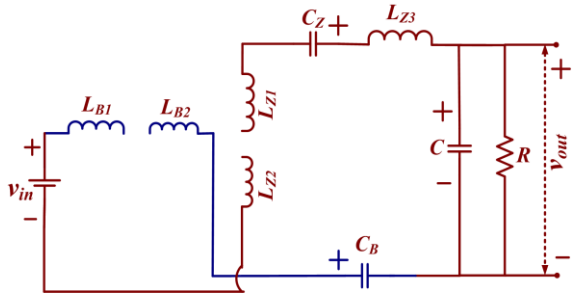

FIGURE 6. DCM operation of proposed converter.

The current through diodes of zeta converter, i.e. D_{Z1}, D_{Z2}, D_{Z3}, and D_Z for time period (t_2 to t_3) is as follows,

$$i_{DZ1} = i_{DZ2} = i_{DZ3} = i_{DZ} = 0 \tag{35}$$

The current through diodes of boost converter, i.e. D_{B1}, D_{B2}, D_{B3}, and D_B for time period (t_2 to t_3) is as follows,

$$i_{DB1} = i_{DB2} = i_{DB3} = i_{DB} = 0 \tag{36}$$

The value of d_x (note: duration of mode 2 is $d_x T_s$) and capacitor C voltage are calculated as,

$$d_x = \frac{4V_{in}d}{V_C - V_{in}} \tag{37}$$

$$V_C = \frac{2V_{out} + V_{in}(1+d)}{3+d} \tag{38}$$

By substituting (37) in (36),

$$d_x = \frac{2V_{in}d(3+d)}{V_{out} - V_{in}} \tag{39}$$

The relation between the current through diode D_Z and D_B and output current can be obtained as follows,

$$I_{out} = I_{DZ,\max}\frac{d_x}{2} = I_{DB,\max}\frac{d_x}{2} = \frac{V_{out}}{R} \tag{40}$$

$$I_{DZ,\max} = I_{DB,\max} = \frac{I_{LZ1,\max} + I_{LZ3,\max}}{2} \tag{41}$$

$$I_{out} = \frac{V_{out}}{R} = \frac{V_{in}^2 d^2 (3+d)}{2f_s L_{eq}(V_{out} - V_{in})} \tag{42}$$

where L_{eq} is considered as equivalent inductance and it is obtained as,

$$L_{eq} = \frac{2L_{Z3}L}{2(1+d)L + L_{Z3}} \tag{43}$$

where, $L = L_{Z1} = L_{Z2} = L_{B1} = L_{B2}$.

From (42), the DCM voltage gain is expressed as,

$$V_{M,DCM} = \frac{V_{out}}{V_{in}} = \frac{1}{2} + \frac{1}{2}\sqrt{1 + \frac{4d^2(3+d)}{K}} \tag{44}$$

where k is a dimensionless parameter obtained as,

$$K = \frac{f_s L_{eq}}{R} \tag{45}$$

C. CCM AND DCM BOUNDARY OPERATING CONDITION

DCM operation occurs when the inductor current reaches zero. By equating equations (20) and (44), the critical value of K, *i.e.* K_{crit} is obtained as,

$$K_{crit} = \frac{4d\,(3+d)\,(1-d)^2}{4d^3+11d^2+32d+6} \tag{46}$$

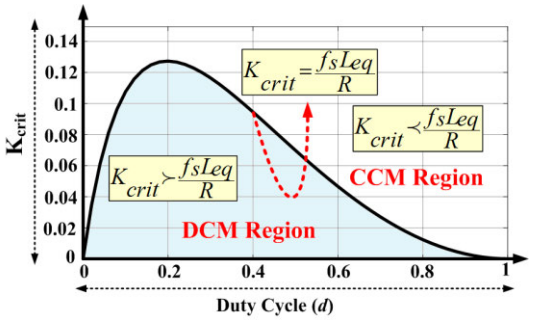

FIGURE 7. CCM and DCM boundary.

Fig. 7 shows that converter works in CCM when $K > K_{crit}$. Also, critical load resistance is computed, and parameter γ which signify the parameterized converter output current is defined as,

$$R_{crit} = \frac{4f_sL_{eq}\left(1+5d+2d^2\right)}{d\,(1-d)^2} \tag{47}$$

$$\gamma = \frac{I_{out}f_sL_{eq}}{V_{in}} \tag{48}$$

The critical value γ is stated in the form of the static gain.

$$\gamma crit = \frac{d^2\,(3+d)}{2\,(V_M-1)} \tag{49}$$

$$\gamma crit = \frac{d\,(1-d)}{4} \tag{50}$$

III. DESIGN CONSIDERATION

Concerning the converter operation in CCM, a detailed study can be achieved for getting the basic equations describing the current and voltage stresses of the elements.

The inductance L_{Z3} can be obtained by,

$$L_{Z3} = \frac{2v_{in}\,(1+d)\,d}{\Delta I_{LZ3}f_s} \tag{51}$$

The average current in output capacitor C_o is zero during the steady-state situation, the average current flowing through output inductor I_{LZ3} becomes equal to the average current flowing through load I_o. Therefore,

$$I_{LZ3} = I_{out} = \frac{1-d}{1+5d+2d^2}I_{in} \tag{52}$$

$$I_{LZ3} = \frac{P\,(1-d)}{v_{in}\left(1+5d+2d^2\right)} \tag{53}$$

The inductance L_{Z1} and L_{Z1}can be obtained by,

$$L_{Z1} = \frac{V_{in}d}{\Delta I_{LZ1}f_s}, \quad L_{Z2} = \frac{V_{in}d}{\Delta I_{LZ2}f_s} \tag{54}$$

The inductance L_{B1} and L_{ZB2} can be obtained by,

$$L_{B1} = \frac{V_{in}d}{\Delta I_{LB1}f_s}, \quad L_{B2} = \frac{V_{in}d}{\Delta I_{LB2}f_s} \tag{55}$$

The average value of the input current is,

$$I_{in} = (4I_L + I_{LZ3})\,d + I_L\,(1-d) \tag{56}$$

where, the average current through inductor L_{Z1}, L_{Z1}, L_{B1} and L_{ZB2} be obtained by,

$$I_L = I_{LB1} = I_{LB2} = I_{LZ1} = I_{LZ2} = \frac{P\left(1+4d+3d^2\right)}{v_{in}\left(1+5d+2d^2\right)(1+3d)} \tag{57}$$

where P is output power. The critical values of capacitors $C' = C_Z = C_B$ can be obtained by,

$$C' = C_B = C_Z = \frac{Pd\,(1-d)}{V_{in}f_s\left(1+5d+2d^2\right)\Delta V_C} \tag{58}$$

The average voltage across capacitor C_B, C_Z and C is obtained by,

$$V_{C'} = V_{CB} = V_{CZ} = \frac{v_{in}\left(1+4d+3d^2\right)}{(1-d)\,(1+d)} \tag{59}$$

$$V_C = \frac{1+5d+2d^2}{1-d}V_{in} \tag{60}$$

The peak voltage across diodes are as follows,

$$V_{DZ1,peak} = V_{DZ2,peak} = \frac{V_{in}-V_C}{4}, \quad V_{DZ3,peak} = -V_{in} \tag{61}$$

$$V_{DB1,peak} = V_{DB2,peak} = \frac{V_{in}-V_C}{4}, \quad V_{DB3,peak} = -V_{in} \tag{62}$$

$$V_{DZ,peak} = -V_{in} - V_{C'}, \quad V_{DB,peak} = -V_{in} - V_{C'} \tag{63}$$

The average current through diodes of switched inductors can be obtained as follows,

$$I_{DZ1} = I_{DZ2} = \frac{P\left(1+4d+3d^2\right)}{V_{in}\left(1+5d+2d^2\right)(1+3d)}d \tag{64}$$

$$I_{DB1} = I_{DB2} = \frac{P\left(1+4d+3d^2\right)}{V_{in}\left(1+5d+2d^2\right)(1+3d)}d \tag{65}$$

$$I_{DZ3} = I_{DB3} = \frac{P\left(1+4d+3d^2\right)}{V_{in}\left(1+5d+2d^2\right)(1+3d)}(1-d) \tag{66}$$

$$I_{DB1} = I_{DB2} = \frac{P\left(1+4d+3d^2\right)}{V_{in}\left(1+5d+2d^2\right)(1+3d)}d \tag{67}$$

The maximum voltage across switches are,

$$V_{SB} = \frac{(1+d)}{(1-d)}V_{in}, \quad V_{SZ} = \frac{(1+d)}{(1-d)}V_{in} \tag{68}$$

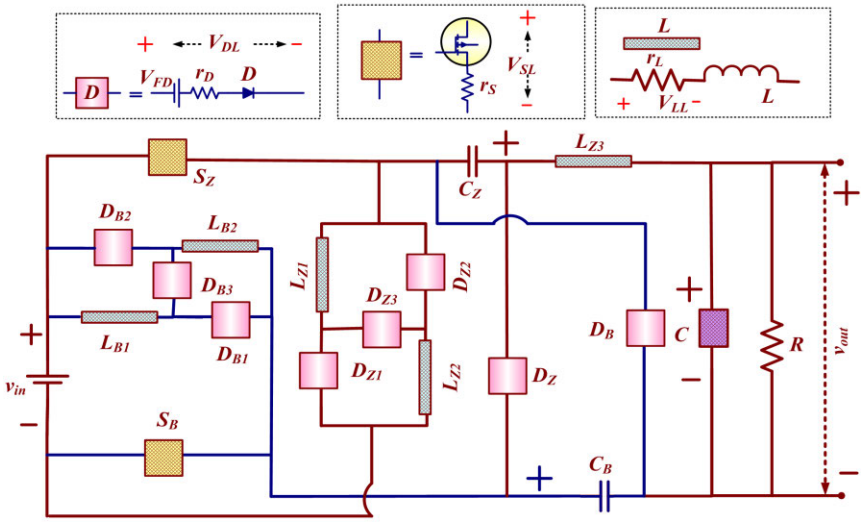

FIGURE 8. Hybrid zeta-boost converter with parasitic of active and passive components.

IV. NON-IDEAL MODEL OF CONVERTER

Fig. 8 depicts the power circuit with non-idealities of elements of the converter, where r_L is resistance of inductor, r_S is resistance of switch, r_D and V_{FD} is resistance and the threshold voltage of the diode.

A. VOLTAGE GAIN WITH NON-IDEAL INDUCTORS

The effect of ESR of inductors L_{B1}, L_{B2}, L_{Z1}, L_{Z2} and L_{Z3} is analyzed while ignoring other parasitic components, i.e. $r_S = 0$, $r_D = 0$, and $V_{FD} = 0$. The inductors L_{B1}, L_{B2}, L_{Z1}, L_{Z2} and L_{Z3} voltages are,

$$\left.\begin{aligned} &V_{LB1} \approx V_{in} - i_{LB1}r_L, V_{LB2} \approx V_{in} - i_{LB2}r_L \\ &V_{LZ1} \approx V_{in} - i_{LZ1}r_L, V_{LZ2} \approx V_{in} - i_{LZ2}r_L \\ &V_{LZ3} = V_{in} + V_{CZ} + V_{CB} - V_{out} - i_{LZ3}r_L \end{aligned}\right\} \text{mode-1} \tag{69}$$

$$\left.\begin{aligned} &V_{LB1} \approx V_{LB2} \approx V_{LZ1} \approx V_{LZ2} \\ &\approx \frac{V_{in} - V_{C'} - i_{LB1}r_L - i_{LB2}r_L - i_{LZ1}r_L - i_{LZ2}r_L}{4} \\ &V_{LZ3} = V_{CZ} - V_{out} - i_{LZ3}r_L \end{aligned}\right\} \text{mode-2} \tag{70}$$

Consider, the drop in voltage across each inductor due to r_L is V_{LL}. Therefore,

$$\left.\begin{aligned} &V_{LB1} = V_{LB2} = V_{LZ1} = V_{LZ2} \approx V_{in} - V_{LL} \\ &V_{LZ3} = V_{in} + V_{CZ} + V_{CB} - V_{out} - V_{LL} \end{aligned}\right\} \text{mode-1} \tag{71}$$

$$\left.\begin{aligned} &V_{LB1} \approx V_{LB2} \approx V_{LZ1} \approx V_{LZ2} \approx \frac{V_{in} - V_{C'} - 4V_{LL}}{4} \\ &V_{LZ3} = V_{CZ} - V_{out} - V_{LL} \end{aligned}\right\} \text{mode-2} \tag{72}$$

As the average voltage across an inductor is null in steady-state, the following expression can be obtained,

$$(V_{in} - V_{LL})\, d + \left(\frac{V_{in} - V_{C'} - 4V_{LL}}{4}\right)(1 - d) = 0 \tag{73}$$

$$(V_{in} + 2V_{C'} - V_{out} - V_{LL})\, d + (V_{C'} - V_{out} - V_{LL})\,(1 - d) = 0 \tag{74}$$

The expression for voltage $V_{C'}$ i.e. voltage across capacitors C_Z or C_B is obtained as follows,

$$V_{C'} = \frac{V_{out} - V_{in}d + V_{LL}}{1 + d} \tag{75}$$

The converter voltage gain is obtained as follows,

$$V_{M,CCM} = \frac{\left(1 + 5d + 2d^2\right) - \left\{(5 + 3d)\, V_{LL}/V_{in}\right\}}{1 - d} \tag{76}$$

Equation (76) is plotted in Fig 9(a) with variation in duty cycle, and the effect of non-ideal inductors on voltage gain is presented.

B. VOLTAGE GAIN WITH NON-IDEAL DIODES

The effect of diodes D_{B1}, D_{B2}, D_{B3}, D_{Z1}, D_{Z2} and D_{Z3}, and diodes D_B and D_S are analyzed while ignoring other parasitic components, i.e. $r_L = 0$, and $r_S = 0$. The inductors L_{B1}, L_{B2}, L_{Z1}, L_{Z2} and L_{Z3} voltages are,

$$\left.\begin{aligned} &V_{LB1} = V_{LB2} = V_{LZ1} = V_{LZ2} \approx V_{in} - i_L r_D - V_{FD} \\ &V_{LZ3} = V_{in} + 2V_{C'} - V_{out} \end{aligned}\right\} \times \text{mode-1} \tag{77}$$

$$\left.\begin{aligned} &V_{LB1} \approx V_{LB2} \approx V_{LZ1} \approx V_{LZ2} \approx \frac{V_{in} - V_{C'} - 3i_L r_D - 3V_{FD}}{4} \\ &V_{LZ3} = V_{C'} - V_{out} - i_L r_D - V_{FD} \end{aligned}\right\} \times \text{mode-2} \tag{78}$$

Consider, the drop in voltage across each inductor due to parasitic of diode is V_{DL}. Therefore,

$$\left.\begin{aligned} &V_{LB1} = V_{LB2} = V_{LZ1} = V_{LZ2} \approx V_{in} - V_{DL} \\ &V_{LZ3} = V_{in} + 2V_{C'} - V_{out} \end{aligned}\right\} \text{mode-1} \tag{79}$$

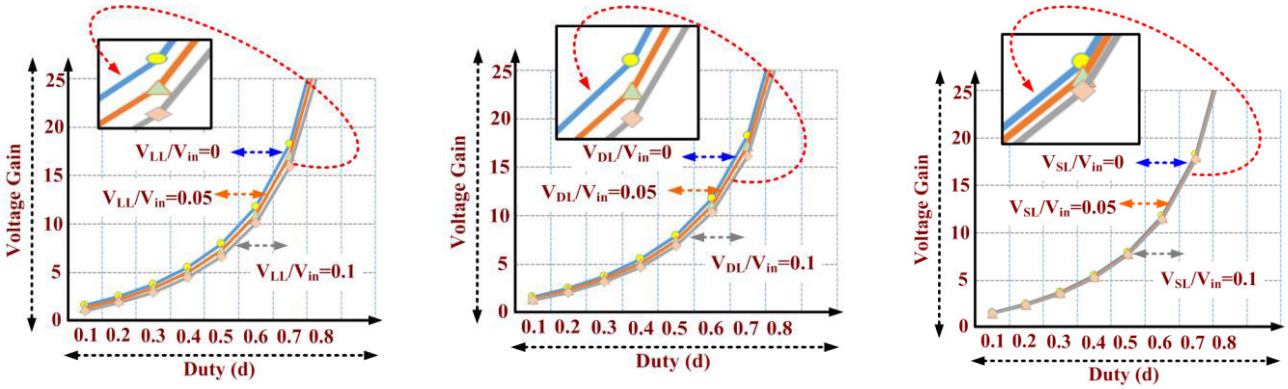

FIGURE 9. Effect of parasitic on voltage gain, (a) voltage gain by considering ESR of inductor, (b) voltage gain by considering diode forward resistance and threshold voltage, (c) voltage gain by considering switch resistance.

$$\left.\begin{aligned} &V_{LB1} \approx V_{LB2} \approx V_{LZ1} \approx V_{LZ2} \approx \frac{V_{in} - V_{C'} - 3V_{DL}}{4} \\ &V_{LZ3} = V_{C'} - V_{out} - V_{DL} \end{aligned}\right\} \text{mode-2} \tag{80}$$

As the average voltage across an inductor is null in steady-state, the following expression can be obtained,

$$(V_{in} - V_{DL})\, d + \left(\frac{V_{in} - V_{C'} - 3V_{DL}}{4}\right)(1-d) = 0 \tag{81}$$

$$(V_{in} + 2V_{C'} - V_{out})\, d + (V_{C'} - V_{out})\,(1-d) = 0 \tag{82}$$

The expression for voltage $V_{C'}$ i.e. voltage across capacitors C_Z or C_B is obtained as follows,

$$V_{C'} = \frac{V_{out} - V_{in} d}{1+d} \tag{83}$$

The converter voltage gain is obtained as follows,

$$V_{M,CCM} = \frac{\left(1 + 5d + 2d^2\right) - \left\{(1+d)\,(3+d)\,V_{DL}/V_{in}\right\}}{1-d} \tag{84}$$

Equation (84) is plotted in Fig 9(b) with variation in duty cycle, and the effect of non-ideal diodes on voltage gain is presented.

C. VOLTAGE GAIN WITH NON-IDEAL SWITCHES

The effect of parasitic of switches S_Z and S_B is analyzed while ignoring other parasitic components, i.e. $r_L = 0$, $r_D = 0$, and $V_{FD} = 0$. The inductors L_{B1}, L_{B2}, L_{Z1}, L_{Z2} and L_{Z3} voltages are,

$$\left.\begin{aligned} &V_{LB1} = V_{LB2} \approx V_{in} - i_{S1} r_S,\ V_{LZ1} = V_{LZ2} \approx V_{in} - i_{S2} r_S \\ &V_{LZ3} = V_{in} + 2V_{C'} - V_{out} - i_{S1} r_S - i_{S2} r_S \end{aligned}\right\} \times \text{mode-1} \tag{85}$$

$$\left.\begin{aligned} &V_{LB1} \approx V_{LB2} \approx V_{LZ1} \approx V_{LZ2} \approx \frac{V_{in} - V_{C'}}{4} \\ &V_{LZ3} = V_{C'} - V_{out} \end{aligned}\right\} \text{mode-2} \tag{86}$$

Consider, the drop in voltage across each inductor due to parasitic of the diode is V_{SL}. Therefore,

$$\left.\begin{aligned} &V_{LB1} = V_{LB2} = V_{LZ1} = V_{LZ2} \approx V_{in} - V_{SL} \\ &V_{LZ3} = V_{in} + 2V_{C'} - V_{out} - 2V_{SL} \end{aligned}\right\} \text{mode-1} \tag{87}$$

$$\left.\begin{aligned} &V_{LB1} \approx V_{LB2} \approx V_{LZ1} \approx V_{LZ2} \approx \frac{V_{in} - V_{C'}}{4} \\ &V_{LZ3} = V_{C'} - V_{out} \end{aligned}\right\} \text{mode-2} \tag{88}$$

As the average voltage across an inductor is null in steady-state, the following expression can be obtained,

$$(V_{in} - V_{SL})\, d + \left(\frac{V_{in} - V_{C'}}{4}\right)(1-d) = 0 \tag{89}$$

$$(V_{in} + 2V_{C'} - V_{out} - 2V_{SL})\, d + (V_{C'} - V_{out})\,(1-d) = 0 \tag{90}$$

The expression for voltage $V_{C'}$ i.e. voltage across capacitors C_Z or C_B is obtained as follows,

$$V_{C'} = \frac{V_{out} - V_{in} d}{1+d} \tag{91}$$

The converter voltage gain is obtained as follows,

$$V_{M,CCM} = \frac{\left(1 + 5d + 2d^2\right) - \left\{(1+d) d i_s r_s / V_{in}\right\}}{1-d} \tag{92}$$

Equation (92) is plotted in Fig 9(c) with variation in duty cycle, and the effect of non-ideal switches on voltage gain is presented.

V. COMPARISON

This section presents a comparative study between proposed converter, classical boost converter [1], converter presented in [7], switched capacitor converter [8], switched inductor converter [9], symmetric hybrid- switched inductor converter [10], and active switched-inductor step-up 2 cell converter [20]. Table 1 shows the comparison in terms of number of components, voltage gain, switches and the diodes voltage stress, type of input current and load. The variation in voltage gain at various duty cycle is shown in Fig. 5. shows the variation of voltage gain with duty cycle. Converter [7] and [9] provide the same gain and similarly, converter [10] and [20] provides the same gain. The main advantages of the proposed circuit against the classical boost converter and compared converter are its low voltage stress and high voltage gain for a given duty cycle. This allows the use of reduced resistance switches that further decreases the conduction losses.

TABLE 1. Comparison of converters.

Converter	Boost [1]	Converter [7]	SC [8]	SI [9]	SH-SL [10]	ASL-SU2C [20]	Proposed Converter
Inductor	1	1	1	2	4	3	5
Diode	1	1	3	4	7	2	8
Switches	1	2	1	1	2	2	2
Capacitor	1	1	3	1	1	3	3
Voltage gain	$\frac{1}{1-d}$	$\frac{1+d}{1-d}$	$\frac{2}{1-d}$	$\frac{1+d}{1-d}$	$\frac{1+3d}{1-d}$	$\frac{1+3d}{1-d}$	$\frac{1+5D+2D^2}{1-d}$
Noramlised Voltage stress of Switches	1	$\frac{G+1}{2G}$	$\frac{1}{2}$	1	$\frac{G+1}{2G}$	$\frac{1}{1+3d}$	$\frac{1+d}{(1-d)G}$
Normalised Voltage stress of P-SL Diode	-	-	-	$\frac{G-1}{2G}, \frac{1}{G}$	$\frac{G-1}{4G}, \frac{1}{G}$	-	$\frac{1-G}{4G(1-d)}, \frac{1}{G}$
Normalised Voltage stress of SC Diode	-	-	-	-	-	$\frac{2}{1+3d}$	$\frac{2}{G(1-d)}$
Normalised Voltage stress of Output Diode	1	$\frac{G+1}{G}$	$\frac{1}{2}$	1	$\frac{G+1}{G}$	-	-
Constant input current	No	No	Yes	Yes	No	No	No
Load Type	Grounded	Floating	Grounded	Grounded	Grounded	Grounded	Grounded

TABLE 2. Simulation parameters.

Parameters	Values
Output Power	500 W
V_{in}	50 V
V_{out}	400 V
Switching Frequency (f)	50 kHz
Inductors	L_{B1}, L_{B2}, L_{Z1}, L_{Z2}=180 µH, L_{Z3}=300 µH
Capacitors	C_Z, C_B=470 µF
	C_O=470 µF
Load (Resistive)	320 Ω

TABLE 3. Experimental parameters.

Parameters	Typical Values
V_{in}	50 V
V_{out}	400 V
Output Power	500 W
Switching Frequency (f)	50 kHz
Inductors	L_{B1}, L_{B2}, L_{Z1}, L_{Z2}=180 µH
	L_{Z3}=300 µH (Core type)
Capacitors	C_Z, C_B= 470µF/400V
	C_O= 470µF/450V
Diodes D_{B1}, D_{B2}, D_{B3}	NTE5812HC
Diodes D_{B1}, D_{B2}, D_{B3}	NTE5812HC
Diode D_B and D_Z	NTE5814HC
Switches S_B and S_Z	IXTH16N20D2

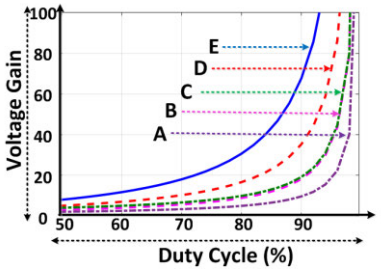

FIGURE 10. Comparison of converter in terms of voltage gain versus duty ratio. A: conventional boost converter, B: converter in [7] and [9], C: converter in [8], D: converter in [10]–[20], E: Proposed converter.

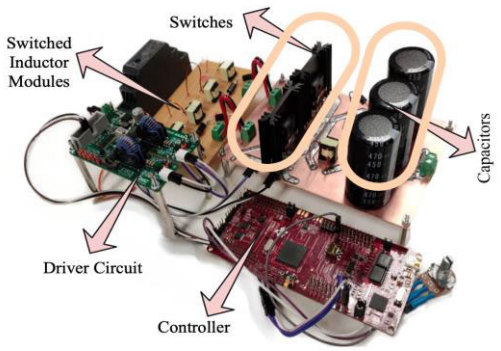

FIGURE 11. Prototype of proposed converter (500W).

VI. SIMULATION AND EXPERIMENTAL RESULTS

Table 2 shows the simulation parameters of the proposed hybrid zeta-boost converter. The performance of the proposed converter is tested in the Renewable Energy Lab (REL) at various power level, and the experimental parameters are given in Table 3. Fig. 11 shows the designed prototype of the proposed converter for power 500 W. Initially, the converter is simulated with ideal component and operates to generate output voltage 400 V. Fig. 12 shows the waveforms obtained during steady-state operation. From Fig 12, it is observed that the voltage and current at the output terminal are 400.1 V and 1.25 A, respectively for the input voltage values of 50 V. The input current is continuous and has an average value of 10.01 A. When the switches S_Z and S_B turned ON, the voltage across switches S_Z and S_B is 150 V, and the average value of current through S_Z and S_B is 4.1 A, respectively. When the switches S_Z and S_B turned ON, the inductors currents increases with a positive slope due to magnetization, the voltages across inductors L_{B1}, L_{B2}, L_{Z1}, L_{Z2} is 50 V, and the voltage across inductor L_{Z3} is 150 V.

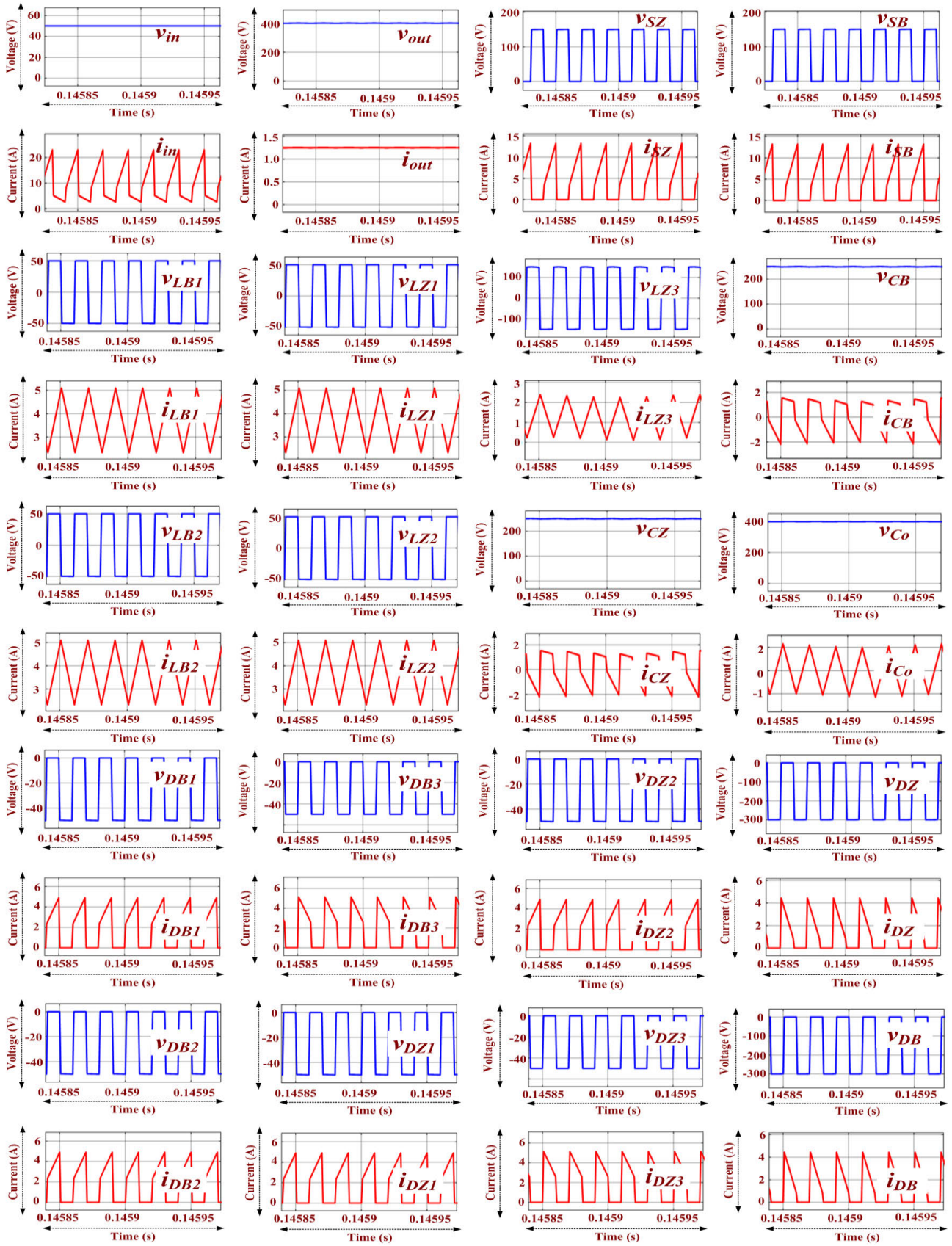

FIGURE 12. Simulation results for the proposed converter under steady-state conditions.

FIGURE 13. Voltage and current at input and output terminal.

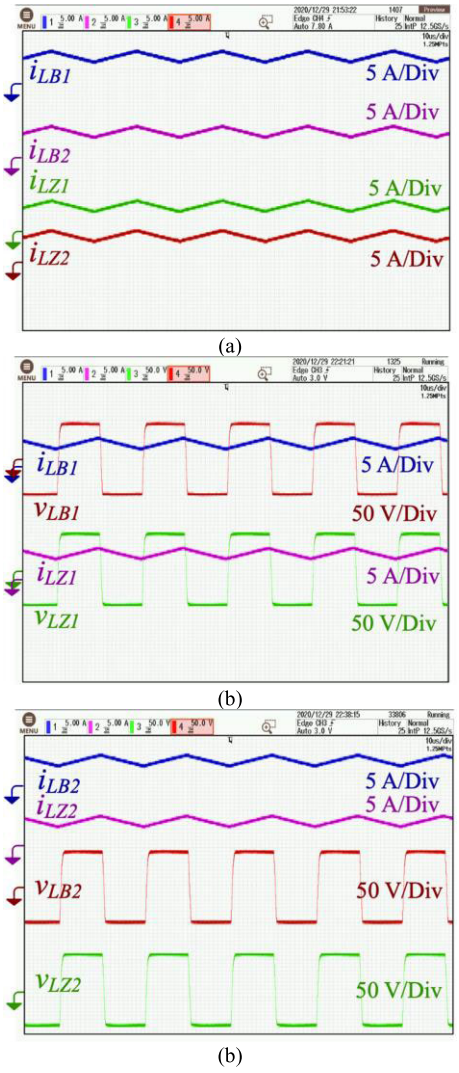

FIGURE 14. Switched inductors waveforms, (a) Current through inductors of switched inductor modules, (b) Current and voltage for inductors L_{B1} and L_{Z1}, (c) Current and voltage for inductors L_{B2} and L_{Z2}.

When the switches S_Z and S_B turned OFF, the inductors currents through the inductors decreases with a negative slope due to demagnetization, the voltages across inductors L_{B1}, L_{B2}, L_{Z1}, L_{Z2} is -50 V, and the voltage across inductor L_{Z3} is equal to -150 V. The average current through inductors L_{B1},

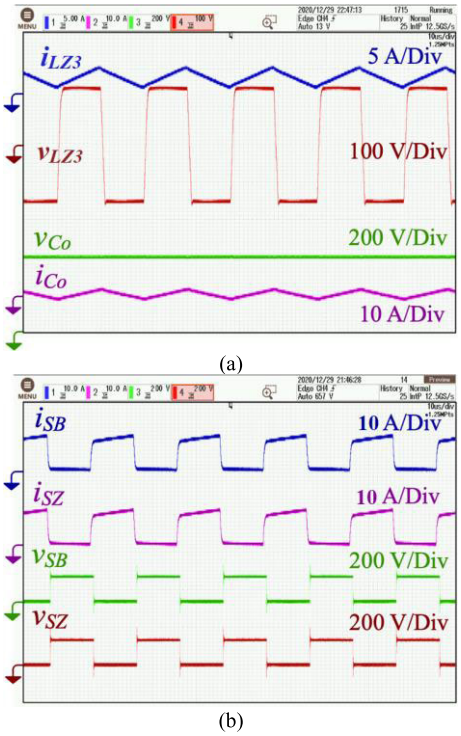

FIGURE 15. Voltage and current waveforms for (a) inductor L_{Z3} and capacitor C_o, (b) switches S_B and S_Z.

L_{B2}, L_{Z1}, and L_{Z2} is equal to 3.757 A, and the average current through inductor L_{Z3} is 1.25 A. The observed value of voltage across C_Z and C_B capacitors is equal to 250 V, and the voltage across C_o capacitor is 400 V. When the switches S_Z and S_B turned ON, the diodes D_{B1}, D_{B2}, D_{Z1} and D_{Z2} are forward biased, and diodes D_{B3}, D_{Z3}, D_B and D_Z are reversed biased and vice versa when switches S_Z and S_B turned OFF. The blocking voltage of diodes D_{B1}, D_{B2}, D_{Z1}, D_{Z2}, D_{B3}, D_{Z3} is -50 V, and blocking voltage of diodes D_B and D_Z are -300 V, respectively. The average current through diodes D_{B1}, D_{B2}, D_{Z1}, D_{Z2} is 1.779 A, the average current through diodes D_{B3}, D_{Z3} is 1.979 A, and the average current through diodes D_B and D_Z are 1.388 A.

From Fig. 13, it is observed that output voltage 399.6 V is generated at the output when input voltage 50.1 V given at the input terminal and load is 320 Ω. The average input and output currents are 10.72 A and 1.25 A, respectively. Fig. 14(a) shows the waveforms of the current through inductors of switched inductor during steady-state conditions. The inductor L_{B1}, L_{B2}, L_{Z1} and L_{Z2} are magnetized during ON state and demagnetized in ON state with the average current 3.84 A, 3.81 A, 3.84 A and 3.86 A, respectively. From Fig.14(b), it is observed that the inductors L_{B1} and L_{Z1} charged with voltage 49.9 V and -49.8 V, and discharged with voltage 49.4 V and -49.3 V, respectively.

From Fig. 14(c), it is observed that the inductors L_{B2} and L_{Z2} charged with voltage 49.8 V and -49.9 V, and discharged with voltage 49.4 V and -49.5 V, respectively. From Fig. 15(a), it is observed that the voltage across inductor

L_{Z3} in ON and OFF states are 149.8 V and −149.3 V, respectively with the average current 1.24 A. It is seen that the capacitor C_o charged and discharged in ON and OFF state, respectively with the average voltage 399.6 V. From Fig. 15(b), it is observed that the voltage across switches S_B and S_Z is 150.1 V and 149.1 V, respectively. The average current through switches S_B and S_Z is 4.34 A and 4.4 A, respectively. The efficiency of the converter is observed for various power level 100 W to 500 W. The efficiency and power loss distribution plots at power 500 W are depicted in Fig. 16. The 92.93% efficiency is observed when load power is 500 W. It is observed that 39.2% and 37.3% of total power loss observed in the diode and switches, respectively.

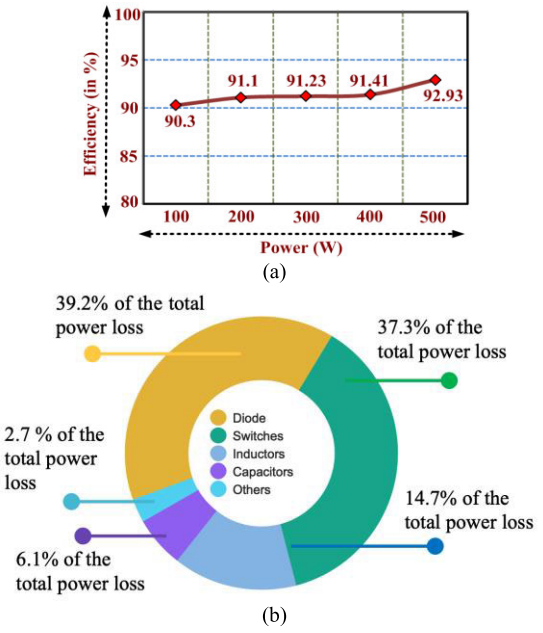

FIGURE 16. Plot (a) Efficiency versus power (b) Power loss distribution of the proposed converter at power 500W and voltage gain 8.

VII. CONCLUSION

A novel hybrid converter based on zeta and boost converter, with active quad switched-inductor (AQSL) is proposed to achieve high voltage gain. The input current division between the switches due to AQSL reduces the inductor and switch current stress. Moreover, the voltage across semiconductor devices are low compared to the output voltage. Therefore, low voltage and current stress across semiconductor components lead to the use of low rating components, reducing the cost and conduction losses. The voltage gain offered by the proposed circuit is more than conventional boost converter and various other switched capacitor/ switched inductor based converters. The CCM and DCM analysis, boundary condition, design consideration, effect of parasitic on voltage gain and comparison with other high-gain converters are explained in detail. The proposed configuration, in comparison with topologies employing the same concepts, provides the merits like the high voltage gain with low voltage stresses across the semiconductor components. The performance of the proposed topology is verified through simulation and experimental work, and efficiency of the designed prototype is 92.93% at power 500W.

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