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Analysis of TSV-Induced Mechanical Stress and Electrical Noise Coupling in Sub 5-nm Node Nanosheet FETs for Heterogeneous 3D-ICs

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ABSTRACT Through-silicon via (TSV)-induced mechanical stress and electrical noise coupling effects on sub 5-nm node nanosheet field-effect transistors (NSFETs) were investigated comprehensively compared to fin-shaped FETs (FinFETs) using TCAD for heterogeneous 3D-ICs. TSV-induced channel length directional stress (S_{ZZ}) predominantly causes variations of on-state current (ΔI_{on}). NSFETs exhibit the greater ΔI_{on} than FinFETs because electron velocities and densities in channels vary with respect to S_{ZZ} in the same directions for NSFETs but do the opposite for FinFETs. Nevertheless, TSV-induced mechanical stress is negligible when TSV is farther than keep-out zone. Meanwhile, TSV signals can be coupled to operating devices through substrate and induce capacitive and back-bias noise coupling currents (I_{cap}, I_{b-b}). NSFETs exhibit the greater $|I_{cap}|/I_{on}$ than FinFETs because its wider source/drain (S/D) epitaxies form larger depletion capacitances between drain and punch-through stopper (PTS). On the other hand, the $|I_{b-b}|/I_{on}$ is smaller for NSFETs because its parasitic bottom transistor alleviates back-bias-induced potential barrier lowering. Furthermore, wide diameter of Cu of TSV increases $|I_{b-b}|/I_{on}$ only, but short rise time of TSV signals increases both $|I_{cap}|/I_{on}$ and $|I_{b-b}|/I_{on}$. Unfortunately, conventional devices cannot satisfy criterion for analog applications ($|I_{cap}$, $I_{b-b}|/I_{on} < 0.5\%$); therefore, a new strategy inserting bottom oxide (BOX) beneath the S/D with undoped PTS is suggested. The $|I_{cap}|/I_{on}$ for NSFETs decreases by undoped PTS, but not for FinFETs due to a remnant depletion capacitance between fin and PTS. The $|I_{b-b}|/I_{on}$ for NSFETs decreases remarkably due to completely blocked I_{b-b} path, but FinFETs still have I_{b-b} path under the fin. Therefore, NSFETs with BOX and undoped PTS are the most suitable for sub 5-nm node heterogeneous 3D-IC, especially in analog applications.

INDEX TERMS Nanosheet FETs, fin-shaped FETs, sub 5-nm node, heterogeneous 3D-ICs, through-silicon vias (TSVs), TSV-induced mechanical stress, TSV-induced electrical noise coupling, TCAD simulations.

I. INTRODUCTION

Silicon fin-shaped field-effect transistors (FinFETs) have been used in the industry since the 22-nm node with excellent gate-to-channel controllability. Since then, they have been successfully scaled down for the 7-nm node [1]–[4]. Concurrently, the number of fins per active area has been decreased from three to one to minimize the standard cell height [5], [6]. However, the significantly fewer fins decrease the drive current by reducing the effective channel width (W_{eff}) [7], and performance modulation that depends on the number of fins is quantized [8]. Meanwhile, multi-stacked silicon gate-all-around (GAA) nanosheet FETs (NSFETs) demonstrate superior gate electrostatics, larger W_{eff} per footprint, and higher drive current than FinFETs below the 7-nm node [7], [9], [10]. Also, NSFETs allow the drive current to

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be linearly modulated by adjusting the NS channel width. Consequently, NSFETs have been regarded as more suitable for scaling the footprint [8].

Recently, heterogeneous three-dimensional integrated circuit (3D-IC) technologies have been highlighted to dramatically increase transistor density without further scaling of the transistors themselves [11]–[13]. In addition, heterogeneous 3D-IC structures enable different functional die to be integrated into one systems-in-package without degrading performance [11], [13]. In stacking die, through-silicon vias (TSVs) should be formed on each die to transmit electrical signal or to deliver supplied power. Therefore, TSV is one of the key components in determining heterogeneous 3D-IC performance.

However, TSVs inevitably impact on operations of nearby devices. One effect is the mechanical stress applied to adjacent devices due to different coefficients of thermal expansion (CTE) between the TSV filling metal and the silicon [14]–[16]. In a via-middle TSV process, the final cooling cycle is known to determine the TSV-induced mechanical stress [17]. Another effect is the electrical noise coupling between the TSVs and operating devices. TSV filling metal surrounded by a dielectric layer (liner) shares common substrate with devices, then noise current can be injected into the devices through the substrate [18]–[21]. This noise current can degrade the performance significantly in sensitive applications such as analog and RF circuits [20]. Analog and RF circuits have traditionally been developed by planar MOSFET-based logic technology; however, short-channel effects limit the planar MOSFETs to be scaled below 20-nm node. Therefore, alternative devices including FinFETs and GAAFETs are being studied to take advantages of advanced logic power/performance/area and of realizing co-integration of analog/RF and digital applications [22], [23]. Here, analog/RF applications require more strict criterions for noise current than digital applications [16], thus satisfying the criterions for analog/RF is essential. Until now, several studies have focused on TSV effects on FinFETs [18], [19], [24], but rarely on GAA-NSFETs.

This work, therefore, presents a comprehensive analysis of these TSV effects on sub 5-nm node GAA-NSFETs using fully calibrated technology computer-aided design (TCAD) (Fig. 1). Sub 5-nm node FinFETs were compared quantitatively to determine which devices are more suitable for heterogenous 3D-ICs. Specifically, the impacts of the TSV on channel stress and on-state current (I_{on}) was analyzed in terms of TSV locations. Next, TSV-induced noise coupling current is analyzed in terms of TSV geometry and TSV signals. Finally, a new strategy to alleviate TSV-induced noise coupling current is suggested, and the most suitable devices for heterogeneous 3D-ICs are explored.

II. SIMULATION STRUCTURES AND METHODOLOGY

In this study, sub 5-nm node n-type three-stacked silicon NSFETs and FinFETs integrated with a TSV were simulated using Synopsys TCAD Sentaurus [25]. First, the NSFETs and

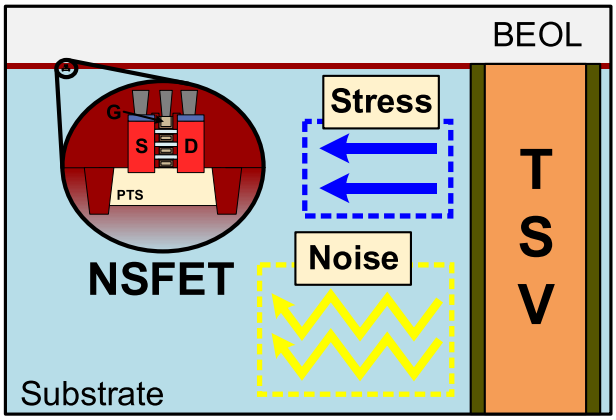

FIGURE 1. Schematic of heterogeneous 3D-IC and TSV-induced mechanical stress and electrical noise coupling effects on devices.

FinFETs [7], [26] underwent the same process flows, followed by via-middle TSV formation [17]. The overall simulation structures containing both a device and a TSV are shown in the Fig. 2a, where two cases of TSV placements were considered: the TSV horizontal to and vertical to the devices. Fig. 2b shows detailed structures of the NSFETs and FinFETs and cross-sectional views of the NSFETs. Source/drain (S/D) epitaxies were formed with $Si_{0.98}C_{0.02}$ and were wrapped with Ti-silicide to reduce S/D resistance [7]. A gate-last process for high-k dielectric (HfO_2)/metal gate (TiN) stacks was used with tungsten (W) as the M0 metal. Substrate contacts were located far from the devices to exclude effects on TSV noise coupling [18], [19].

The S/D epitaxies were highly doped with 1×10^{20} cm^{-3} phosphorus; both silicon NS channels and silicon substrate were undoped (1×10^{15} cm^{-3}). The doping concentration of punch-through stopper (N_{PTS}) was as high as 5×10^{18} cm^{-3} of boron to minimize leakage current flowing through the substrate. In addition, the dielectric constants of the interfacial layer (SiO_2), spacer, and high-k dielectric (HfO_2) were 3.9, 3.9, and 22.0, respectively. Contact resistivity of the wrap-around contact was $10^{-9}\Omega\cdot$cm^2 [27], and operation voltage (V_{DD}) was 0.7 V. The on-state condition was defined as the gate (V_{gs}) and drain voltages (V_{ds}) of the V_{DD} and the off-state condition was defined as the V_{gs} of 0 and the V_{ds} of the V_{DD}.

The TSV structure and its cross-section are shown in Fig. 2c. Cu, Ta, and SiO_2 were used as the TSV filling metal, diffusion barrier, and dielectric liner, respectively. The Cu was 5 μm in diameter (D_{Cu}), and the barrier and liner were 5 and 200 nm thick, respectively (T_{bar}, T_{lin}) [17]. The substrate thickness and height of the TSVs (H_{TSV}) were same as 15 μm, considering wafer thinning in 3D-ICs [28]. The CTEs of Cu, Ta, SiO_2, and Si were 17.7, 6.3, 0.51, and 3.05 ppm/°, respectively. Geometrical and process parameters are summarized in Table 1.

For the Sentaurus device simulation [25], drift-diffusion model equations with Poisson and carrier continuity equations were self-consistently solved for carrier transport. Lombardi, inversion and accumulation layer, thin-layer, and

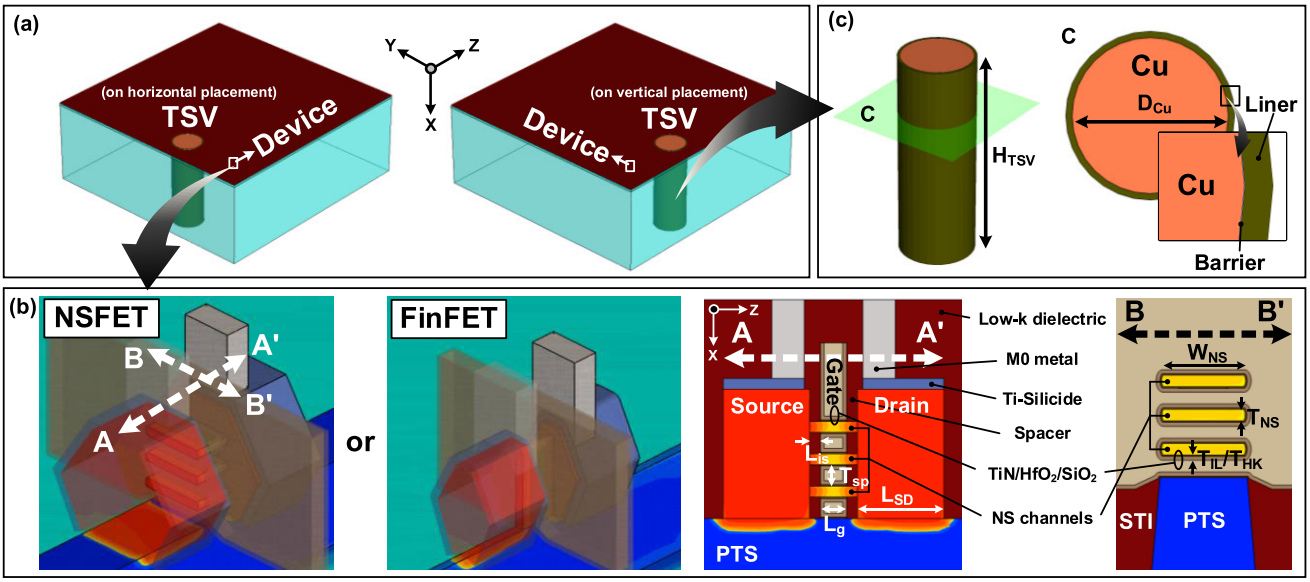

FIGURE 2. (a) Overall simulation structures of heterogeneous 3D-ICs containing a device and TSV. Detailed structures of (b) sub 5-nm node three-stacked NSFETs, FinFETs, and (c) the TSV.

TABLE 1. Geometrical and process parameters for sub 5-nm node devices and TSV.

Parameters	Values
Gate length (L_g)	12 nm
Spacing thickness (T_{sp})	10 nm
S/D length (L_{SD})	40 nm
Inner-spacer length (L_{is})	5 nm
NS thickness (T_{NS}) / Fin height (H_{fin})	5 nm / 46 nm
Interfacial layer and HfO_2 thickness (T_{IL}, T_{HK})	0.7 / 1.7nm
NS width (W_{NS}) / Fin width (W_{fin})	38 nm / 5 nm
S/D doping concentration (N_{SD})	$1x10^{20}$ cm^{-3}
PTS doping concentration (N_{PTS})	$5x10^{18}$ cm^{-3}
Cu diameter (D_{Cu})	5 µm
Barrier / Liner thickness (T_{bar}/T_{lin})	5 nm / 200 nm
TSV height (H_{TSV})	15 µm
CTEs of Cu, Ta, SiO_2, and Si	17.7, 6.3, 0.51, 3.05 ppm/°C

low-field ballistic mobility models were also included to compute carrier mobility, considering several contributions to carrier mobility degradation. Furthermore, Shockley-Read-Hall, Auger, and Hurkx band-to-band tunneling models were used for the generation-recombination process. A density-gradient model was included to examine quantum confinement effects, and a deformation potential model was employed to determine the strain dependency of effective mass, effective density-of-states, carrier mobility, and band structure. Finally, the Slotboom bandgap narrowing model explored bandgap energy narrowing relative to the doping concentration.

Both devices share the physical parameters fully-calibrated by fitting I-V curves of 10-nm silicon FinFETs [3] as presented in a previous paper [29]. By adapting identical physical parameters, characteristics of FinFETs and NSFETs are compared fairly. First, subthreshold swing and drain-induced barrier lowering were fitted by adjusting the S/D doping concentration and its diffusion toward the channels. Then, saturation velocity and low-field mobility of the carrier were adjusted by fitting the drain current in the saturation and linear regions, respectively.

III. ANALYSIS OF TSV EFFECTS ON NSFETs AND FinFETs

A. TSV-INDUCED MECHANICAL STRESS EFFECTS ON NSFETs AND FinFETs

Because Cu having a higher CTE than Si is constrained by a TSV hole, the mechanical stress is applied to the Si substrate and NSFETs near the TSV at room temperature after the TSV process [17], [30]. Fig. 3a shows the mechanical stress profiles of the z- and y-direction components (S_{ZZ} and S_{YY}, respectively) applied to the Si substrate. TSV-induced x-direction stress component is negligible, thus not addressed in this work [17]. According to the placements of the TSV, the different directional TSV-induced mechanical stress is applied to the devices, so two cases of TSV placements were considered: the TSV on horizontal to and vertical to the devices. Fig. 3b shows channel stress of devices when distance from the center of the TSV to the devices (d_{FET}) varies from 3.5 to 20 μm. Here, the S_{ZZ} (S_{YY}) is in the channel length (width) direction. When the TSV is horizontal to NSFETs, the S_{ZZ} (S_{YY}) of the NS channels at the d_{FET} of 3.5 μm decreases (increases) 140 (170) MPa compared to when the d_{FET} is 20 μm. Likewise, when the TSV is placed vertically to NSFETs, the S_{ZZ} (S_{YY}) increases (decreases) by similar magnitudes. However, TSV-induced mechanical stress on the devices greatly diminished as the d_{FET} becomes greater than 15 μm.

Fig. 4 shows TSV mechanical stress-induced I_{on} variations (ΔI_{on}) of NSFETs and FinFETs. Here, a device at the d_{FET} of 30 μm has almost negligible TSV-induced mechanical

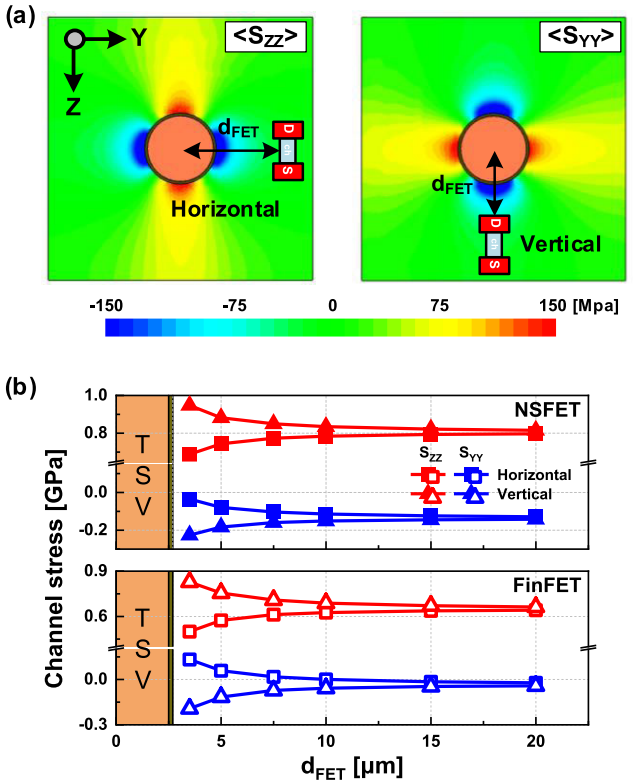

FIGURE 3. (a) TSV-induced S_{ZZ} and S_{YY} profiles and two cases of the TSV placements: TSV on the horizontal and vertical placements to the devices (device size is exaggerated). (b) S_{ZZ} and S_{YY} of the channels according to the d_{FET}.

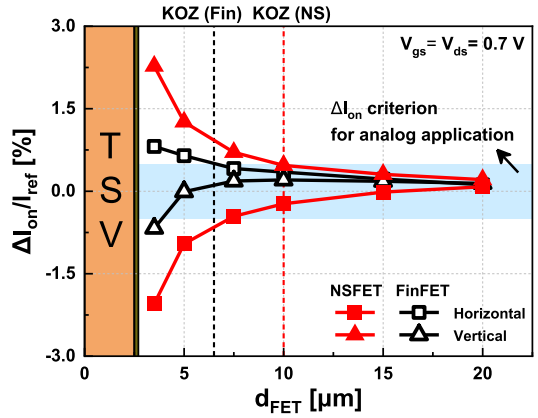

FIGURE 4. TSV mechanical stress-induced $\Delta I_{on}/I_{ref}$ according to the d_{FET} for both NSFETs and FinFETs. The dashed lines show KOZs for analog applications.

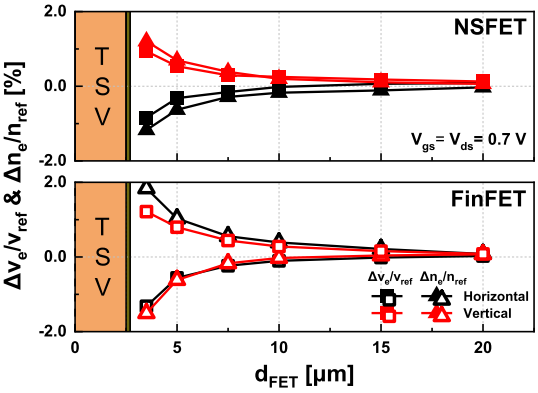

FIGURE 5. $\Delta v_e/v_{ref}$ and $\Delta n_e/n_{ref}$ of the channels according to the d_{FET} for NSFETs and FinFETs.

stress effects (not shown in the Fig. 3). This was chosen as a reference for the following analysis. Off-state currents of the reference device is fixed to 1 nA, and I_{ref} indicates the I_{on} of the reference devices. Interestingly, NSFETs and FinFETs show opposite trends for ΔI_{on} in relation to the d_{FET}. The I_{on} of NSFETs decreases (increases) with a shorter d_{FET} when the TSV is located horizontal (vertical) to the device, whereas FinFETs exhibit opposite trends. In addition, the $|\Delta I_{on}|/I_{ref}$ is greater for NSFETs than for FinFETs; the maximum $|\Delta I_{on}|/I_{ref}$ is 2.3 % for NSFETs but 0.8 % for FinFETs. For analog applications, the $|\Delta I_{on}|/I_{ref}$ should be less than 0.5 % [16], meaning that the keep-out zone (KOZ) is 10 μm for NSFETs and 6.5 μm for FinFETs.

The ΔI_{on} tendencies caused by TSV-induced mechanical stress can be understood through electron velocity (v_e) and electron density (n_e) (Fig. 5). The v_e and n_e are averaged values over the channel region at on-state, and the I_{on} is proportional to the multiplication of the v_e and n_e. For NSFETs, signs of the Δv_e and Δn_e according to the d_{FET} are the same, whereas those of FinFETs are the opposite. Consequently, the $|\Delta I_{on}|/I_{ref}$ according to the d_{FET} is greater for NSFETs than for FinFETs. Furthermore, the $|\Delta n_e|/n_{ref}$ of FinFETs is greater than $|\Delta v_e|/v_{ref}$, so the ΔI_{on} directions follow those of the Δn_e, where n_{ref} (v_{ref}) is n_e (v_e) of reference device.

In more detail, the ΔS_{ZZ} affects the ΔI_{on} much more than the ΔS_{YY} [31], [32], in the other words, the Δv_e and Δn_e are predominantly determined by the ΔS_{ZZ} of the channels. The Δv_e tendencies of both devices match well with the ΔS_{ZZ}; tensile S_{ZZ} boosts the v_e (Fig. 3b and 5). Next, surface orientations where electrons mainly reside should be consider-ed to understand Δn_e tendencies. Electrons mainly flow near (100) surfaces in NSFETs, which are the top and bottom surfaces of the NS channels, but in FinFETs, they flow near (110) surfaces, which are the sidewalls of the fin channels. Flat-band voltages of the devices decrease in (100) surfaces and increase in (110) surfaces as the S_{ZZ} of the channels becomes more tensile; consequently, threshold voltages decrease and increase, respectively [33]. As a result, the n_e of NSFETs increases, but that of FinFETs decreases as the d_{FET} decreases on vertical placements.

B. TSV-INDUCED NOISE COUPLING EFFECTS ON NSFETs AND FinFETs

Besides the TSV-induced mechanical stress effects, TSV signals can be electrically coupled to operating devices [18]–[21]. Fig. 6a presents a transient I_{on} characteristic of NSFETs located horizontally 10 μm away from TSV transmitting a step voltage signal (V_{TSV}) with rise time (t_{rise}) of 10 ps (devices locating vertical to TSV are not shown because the

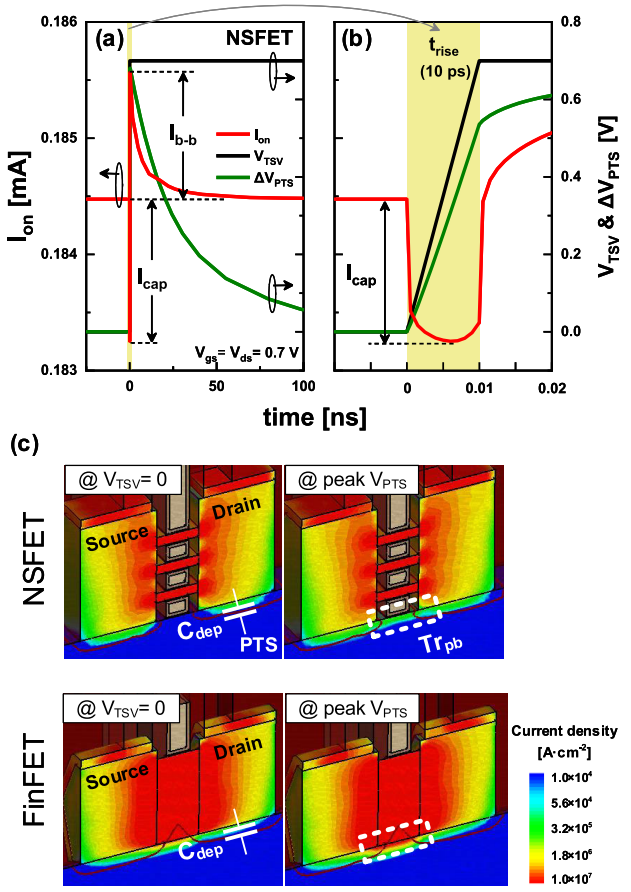

FIGURE 6. (a) A transient I_{on} characteristic of NSFETs as a step V_{TSV} passes through the TSV (t_{rise} = 10 ps). (b) Enlarged view of (a) during V_{TSV} switching from 0 o V_{DD}. (c) I_{on} densities of the NSFETs and FinFETs at the V_{TSV} of 0 and peak V_{PTS} (white boxes indicate the regions where back-bias effects occur).

result is the same as horizontal locations). The V_{TSV} varies electrostatic potential in the PTS (V_{PTS}) and induces two types of noise coupling currents ($I_{coupling}$): capacitive (I_{cap}) and back-bias coupling currents (I_{b-b}). Capacitive coupling occurs at depletion capacitance (C_{dep}) between drain and PTS while the V_{TSV} switches from 0 to V_{DD}, and the I_{cap} is defined as the maximum I_{on} reduction during V_{TSV} switching (Fig 7b). The I_{cap} is proportional to C_{dep} and voltage change per time between drain and PTS, that is, the I_{cap} can be described as (1).

$$I_{cap} \propto C_{dep} \frac{\delta(V_{ds} - V_{PTS})}{\delta t} \quad (1)$$

Next, the back-bias coupling occurs as the increased V_{PTS} lowers potential barrier of the region under the channels (Fig. 6c). Especially, in NSFETs, this region is called parasitic bottom transistor (Tr_{pb}), where gate dielectric layers and gate metal are formed unlike FinFETs [34]. The maximum current induced by the back-bias effect is defined as the I_{b-b}, which occurs at the peak V_{PTS}. The back-bias coupling only affects the Tr_{pb} and the sub-fin region, not the NS and fin channels (Fig. 6c) [35].

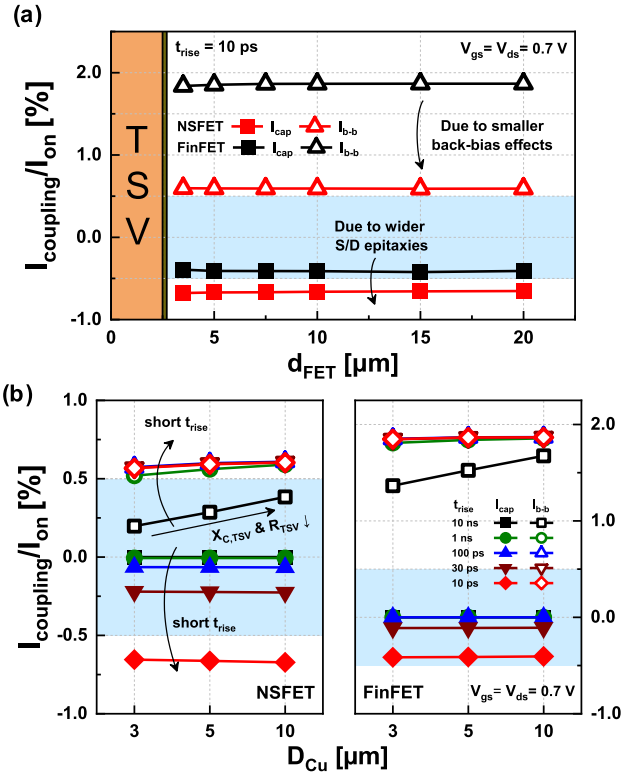

FIGURE 7. (a) $I_{coupling}/I_{on}$ according to d_{FET} for t_{rise} = 10 ps and (b) according to the D_{Cu} and t_{rise} at d_{FET} = 10μm.

The $I_{coupling}/I_{on}$ according to d_{FET} at t_{rise} of 10 ps is shown in Fig. 7a. Unlike the TSV-induced mechanical stress effects on devices dramatically reducing in KOZ (Fig. 4), the $I_{coupling}/I_{on}$ is hardly diminished. In addition, NSFETs show the larger $|I_{cap}|/I_{on}$ compared to FinFETs because the wider S/D epitaxies of NSFETs result in the greater C_{dep}. On the other hand, NSFETs have the smaller $|I_{b-b}|/I_{on}$ than FinFETs because gate electrostatic of the Tr_{pb} can alleviate the back-bias-induced potential barrier lowering, happened under the channel.

Impacts of the D_{Cu} of TSV and t_{rise} of V_{TSV} are also analyzed as critical factors determining $I_{coupling}$ in sub 5-nm node devices (Fig. 7b). The $|I_{cap}|/I_{on}$ is not affected by the D_{Cu} because it does not affect either C_{dep} or $\delta(V_{ds}$-$V_{PTS})/\delta t$ significantly. On the other hand, the $|I_{b-b}|/I_{on}$ increases with large D_{Cu} and short t_{rise}. The relation among the D_{Cu}, t_{rise}, and I_{b-b} can be understood using simple RC components described in Fig. 8a. The ΔV_{PTS} can be described as (2).

$$\Delta V_{PTS} = \frac{R_d + X_{C,dep}}{R_d + R_{PTS} + R_{sub} + R_{TSV} + X_{C,TSV} + X_{C,dep}} V_{TSV} \quad (2)$$

where R_d, R_{PTS}, R_{sub}, R_{TSV}, $X_{C,TSV}$, and $X_{C,dep}$ are resistances of the drain, PTS, substrate, TSV, and reactances of the C_{TSV} and C_{dep}, respectively. The large D_{Cu} decreases both the $X_{C,TSV}$ (by increased C_{TSV}) and R_{TSV} (by widen TSV cross-section), then increases the ΔV_{PTS} (Fig. 8b). However, the impacts of the D_{Cu} on the $|I_{b-b}|/I_{on}$ are diminished at

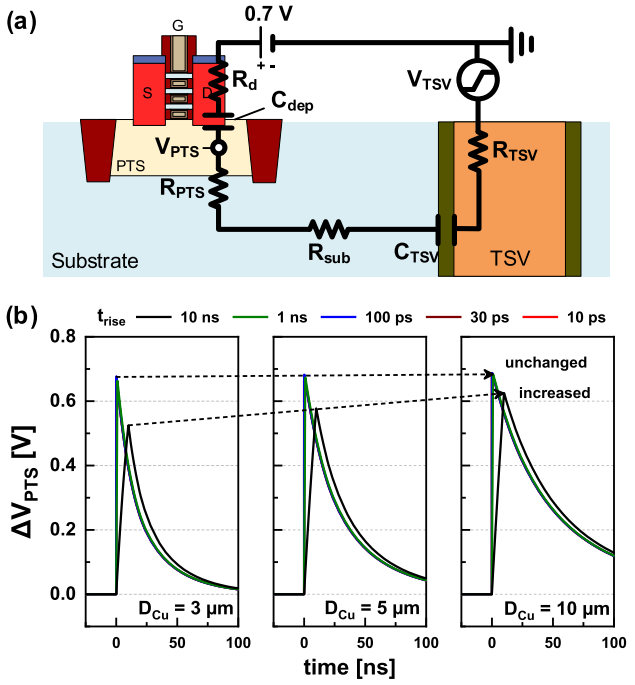

FIGURE 8. (a) Schematic of RC components between device and TSV. (b) ΔV_{PTS} of NSFETs according to the t_{rise} and D_{Cu} (plots for t_{rise} from 1 ns to 10 ps are overlapped).

the short t_{rise}. This can be understood in frequency domain, where short t_{rise} in time domain is equivalent to high frequency [36]. Thus, as the t_{rise} is shorter, the $X_{C,TSV}$ and $X_{C,dep}$ become smaller and finally almost neglectable when the t_{rise} is shorter than 1 ns. As a result, minor ΔV_{PTS} with respect to the D_{Cu} is observed at short t_{rise}.

Unfortunately, both NSFETs and FinFETs do not satisfy the criterion for analog applications ($|I_{coupling}|/I_{on} < 0.5\%$) at the short t_{rise} [16]. To solve this problem, we suggest a new strategy for alleviating the $I_{coupling}$ in following *subsection C*.

C. A STRATEGY FOR ALLEVIATING TSV-INDUCED NOISE COUPLING CURRENT

To suppress the $I_{coupling}$, several strategies such as guard rings surrounding TSVs or susceptible devices [19], [20], [37], ground TSVs [38], [39], and placing substrate contact close to susceptible devices [18], [19] have already been suggested. However, these strategies require additional area for guard rings and ground TSVs, or additional layout adjustment for substrate contact. Hence, we suggest a new strategy to alleviate the TSV-induced $I_{coupling}$ dramatically without further area consumption and layout modification. The key feature of our strategy is isolating S/D epitaxies from the PTS region using oxide layers, called bottom oxide (BOX) [40], [41], because both the I_{cap} and I_{b-b} mainly come from PTS to drain (Fig. 9a). As expected, both the $|I_{cap}|/I_{on}$ and $|I_{b-b}|/I_{on}$ remarkably decrease with a 10 nm thick BOX, especially for the $|I_{b-b}|/I_{on}$ (Fig. 9b). To analyze the I_{cap} of devices with BOX, the C_{dep} in (1) should be substituted as $(C_{BOX}C'_{dep})/(C_{BOX} + C'_{dep})$ where C_{BOX} is BOX capacitance and C'_{dep} is depletion capacitance formed under BOX. Since both C_{BOX} and C'_{dep} are smaller than C_{dep}, $|I_{cap}|/I_{on}$ decreases with BOX. On the other hand, the $|I_{b-b}|/I_{on}$ can be significantly decreased since the I_{b-b} is blocked by BOX. Especially, I_{b-b} is completely blocked in NSFETs, whereas that of FinFETs can still penetrate through the bottom of the fin channel into the drain. Therefore, NSFETs with BOX are more robust to back-bias coupling.

Another merit of inserting the BOX is that the N_{PTS} can be lowered without punch-through effects in the substrate. Fig. 9c shows the $I_{coupling}/I_{on}$ of devices with BOX as the N_{PTS} lowers from 5×10^{18} to 1×10^{15} cm^{-3}(undoped). Low N_{PTS} decreases the C'_{dep} and slows down response time of carrier (hole) in PTS to V_{TSV} signals [42], which decreases $\delta(V_{ds}\text{-}V_{PTS})/\delta t$ for both devices. However, for FinFETs, a remnant depletion capacitance is formed between the fin and PTS of low N_{PTS} by S/D dopant diffusion into the PTS (Fig. 9d). This depletion capacitance causes the remnant I_{cap} path, thus the $|I_{cap}|/I_{on}$ doesn't decrease effectively in FinFETs with the low N_{PTS}. Next, the $|I_{b-b}|/I_{on}$ is not affected by the N_{PTS} for NSFETs due to completely blocked I_{b-b} by BOX, whereas the $|I_{b-b}|/I_{on}$ of FinFETs decreases as the N_{PTS} is lowered. This is because increase of the R_{PTS} and decrease of the C'_{dep} caused by the low

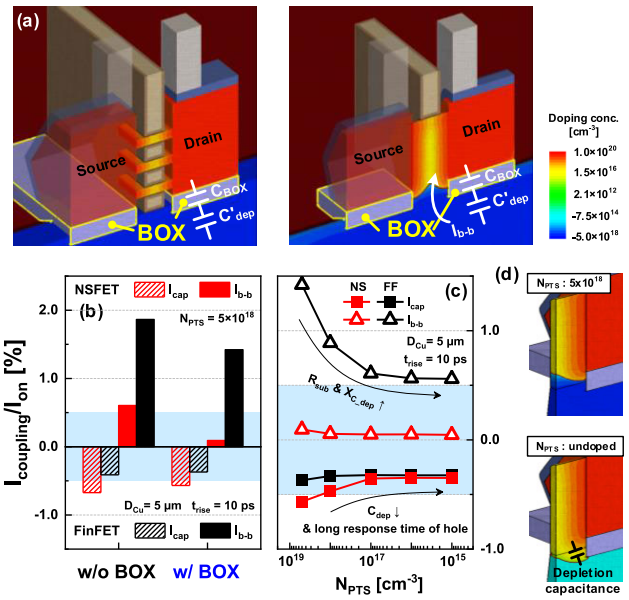

FIGURE 9. (a) Schematic of the NSFETs and FinFETs having BOX under the S/D. (b) $I_{coupling}/I_{on}$ with or without the BOX. (c) $I_{coupling}/I_{on}$ of the devices with BOX according to the N_{PTS}. (d) A remnant depletion capacitance between fin and PTS of low N_{PTS} formed by S/D dopant diffusion into the low PTS.

N_{PTS} reduce the ΔV_{PTS} according to (2). Finally, we summarized the $I_{coupling}/I_{on}$ in terms of the BOX, D_{Cu}, t_{rise}, and N_{PTS} (Fig. 10). As a conclusion, NSFETs having the BOX and undoped PTS demonstrate the best TSV-induced noise immunity and are the most suitable for analog applications using heterogeneous 3D-ICs.

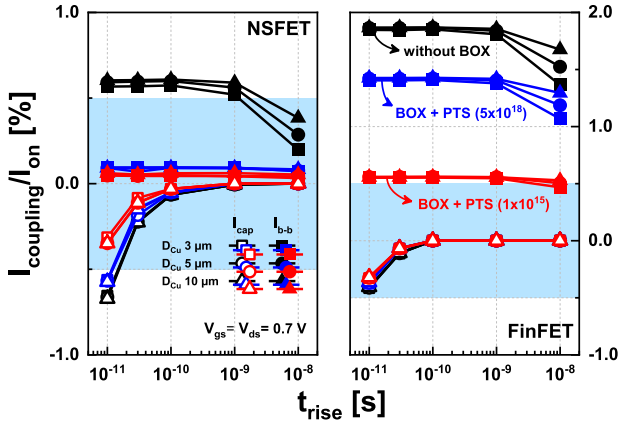

FIGURE 10. Immunity of $I_{coupling}/I_{on}$ according to with or without the BOX, D_{Cu}, t_{rise}, and N_{PTS}.

IV. CONCLUSION

TSV-induced mechanical stress effects and electrical noise coupling effects on sub 5-nm node n-type NSFETs were explored compared to FinFETs quantitatively. The TSV-induced ΔS_{ZZ} of the channels predominantly causes ΔI_{on} in both NSFETs and FinFETs. The large tensile S_{zz} of channels increases the v_e for both NSFETs and FinFETs, but simultaneously increases (decreases) the n_e for NSFETs (FinFETs) due to the different surface orientations where electrons reside. Thus, the $|\Delta I_{on}|/I_{ref}$ caused by TSV-induced mechanical stress is greater in NSFETs than in FinFETs. However, TSV-induced mechanical stress can be negligible for devices to be located more farther than the KOZ. Unfortunately, the $I_{coupling}$ caused by TSV-induced noise coupling is not diminished even with a large d_{FET}. NSFETs have the larger $|I_{cap}|/I_{on}$ and smaller $|I_{b-b}|/I_{on}$ than FinFETs because NSFETs have the larger C_{dep} and gate electrostatic of Tr_{pb} alleviate back-bias effects on the PTS. Furthermore, the $|I_{cap}|/I_{on}$ is not affected by the D_{Cu} of TSV, but the shorter t_{rise} causes the greater $|I_{cap}|/I_{on}$. On the other hand, the $|I_{b-b}|/I_{on}$ increases with the larger D_{Cu}, but neglectable with short t_{rise}. Unfortunately, both conventional NSFETs and FinFETs do not satisfy the criterion for analog applications ($|I_{coupling}|/I_{on} < 0.5$ %), thus a new strategy to insert BOX beneath the S/D with undoped PTS is suggested. Compared to conventional devices, both $|I_{cap}|/I_{on}$ and $|I_{b-b}|/I_{on}$ can be reduced due to low N_{PTS} and blocked I_{b-b} path, respectively. However, $|I_{cap}|/I_{on}$ and $|I_{cap}|/I_{on}$ do not decrease much in FinFETs because I_{cap} and I_{b-b} paths are still existent under the fin channel, thus FinFETs are unable to satisfy criterion for analog applications even with BOX and undoped PTS. Therefore, NSFETs with both BOX and undoped PTS are the most suitable for sub 5-nm node heterogeneous 3D-IC, especially in analog applications.

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