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Key Technology Practice of High-Speed Access and Research on the Temperature Dependence of Key Time Parameters Based on NAND Flash Memory

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ABSTRACT This paper focuses on the NAND flash memory as a data storage medium in the Internet of things data acquisition system, which plays an important role from beginning to end. The flow process of multi-channel sensor data sampling, holding, conversion, coding, and storage in the data acquisition system is described. The basic working principle and working process of NAND flash memory are introduced. Based on Interleaved Two-plane Program Technology, and the solution of burst massive throughput in high-speed data transmission is proposed. Compared with previously published papers, the temperature dependence of key time parameters of NAND flash memory is studied and analyzed under the condition of temperature change more concretely. The changing trend of three key time parameters of NAND type flash under different temperatures is analyzed by using appropriate test samples. At the same time, the analysis of the causes of reflection from the phenomenon is further expanded and discussed. The combination of theory and practice can provide powerful suggestions for more efficient and accurate application of NAND flash memory.

INDEX TERMS NAND flash, interleave two-plane program, burst massive data, temperature dependence.

I. INTRODUCTION

With the advent of the Internet of things [1], [2] era, the interconnection of all things has become an inevitable trend. It means that more data information needs to be processed and more sensors will be widely deployed and used [3]–[14]. As a result, the demand for data storage becomes increasingly strong. Most of the dynamic parameters of the external world sensed by sensors are finally stored in the form of digital quantities. As an indispensable member of the flash memory family, NAND flash memory plays an important role [15]–[20]. As a non-volatile storage device, it plays an important role in promoting the process of the Internet of things with low power consumption, low cost, and stable performance. As we all know, NOR [21]–[23] and NAND are the two main non-volatile flash technology in the market. INTEL first developed NOR flash technology in 1988, which completely changed the situation that EPROM and EEPROM [24]–[26] dominate the world. Then, in 1989, Toshiba released NAND flash architecture, which emphasizes reducing the cost per bit, higher performance, and being able to easily upgrade through the interface like a disk. Compared with NOR, NAND is an ideal solution for high data storage density. NAND structure can provide very high cell density, which can achieve high storage density, and the speed of writing and erasing is also very fast.

Based on the consideration of product maturity, the traditional 2-D NAND flash memory is still used in this paper. However, it is worth noting that as a new generation of storage products, 3-D NAND flash memory is receiving high attention now. The main reason for this above is that after many years of development, NAND flash memory is not only divided into SLC, MLC, and TLC. To further improve the capacity and reduce the cost, NAND's manufacturing process is also rapidly improved, from 50nm to 16nm or even smaller. However, with the progress of technology, NAND's oxide

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layer is thinner, which leads to the decline of reliability. Under such a bottleneck problem, 3-D NAND flash memory was born, and several layers of 2-D NAND flash memory were superimposed together, which not only ensured the reliability but also increased the capacity. Because of the technology of 3-D NAND, some TLC products with corresponding technology have achieved the performance of MLC, which is what we often call 3-D TLC. The research on 3-D NAND flash memory is being carried out all over the world, both in application and technology [27]–[29].

II. RESEARCH ON THE RELATIONSHIP BETWEEN THE TOTAL BANDWIDTH OF MULTI-CHANNEL ACQUISITION AND ERASURE MODE

The core task of a multi-channel sensor data acquisition system is to accurately collect and record the time series of all channel dynamic parameters. The essence of task implementation is to sample, hold, convert, encode, and store under the control of the CPU (such as programmable logic device FPGA [30]–[32]).

The multi-channel sensor data acquisition system uses flash memory based on the NAND principle. The operation of NAND flash memory mainly includes erasing, writing, and reading. Before writing data, NAND flash memory needs to be erased first. Erasing is performed on a block by block basis, and a single block, multi-block, or whole memory can be erased at one time. There are two erasure methods used in the development of a multi-channel sensor data acquisition system. One is ''write while erasing'', and another is ''erase before writing''. ''Write while erasing'' refers to erasing one block at a time, then writing one block, erasing and writing in turn. ''Erase before writing'' means that after receiving the ''erase'' instruction, the whole memory address space is erased first, and then the data is continuously written. The erasure method adopted depends on the maximum erasure time T_e, and the amount of data written to memory per unit time D_u, and F_{fifo} which is the capacity of FIFO that can be built-in CPU.

According to the system redundancy design principle and previous design experience. If the above three parameters meet the following formula 1, ''write while erasing'' can be adopted and used.

$$T_e \times D_u \leq \frac{3}{4} F_{fifo} \tag{1}$$

On the contrary, when the following formula 2 is satisfied, ''erase before writing'' will be the choice.

$$T_e \times D_u \geq \frac{3}{4} F_{fifo} \tag{2}$$

When formula 1 is satisfied, ''write while erasing'' can improve the reliability of the data storage procedure. In this way, there may not be a special erase command link between the multi-channel sensor data acquisition system and the monitoring background. Acquisition systems often work independently to reduce the risk of data being erased when retrieving readings. However, if formula 2 is satisfied, the internal FIFO data overflow of the CPU may occur during the system erasing memory, resulting in data loss.

When formula 2 is satisfied, ''erase before writing'' can alleviate the contradiction between insufficient system resources and a high amount of data written per unit of time. However, it also increases the possibility of data erasure due to operational errors or control link interference when retrieving readings.

For example, a multi-channel sensor data acquisition system is equipped with a 16-bit analog-to-digital conversion chip. Its total sampling rate is 1msps and the amount of data written to memory per second is 2Mbytes. The CPU adopts a programmable logic device FPGA whose internal FIFO can be up to 4Kbytes (32Kbits). The capacity of NAND flash memory is 1Gbytes, and the maximum erasing time is 2ms.

Formula 3 is as follows.

$$\begin{aligned} T_e \times D_u &= 2 \times 10^{-3} s \times 2 \times \frac{10^6 bytes}{s} \\ &= 4 \times 10^3 bytes \geq 3Kbytes = \frac{3}{4} F_{fifo} \end{aligned} \tag{3}$$

In this case, it is suitable to use the ''erase before writing'' method.

III. THE INTERLEAVE TWO-PLANE PROGRAM TECHNOLOGY FOR BURST MASSIVE DATA IN HIGH-SPEED DATA TRANSMISSION

The manufacturer's NAND flash memory has a nominal maximum write speed of 40Mbytes/s. However, the average write speed of the developed system is lower than this character. There are two reasons for this. One is to use programmable logic devices to control the memory, which contains many instructions, and the execution of instructions takes time. Second, the data of NAND flash memory is written on a page by page basis. Each time a page is written, it needs ''page programming time''. Generally, this time parameter is $200\mu s \sim 700\mu s$. Therefore, it can be assumed that in this case, regardless of the time taken by the instructions, the data flows continuously to the memory and does not pass through the internal FIFO of the CPU. The capacity of each page is 4Kbytes, the peak speed is 40Mbytes/s, and the programming time is $200\mu s$. The expression of the average write speed V_P of the maximum data is as follows.

$$\begin{aligned} V_P &= 4Kbytes/(\frac{4Kbytes}{40Mbytes/s} + 200\mu s) \\ &\approx 13.544973Mbytes/s \end{aligned} \tag{4}$$

The calculation method is given in formula 4 still contains some assumptions, but the calculation results are close to the real situation that data writing under normal mode of NAND flash memory enters the ''page programming'' link, which is suitable for systems with average data writing speed lower than 13.5Mbytes/s. When the sampling frequency is very high and the amount of data written per second is more than 13.5Mbytes, the manufacturer provides another solution: Interleave Two-Plane Page Program Technology.

Based on the spatial structure of NAND flash memory, erasing, writing, and reading operations of Interleave

Two-Plane Page Program Technology are carried out on multiple pages in a plane interleaved manner. The capacity of the object studied and tested in this paper is 4Gbytes. The memory space of a single chip is composed of two 2Gbytes memories. The memory space consists of eight planes. The capacity of each page is 4Kbytes. The crystal frequency is 60MHz. The used frequency is 1/2 division of the crystal frequency. The specific steps of interleaved plane programming are as follow.

A. By using Interleave Two-Plane Page Program Technology, the command and data are written to the 4Kbytes storage space of the first and second plane in the first 2Gbyte memory;
B. By using Interleave Two-Plane Page Program Technology, the command and data are written to the 4Kbytes storage space of the first and second plane in the second 2Gbyte memory;
C. In steps A and B, there is no waiting time between operations on two pieces of 2Gbytes memory;
D. After step B, wait for about 50μs and repeat steps A∼D;
E. Interleave Two-Plane Page Program is done.

In practical application, A∼B of the above steps show multiple cycles. The waiting time in step D is 50μs. It corresponds to the page programming time of 4Kbytes on page 1 of the second plane in the second 2Gbytes memory of step B. A total of 16Kbytes of data is written to 4 pages in a single cycle. But the overall waiting time is the only 50μs. The test data and calculation results are shown in Table 1.

TABLE 1. List of test data and calculation results based on Interleave Two-Plane Page Program Technology.

Location of sequential page writing	Time of control instruction	Write time of 4kbytes data in the page	Waiting time of page programming	Note
Chip 1/plane 1 page 1	0.767μs	136μs	0μs	Total 16kbytes data in 4 pages written in a single cycle
Chip 1/plane 2 page 1	0.767μs	136μs	0μs	
Chip 2/plane 1 page 1	0.767μs	136μs	0μs	
Chip 2/plane 2 page 1	0.767μs	136μs	50μs	
Total single write cycle time		597.134μs		
Peak write speed of a single cycle		30Mbytes/s		
Average write speed of a single cycle		27.437Mbytes/s		

It can be seen from Table 1 that the average write speed of a single cycle with Interleaved Two-Plane Program Technology is 27.437Mbytes/s at 1/2 frequency division of 60MHz.

IV. RESEARCH ON THE TEMPERATURE DEPENDENCE OF KEY TIME PARAMETERS BASED ON NAND FLASH MEMORY

A. TEST AND ANALYSIS OF TEMPERATURE DEPENDENCE OF THREE KEY TIME PARAMETERS

As mentioned above, the multi-channel sensor data acquisition system uses flash memory based on the NAND principle. Its operation mainly includes erasing, writing, and reading. The typical and maximum erasure time, page programming time, and read operation waiting time are given by the manufacturers. In the environmental adaptability test of several test systems, it is found that the above three key time parameters will change with the environmental temperature due to the correlation between the electrical parameters of the internal circuit and the temperature [33]–[36]. No matter the temperature increases or decreases, the changing trend of the three parameters is similar, and the change range cannot be ignored. It is important to point out that these key time parameters are the objects that must be considered in the storage and test of a multi-channel sensor data acquisition system. They are related to the successful storage and reading of test data. When the temperature changes lead to the corresponding changes of these parameters and the change range cannot be ignored, designers must provide accurate parameter range for data storage link according to repeated test verification, to make reasonable prediction and planning for further design.

Table 2 is a list of tested data of three key time parameters of several NAND flash memory chips with multiple brands and capacities for many times from high to low temperature.

As can be seen from table 2, taking NAND flash memory programming time parameters as an example, when the temperature range changes from −45°C to +100°C above zero, the maximum difference of programming time is nearly 27μs with the change of temperature. The transverse comparison curves of the same type of time parameters are shown in Fig. 1∼3.

When the multi-channel sensor data acquisition system stores the sampled data, FIFO is usually set to buffer the data. When the total sampling rate of the system is high and the amount of data generated per second is large, the size of FIFO must be designed from the perspective of maximum programming time to ensure that data transmission and storage will not be lost. If the temperature range of the multi-channel sensor data acquisition system is underestimated, the designed FIFO size may not guarantee the data validity under extreme temperature conditions during data transmission and storage.

B. DISCUSSION AND RESEARCH ON THE ROOT CAUSE OF TEMPERATURE DEPENDENCE OF KEY TIME PARAMETERS BASED ON STA

Semiconductor Wafer which is used for manufacturing FPGA, NAND flash memory, and all kinds of chips is composed of numerous transistor logic gates by special technology. From the day the chip was born it is one of the common goals of all electronic designers to predict the time delay of full-custom integrated circuits. However, due to the physical phenomenon of the nonlinear and complex model and based on effective working conditions such as voltage, temperature, and process, it is not easy to achieve accurate time delay prediction.

Static Timing Analysis, STA, is the workflow of computing and predicting chip timing in electronic engineering. The process does not need to be simulated by providing input incentives. The purpose of Static Timing Analysis is to ensure the normal operation of time sequence logic. Whether for

TABLE 2. Test value list of NAND flash key time parameters with temperature.

storage capacity (Mbytes)	Measurement parameter name	Temperature conditions at the time of measurement(℃)				
		100℃	90℃	80℃	70℃	65℃
		Test value(μs)				
128 [a]	erasure time	--	--	--	--	--
	page programming time	176	175	173	171	170
	read operation waiting time	22.9	22.7	22	22	21.9
256	erasure time	1420	1410	1410	1390	1390
	page programming time	171	170	170	169	168
	read operation waiting time	17.9	17.7	17.7	17.6	17.6
2048	erasure time	1480	1480	1470	1470	1470
	page programming time	168	167	165	165	164
	read operation waiting time	18	18.1	17.9	17.7	17.7
storage capacity (Mbytes)	Measurement parameter name	Temperature conditions at the time of measurement(℃)				
		60℃	55℃	50℃	26℃	-30℃
		Test value(μs)				
128 [a]	erasure time	--	--	--	--	--
	page programming time	169	168	165	162	156
	read operation waiting time	21.8	21.6	21.3	21	20.3
256	erasure time	1380	1380	1370	1360	1310
	page programming time	168	166	166	163	159
	read operation waiting time	17.5	17.6	17.4	17.1	16.7
2048	erasure time	1460	1460	1450	1370	1300
	page programming time	164	162	160	158	150
	read operation waiting time	17.6	17.6	17.4	17	16.2
storage capacity (Mbytes)	Measurement parameter name	Temperature conditions at the time of measurement(℃)				
		-35℃	-40℃	-45℃		
		Test value(μs)				
128	erasure time	--	--	--	--	--
	page programming time	151	150	149		
	read operation waiting time	19.5	19.4	19.3		
256	erasure time	1280	1280	1270		
	page programming time	156	155	155		
	read operation waiting time	16.4	16.3	16.2		
2048	erasure time	1300	1300	1290		
	page programming time	148	148	148		
	read operation waiting time	16	16	16		

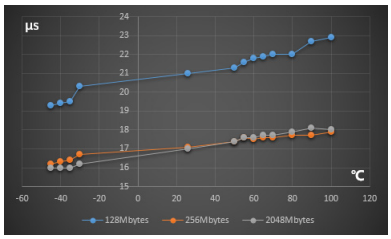

FIGURE 1. The transverse comparison curve of read operation waiting time.

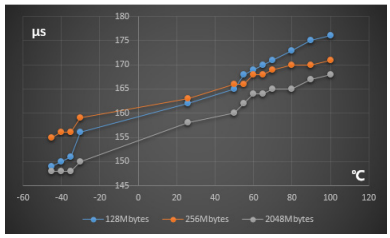

FIGURE 2. The transverse comparison curve of page programming time.

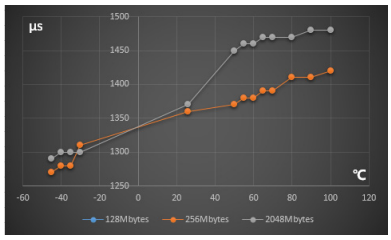

FIGURE 3. The transverse comparison curve of erasure time.

FPGA or NAND flash memory, the delay of the combinational logic circuit mainly depends on line delay and gate delay. Among them, the line delay refers to the transmission delay caused by the connection to the electrical signal. The line delay is closely related to the impedance model of the connection, sectional parasitic capacitance, inductance, and the length of the connection, etc. it depends on the final layout and wiring of the chip design. Gate delay refers to the delay caused by the specific gate unit circuit used in combinational logic in the process of electrical signal processing. But even if the chip design has been realized by a certain gate circuit and a certain physical connection, there are still variables in the line delay and gate delay, because the characteristics of the physical circuit are affected by many factors, the most important of which are temperature and voltage.

Based on the analysis above, the influence of temperature on timing delay is further discussed. Considering the parasitic capacitance and resistance of NAND flash memory or FPGA internal circuit, ignoring some non-important parameters, taking the inverter as an example, considering the input connection, the corresponding CMOS principle circuit can be approximate as shown in Figure 4.

In general, the higher the temperature is, the more intense the thermal motion of molecules will be, which is easier to

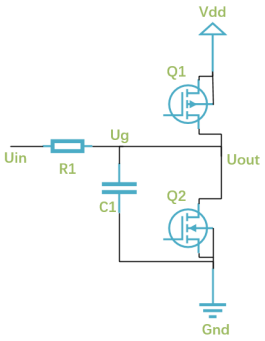

FIGURE 4. The transverse comparison curve of erasure time.

hinder the movement of electrons in the conductor and semiconductor, and the most significant effect is to increase the resistance. Corresponding to the inverter circuit in Figure 4, R_1 becomes larger, thus R_1C_1 becomes larger. Assuming that V_{dd} remains unchanged, then.

The length of time changes from U_{in} turning from logic 0 to logic 1 to U_{out} turning from logic 1 to logic 0. Firstly, the response speed of U_{out} from logic 1 to logic 0 mainly depends on the speed of NMOS conduction under the circuit, and the condition of NMOS conduction is that U_g is greater than the threshold voltage. As the temperature increases, R_1C_1 becomes larger, so the time required for U_g to increase from 0V to threshold voltage becomes longer, which will eventually lead to U_{out} changing to logic 0 after a long time.

Using a similar analysis method, the length of time changes from U_{in} turning from logic 1 to logic 0 to U_{out} turning from logic 0 to logic 1. Firstly, the response speed of U_{out} from logic 0 to logic 1 mainly depends on the speed of PMOS conduction above the circuit, and the conduction condition of PMOS is that U_g is less than the threshold voltage. As the temperature increases, R_1C_1 becomes larger, so the time required for U_g to decrease from V_{dd} to threshold voltage becomes longer, which will eventually lead to U_{out} becoming logic 1 after a long time.

Through the above analysis, it can be concluded that the higher the temperature, the greater the internal delay of the chip. The test concluded that the key time parameters change with the temperature in Section 4.1 of this paper has good theoretical support. At the same time, it can also be used as one of the design suggestions to suppress the chip working in a higher temperature environment as far as possible.

V. SUMMARY

On the one hand, the solution of burst data acquisition has been given. But the high demand for flash memory technology is not only limited to write but also fast erase and high-speed read and so on. In the same way, they can also be solved by Interleaved Two-Plane Program Technology. On the other hand, the numerous sensors in the Internet of things have their application environment across the globe, and they are always facing the extreme weather environment. How to ensure the durability and stability of the multi-channel sensor data acquisition system, the research on the time correlation of the key time parameters of the measurement system becomes one of the support points. In the Internet of things era, flash memory technology cannot be avoided as a data storage medium, and NAND flash memory always plays an important role.

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