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Analysis and Design of a 35-GHz Hybrid π-Network High-Gain Phase Shifter With 360° Continuous Phase Shifting

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ABSTRACT This paper presents the analysis and design of a 35-GHz high-gain phase shifter with 360° continuous phase shifting. To enhance the phase shift range, a hybrid π-network realized by combining the electrical tuning through capacitors and magnetic tuning through transformers is developed. The phase shift modules are inserted between the vertically stacking transistors to achieve the embedded phase shifting with the minimum loss. Furthermore, the Gm stages offer additional signal gain to suppress attenuation in the passive phase shifter. The capacitive neutralization technique is utilized to further increase the gain and enhance stability. This prototype, fabricated in a 28-nm CMOS process, demonstrates a 360° continuous phase shift with a maximum gain of 25.6 dB and a minimum noise figure of 4.1 dB. It consumes 26-mW power with a supply voltage of 0.9 V and 1.25 mm × 0.75 mm chip area.

INDEX TERMS Phase shifter, π-network, low-noise amplifier, tunable inductor, transformer.

I. INTRODUCTION

The spectrum from 24.5 GHz to 42.5 GHz is allocated for the 5th-generation wireless communication, automobile radar, and other applications where multiple-element array architectures are widely adopted [1]–[3]. The beamforming techniques have been extensively investigated due to the advantage of path loss compensation [4]–[7]. The beam direction of a phased-array system can be electronically steered by adjusting the phase of each array element. The RF phase shifter is one of the critical and challenging components.

The main challenges associated with RF phase shifters are the required large phase shift range in addition to high gain and low power consumption. The state-of-the-art mm-wave phase shifters can be categorized into the active phase shifters and the passive phase shifters [8]–[10]. It is challenging for both types of phase shifters to realize a 360° phase shift range.

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Active phase shifters are mainly based on the quadrature vector-summing technique, typically composed of an in-phase/quadrature-phase (I/Q) generator with cascaded variable-gain amplifiers (VGAs) [11]–[15]. Active phase shifters typically exhibit the characteristics of low insertion loss, small chip area, and high phase shift resolution at the expense of poor linearity and high power consumption [16]–[20]. Furthermore, the resolution of the vector-summing phase shifter is limited by the amplitude/ phase error of the IQ generator and the phase variation of the VGA. Recent research mainly focuses on the improvement of the resolution and linearity at the cost of increased circuit complexity or power consumption [21]–[24].

Passive phase shifters exhibit the benefits of zero dc power consumption and high linearity compared with the active phase shifters but suffer from the high insertion loss and large chip size [25]–[27]. The switched high-pass, low-pass [28]–[30], and the reflection-type [31]–[33] structures are widely adopted in the passive phase shifters. The high-pass

and low-pass topologies usually require multiple cascaded cells to overcome the phase-shift limitation of a single unit. The reflection-type phase shifter is composed of a 90° coupler and two identical reflective loads, and the phase shift range is determined by the reflection coefficient of the two reflective loads [34], [43]. For passive phase shifters, recent studies concentrate on the reduction of the loss and loss fluctuation as well as achieving a full 360° phase shift range [35].

Gm-stages are used to boost the signal swing for the LC-based phase shifter [36], [37], but the phase shift range is small. To address the challenges of limited phase shift range and large insertion loss, a new hybrid π-network phase shifter with Gm stages is proposed [38], as shown in Fig. 1. The proposed hybrid π-network phase shifter employs the capacitor-based electrical tuning and transformer-based magnetic tuning. The phase shifter embedded Gm stages helps boost gain efficiently with minimum phase-shifter attenuation. The hybrid π-network phase shifter, fabricated in a 28-nm CMOS process, has demonstrated the full-360° phase shift range and 25.6-dB gain at 35 GHz with competitive power consumption and chip area.

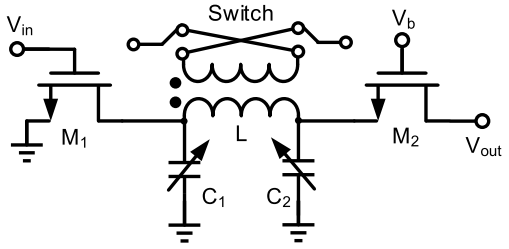

FIGURE 1. The topology of the hybrid π-network phase shifter with Gm stages.

As an extension of [38], this work provides a supplementary analysis and optimization strategy for the hybrid π-network phase shifter, the factors affecting the phase shift range and gain are theoretically analysed to extend phase shift range and minimize the insertion loss simultaneously. Besides, this work introduces a prototype of circuits, combining an LNA and a phase shifter, to save the power consumption and chip area of the receiver front end. This paper is organized as follows. In Section II, the detailed analysis is presented to explain the operating principle and optimization methods of the proposed π-network with Gm stages. In Section III, the design of a 35-GHz hybrid π-network high-gain phase shifter with a 360° continuous phase shift range is described. In Section IV, the results of their experimental characterizations are reported. The conclusions are drawn in Section V.

II. ANALYSIS OF THE π-NETWORK WITH GM STAGES

A. THE CONVENTIONAL π-NETWORKS

The high-pass and low-pass structures are widely utilized in passive phase shifters. The π-network composed of an inductor and two capacitors is the best choice for on-chip implementation considering the chip area. The conventional π-network with losses is shown as Fig. 2(a), the π-network

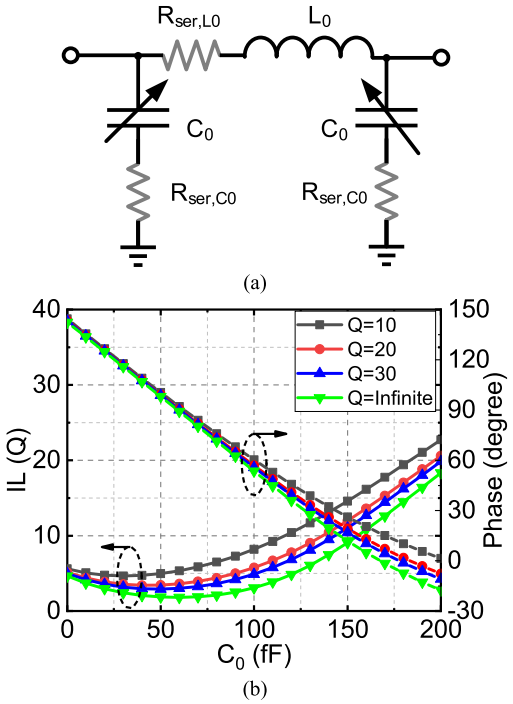

FIGURE 2. (a) Schematic of the conventional π-Network. (b) Calculated insertion loss and transmission phase of the π-Network.

can be cascaded to achieve a larger phase shift range while only one bias voltage is needed to control the varactors.

In the following, the phase shift characteristics and the transmission loss of the π-network are analyzed. The transmission term of the scattering matrix can be calculated by

$$S_{21} = \frac{2}{A + B/Z_0 + C \cdot Z_0 + D} = \frac{2}{2\,(1 + Z_{L0}Y_{C0}) + \frac{Z_{L0}}{Z_0} + 2Z_0Y_{C0} + Z_0Z_{L0}Y_{C0}^2}. \quad (1)$$

where Z_{L0} is the impedance of the inductor and Y_{C0} is the admittance of the varactors with $Z_{L0} = j\omega L_0(1 - j/Q_{L0})$ and $Y_{C0} = j\omega C_0/(1 + j/Q_{C0})$. Z_0 is the characteristic impedance. Q_{L0} and Q_{C0} are utilized to characterize the loss of the inductor and capacitors, $Q_{L0} = \omega L_0/R_{ser,L0}$, $Q_{C0} = 1/\omega C_0 R_{ser,C0}$.

The insertion loss (IL) of the π-network is the S_{21} due to the characteristics of passive circuits. Fig. 2(b) shows the calculated insertion loss of the conventional π-network at 35 GHz. The Q_{L0} and Q_{C0} are both equal to Q for simplifying the calculation.

For a lossless π-network with perfect matching, the minimum insertion loss is 0 dB. However, the minimum insertion loss is increased due to the resistive loss and reactive mismatch [8]. The IL variation caused by Q is almost unchanged as C_0 changes. In other words, the effect of resistive loss is much smaller than the reactive mismatch. In the practical circuits design, the Q_{L0} and Q_{C0} are usually large than 10 at 35 GHz [31]. Thus we ignore the resistive loss characterized by Q. Then $Z_{L0} \approx j\omega L_0$ and $Y_{C0} \approx j\omega C_0$, the S_{21} can be

simplified as

$$S_{21} = \frac{2}{A + B/Z_0 + C \cdot Z_0 + D} = \frac{2}{2\left(1 - \omega^2 L_0 C_0\right) + j\left[\frac{\omega L_0}{Z_0} + \omega C_0 Z_0 \left(2 - \omega^2 L_0 C_0\right)\right]}. \tag{2}$$

And the corresponding transmission phase is

$$\psi_{21} = \tan^{-1}\left[-\frac{\omega L/Z_0 + \omega C Z_0 \left(2 - \omega^2 LC\right)}{2\left(1 - \omega^2 LC\right)}\right]. \tag{3}$$

The phase shift range is dependent on the capacitance variation, and the largest phase shift range can be

$$\Delta\varphi = \psi_{21,\max} - \psi_{21,\min}. \tag{4}$$

As Fig. 2(b) shows, the phase shift range is extended with the increasing capacitance variation, but the insertion loss is also increased. There is a trade-off between the large phase shift range and the low insertion loss.

B. THE PROPOSED π-NETWORK WITH GM STAGES

To compensate for the insertion loss from (2), we proposed a new π-network embedded with Gm stages. As Fig. 3(a) shows, the proposed π-network with Gm stages includes a common-source stage, a conventional π-network, and a common-gate stage. The phase shift range of the conventional π-network is mainly determined by the tuning range of the capacitors C_1 and C_2. The tuning range will be decreased due to the parasitic capacitances, including the ones from the transistors and interconnect, etc.

In order to figure out the relationship between the phase shift range and the components of the π-network with Gm stages, the equivalent model of the transistor is established as shown in Fig. 3(b). C_{gs1} and C_{gs2} are the parasitic capacitors between the gate and source terminals of transistors. C_{gd1} and C_{gd2} are parasitic capacitors between the gate and drain terminals of transistors. The R_{ds1}, R_{ds2}, C_{ds1}, and C_{ds2} determine the impedance at drain terminals.

To simplify the analysis process, except for the main parasitics, all other parasitics are ignored. As shown in Fig. 3(b), the elements in the blue rectangle with the dashed line are considered as the main components that affect the phase shifting. The ABCD matrix of the π-network with the active device parasitics in the blue rectangle can be calculated as

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} \frac{-1}{g_{m1}R_{ds1}} & \frac{-1}{g_{m1}} \\ 0 & 0 \end{vmatrix} \times \begin{vmatrix} 1 + Z_L Y_{C_2} & Z_L \\ Y_{C_1} + Y_{C_2} + Z_L Y_{C_1} Y_{C_2} & 1 + Z_L Y_{C_1} \end{vmatrix} \begin{vmatrix} \frac{1}{1+g_{m2}R_{ds2}} & \frac{R_{ds2}}{1+g_{m2}R_{ds2}} \\ 0 & 1 \end{vmatrix} \tag{5}$$

with

$$Y_{C1} = j\omega C_1' = j\omega\left(C_1 + C_{ds1}\right) \tag{6}$$

$$Y_{C2} = j\omega C_2' = j\omega\left(C_2 + C_{gs2}\right). \tag{7}$$

To further simplify the calculation, assume that the two transistors have the same size and bias condition, which means $g_{m1} = g_{m2} = g_m$, $C_{gs1} = C_{gs2} = C_{gs}$, $C_{gd1} = C_{gd2} = C_{gd}$, $R_{ds1} = R_{ds2} = R_{ds}$. Then (5) can be derived as (8), shown at the bottom of the page, where $G = g_m R_{ds}$. The transmission term of the scattering matrix can be calculated by (9), shown at the bottom of the page, where Z_0 is the characteristic impedance. And the corresponding transmission phase is written as (10), as shown at the bottom of the page.

From (10), the transmission phase changes as the varactors change once the design is fixed. Fig. 4(a) shows the phase of the π-network with Gm stages versus the capacitance and inductance under the condition of the $C_2 = C_1$ at 35 GHz. The g_m is about 14 mS under the proper bias condition. Based on the extraction of the transistors, the parasitic capacitances C_{gs} and C_{gd} are set as 20 fF and 15 fF, respectively. The varactors and inductors are selected to minimize insertion loss and obtain large phase variation. When the inductance L is small, the phase is difficult to be changed as the capacitances are varied. As the inductance increases, the phase

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = -\begin{vmatrix} \frac{1+Z_L Y_{C_2} + R_{ds}\left(Y_{C_1} + Y_{C_2} + Z_L Y_{C_1} Y_{C_2}\right)}{G^2} & \frac{R_{ds}\left[1 + Z_L Y_{C_2} + R_{ds}\left(Y_{C_1} + Y_{C_2} + Z_L Y_{C_1} Y_{C_2}\right)\right] + (1+G)\left[Z_L + R_{ds}\left(1 + Z_L Y_{C_1}\right)\right]}{G(1+G)} \\ 0 & 0 \end{vmatrix} \tag{8}$$

$$S_{21} = \frac{2G(1+G)}{\left(1 - \omega^2 LC_2'\right) + \frac{R_{ds}}{Z_0}\left[1 - \omega^2 LC_2' + (1+G)\left(1 - \omega^2 LC_1'\right)\right] + j\left[\omega R_{ds}\left(C_1' + C_2' - \omega^2 LC_1' C_2'\right) + \frac{R_{ds}}{Z_0}\omega R_{ds}\left(C_1' + C_2' - \omega^2 LC_1' C_2'\right) + (1+G)\frac{L}{Z_0}\right]} \tag{9}$$

$$\varphi_{21} = \arctan\left[-\frac{\left(1 + \frac{R_{ds}}{Z_0}\right) R_{ds}\omega\left(C_1' + C_2' - \omega^2 LC_1' C_2'\right) + \frac{\omega L}{Z_0}(1+G)}{\left(1 + \frac{R_{ds}}{Z_0}\right)\left(1 - \omega^2 LC_2'\right) + \frac{R_{ds}}{Z_0}(1+G)\left(1 - \omega^2 LC_1'\right)}\right] \tag{10}$$

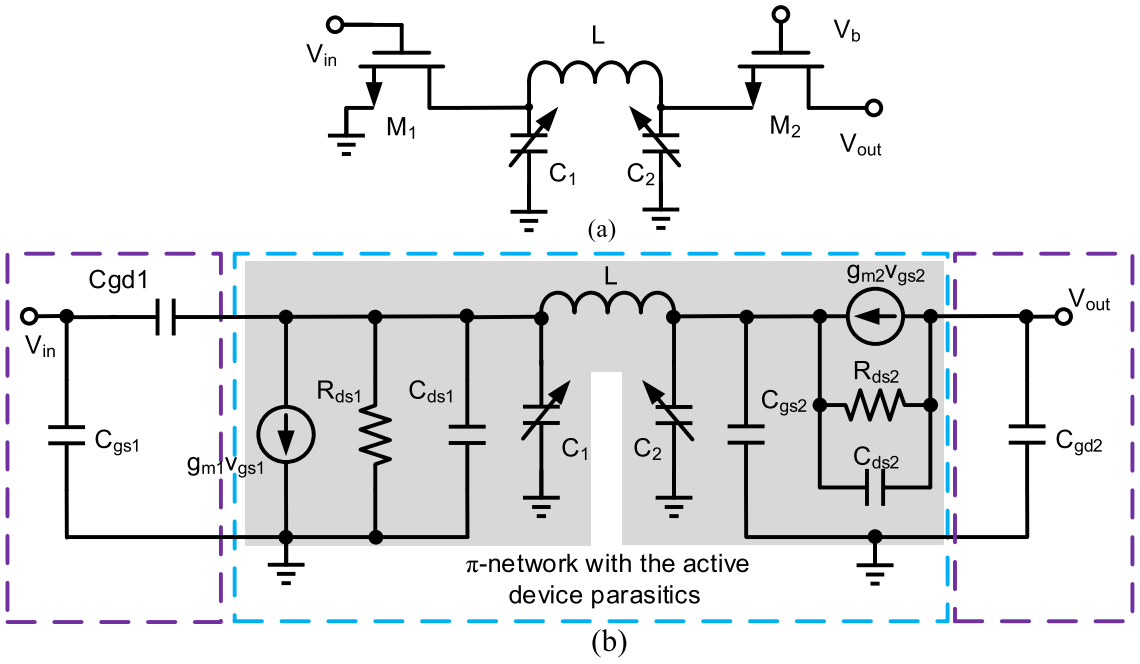

FIGURE 3. (a) Proposed π-network with the Gm-stages (b) Simplified equivalent circuits of the π-network with the Gm-stages.

shift range increases and then decreases accordingly. If α is defined as the relative tuning range of the capacitors, $\alpha = C_{1,max}/C_{1,min}$. In general, α is about 2–3 at millimeter-wave frequency. As shown in Fig. 4(b), α mainly determines the phase shift range when L is constant. As the inductance and capacitance increase, the resonance frequency ω_r decreases and reaches the operation frequency. As shown in Fig. 5, S_{21} of the proposed π-network with Gm stages decreases sharply around the resonance frequency ω_r. Therefore, the inductor needs to be carefully designed to obtain a large gain. Fortunately, a relatively large phase shift range and a large gain can be obtained at the same time with an optimum inductance. Optimum inductance exists for a specific α.

To further explore the phase shift range versus the two capacitors, the capacitance ratio between the two capacitors is defined as

$$k = \frac{C_2}{C_1}. \tag{11}$$

k also affects the phase shift range. Fig. 6(a) shows the phase versus the independent capacitor C_1 and capacitance ratio k. The capacitor tuning range is 3, the inductance is 500 pH. As the k increases, the phase shift range increases to the largest value and then decreases, as shown in Fig. 6(b). The optimum k for the largest phase shift range is related to the inductance. As the inductance changes from 300 pH to 700 pH, the optimum k changes from 2.4 to 0.6.

Fig. 7(a) shows the phase of the π-network with the independent capacitor C_1 and gm of the transistors. The phase shift range increases as g_m decreases, which is a benefit for a large phase shift range and low power consumption. However, the gain decrease as g_m decreases. Thus, there is a trade-off between the phase shift range and gain, shown in Fig. 7(b).

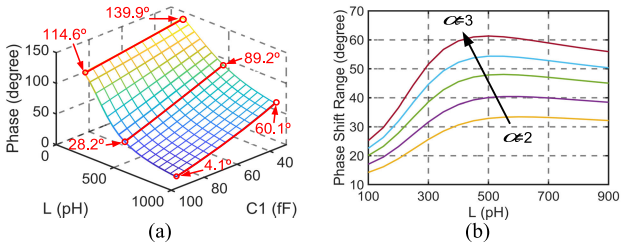

FIGURE 4. (a) Transmission phase of the proposed π-network with Gm stages versus the capacitance and inductance. (b) Maximum phase shift range versus the inductance, the step of α is 0.25.

As mentioned above, besides the lumped elements of the basic π-network, the parasitics of the transistors will also affect the phase shift range. Fig. 8 shows the maximum phase shift range with the effects of C_{ds} and C_{gs}. The maximum phase shift range decreases as C_{gs} and C_{ds} increase. Thus the parasitic capacitances need to be considered in the circuits and layout design.

In conclusion, the phase shift range of the proposed π-network with Gm stages is determined by the capacitors and inductors and is also affected by the parasitics of transistors. By optimizing the inductance and capacitances, the maximum phase shift range can be extended while maintaining a relatively high gain. However, a trade-off between the phase shift range and gain is made due to the gm of transistors.

III. CIRCUITS IMPLEMENTATION

A. HYBRID π-NETWORK PHASE SHIFTER

Based on the analysis in section II, a 35 GHz hybrid π-network phase shifter is designed. Fig. 9 illustrates the topology of the proposed hybrid π-network phase shifter with

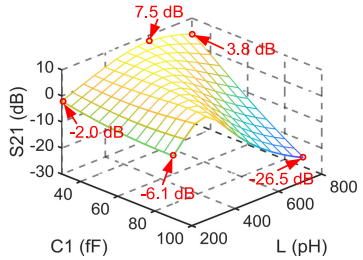

FIGURE 5. S21 of the proposed π-network with Gm stages versus the capacitance and inductance.

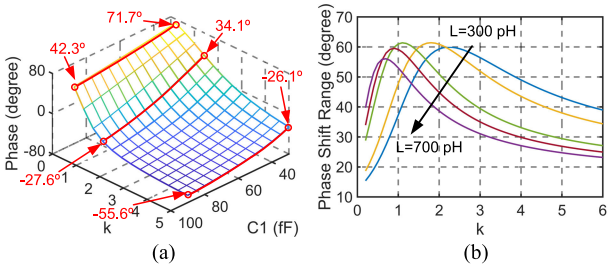

FIGURE 6. (a) Transmission phase versus the capacitor C1 and the capacitance ratio k. (b) Maximum phase shift range versus the capacitance ratio k, the step of L is 100 pH.

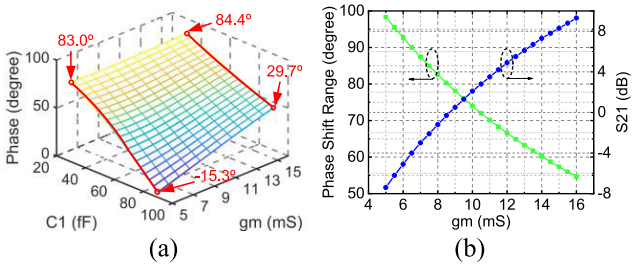

FIGURE 7. (a) Transmission phase versus the capacitor C1 and gm. (b) The phase shift range and S21 versus the gm of the transistors.

four Gm stages. To improve noise performance and bandwidth, the 3-coil transformer is used for the input matching [39], [40]. The inter-stage matching and output matching are implemented by compact transformers.

In the proposed phase shifter, the hybrid tuning π-networks are added between the two vertically stacked transistors. As described in section II, the phase shift range of the pi-network is limited by the capacitance variation range and the trade-off between the phase shift range and the gain. Considering the design margin, around four π-networks with Gm-stages are needed to cover the 180° phase shift range, and then the 360° phase shift range can be achieved through the inverting switch. To decrease the chip size and power consumption, the switchable inductor through magnetic coupling is proposed to minimize the number of π-networks.

In the proposed design, switchable inductors are adopted in the hybrid π-network of third and fourth stages. In the second stage, only capacitor tuning networks are adopted to minimize the influence on noise performance. In the third and fourth stages, The Gm stages are adopted in the proposed

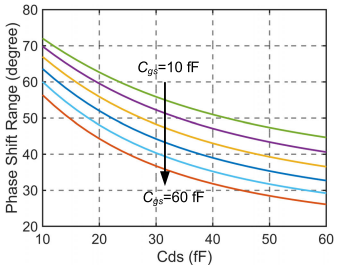

FIGURE 8. Maximum phase shift range versus the parasitic capacitors Cds, the step of Cgs is 10 fF.

phase shifter design to provide a large gain. The transistors are optimized to improve the matching condition and reduce the parasitics with acceptable power consumption. Table 1 shows the size of the transistors. The capacitive neutralization technique is utilized to improve the gain and enhance stability, the neutralization-capacitors are implemented by the NMOS transistors due to the process variation tolerance [25].

TABLE 1. Size of the transistors in the phase shifter.

Transistor	M_1, M_2	M_3, M_4 M_7, M_8	M_5, M_6 M_{11}, M_{12}	M_9, M_{10}
W/L (um)	17.6/0.03	15.1/0.03	12.6/0.03	3.4/0.03

In the proposed design, based on the analysis of the phase shift range and S_{21} shown in Fig. 5 and Fig. 6, the equivalent inductances are designed as 400 pH to 600 pH. The capacitors are designed at dozens of pico-farads. Within the region, the relatively high gain and large phase shift range can be obtained simultaneously. Fig. 10(a) shows the simulated capacitance variation of C_1 versus the bias voltage, the capacitance changes from 30 fF to 86 fF. The tuning ratio of the varactors is 2.7. The Q of the capacitor is 15.5, shown in Fig. 10(b).

To obtain a phase shift range of 180°, two sets of the voltage-control switch (V_S) are utilized to change the coupling inductance, and the capacitance is tuned by a continuous control voltage (Vctr). Fig. 11(a) shows the simulated transmission phase versus the Vctr under the inductances of L_1 and L_2, the inductance is switched by the Vs. With the inductor L_1, the normalized phase shift range is 133°, the phase shift range is extended to 168° when L_1 is switched to L_2. Around 35° phase shifting can be obtained by changing the inductors. The equivalent inductances L_1 and L_2 are around 410 pH and 540 pH, respectively. For the 3rd and 4th stages, each π-network has 2 different equivalent inductances switched by the Vs, such as L_1 and L_2. The phase shift range is more than 180° based on the 4 cases, shown in Fig.11(b).

And another set of switches (V_{SW}) at the last stage is used for phase inversion to further extend the phase shift range to 360°.

B. TRANSFORMER-BASED TUNABLE INDUCTOR

The two switchable inductors provide an additional 80 degrees of phase shift range, which is similar to the phase shift

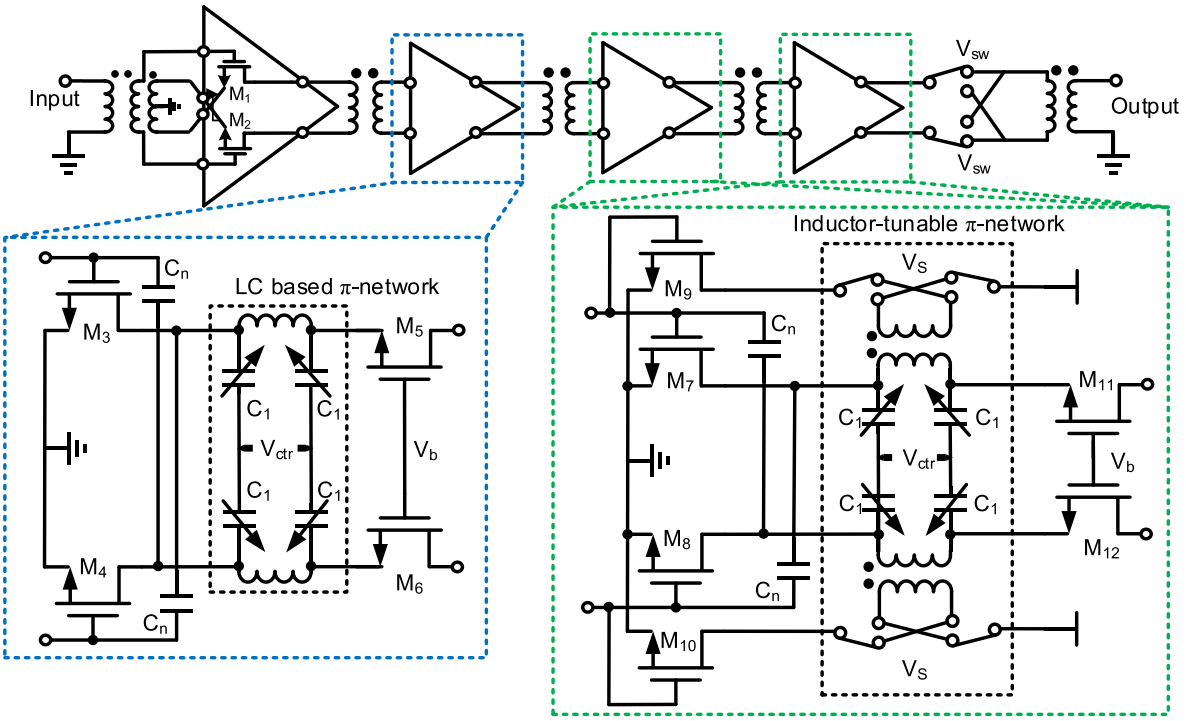

FIGURE 9. The topology of the proposed hybrid π-network phase shifter with four Gm stages.

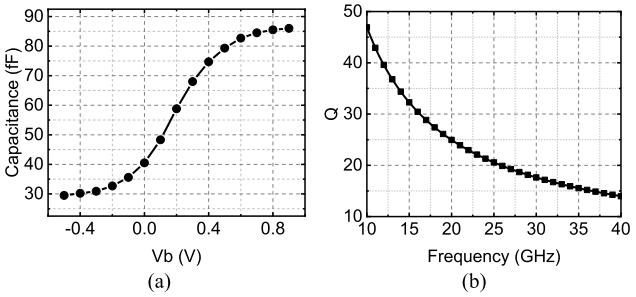

FIGURE 10. (a) Simulated capacitor C1 versus the bias voltage. (b) Simulated Q value of the capacitor versus the frequency.

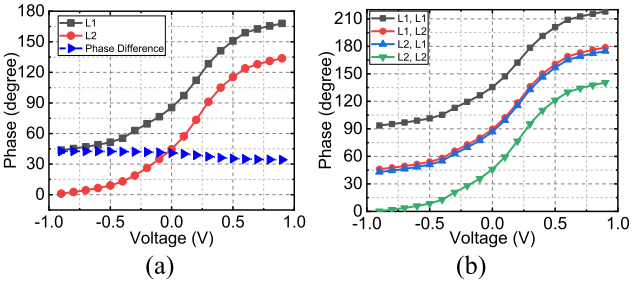

FIGURE 11. Simulation results of (a) normalized transmission phase versus the control voltage and the switchable inductors. (b) normalized transmission phase for the 4 cases.

range of one π-network. However, it is a challenge to make inductance tunable compared with varactors. The on-chip transformer is a good solution to make the equivalent inductance tunable by changing the coupling condition. Fig. 12 shows the topology of the transformer-based π-network. The transient current i_p and i_s are related, the direction of the transient current determines the coupling polarity of the transformer. Thus the equivalent inductor of the π-network can be switched by changing the direction of the transient current flowing through the secondary inductor. The equivalent inductance is decided by the primary inductor L_P and the mutual inductance. And the equivalent inductance L_{eq} can be calculated as

$$L_{eq} = L_p \pm nM. \tag{12}$$

where M is the mutual inductance of the transformer. The current ratio $n = i_s/i_p$, i_s and i_p are dependent on the gm of the M_9 and M_7. Thus, the equivalent inductance is tuned by gm of M_9. The ± is determined by the coupling polarity, which is controlled by the switch voltage V_S.

When V_S =0 V, the transistors M_{13} and M_{14} are turned off, and the transistors M_{15} and M_{16} are turned on. The primary and secondary coils of the transformer are reverse coupled. The equivalent inductance of the π-network can be calculated as

$$L_{eq,1} = L_p - nk_C\sqrt{L_pL_s}. \tag{13}$$

where L_S is the secondary inductor, k_C is the coupling coefficient of the transformer.

When V_S = 1 V, the transistors M_{13} and M_{14} are turned on, and the transistors M_{15} and M_{16} are turned off. The primary and secondary coils of the transformer are in-phase coupled. The equivalent inductance of the π-network can be

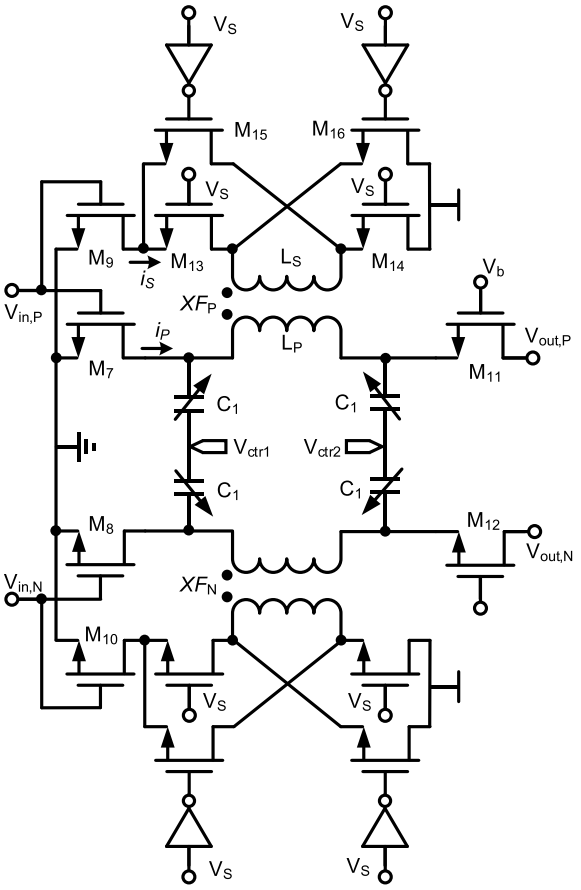

FIGURE 12. Schematic of the hybrid π-network with the transformer-based inductor tuning and varactor-based capacitor tuning.

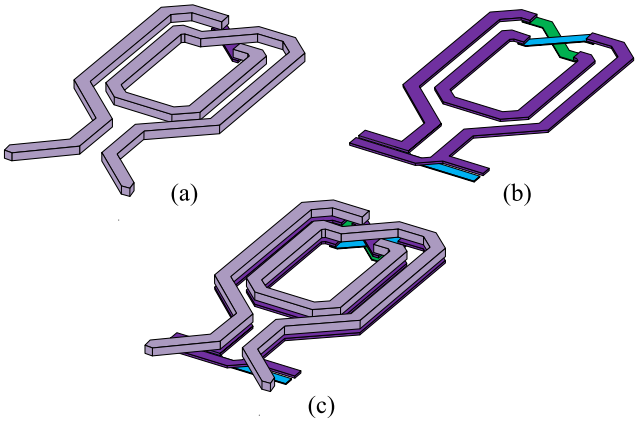

FIGURE 13. Layouts of the proposed switchable inductor. (a) The primary inductor of the transformer. (b) The secondary inductor of the transformer. (c) Vertically coupled transformer.

calculated as

$$L_{eq,2} = L_p + nk_C\sqrt{L_pL_s}. \tag{14}$$

In general, the vertically coupled structure is adopted to maximize the coupling coefficient in the transformer design. In the transformer, the primary inductance is usually approximately equalled to the secondary inductance.

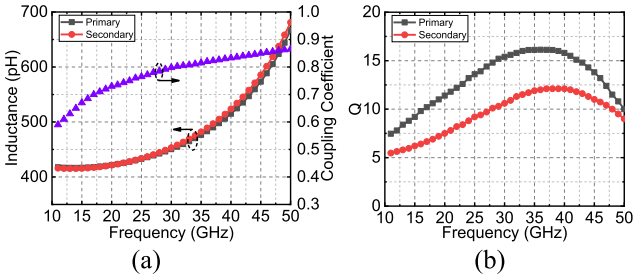

FIGURE 14. Simulated (a) inductance and coupling coefficient of the transformer. (b) Q value of the primary and secondary inductor.

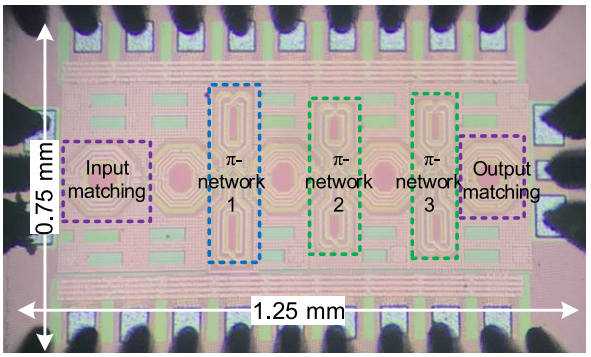

FIGURE 15. Chip photo of the proposed hybrid high gain π-network phase shifter.

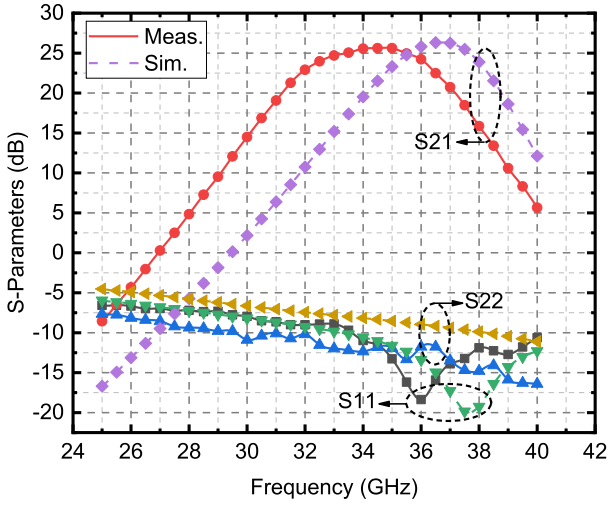

FIGURE 16. Measured S-parameters versus the simulation results.

And the coupling coefficient can reach 0.8-0.9. Then $L \approx L_P{\cdot}(1 \pm n \cdot k_C)$, the inductance difference is determined by the size of the M_9 and M_7.

The transformer-based switchable inductors are shown in Fig. 13. Fig. 13(a) is the primary inductor of the proposed transformer, in which the top layer metal is adopted to maximize the Q value of the inductor. Fig. 13(b) is the secondary inductor and Fig. 13(c) is the vertically coupled transformer to maximum the coupling coefficient. The primary and secondary inductances are 480 pH and 490 pH at 35 GHz, as shown in Fig. 14. The coupling coefficient of

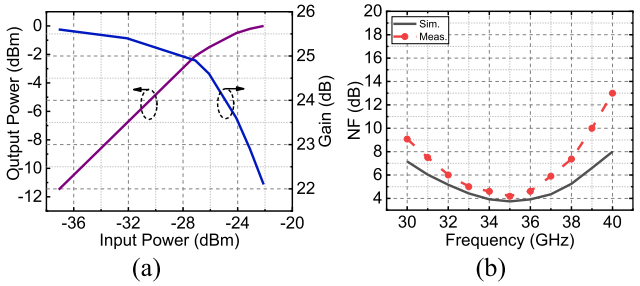

FIGURE 17. (a) Measured output power and gain versus the input power. (b) Measured and simulated noise figure.

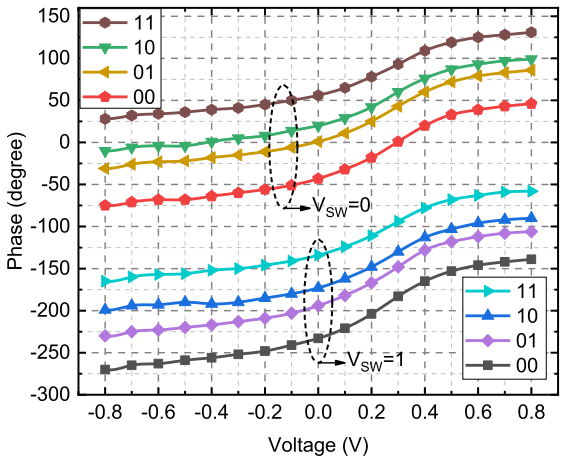

FIGURE 18. Measured phase shift versus the control voltage at different codes.

the transformer is 0.8. The Q of the primary and secondary inductors are 16 and 12, respectively.

IV. MEASUREMENT RESULTS

The proposed hybrid π-network phase shifter with 360° phase shifting is fabricated in a 28 nm CMOS process. Fig. 15 shows the die photo, and the full chip occupies an area of 1.25 mm × 0.75 mm including the pads.

The S-parameters and transmission phase are measured by direct probing with a Keysight network analyzer N5247B. The on-chip calibration is done with a short-open-load-through technique up to probe tips. Fig. 16 shows the measured S-parameters versus the simulated S-parameters. From the measured results, the maximum gain is 25.6 dB at 35 GHz, and the 3-dB bandwidth is 4.5 GHz, from 32.0-36.5 GHz. The power consumption is 26 mW with a supply voltage of 0.9 V. The peak frequency shifts down about 2 GHz, which is due to the model inaccuracy of the active and passive devices. The transformers are modeled through full-wave electromagnetic (EM) simulation via the high-frequency structure simulator (HFSS). However, to reach the requests of layout density, lots of dummy cells are filled around the passive devices. The dummy cells were not modeled due to the large number and limitation of computing resources.

The input 1-dB compression point (IP_{1dB}) is measured with the analog signal generator E8257D and the signal analyzer N9040B. Fig 17(a) shows the output power and gain versus

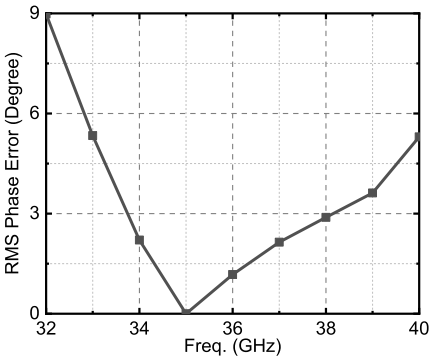

FIGURE 19. Measured RMS phase error versus frequency.

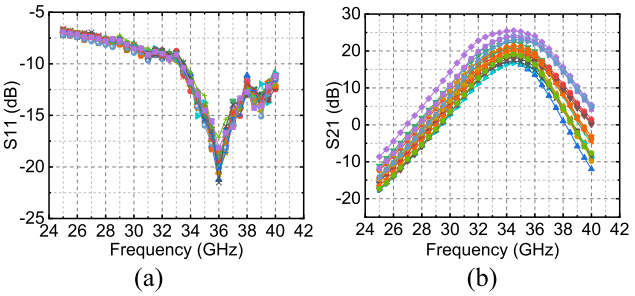

FIGURE 20. (a) Measured S11 under the different bias condition. (b) Measured S21 under the different bias condition.

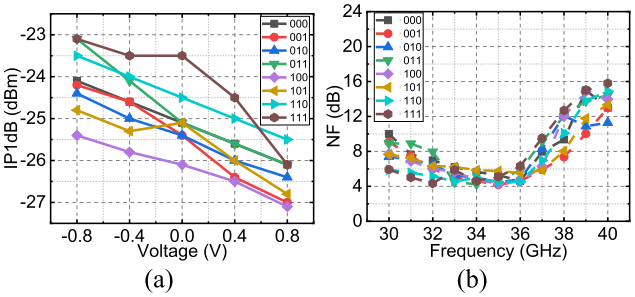

FIGURE 21. (a) Measured IP1dB with the different codes. (b) Measured NF variation with the different codes.

the input power. The IP_{1dB} is about -26.1 dBm at 35 GHz with a maximum gain of 25.6 dB. The noise performance is measured with the noise source 346CK40 and the signal analyzer N9040B. Fig. 17(b) shows the measured double-side-band (DSB) noise figure (NF) and simulation results. From the measurements, the minimum NF is about 4.2 dB at 35 GHz. The NF is less than 6 dB from 32.0-36.5 GHz.

Fig. 18 shows the measured phase shift range at 35 GHz. First, set the bias voltage of the two sets of voltage-control switches of the third stage and the fourth stage (e.g. V_S1 and V_S2) to 00, and then continuously slide the control-voltage (Vctr) to adjust the varactors. Second, set the V_S1 and V_S2 to 01, 10, and 11 separately, and slide the Vctr under each bias condition to obtain the phase shift. The Vctr is changed from-0.8 V to 0.8 V to obtain the maximum phase shift range. Finally, change the bias voltage of the reverse switch (V_{SW}) and repeat the previous operation to obtain the

TABLE 2. Comparison of the state-of-art phase shifters.

Reference	[4]	[10]	[16]	[19]	[34]	[35]	[42]	This work
Process	45 nm SOI CMOS	120 nm SiGe	90 nm CMOS	130 nm CMOS	130 nm Bi-CMOS	65 nm CMOS	65 nm CMOS	28 nm CMOS
Centre Freq. (GHz)	27	35	60	23	62	29	60	35
Band Width (GHz)	4.0	8.0	7.0	3.0	5.0	4.0	10.0	6.0
Phase shift Range (°)	360	360	360	300	360	360	90	360
Phase Resolution	5-bit	4-bit	4-bit	Continuous	Continuous	Continuous	4-bit	Continuous
Maximum Gain (dB)	12.2	11.3	1.1	-2.9	-3.7	-7.2	6.2	25.6
RMS Phase Error (°)	4	4	7.6	N/A	N/A	N/A	3.5	<3.4
Gain Variation (dB)	±1	±1.3	±1.5	±4.5	±3.3	±1.1	±0.8	±4.3
Minimum NF (dB)	4.2	3.8	9.7	N/A	N/A	N/A	5.7	4.2
IP_{1dB} (dBm)	-8.0	-28.0	-9.8	N/A	13.8	N/A	-19	-26.1
Power (mW)	42	33	19.8	18.5	0	0	8.8	26
Area (mm^2)	1.75	0.33*	0.61	0.44*	0.16	0.08	< 0.93	0.94
Topology	Switched LC+LNA	Switched LC+LNA	Vector Modulator	Vector Modulator	Reflection Type	Reflection Type	Switched Type+LNA	Proposed π-network

* Without the PADs

complete phase shift range, which covers 360°. The phase shift is dependent on the bias condition. Fig. 19 shows the rms phase error versus the frequency, the control voltage is chosen to have zero rms phase error at 35 GHz, the rms phase error is less than 3.4° from 34-39 GHz.

Change of bias condition will inevitably introduce gain variation. Fig. 20 shows the measured S11 and S21 under the different bias condition which covers the full 360° phase shift range. The S11 is less than -13 dB at 35 GHz. The S21 is about 21.3±4.3 dB. The gain variation can be compensated by the variable-gain-amplifier (VGA) which is usually utilized together with the LNA and phase shifter in a phased-array receiver front-end to ensure the gain accuracy [4]–[7]. Fig. 21 shows the IP_{1dB} variation and NF variation with the different codes of the switch, the control voltage is set as 0 V. The IP_{1dB} is about -25.2±2.0 dBm, the NF is about 5.0±0.8 dB.

Table 2 summarizes the performance of the proposed hybrid phase shifter and compares it with the state-of-the-arts (SOAs) phase shifters. This work demonstrates the 360° continuous phase shift range and the largest gain with competitive noise figure and relatively low power consumption, which achieves a good power efficiency.

V. CONCLUSION

This paper presents a hybrid π-network phase shifter, which covers a complete 360° continuous phase shift range with more than 25-dB gain at 35 GHz. The hybrid tuning scheme with both electrical and magnetic tunings contributes to an effective wide phase shift range. The embedded Gm stages enhance gain performance and power efficiency. Besides, the proposed phase shifter has competitive noise performance, the combination of the LNA and the phase shifter saves the power consumption and chip area of the receiver front end. This design idea can be widely deployed in RF signal paths for RF/mm-wave phased-array systems.

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