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# A Compact Octave Tunable Switched-Power-Combining PA

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**ABSTRACT** This paper presents a switched-power-combining RF power amplifier (PA) architecture, using evanescent-mode resonators as input splitters and output combiners. The input resonator also provides proper input matching to the transistor, eliminating the need for an input matching network, which reduces the overall size of the PA. The external couplings into the resonators are switchable to allow for activating one, two, or all three sub-PAs, depending on the power requirement. This results in a higher Output Back-off (OBO) efficiency, compared to a single PA. The presented concepts for the proposed architecture are supported by theoretical analysis and experimental validation. The implemented PA is based on Class-E sub-PAs, operates in the 1.2–2.4 GHz range, provides 36–40 dBm output power, and occupies an area of $41 \times 82$ mm$^2$. Compared to the state-of-the-art amplifiers operating at this frequency range, this resembles an average of 80% reduction in size.

**INDEX TERMS** Power amplifier (PA), power-combining, switched path, GaN, tunable amplifier, wideband.

## I. INTRODUCTION

Power amplifiers (PAs) play a significant role in evolving 5G systems. The projected omnipresence of picocells mandates strict limitations on their size, efficiency, and operating frequency range [1]. In addition, for sub-6 GHz base stations, a wide output power dynamic range is expected due to the long range of these signals (20 dB for LTE [2]). As a result, a significant amount of research has been published in the literature to explore various methods to enhance PAs performance.

Class-E PAs are typically preferred for their high peak efficiencies, reaching 85% [3], [4]. Their limited back-off efficiency can often be mitigated using advanced techniques such as envelop tracking. This, however, comes at the cost of limited bandwidth and added design complexity, which can prevent those amplifiers from becoming a ''drop-in-module'' in base stations [5]. Alternatively, Doherty-based amplifiers can deliver higher back-off efficiency using various power-combining and bandwidth-enhancing techniques. To improve the back-off efficiency, several three-stage Doherty amplifiers are proposed [6]–[9]. Such an architecture results in significant enhancement in back-off efficiencies (40% at 10 dB back-off). The required complex structure to split and combine the RF power, however, limits their bandwidth [7], [9], and results in larger form factor [6], [8]. Load-modulated balanced amplifiers [5], [10] also enhance the efficiency of amplifiers by injecting an additional control signal with pre-determined amplitude and phase. This might be a limitation since the phase of the additional signal source needs to be accurately controlled for every power level, adding to the power, size, and complexity of the design.

To enhance the bandwidth of Doherty PAs, distributed-element frequency compensation has been used to widen the frequency range to 3.0–3.6 (18%) GHz [11]. Further bandwidth enhancement can be achieved by using cascaded combiners/dividers or hybrid couplers at the input and the output of the amplifiers [12], or wideband commercially available hybrid couplers [6]. This increased the fractional bandwidth to 38–57%. Nonetheless, the cascaded dividers and hybrid couplers are composed of several $\lambda/4$ microstrip lines, resulting in an increased size of the amplifier. Circuit-based synthesis of discrete-component combiners have also been demonstrated for up to six transistors [4], delivering

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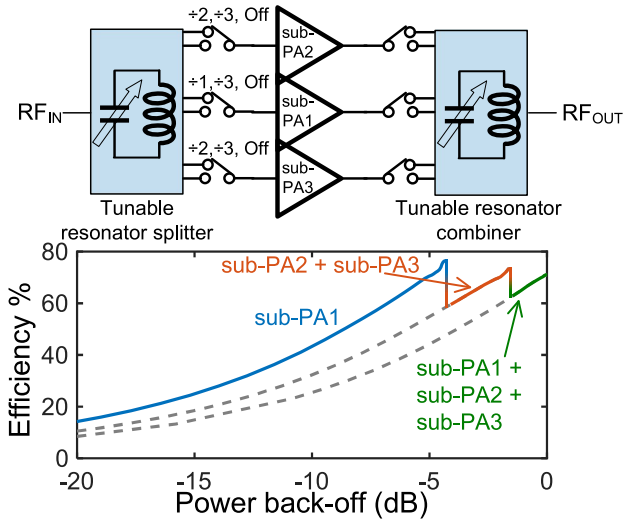


**FIGURE 1.** Switched-power-combining PA with resonators realizing input/output splitters/combiners. The efficiency versus power back-off (or output power normalized to maximum power) shows that the efficiency is increased compared to a single static PA.

1,500 W. This technique, however, is limited to relatively low frequencies (40 MHz), and operates over a narrow band. Furthermore, all the above mentioned amplifiers require a wideband input matching network (IMN) for each transistor to maintain the operational bandwidth.

In this paper, an architecture of switched-power-combining amplifiers is presented, with resonators as input splitters and output combiners. The advantage of having a switched-power-combining is that individual sub-PAs can be turned off to enhance back-off efficiency depending on the required output power. This is typically limited to on-chip transformers solutions [13]. The resonators used for splitting and combining the power are frequency-tunable evanescent-mode, which are known for their compactness ($\ll \lambda$), wide tuning range (approximately an octave), high power handling (10–100 W), high quality factor (100–1000), and coupling versatility [14]–[16]. As a result, the input splitter is also used as an impedance transformer, eliminating the need for an IMN. This architecture is demonstrated with three class-E sub-PAs, as conceptually shown in Fig. 1. The PA can operate between 1.2–2.4 GHz (67%), delivering 36–40 dBm peak output power. This wide operating frequency range, compact size, along with the ability of choosing the number of active PAs, makes this architecture suitable for high-density base stations such as in 5G systems.

## II. TUNABLE RESONATOR DESIGN

Evanescent-mode resonators are a suitable choice for the presented amplifier. This is primarily because they are compatible with PCB fabrication process, in addition to the electrical performance advantages mentioned earlier. Furthermore, the external coupling of evanescent-mode resonators allows for controlling the output impedance of the resonator in the design stage. As a result, the output impedance is designed such that it maintains its value regardless of the switching state (÷1, ÷2, or ÷3). In this section, the design of each of the resonators is detailed, along with their corresponding impedance role in the overall PA.

### A. INPUT SPLITTING RESONATOR

The main role of the input resonator is to split the input power to active sub-PAs. This can be realized by having a first order bandpass filter-like structure with multiple outputs (six in this work, see Fig. 1).

Fig. 2(a) and (b) show the proposed structure in evanescent-mode resonators. Each output is switched through a PIN diode, and coupled with a dc blocking capacitor that allows biasing the input of the sub-PAs and the PIN diodes independently.

The operation of the splitter is eminent around the resonant frequency. The cylindrical structure of an evanescent-mode resonator behaves as an inductor, which resonates with the post capacitance. As a result, the resonant frequency can be tuned by controlling the value of the capacitance between the center post and the outside of the cylindrical structure (shown as a lumped capacitor in Fig. 2(b)). The frequency response of the splitter is shown in Fig. 2(c) at various tuning capacitance values. Depending on the switch configuration, the splitter delivers the RF power to PA1 only, or divides it equally between PA2 and PA3 or among all three sub-PAs. The dimensions provided in Fig. 2 are designed such that the center frequency is 1.8 GHz.

To find the external coupling values that deliver the dividing responses, a single output (÷1) is first analyzed. From filter synthesis theory, the external coupling values are found by solving [17]

$$S_{21}(s) = 2\left(\begin{bmatrix}1&0&0\\0&s&0\\0&0&1\end{bmatrix} + jM\right)^{-1}_{3,1}, \tag{1}$$

where $M$ is the $3 \times 3$ normalized coupling matrix, and $s$ is the normalized complex frequency. For a maximally flat $S_{21}$, the external coupling is $M_{01} = 1/\sqrt{2}$. The coupling values for the outputs are then scaled with respect to the division ratios (1 for ÷1, $1/\sqrt{2}$ for ÷2, and $1/\sqrt{3}$ for ÷3).

As a result of the synthesis above, the ideal corresponding S-parameters for these three division modes at the center frequency are given by:

$$|S_{\div 1}| = \begin{bmatrix}0&1\\1&0\end{bmatrix} \tag{2a}$$

$$|S_{\div 2}| = \frac{1}{\sqrt{2}}\begin{bmatrix}0&1&1\\1&0&0\\1&0&0\end{bmatrix} \tag{2b}$$

$$|S_{\div 3}| = \frac{1}{\sqrt{3}}\begin{bmatrix}0&1&1&1\\1&0&0&0\\1&0&0&0\\1&0&0&0\end{bmatrix} \tag{2c}$$

It is important to note that the splitter resonator operates strictly as an even-mode divider, as the outputs are all

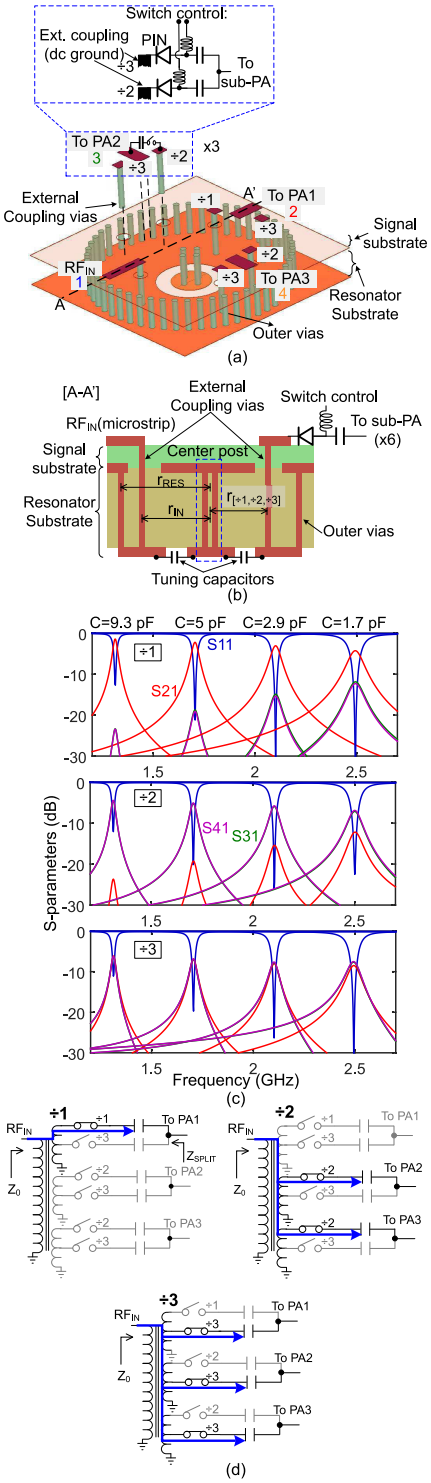


**FIGURE 2.** (a) An exploded view and (b) a cross section view of the splitter evanescent-mode resonator. (c) The simulated frequency response of the splitter at various capacitance values at all three dividing combinations (÷1, ÷2, and ÷3). (d) Equivalent circuit models for the splitter in the vicinity of the resonant frequency for all three modes. (Simulations are made with $r_{RES}$ = 10 mm, $r_{IN}$ = 6.5 mm, $r_{\div 1}$ = 5.9 mm, $r_{\div 2}$ = 6.7 mm, $r_{\div 3}$ = 7.3 mm, resonator substrate: TMM3 3.175-mm thick, and signal substrate: RO4350B 0.508-mm thick).

in-phase. As a result, there is no need for an additional resistor for matching in the odd mode (such as the one in Wilkinson dividers).

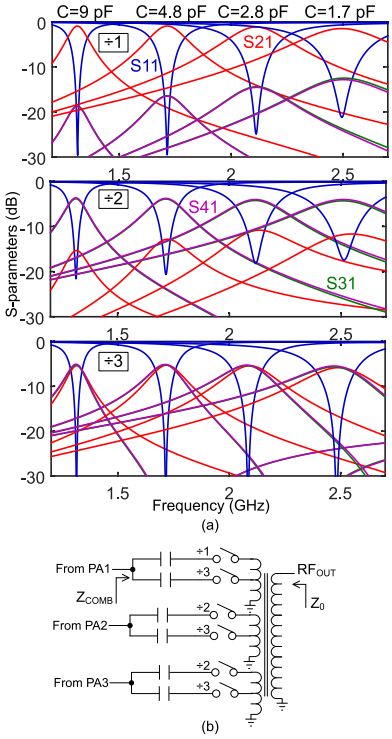


**FIGURE 3.** (a) Simulated frequency response of the combiner at various capacitance values at all three division combinations (÷1, ÷2, and ÷3). (b) Equivalent circuit model for the splitter in the vicinity of the resonant frequency. (Simulations are made with $r_{RES}$ = 10 mm, $r_{IN}$ = 4 mm, $r_{\div 1}$ = 4.2 mm, $r_{\div 2}$ = 5.2 mm, $r_{\div 3}$ = 6 mm, resonator substrate: TMM3 3.175-mm thick, and signal substrate RO4350B-0.508 mm thick).

At the splitter resonant frequency, each external coupling in the resonator can be modeled as a transformer [18]. The de-normalized output external coupling values (which dictate the location of the coupling vias) are chosen such that the impedance seen by each active transistor in the sub-PA is in the vicinity of the optimal input impedance $Z_{IN\ OPT}$ (the sub-PAs are designed such that $Z_{IN\ OPT}$ is real, details in Section III). This eliminates the need for a wideband IMN, resulting in a more compact design. The input impedance, however, is maintained at $Z_0$. The equivalent circuits that demonstrates this concept, at all division modes, are shown in Fig. 2(d).

### B. OUTPUT COMBINING RESONATOR

The design concepts of the output combiner resonator are similar to that of the input resonator. This includes the structure in Fig. 2(a) and (b) (with different dimensions for the external couplings), and the design equations. As a result, only the differences are discussed here.

The impedances at all ports of the combiner are kept at $Z_{COMB} = Z_0$. This is because the output of each sub-PA is matched to $Z_0$ as discussed in the next section. The response of the combiner resonator is shown in Fig. 3(a) at all three division configurations, at various frequency-tuning capacitor values. The output resonator is also centered at 1.8 GHz. The circuit model in the vicinity of the resonant frequency is shown in Fig. 3(b). The simulated combiner loss, which is

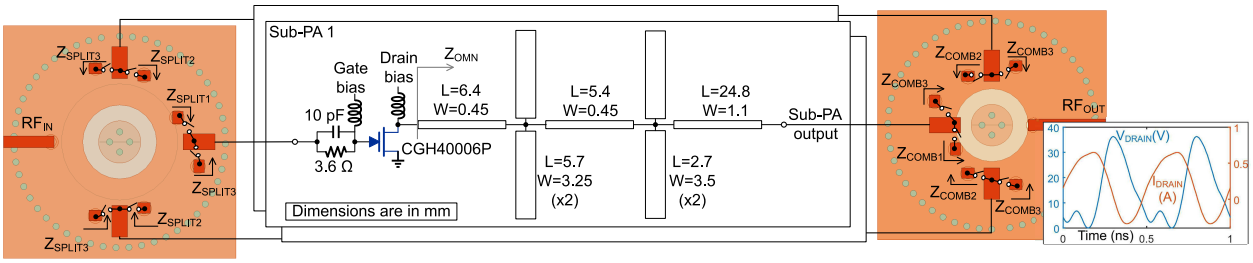


**FIGURE 4.** The schematic the PA showing the divider, combiner, and the OMN of the transistor. The divider delivers the required impedance to the transistor. As a result, no IMN is required. The three sub-PAs are identical. The time domain simulated current-voltage waveforms are also shown for a single PA ($P_{IN}$ = 23 dBm, f = 2 GHz).

critical in the efficiency of the PA, is 0.3–1.4 dB, taking into consideration the intrinsic division loss. Further reduction of the insertion loss can be achieved by using tuners with high quality factors, such as MEMS and piezoelectric-based ones [16], [19]–[21].

## III. CORE PA (SUB-PA) DESIGN

The three sub-PAs in Fig. 1 are identical. In this work they are biased in a class-E condition, using CGH4006P GaN transistor from Wolfspeed as the power device. The schematic diagram and the time domain waveforms of the PA are shown in Fig. 4. The details of the input and output matching are discussed in this section.

### A. INPUT MATCHING

To find the optimal input impedance for the maximum efficiency, source pull simulations are used including the device package. It can be seen from Fig. 5 that the maximum efficiency area is centered around $Z_{IN\ OPT} \approx 10 - 25\ \Omega$. As discussed in Section II-A, the output impedance of the splitter ($Z_{SPLIT}$) is designed such that it matches this impedance throughout the frequency tuning range. As a result, the input splitting resonator is sufficient for the sub-PA to operate at high efficiency.

To ensure a stable operation of each sub-PA at all frequencies, a parallel RC network is used at the gate of the transistor.

### B. OUPUT MATCHING

To design a compatible output matching network (OMN) for this widely tunable PA, the following factors are considered: 1) wideband response, 2) higher harmonic loading, 3) low loss, and 4) high power handling capacity. Using the synthesis techniques in [22], [23], a low-pass microstrip line OMN is synthesized for the sub-PAs.

As shown in Fig. 4, the second-order OMN is designed for the trade-offs between the wideband fundamental impedance load, and the higher-order impedance loading. A 50 Ω transmission line connects the OMN to the output combiner resonator, to maintain the same output impedance as well as the low loss connection. Fig. 5 also shows how the input impedance of the combiner inputs ($Z_{COMB}$) are matched to $Z_0$.

The impedances from the OMN, and from the load pull simulations are also shown in Fig. 5. The OMN maintains its impedance ($Z_{OMN}$) within the high-efficiency load pull circle throughout the tuning range (1.2–2.4 GHz). Furthermore, the harmonics are matched to the proper edge of the Smith chart (achieved by harmonic load pull) to enhance the efficiency. The load pull simulations are made at the center frequency (1.8 GHz). While the load pull circles are frequency-dependent, the drift due to frequency is reasonably small such that the concepts discussed above hold across the whole frequency range.

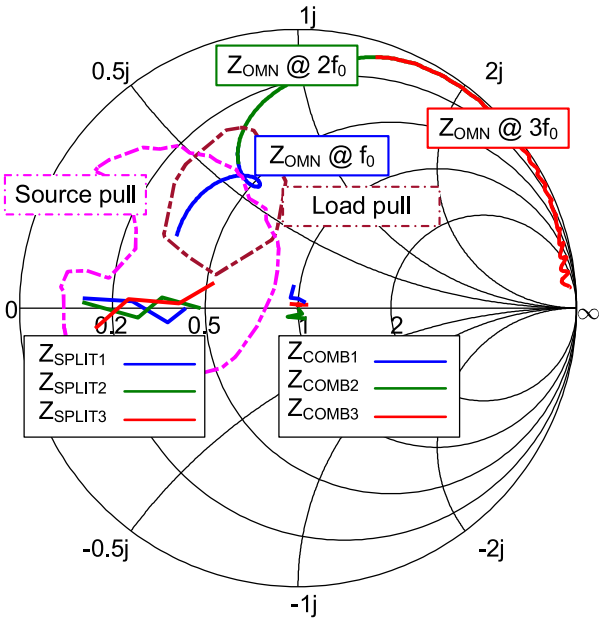


**FIGURE 5.** The output impedance of the splitter ($Z_{SPLIT}$) falls within the optimal input impedance of the transistor (source pull) throughout the tuning range (simulated). The OMN also shows good matching with the optimal output impedance of the transistor (load pull), and proper harmonic matching as well (measured). The combiner input and output impedances ($Z_{COMB}$) are maintained at 50 Ω (simulated). Load pull and source pull simulations are at 1.8 GHz.

### C. PA-RESONATOR CO-SIMULATION

The resonators and the three sub-PAs are designed and simulated to study the feasibility of this architecture in terms of tuning range and OBO efficiency. The efficiency and gain simulations, shown in Fig. 6, demonstrate that the PA operates at maximum efficiency when delivering the maximum power.

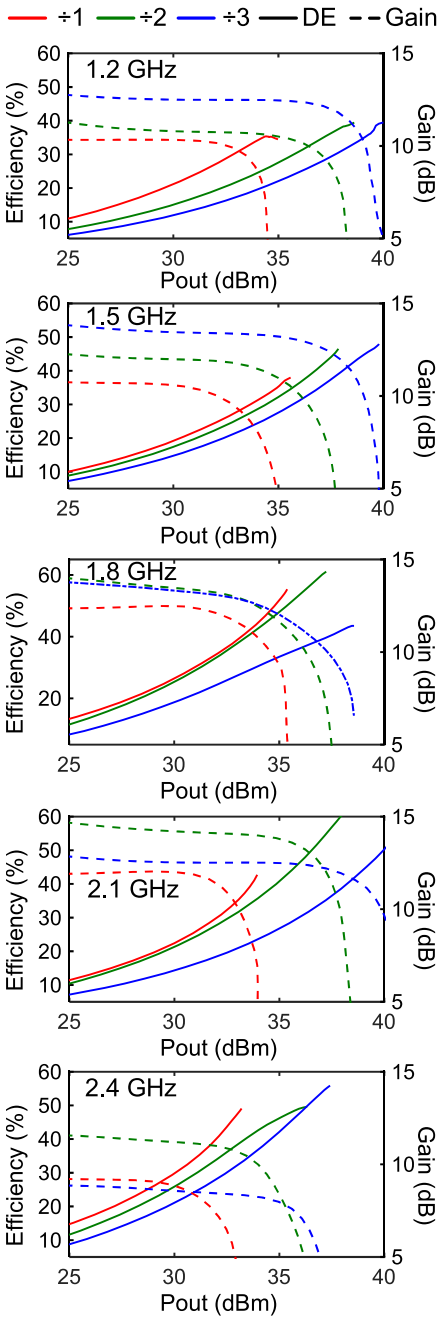


**FIGURE 6.** Simulated drain efficiencies and gain of the PA and the splitter/combiner resonators across the tuning range of 1.2–2.4 GHz.

Below that, it can be more feasible to turn one or two of the sub-PAs off to maintain the high efficiency operation. This behavior is observed over the tuning range of the resonators.

## IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

### A. PIN DIODE POWER LIMIT

PIN diodes have a finite resistance when turned ON. As a result, there is a finite amount of power that they can pass before they overheat. The power dissipated in a PIN diode, $P_{PIN}$, is given by [24]

$$P_{PIN} = \frac{4R_S Z_S}{(2Z_S + R_S)^2} P_{AV} \approx \frac{R_S}{Z_S} P_{AV}. \quad (3)$$

where $R_S$ is the effective series resistance of the diode, $Z_S$ is the system characteristic impedance ($Z_{SPLIT}$ at the input resonator, $Z_{COMB} = Z_0$ at the output resonator), and $P_{AV}$ is the available RF power. The approximation stems from the fact that $R_S$ is typically much smaller than $Z_S$.

From (3), it can be noticed that the dissipated power in the PIN diode is inversely proportional to $Z_S$. This is critical because, at the input, the system impedance is relatively low $Z_S = Z_{SPLIT} \approx 10\ \Omega$. As a result, even though the input to the transistor has a lower power than the output, the power dissipated in the PIN diode can still be significant.

For the diode in this work, BAP55LX from NXP semiconductors, the maximum value of $P_{PIN}$ is 0.135 W, and a typical ON resistance is 1 Ω (at 10 mA forward bias). Using (3), it can be found that the maximum available power that can exist at the input of the transistor is 1.35 W. At the output of the transistor, this power is 6.75 W. These values are above the target of this work. As a result, the selected PIN diode is suitable for this application.

### B. PA ASSEMBLY

The PA is implemented in two substrates: the signal substrate (RO4350B 0.508-mm thick), which contains the discrete components and the OMN, and the resonators substrate (TMM3 3.175-mm thick). The substrates are then laminated and the external coupling vias are connected manually. The resonators are tuned by adjusting the value of the tuning capacitors. Numerous tuning techniques, however, exist to tune evanescent-mode resonators in the field repeatably and accurately [16], [19], [25]–[27]. The picture of the implemented PCBs are shown in Fig. 7(a). Fig. 7(b) shows the final assembled PA.

The bias voltages of the transistors are $\sim -2.7$ V for the gate, and 16 V for the drain. For any unused sub-PA, the drain is grounded and the gate is biased at $-8$ V, to minimize any loading effect on the rest of the circuit. The PIN diode switches are biased with 10 mA for the ON state, and $-20$ V for the OFF states. For all dc bias voltages, BCL-531 conical inductors, from Coil Craft, are used as RF chokes.

### C. EXPERIMENTAL RESULTS

The PA test setup is shown in Fig. 8. The PA is tested at all three dividing conditions with a continuous-wave (CW) signal.

In Fig. 9, the efficiency and gain of the PA are measured at various frequencies within the tuning range. The design is centered around 1.8 GHz, and coveres the octave of 1.2–2.4 GHz.

At a specific power back-off from the maximum, the required output power can be delivered with two amplifiers (÷2) at a higher efficiency. As a result, this output power level is the threshold to maximize the efficiency. Similarily, another threshold exist between (÷2) and (÷1).

A summary of the measured drain efficiencies is shown in Fig. 10(a). For the majority of the spectrum, the maximum

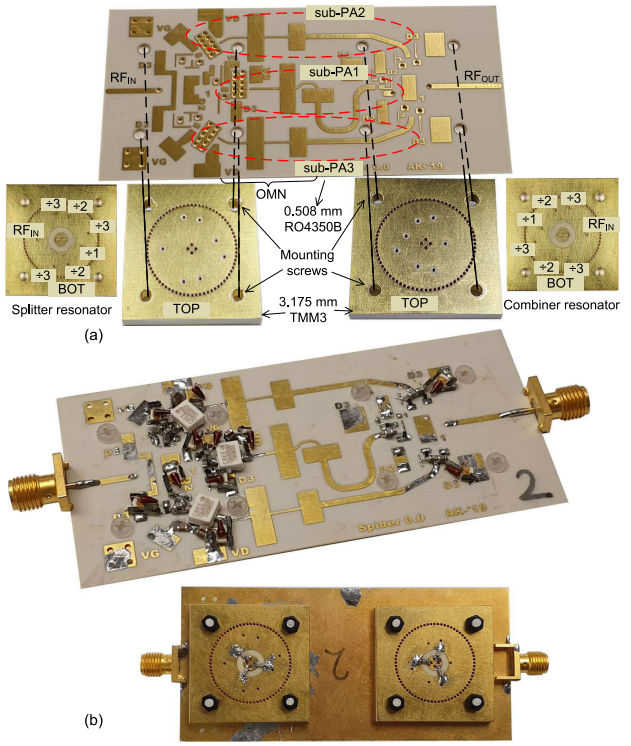


**FIGURE 7.** A photograph of the presented work prototype. (a) Bare PCBs. (b) Assembled and populated PA (bias wires are removed for clarity).

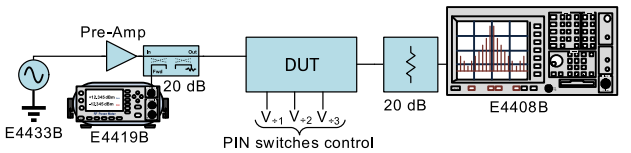


**FIGURE 8.** A schematic of the test setup of the presented PA.

efficiency from a single amplifier is higher than that of two or three amplifiers. This is expected since, for the (÷1) configuration, the signal goes through less PIN switches. The difference between the ÷2 and ÷3 configurations, however, is negligible. The drain efficiency is also shown for 6 dB Output Back-Off (OBO).

Another important measure shown in Fig. 10(a) is the OBO at which a transition between dividing configurations is necessary. This data can be saved in a controller to dictate which sub-PAs to activate at a given required output power.

The maximum output powers delivered from the PA is shown in Fig. 10(b). Naturally, the ÷3 configuration delivers the highest power, which is between 36 dBm and 40 dBm. The maximum output powers from the ÷2 and ÷1 are also shown, along with OBO at which it is feasible to change the number of active PAs. The difference between those powers shows a reasonable agreement with the theoretical expected values (3 dB and 4.7 dB).

To demonstrate the functionality of the presented PA in a realistic scenario, a 16QAM signal is used to modulate the

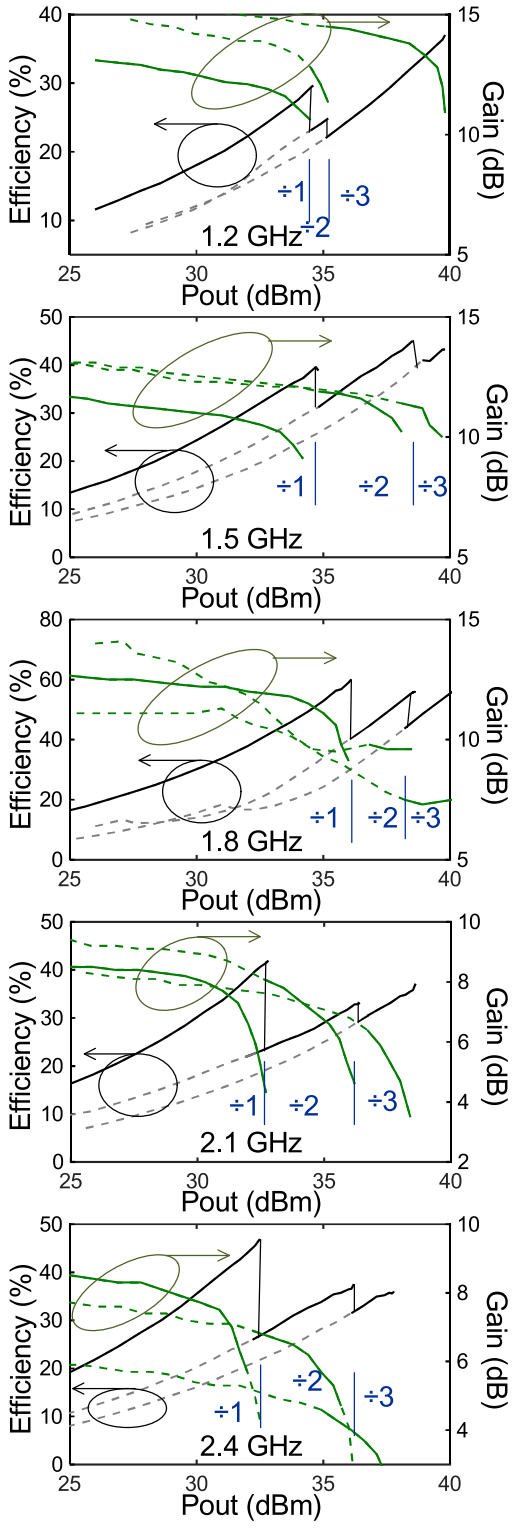


**FIGURE 9.** Measured drain efficiencies and power gains versus the output power. Depending on the required output the number of active sub-PAs is chosen to maximize the efficiency. The PA operates between 1.2–2.4 GHz.

carrier, and the Adjacent Channel Power Ratio (ACPR) is measured for all three dividing configurations. Fig. 11 shows the measured spectrum and ACPR values, along with the

**TABLE 1. State-of-the-art comparison table (GaN-based PAs).**

| Ref. | year | Architecture | Area (mm×mm) | Freq. range (GHz) | BW (%)[a] | $P_{MAX}(dBm)$ | DE @ $P_{MAX}$ (%) | DE @ 6 dB OBO (%) |
|---|---|---|---|---|---|---|---|---|
| [7] | 2017 | 3-way Doherty | 139 × 104 | 2.14 | 0 | 50 | 33.7 | 30[b] |
| [6] | 2019 | 3-way Doherty | 170 × 100[c] | 1.6–2.6 | 48 | 46 | 53–66 | 52–63 |
| [9] | 2018 | 3-way Doherty | 110 × 80[c] | 2–2.6 | 26 | 43–45 | 53–76 | 45–60 |
| [28] | 2020 | Doherty/Balanced | 113 × 88 | 3.4–3.6 | 6 | 42 | 67[b] | 50[b] |
| [12] | 2019 | Doherty/Traveling Wave[d] | 120 × 95[c] | 2.5–3.8 | 40 | 49–50 | 54–67 | 43–53 |
| [11] | 2017 | Doherty w/ freq. comp. | 60 × 78 | 3–3.6 | 18 | 48–49 | 46–50 | NA |
| [5] | 2020 | Doherty/Load mod. | 203 × 102 | 1.5–2.7 | 57 | 43 | 58–72 | 47–61 |
| [10] | 2018 | Load modulated | 170 × 70[c] | 1.7–2.5 | 38 | 48–49 | 48–58[e] | 43–53[e] |
| [3] | 2013 | Class-E | 140 × 80[c] | 0.9–1.5 | 50 | 49.5[f] | 85 | NA |
| [4] | 2020 | Class-E[g] | 160 × 120 | 0.04 | 0 | 62 | 89 | NA |
| This work | | Switched Class-E | 41 × 82 | 1.2–2.4 | 67 | 36–40 | 33-54 | 27–50 |

[a] BW=2($f_{max}$-$f_{min}$)/($f_{max}$+$f_{min}$). [b] Estimated from plots. [c] Approximated from photograph.
[d] Five transistors. [e] PAE. [f] CW signal (not pulsed). [g] Six transistors.

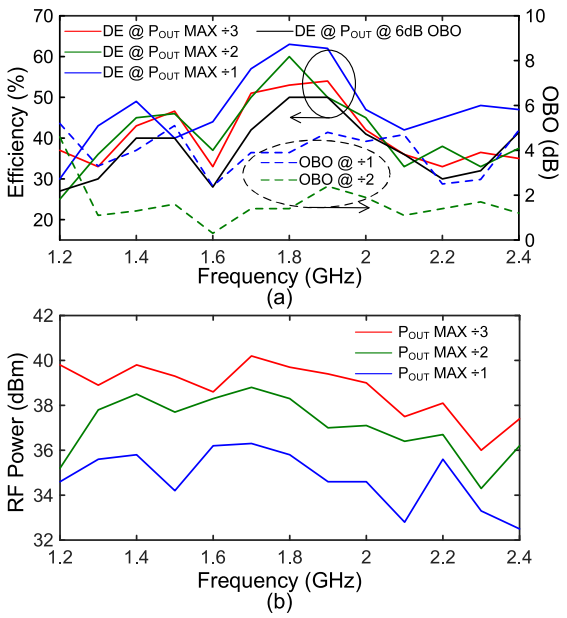


**FIGURE 10.** (a) Drain efficiencies at the maximum output power for all three configurations, in addition to 6 dB OBO, are shown versus frequency. Also, the OBO compared to the maximum power, at which the PA can switch between different dividing configurations to increase the efficiency, are plotted in dashed lines. (b) The maximum deliverable output power for each dividing configuration across the tuning range is shown versus frequency.

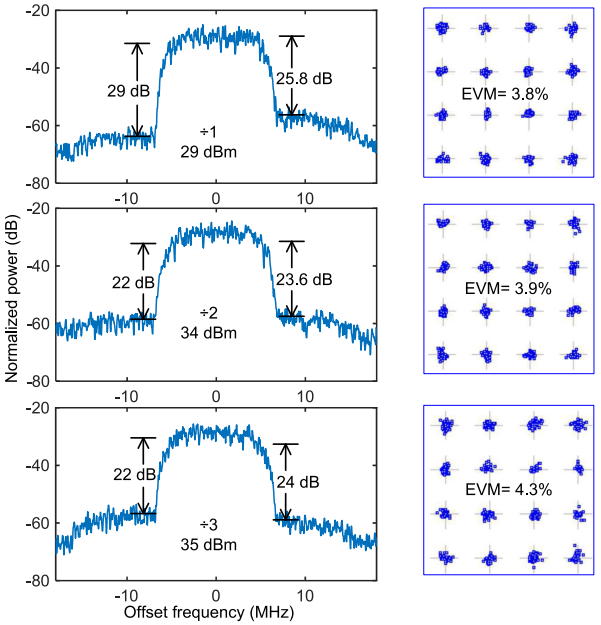


**FIGURE 11.** Measured spectrum and ACPR, in addition to the constellation of a 16QAM signal at various output powers (Measured with 10 MSPS without digital predistortion).

signal constellation. The PA maintains a fairly constant Error Vector Magnitude (EVM) across a wide output power range, with no digital predistortion (DPD).

Table 1 summarizes a comparison with the state-of-the-art GaN-based amplifiers. Typically the size of a PA is compromised for a wide operating frequency range, primarily due to the use of multi-stage hybrid couplers. Also, while published class-E amplifiers have high Drain Efficiency (DE) at the maximum output power ($P_{MAX}$), the OBO efficiencies are typically low and not reported. Compared to amplifiers operating in a similar frequency range [5], [6], [10], the presented amplifier occupies 80% less area in average. The presented PA can achieve an octave frequency range, while maintaining a small form factor, and good OBO efficiency.

## V. CONCLUSION

The novel PA architecture presented in this work delivers an octave frequency tuning range without the need of multi-stage combining network. This reduces the design area by 80%, compared to reported amplifiers operating in a similar frequency range. Furthermore, the ability of switching the number of active sub-PAs enhances the OBO efficiency compared to conventional class-E architectures. These features result in an amplifier that is suitable for high-density base stations, where efficiency, size, and wide frequency operation is essential.

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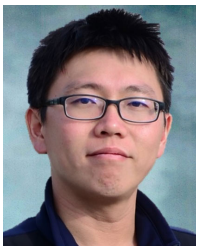

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