IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received December 6, 2020, accepted December 26, 2020, date of publication January 11, 2021, date of current version January 22, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3050705

A Novel Real-Time Fast Fault-Tolerance Diagnosis and Fault Adjustment Strategy for m-Phase Interleaved Boost Converter

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This work was supported by the National Undergraduate Innovation and Entrepreneurship Training Program under Grant 201910500009.

ABSTRACT In order to address the problem of power transistor fault in interleaved boost converter (IBC) of any interleaved phase, we propose a real-time fast diagnosis and fault-tolerant method of power transistor. With the single boost converter as the object, we analyze the logical relationship between inductor voltage and drive signal under continuous conduction mode (CCM) and dis continuous conduction mode (DCM). To reduce the cost, the inductor voltage can be obtained based on the winding applied on the toroidal inductor, which does not require introducing additional measurement component. The fault is supervised in a real-time manner, which makes the online processing of fault possible. Considering that the current is no longer symmetrical after removing fault, which will cause increase of harmonic content in the output fault, this article proposes a strategy to adjust the phase and frequency, and this method can realize operation of interleaved converter with reduced interleaving phase, thus reducing the influence of fault to the minimum. Finally, the accuracy and effectiveness of fault diagnosis and fault tolerance are proved by simulation and experiment, and the effectiveness of adjustment strategy after the fault is also verified.

INDEX TERMS Interleaved boost converter, power transistor fault, real-time fault detection, fault adjustment strategy.

I. INTRODUCTION

With the development of new energy, the solar street lamp has gradually attracted more concern. The solar street lamps can be used in large scale on large scale in the areas with abundant sunlight, but such areas might have harsh natural conditions. The direct sunlight during the day might generate high temperature, and if the solar street lamp is installed in an open space, it may suffer from lightning stroke, which may damage the power converter. Practices show that power transistor is the weakest link in converter, and most faults are manifested as the open circuit and short circuit of power transistor [1]. The damage of power transistor might increase the voltage and current stresses of other components in the circuit, and if the fault is not removed in time, it will cause a secondary fault, which will finally lead to the crash of the entire system. In order to ensure the power supply and illumination of street lamp, the converter should still be able to continue working even when there is damage to the power transistor. Therefore, the online real-time detection of power transistor fault and the fault tolerance and control strategy of converter has great significance in improving the reliability of the power supply system of solar street lamp.

In order to achieve this objective, choose the converter with the topology that has integrated a backup branch, and interleaved converter satisfies this design requirement. Furthermore, the interleaved parallel structure of interleaved DC/DC converter can not only improve the power capacity of converter [2], but also increase its equivalent switching frequency, which has significant advantages on the aspects of current ripple and harmonic characteristic [3], [4]. This kind of converter is applicable to high-power energy transformation.

To realize real-time fault diagnosis correction, the fault that occurred in the circuit should be detected first. There are many fault detection methods. For example, in [5] , the duty cycle inter-partition analysis of drive signal under CCM is conducted to obtain the characteristics of input current, and then, the sampling analysis of input current is conducted. However, in engineering, this method has a high requirement

The associate editor coordinating the review of this manuscript and approving it for publication was Zhixiang Zou.

for the precision of current sampling. Furthermore, under extreme conditions, analog components (e.g.: operational amplifier, etc.) are under significant influence from environmental factors, such as temperature, which are not suitable for our design. In [6], [7], a fuse is integrated into the ground connection of power transistor, the fuse will blow out when it reaches the maximum current during short circuit, and the short circuit can be transformed open circuit for analysis. However, the author believes that if a fixed current is set as the basis to determine short current, it will take certain time for the current to reach the preset maximum current. If this preset value is too high, it will cause an impact on the components and lacks sensitivity; on the contrary, if this value is too low, it may cause misjudgment during normal fluctuation of current or short-term impact, which cannot ensure stability. Furthermore, with the change of load, the standard based on which to set this current will also change, and it is not easy to adjust the maximum current. In [8], with 3-phase IBC as an entirety, they also analyzed the duty cycle in segments. There are many classified discussions, which are very difficult for analysis, and it will become more complicated after being extended to higher order of interleaving. Reference [7] provides an adjustment strategy after fault, which also deserves further investigation. In [9], [10], based on the shape of inductor current, the detection and fault diagnosis are conducted by the single field-programmable gate array (FPGA), which can realize recognition and handling of short-circuit and open-circuit faults of a power transistor. However, it also has the defects of complicated diagnosis method, difficulty for implementation and high cost.

After analysis of the basic principle and harmonic characteristics of IBC, this article proposes a method capable of fast online fault diagnosis of power transistor under both CCM and DCM. In other words, by using the winding applied on the toroidal inductor as the voltage transformer, measure the voltage on the two sides of inductor. After splitting the IBC into basic boost converter for analysis, for each phase of IBC, we design the circuit which can provide isolation amplification for inductor voltage signal, determine the state logic and eliminate the interference. The fault of each phase can be detected quickly and accurately within one switching cycle. This method does not need to consider the change of duty cycle, the change of load and other factors, and compared to other methods, it has lower cost of circuit and faster detection of higher sensitivity, which applies to interleaved circuit of any order and has broader application scope. After fault recognition, the short-circuited branch can be actively disconnected by controlled switch such as controlling relay, so that the short-circuit fault (SCF) can be transformed to open-circuit fault (OCF), and then, it will be handled as an open-circuited problem, which can simplify the fault handling process. We should discuss various possible open-circuited states, provide solutions for various faults, adjust the control strategy and reduce the output current ripple, to realize the minimum influence of power transistor damage on converter.

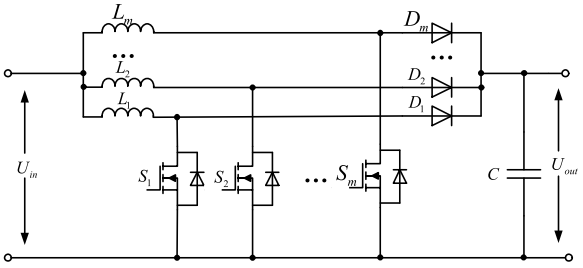

FIGURE 1. The topology of the IBC.

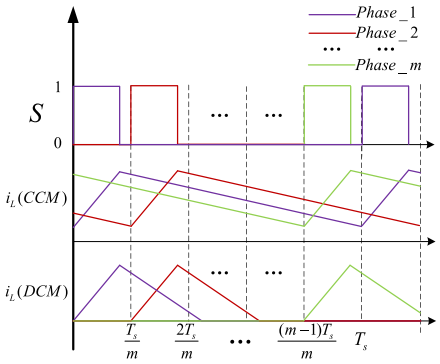

FIGURE 2. State of transistor and inductor current for each phase.

II. CURRENT ANALYSIS AND CURRENT HARMONIC CALCULATION OF IBC

A. CURRENT ANALYSIS AND CALCULATION ON HARMONIC

The topology of the IBC is as shown in Fig. 1, which combines multiple boost converters with the same structure to form a complex convertor through phase interleaved [11]–[13]. Assume this IBC contains m phases, which will be called m-phase IBC hereinafter. In the topology, $S_1 \sim S_m$ are the power transistors, which can be composed of MOSFET or IGBT; $D_1 \sim D_m$ are diodes, which are used to ensure that the current will only flow to the load; $L_1 \sim L_m$ are the inductors of various phases; the output C is the filter capacitor.

Inductor is the core component of boost convertor, and if the convertor is working under CCM, the current flowing through inductor at steady state only experiences the following two processes: linear increase during charging of inductor and linear decrease during discharging of inductor; if the convertor is working under DCM, there is one more zero-current state than that under CCM during steady-state operation.

For the m–phase current analysis, assume the switching period of each phase is T_s, the switching frequency of power transistor is f_{sw}, the duty cycle of PWM signals in each phase is D, and the inductor current for the n^{th} phase is i_{Ln}. In order to ensure the symmetry of output current, the switching period is divided into m parts, and the phase difference between the PWM of one phase and PWM of the adjacent phase is all T_s/m. Analyze the power transistor state S and the waveform of the inductor current for each phase.

It can be seen that under the same duty cycle of PWM, the waveform of inductor current is completely identical. The phase difference is T_s/m, and by adding the inductor current of all phases, we can obtain the input current i_{in}:

$$i_{in} = \sum_{n=1}^{m} i_{Ln} \tag{1}$$

Next, the ripples of the input current and output current of converter are analyzed from the perspective of frequency domain [14], which can provide theoretical basis for the analysis of ripple change after a fault in the following part.

Because the current waveform of CCM is different from that of DCM, the current harmonics under CCM are analyzed first. Assume the DC component is I_0, take the j^{th} period, and express this process with the following mathematical formula:

$$\begin{aligned} i_L(t) &= \begin{cases} I_0 + \dfrac{\Delta I_L}{DT_s}\left[t - (j+\dfrac{D}{2})T_s\right], & t \in [t_{start}, t_m] \\ I_0 - \dfrac{\Delta I_L}{(1-D)T_s}\left[t - (j+\dfrac{1+D}{2})T_s\right], & t \in [t_m, t_{end}] \end{cases} \\ t_{start} &= jT_s, \quad t_m = (j+D)T_{s,end} = (j+1)T_s \end{aligned} \tag{2}$$

Conduct Fourier series expansion of this periodic current, and we can obtain as follow:

$$\begin{aligned} i_L(t) &= I_0 + \sum_{n=1}^{\infty} A_n \cdot \sin(n\omega_s t + \theta) \\ A_n &= \frac{\Delta I_L \, |\sin(nD\pi)|}{\pi^2 n^2 D(1-D)} \\ \theta &= \arctan\left(\frac{\cos(2nD\pi) - 1}{\sin(2nD\pi)}\right) \end{aligned} \tag{3}$$

Substitute the current of one phase to (1) to obtain:

$$\begin{aligned} i_{in}(t) &= i_L(t)(1 + e^{-j\frac{2n\pi}{m}} + \ldots + e^{-j\frac{2(m-1)n\pi}{m}}) \\ &= \begin{cases} 0, & n = mk + p \\ m i_{Ln}, & n = mk \end{cases} \\ & \qquad (k \in N; p = 1, 2, \ldots, m-1) \end{aligned} \tag{4}$$

Therefore, it can be seen that the input current of m-phase IBC only contains the harmonic component of m-time inductor current switching frequency, so the equivalent switching frequency of m-phase IBC is $f_{eq} = m \cdot f_s$.

Let $n = 1, 2, 3$, and the relational graph between various harmonic components and duty cycles of single-phase converter, three-phase converter and five-phase converter can be drawn, as shown in Fig 3.

Under DCM, only the inductor current is different from that under CCM. The analysis method is also the same: list the expression of inductor current, and then conduct Fourier series expansion. Because related analysis is length, we will quote the conclusion reached in [16]–[19], and according to their conclusion, the total current harmonics still only contain the harmonic component which is m times of the harmonic of inductor current, which still satisfies $f_{eq} = m \cdot f_s$.

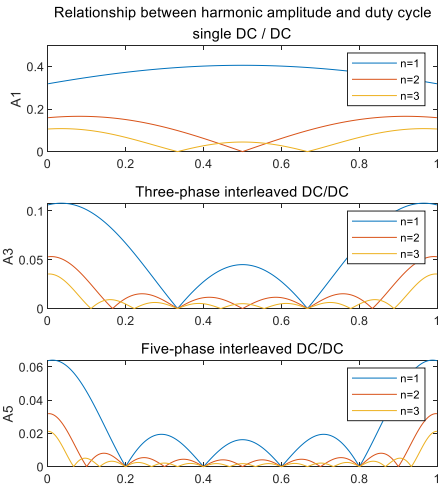

FIGURE 3. Relationship between harmonic component amplitude and duty cycle for different phase IBC.

B. SUMMARY

According to the above analysis of current, the total current is evenly distributed to each phase. The power capacity of converter can be effectively expanded by adopting the multi-phase structure, which can be applied to the scenario with high conversion power.

Based on the above harmonic analysis of m-phase IBC, it can be seen that the equivalent switching frequency of m-phase IBC is m times of the switching frequency, and the ripples show a significant weakening trend with the increase of phases. Furthermore, if the duty cycle is near p/m ($p = 1, 2, \ldots, m-1$), each harmonic will be close to 0, which can significantly optimize the subsequent filter design.

III. FAST FAULT DIAGNOSIS

A. ANALYSIS OF SINGLE PAHSE FAULT

According to the above analysis, the inductor current of each phase is of the same amplitude, so we only analyze one phase to simplify the analysis process. Because inductor voltage is not only closely related to power transistor, which is not under indirect disturbance from the parameter fluctuations of other components. we choose inductor voltage as the fault characteristic signal. In order to prevent using additional sensor and to reduce cost, in this article, the winding coil wound on the same ferrite core as the original inductor coil in the same direction is added and used to measure the inductor voltage, which is denoted as voltage U_k of the inductor. The winding coil will be called mutual inductor hereinafter.

A relay or switching element is added between inductor and power transistor to detect the short-circuit fault (SCF) and then shut down the circuit. Each phase of the circuit can be transformed as shown in Fig. 4.

Under normal circumstance, the waveforms of the inductor voltage and inductor current under steady-state operation are as follows:

According to the drawing, when the power transistor drive signal PWM is at the high-level current rise period, U_k is positive voltage; while when PWM is at the low-level current

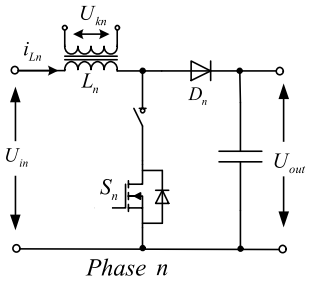

FIGURE 4. Improvements in the basic converter to detect fault and protect circuit.

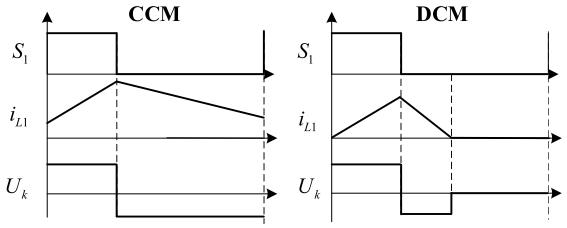

FIGURE 5. The waveforms of the inductor voltage and inductor current under steady-state.

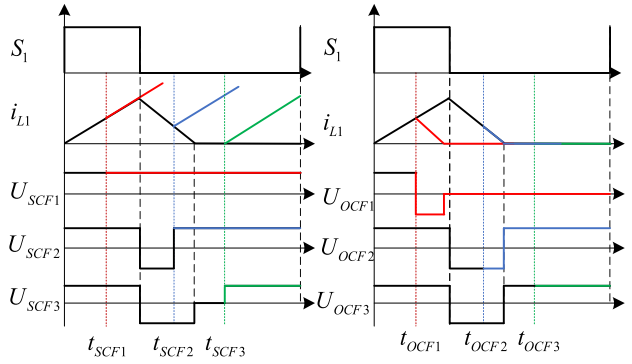

FIGURE 6. Waveforms of mutual inductor when SCF and OCF occur. where, the black waveform is the waveform under normal operation, while the red, blue, and green ones are the waveforms of inductor current and mutual inductor voltage after a fault occurs at different moments.

decline period, U_k is negative voltage; when the current is 0, U_k is zero, and CCM can be regarded as a special case of DCM. Therefore, next, we will analyze the change of inductor current and mutual inductor voltage after failure under DCM.

Under DCM, sudden SCF may occur at certain moment t_{SCF1} during the rise of inductor current, and it may also occur at moment t_{SCF2} during current decline or moment t_{SCF3} when the current is 0. A sudden open-circuit fault may also occur during these three periods, and the moments when fault occurs in these three periods are denoted as t_{OCF1}, t_{OCF2} and t_{OCF3}, respectively. We analyze the voltage waveforms of mutual inductor when SCF and OCF occur during these periods, and draw their waveform graphs as follows.

Based on waveform analysis, we can obtain the following two conditions:

(1) if there is short-circuit fault, the short-circuit information will only be reflected when PWM is at low level, all faults of $SCFx(x = 1, 2, 3)$ will result in positive voltage of U_k within the current switching period, and in other words, the short-circuit fault can be determined within the current switching period T_s.

(2) If there is open-circuit fault, the open-circuit fault information OCF can only be presented when PWM is at high level, which is represented as U_k is negative voltage or 0. Firstly, for the open-circuit fault occurred at moment t_{OCF1}, because PWM is at high level, when the mutual inductor voltage shows non-positive voltage signal, the fault can be immediately detected within the current period. Ultimately, for the open-circuit fault occurred at moments t_{OCF2} and t_{OCF3} when PWM is at low level, the mutual inductor voltage U_k presents consistent trend as that in normal situation, and the fault cannot be detected when PWM is at low level. However, when PWM is at high level in the next switching period, because U_k is not positive voltage, the fault will be immediately detected. In other words, after the open-circuit fault has occurred, the fault can also be detected within one switching period.

In conclusion, by combining the above analysis, accurate detection of two faults can be realized within one switching cycle by comparing the logic relationship between PWM and U_k. This method can be applied to diagnose the fault that occurred in a fast and sensitive way, and the corresponding adjustment can be applied as soon as possible after the fault has occurred in the circuit.

B. SIMPLIFICATION OF DIAGNOSIS MODEL

Based on the above fault diagnosis and analysis, there is no difference during fault detection when $U_k = 0$ and when Uk is negative voltage, we combine these two situations and only consider $U_k = 0$, and when U_k is positive voltage, it is regarded as high level. For the convenience of description in the following part, $S_k = 1$ is used to express that U_k is at high level, and $S_k = 0$ is used to represent that U_k is at low level. By further simplifying the state, we can obtain the following conclusion. When $S_k = 1$, SCF; is output only when PWM is at low level. When $S_k = 0$, OCF, is output only when PWM is at high power level, and other conditions are low level.

The logic circuit diagram of fault signal output can be established based on above analysis, and the circuit consists of an OR gate, a tristate transmission gate enabled by low level and a tristate NOT gate enabled by high level. The PWM signal is the enable signal, S_k is the input signal of two tristate transmission gates, the output signal SCF and signal OCF are both faults, so the final output signal is *Fault* after OR operation.

C. IMPROVEMENT OF FAULT DIAGNOSIS CIRCUIT

1) IMPROVEMENT ONE: ELIMINATION OF FALSE TRIGGERING

The above analysis is based on the assumption that the digital logic device is working at an ideal state, but in reality, various effects may result in time difference between the PMW signals and mutual inductor signals, such as the layout of

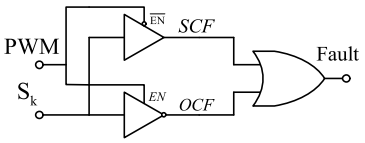

FIGURE 7. Logic circuit diagram.

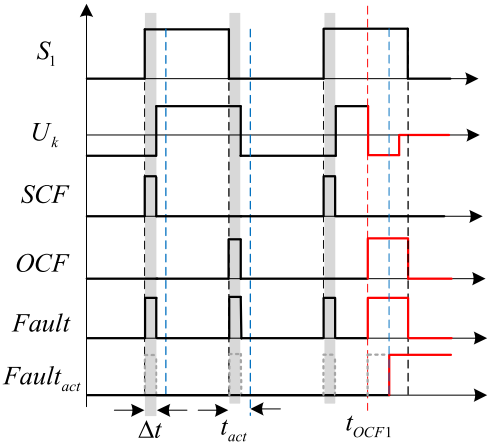

FIGURE 8. Signals in reality, U_k lags behind the PWM signal and the grey area indicates the time difference Δt, and the red line indicates the waveform after the fault.

component and the delay in turning on and off the power transistor, which may cause misdiagnosis of fault and further lead to malfunction of circuit. In practical engineering applications, to improve the accuracy and effectiveness of circuit fault diagnosis, the circuit should have certain tolerance of fault signal *Fault*. Based on analysis under CCM, assume the open-circuit fault suddenly occurs during the rise of i_L. In practice, the interference from device wiring can be removed via optimization in actual design, but certain switching delay t_{delay} when turning on power transistor cannot be eliminated through design optimization. As a result, U_k lags behind the PWM signal.

Assuming the time difference is Δt, accurate time data can be obtained by measuring the time difference between two signals in practice. To eliminate this influence, we can set an actuation time t_{act}, and make $t_{act} > \Delta t$. If the high-level time of detected fault signal *Fault* is shorter than t_{act}, the final output $Fault_{act}$ does not actuate; if it is longer than t_{act}, the fault actuating signal $Fault_{act}$ is triggered and maintains at high level.

2) IMPROVEMENT TWO: SIGNAL ISOLATION

If the auxiliary winding voltage is directly collected, it will be affected by the ripple voltage. In order to address this problem, an isolation amplification circuit is designed in this article for preprocessing of voltage, and its principle is basic as that of [15].

In summary, the complete module which can $Fault_{act}$ consists of four parts, which are the mutual inductor voltage signal collection and isolation amplification circuit, the logic judgment circuit, the low-pass filter, and the

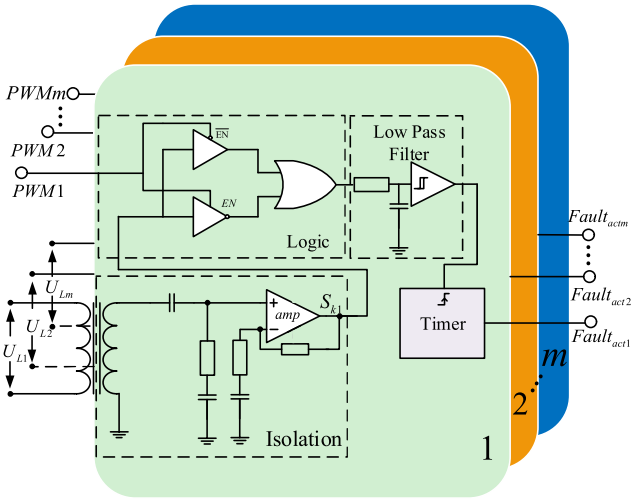

FIGURE 9. The complete real-time fast diagnosis and fault-tolerant method of power transistor module for m-phase IBC.

time-delay operation timer, respectively. The integration module consisting of *m* phases is as follows, shown in Fig 9:

D. COST AND IMPLEMENTATION DIFFICULTIES

Compared with the basic boost circuit, IBC need more power transistors, but it increases the power capacity of the converter. On the assumption of keeping the power capacity unchanged, IBC can use the power transistors which are lower than the rated current of the basic boost circuit to reduce the cost. In the basic boost circuit, the inductor contains winding and ferrite cores itself, but the method proposed in this article only needs to add several turns of coils in the ferrite cores. Compared with IBC, the increased cost can be ignored.

The components for accurate current measurement are omitted, and the cost is reduced. However, in the actual circuit design, the time difference caused by the voltage of the inductor caused by the switch delay lagging behind the PWM signal can't be accurately controlled, and the action time can only be determined by accurate measurement in advance.

IV. CORRECTION AND ADJUSTMENT OF CONVERTER CONTROL SIGNAL AFTER FAULT

A. CORRECTION OF SHORT-CIRCUIT FAULT

If a short-circuit fault occurs to the power transistor, but the short-circuit source is not cut off in time, the power source, inductor and short-circuit power transistor will form a closed circuit, the current will increase sharply within short time, and the power source and device will suffer from high voltage and current stresses. If the fault actuating signal $Fault_{act}$ of one phase is detected, immediately remove the relay enable signal of this phase to disconnect this phase, and make the phase at open-circuit state. In this way, SCF will be transformed to OCF, and then subsequent processing can be conducted. In the meantime, the information can also be reflected to the general control desk using communication approaches such as Lora, so as to notify the supervisor of the convertor state.

TABLE 1. Phase shift strategies for three-phase converter.

$Fault_{act}$ for each phase			phase difference of 1st phase and others	
$Fault_{act1}$	$Fault_{act2}$	$Fault_{act3}$	2nd phase	3th phase
0	0	0	1/3T	2/3T
1	0	0	1/3T	2/3T
0	1	0	-	1/2T
0	0	1	1/2T	-
1	1	0	-	-
1	0	1	-	-
0	1	1	-	-

"-" represents nonsense so the number can be ignored

B. CORRECTION OF OPEN-CIRCUIT FAULT AND RECONFIGURATION OF CONTROL SIGNAL

After open-circuit fault occurs, if no adjustment is adopted, although it won't cause severe impact on circuit like short-circuit fault, some negative consequence will still be generated after long-term running, which is specifically represented as:

1) After multi-phase symmetrical alternating current is transformed to asymmetrical alternating current, the ripple size of input current will increase, and the quality of output waveform will decline.

2) In the meantime, the size of converter output ripple grows, which tends to cause overheating of capacitor used for filtering at the output end and shorten its service life.

To prevent these problems, the control signal must be reconfigured based on the improvement of control strategy, so as to improve the ripple characteristics. After fault occurs, the main cause for the increased amplitude of current ripple is asymmetrical current in the other phases, and the ripple frequency has also changed.

Therefore, in what follows, the influence of fault will be reduced to the minimum by changing:

(1) inductor current phase

(2) PWM frequency of various phases.

(3) power adjustment

Adjustment 1 (Phase Adjustment): Because many possible faults may occur, there may be single-phase fault, or fault may occur in two phases simultaneously. Based on the first phase, we will investigate the PWM phase shift in the rest phases after these faults have occurred one by one. With OCF occurred in the k^{th} phase as example, after OCF, it degrades from m–phase to $(m-1)$–phase. At this point, the phase difference of each phase has changed from T_s/m to $T_s/(m-1)$. The PWM of the first phase stays the same, while the PWM of the k^{th} phase can be ignored, and the PWM of the rest non-fault phase has all lag behind for $T_s/m(m-1)$.

According to above principle, take three-phase converter for example, the following phase shift strategies are listed for various faults.

After removing the fault phase, the structure of circuit has changed from three-phase alternating parallel topology to the two-phase structure. According to the analysis above, the size of its current ripple will be smaller than that of unadjusted fault current ripple, but its equivalent frequency is $2f_{sw}$, which has a certain difference from the previous frequency of $3f_{sw}$.

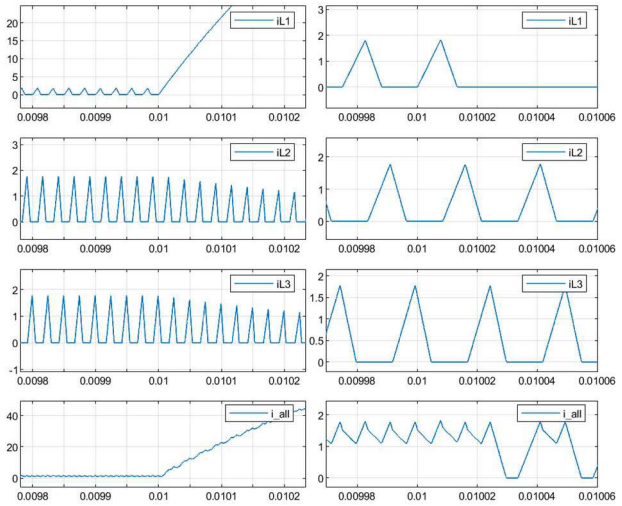

FIGURE 10. Simulink model of three-phase IBC.

In order to further optimize the current ripple after fault has occurred, the switching frequency can be increased under the precondition that the power transistor still has a certain margin.

Adjustment 2 (Switching Frequency Adjustment): For a m–phase converter, the equivalent frequency f_{eq} before fault satisfies $f_{eq} = m \cdot f_s$.

Therefore, after removing a phase with fault, in order to keep the equivalent frequency unchanged, the new switching frequency f_{sw0} should satisfy:

$$f_{sw0} = \frac{m}{m-1} f_{sw} \tag{5}$$

Because it will aggravate the burden on the power transistor by increasing the switching frequency, if there is no strict requirement for the quality of waveform, it is preferred not to adjust the frequency.

Adjustment 3 (Power Adjustment): After the fault has occurred, because the remaining phases need to undertake the previous power, the power transistor with certain margin of power capacity should be selected, or properly reduce the power during operation after the fault to ensure that the power transistors of remaining phases are working within a safe range.

V. SIMULATION RESULTS

For analysis of circuit with multi-phase topology, we will discuss the case of three phases. A converter model was built on the Simulink platform, where, the power source is 12V, the three inductors are $L_1 = L_2 = L_3 = 50\mu$H, the filter capacitance is 100μF, the switching frequency is 40kHz, the duty cycle is 0.45, and the simulation duration is 0.03s.

A. CORRECTION OF SHORT-CIRCUIT FAULT

When the load resistance is 50Ω, the inductor current is discontinuous. As shown in Fig 10, The first phase has SCF at moment t = 0.01s (left diagram), and the first phase has OCF at moment t = 0.01002s (Right diagram).

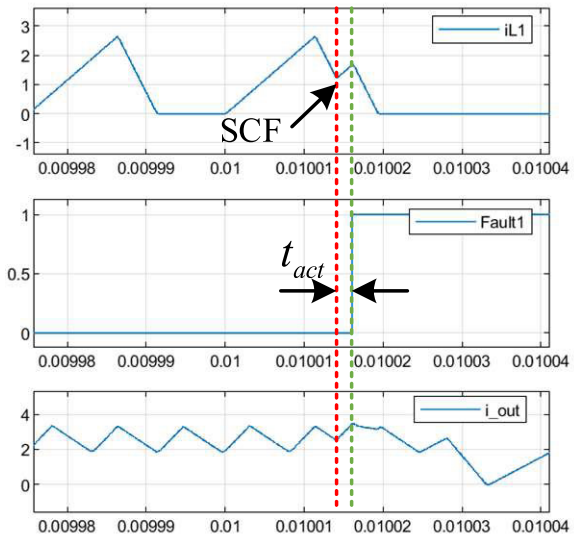

FIGURE 11. (a) Inductor current waveforms after SCF and OCF occurred if no action was taken. (b) inductor current,output current and fault signal of short-current phase.

According to the diagram, after the short-current fault has occurred, if it is not handled in a timely manner, the current will increase sharply, which will cause severe damage to the circuit. For the convenience to check the set threshold actuation time mentioned in this article, assume the short-current fault occurs at moment t = 0.010014s when the current is at declining state, the waveforms of inductor current and fault signal of short-current phase are as shown in Fig 11.

It can be seen that the scheme proposed in this article can be used to effectively detect the fault, which can provide the basis to take correct measures to handle the situation.

B. SIMULATION OF FAULT ADJUSTMENT STRATEGY AND HARMONIC ANALYSIS

When the load resistance is 8Ω, the inductor current is continuous. The first phase has fault at moment t = 0.01s, and by comparing the situation of not taking any measure (Fig 12(a)) with that of conducting PWM phase shift operation (Fig 12(b)), it can be seen that the ripple in the lower diagram is much smaller than that in the upper diagram.

Fig 13 shows the PWM signal after phase adjustment. It can be observed that after the fault has occurred, the third phase has moved forward for $T_s/6$, its difference from the second phase is maintained at $T_s/2$, and the two-phase symmetrical control has been established.

In order to verify whether the harmonic of output current can be reduced after phase shift, spectral analysis of the current waveform before fault, the current waveform after fault without taking any measure and the current waveform after fault after phase shift, and the results are as follows:

In order to facilitate observation, harmonic component details are list in the Table 2.

According to the table, if no measure is taken after the fault has occurred, the harmonic components one time and

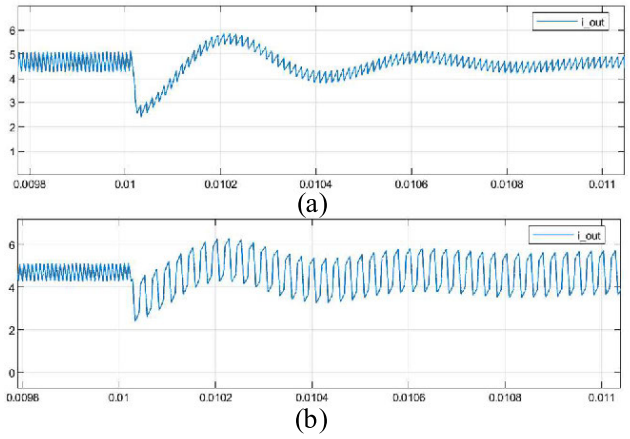

FIGURE 12. The simulation waveform of current after a SCF.

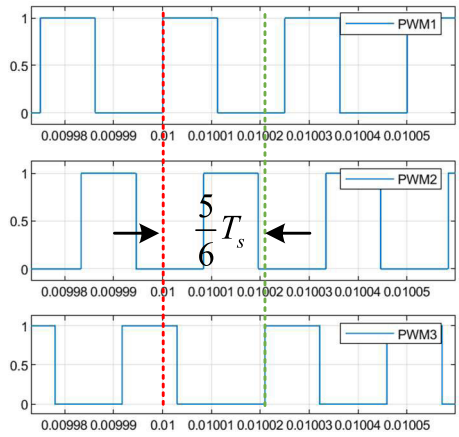

FIGURE 13. The simulation waveform of PWM after a SCF.

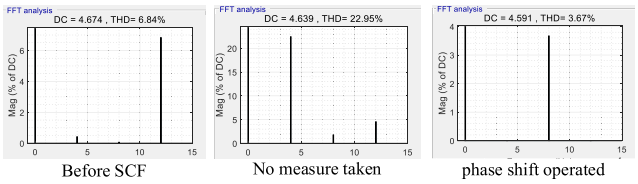

FIGURE 14. Spectral analysis of the current waveform in different situation.

TABLE 2. Harmonic component.

	Before	No measure taken	Phase Shift
DC(Ampere)	4.674	4.639	4.591
THD	6.84%	22.95%	3.67%
Mag (f_{sw})	0.5%	22.4%	0
Mag ($2f_{sw}$)	0	2%	3.6%
Mag ($3f_{sw}$)	5.8%	4.9%	0

two times of the switching frequency have both increased, and the harmonic component of switching frequency shows sharp growth, which has severely affected the waveform quality. However, by adopting the phase shift adjustment strategy, only the harmonic component two times the switching frequency has increased. Therefore, the simulation

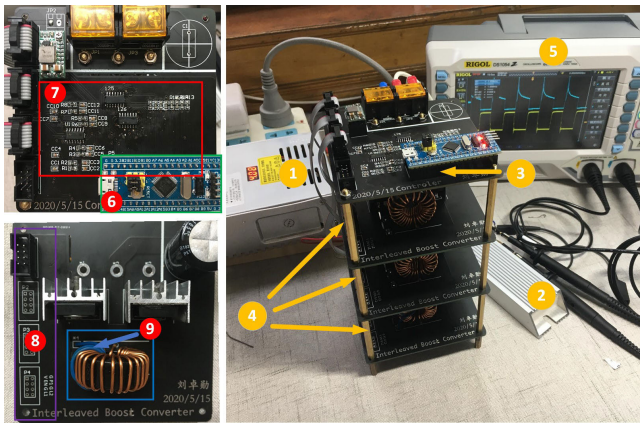

FIGURE 15. 1. Adjustable DC power supply 2. Load 3. controller board 4. power conversion circuit of each phase 5. Oscilloscope. Details on PCB:6. Microcontroller Unit (STM32F103C8T6) 7. Isolation circuit and logic gates 8. MOSFET Gate driver and signal isolation 9. A winding is applied on the toroidal inductor.

TABLE 3. System properties.

Symbol	Parameters	Value
U_{in}	Input voltage	9/16V
L	Inductance of each phase	50μH
C	Filter capacitor	220μF
R_L	Load	10/5Ω
D	Duty Ratio	0.45
f_{sw}	Switching frequent	40kHz
T_w	Turns of winding	2 turns
$Fault_{act}$	Fault act time	1.5μs

results prove the effectiveness of the phase shift adjustment strategy.

VI. EXPERIMENTAL RESULTS

In order to validate the feasibility of the proposed control method, a Three-Phase Interleaved Boost Converter is set up as an example of m-phase IBC, as shown in Fig. 15.

In order to realize multi-phase adjustment, a separated power conversion circuit is designed. In engineering applications, the modular structure easy to dismantle can realize fast replacement of circuit part of fault during repair, so as to reduce the maintenance time to the minimum. The top main control panel is used to measure inductor voltage, isolate the amplifying signal and generate PWM to drive MOSFET.

In order to simulate removal of SCF, the driver chip with enable function is used. When there is external SCF, the enable signal EN is removed, and the circuit is cut off. In the meantime, the controlled SCF function is designed. The SCF signal SCF_{EN} can be controlled by Microcontroller Unit (MCU). If the SCF signal is of low level, the driver chip outputs constant high level, and the power transistor is continuously connected. the converter parameters are listed in Table 2.

Experiments are tested in the following cases: Case A verifies the basic performance of a single phase of the converter; Case B Compares the influence of phase adjustment on harmonic.

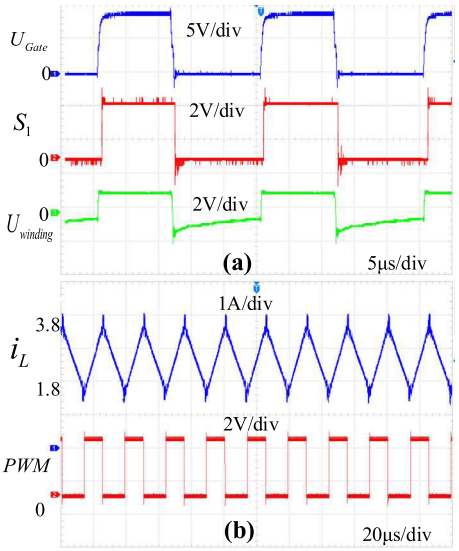

FIGURE 16. (a) The waveforms of gate voltage U_{Gate}, state of inductor voltage S_1, adding winding voltage $U_{winding}$. (b) The waveforms of inductor current i_L and PWM.

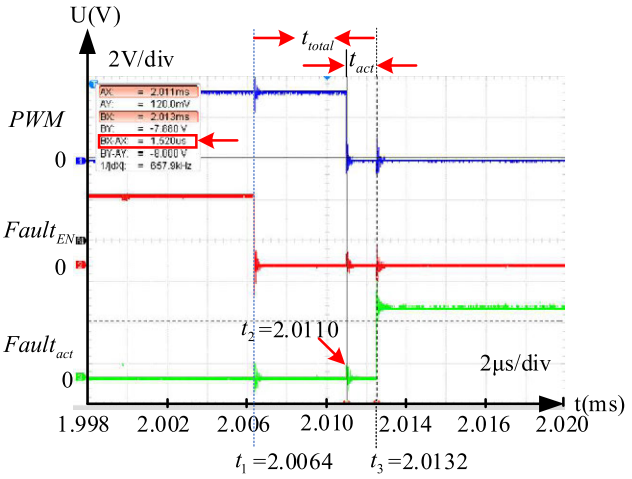

FIGURE 17. The waveforms of SCF enable signal SCF_{EN}, fault actuating signal $Fault_{act}$ and PWM after a testing SCF happened.

Case A: Basic Performance of A Single Phase of Converter

In order to prevent excessive current for a single phase, Adjust the input voltage to 9V and load to 10Ω to test the system. Measure signals of the first phase circuit. The waveforms are shown in Fig 16.

According to the waveforms, under CCM, although the inductor voltage does not present an ideal straight line during the decline of current, this error almost has no influence on the inductor voltage signal. Even though there is a small phase difference between grid voltage and, however, this influence can be ignored after output filtering. Then turn to observe the signals after a testing SCF happened. The waveforms are shown in Fig 17.

When the enable signal of SCF has become low level, the gate voltage of MOSFET is directly increased, and the power transistor is continuously connected without being controlled. When the PWM signal has become low level,

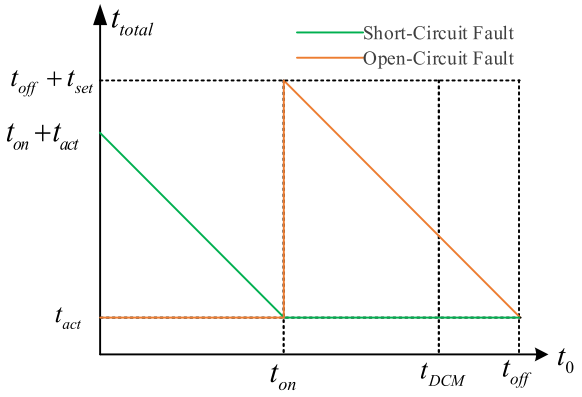

FIGURE 18. The functional relationship between the fault time t0 and the total action time t_{total}.

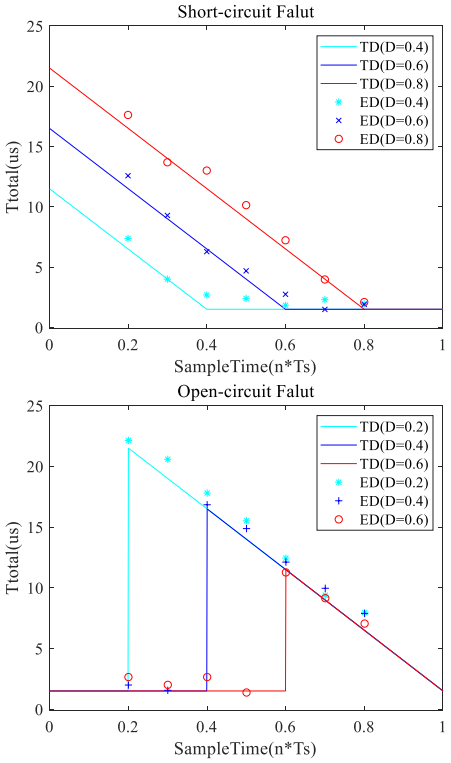

FIGURE 19. The relationship between TD and ED. TD for theoretical data and ED for experiment data.

the fault is detected, and S_1 immediately becomes low level. The elapsed timer continuously detects the level of fault signal during t_{act}, and finally outputs the fault actuating signal $Fault_{EN}$ to the microcontroller to make preparation for subsequent protection. The experimental results show that the time from the occurrence of fault when the fault actuating signal is output is within one period.

A. VERIFICATION OF ON-LINE

When t = 2.0064ms, the short-circuit fault enable signal become low level, the gate voltage of the MOSFET is pulled up directly, and the power transistor is turned on continuously without control. When t = 2.0110ms, the PWM signal becomes low, and when the fault is detected, S1 immediately becomes low level. The Fault signal level is continuously detected in the tact through Timer. When t = 2.0132ms, fault actuating signal $Fault_{act}$ output high level, to prepare for follow-up protection. From the whole process, the whole system can monitor the fault on-line.

B. VERIFICATION OF FAST

Because the faults of short circuit and open circuit are actively controlled by microcontroller, it is easy to accurately control the time of the time when the fault occurs, and the total time t_{total} from the occurrence of the fault to the response of fault can be accurately measured by detecting the time difference between the falling edge of $Fault_{EN}$ and the rising edge of $Fault_{act}$. As shown in figure 17, tact = 1.52μs is similar to the set actuating time of 1.5μs. T_{total} = 6.8μs, less than a switching period which cost 25μs.

The above fault analysis is carried out under the condition of specific duty cycle and specific fault point, but the fault may occur at any time. In order to verify that the scheme can be detected in one switching period at any duty cycle and any fault time, the switching period Ts of fault occurrence is taken for follow-up analysis. So that the starting time of the cycle is 0, the duration of the high level is ton, the duration of the low level is t_{off}, and the point of fault can occur anywhere in the t_0 = 0∼Ts. The functional relationship between the fault time t_0 and the total action time t_{total} is as follows:

From the curve, it can be seen that the factors affecting t_{total} are the duration of high level t_{on} (duty cycle D) and fault time t0, which has nothing to do with whether the current is continuous or not. When testing the short-circuit fault, the duty cycle D = 0.2, 0.4 and 0.6, respectively, and under each certain duty cycle, the short-circuit fault and open circuit fault at $t_0 = nT_s$ (n = 0.2, 0.3, . . . , 0.8) are tested respectively, and t_{total} required from fault occurrence to detection is recorded. The experimental data and the theoretical analysis curve are drawn in one diagram. When testing the open-circuit fault, the duty cycle is 0.4, 0.6 and 0.8, and the rest is the same as the short-circuit fault test.

From the experimental data, under the occurrence of short-circuit and open-circuit faults, the experimental data have a high degree of fit with the curves obtained by theoretical analysis under different duty cycle and t_0, which verifies the correctness of the theoretical analysis. That is, under any duty cycle, the scheme can quickly judge short-circuit and open-circuit faults in one switching period.

Case B: Compare the influence of phase adjustment on harmonic.

Adjust the input voltage to 16V, and check whether the waveform adjustment strategy is effective after the fault. After the circuit has reached steady-state condition, it is still MCU which sends the short-circuit fault to enable signal to make the MOSFET connected. Fig 20(a) shows the current waveform without making any adjustment after removing fault; Fig 20(b) shows the current waveform after PWM

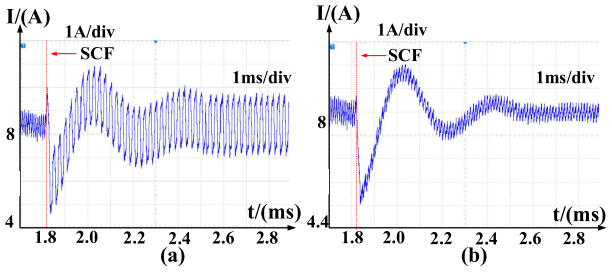

FIGURE 20. **Current waveform without making any adjustment AND shift phase operated after a SCF.**

adjustment for the rest phases, and its waveform is similar to the simulation result in Figure 12.

Fig 20. also proves that after the SCF has occurred, MCU can respond to the $Fault_{act}$ sent from the detection circuit and remove the fault in a timely manner. The difference is that the waveform quality is significantly improved after adjustment, which also proves the conclusion of simulation.

VII. CONCLUSION

After theoretical analysis, simulation and experiment, the following conclusions are obtained:

No matter under CCM or DCM, the inductor voltage can be accurately tested by adding winding to the toroidal inductor, and PWM can be combined to detect the circuit fault within one switching period. But diagnosis error may occur in practice, and malfunction can be prevented through continuous detection during proper actuation time. After the SCF occurred, MCU can respond to the fault actuating signal sent from the detection circuit and realize timely removal of SCF. By adjusting the PWM phase strategy, the size of input and output current ripples can be effectively reduced, and the quality of output waveform can be ensured.

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