A High-Speed Well Logging Telemetry System Based on Low-Power FPGA

HONGWEI ZHAO[iD], **(Graduate Student Member, IEEE), KEZHU SONG, (Member, IEEE), KEHAN LI, CHUAN WU, AND ZHUO CHEN**
State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei 230026, China

Corresponding author: Kezhu Song (skz@ustc.edu.cn)

ABSTRACT This paper presents a field-programmable gate array (FPGA)-based design, implementation, and measurement of a high-speed telemetry system for well-logging. In the application of geophysics, telemetry is an essential part. With the continuous development of new logging theory and new methods, the telemetry system must accurately upload more and more information in real-time. The methods and techniques used to improve the data transmission system's performance have become a significant problem in developing a well-logging instrument. The proposed design realized the application of orthogonal frequency division multiplexing (OFDM) in the high-speed cable telemetry system. Besides, We have optimized the calculation of some modules such as symbol synchronization, frequency domain equalization, data compression, and sampling clock offset compensation while not losing performance as much as possible so that the modulation and demodulation algorithm can be implemented on a low-power FPGA. With this system, the modulated data transmitted over a 7,000-meter armored cable can be demodulated in real-time. Compared to conventional devices using digital signal processors, this FPGA-based telemetry system shows advantages in power consumption and real-time performance. Test results show that the FPGA power consumption is 169.7mW, and the high-speed cable telemetry system can transmit data stably at 1.4 to 2.3Mbps through a 7,000-meter armored logging cable.

INDEX TERMS Telemetry, well logging, armored cable, OFDM, FPGA.

I. INTRODUCTION

Data telemetry is one of the most critical technologies in geophysical applications such as mining, oil, and gas production [1]. In some applications, such as oil well logging, telemetry systems must transmit data through harsh environments. In logging operations, it is often necessary to place high-precision electronic instruments in the borehole at a depth of more than 5,500 meters. The temperature exceeds 175 degrees Celsius, and the pressure is more significant than 140MPa [2], [3]. In this case, the downhole instrument must have a simple structure and low power consumption. Although optical fibers have better communication performance, armored cables (single-core or multi-core cables) are usually used as transmission channels between the ground and downhole instruments because they are corrosion-resistant, wear-resistant, and can withstand greater

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tension. Generally, the length of these logging cables is more than 5,000 m, and even more than 10,000 m in some cases [4]. Unfortunately, long-distance cables cannot transmit electrical signals as completely as short-distance cables. Each cable forms a non-linear transmission channel, which severely attenuates the high-frequency part of the signal and causes signal distortion, attenuation [5], and narrowing of the available bandwidth of the cable channel. Fig. 1 shows the frequency domain characteristics of the 7,000m Rochester 7-H-464D logging cable [6]. The HP3598A network analyzer measures it. The low working environment and poor transmission channel make it challenging to restore the signal and increase the data transmission rate.

The development of communication technology has facilitated the advancement of long-distance logging cable transmission technology. Several methods have been studied in the past to alleviate the problem of long-distance cable transmission. One method is to use pulse code modulation (PCM) [7]. The primary process is to sample the analog signal at regular
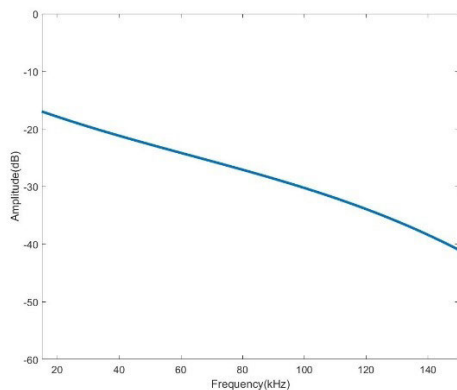
FIGURE 1. Amplitude frequency response of rochester 7-H-464D.

intervals to discretize it while round the sampled value to the nearest integer, and then use the binary code to represent it. PCM requires a very accurate clock. The number of samples per second is between 8,000 and 192,000, which is usually several times the maximum frequency (in Hertz (Hz)) of the analog waveform or the number of cycles per second (between 8 and 192 kHz). ATLAS's early telemetry system WTS3502 used PCM, and its data rate can only reach 7.5kbps [8].

The Manchester II coding technique is another method [9]. Manchester II encoding technology makes full use of cable bandwidth and increases the data transmission rate. Especially for long-distance data transmission, Manchester II has the advantages of bandwidth, error detection, synchronization, clock recovery, and anti-interference compared with non-return-to-zero (NRZ) codes [10]. To improve transmission efficiency, usually, the transmitted Manchester II data is first converted into an alternate mark inversion (AMI) code [11]. The encoder generates a positive AMI pulse on the Manchester II code's rising edge and a negative pulse on the falling edge of the Manchester II code. After that, the AMI pulse is shaped by a low-pass filter and sent to the transmission logging cable. The receiver extracts AMI pulses from the received signal, regenerates Manchester II codes based on these AMI pulses, and then sends them to the designated decoder chip or digital signal processor to complete the decoding [12].

Another method is to use the Asymmetric Digital Subscriber Line (ADSL) technology. ADSL is one of the digital subscriber line (DSL) technologies. It is a data communication technology that can achieve faster data transmission through copper telephone lines than traditional voice band modems. The primary modulation scheme of ADSL is Discrete Multitone Modulation (DMT) [13]. This method is a multi-carrier modulation technology that uses a discrete Fourier transform method to divide the available bandwidth into 256 sub-channels. Before starting data transmission, DMT measures each channel's signal-to-noise ratio separately and allocates the transmission bits of each sub-channel accordingly [14]. Generally, compared to high-frequency

subchannels, more bits are allocated on low-frequency subchannels because the signal is attenuated more at high frequencies. This process enables the system to realize adaptive transmission on transmission channels with different characteristics. The latest telemetry system HALLIBURTON's IQLOG, is based on ADSL technology, can transmit data at 800kbps on a 7000m logging cable [8].

Recently, a telemetry system based on Orthogonal Frequency Division Multiplexing (OFDM) has been proposed, and it has been verified in simulations and experiments [15]–[17]. OFDM is a multi-carrier modulation. It divides the channel into several orthogonal sub-channels, converts high-speed data signals into parallel low-speed subdata streams, and modulates them for transmission on each sub-channel. Each carrier in OFDM is orthogonal to each other. Each carrier has an integer number of carrier periods within one symbol time. The spectrum zero of each carrier overlaps with adjacent carriers' zeros, which reduces the interference between carriers. The partial overlap between the carriers improves the frequency band utilization compared with the traditional multi-carrier modulation method.

The characteristics of OFDM make it very suitable as a modulation method for logging and telemetry systems. This paper proposes a high-speed logging telemetry system based on OFDM and Field Programmable Gate Array (FPGA). The system can effectively and accurately transmit data through 7000m armored cables. Compared with traditional telemetry systems using digital signal processors, the FPGA-based system has the advantages of simplicity, low power consumption, and real-time performance. In addition to oil logging applications, the system can also be used on other applications such as environmental and nuclear logging that require high-speed data transmission through long-distance cables.

The rest of this paper is structured as follows. In the next section, we introduce the structure and the working process of the well logging telemetry system. Next, we illustrate the detailed FPGA implementation in the system, which are introduced in the section III. In the section IV, the experiments and measurements are discussed. Finally, some conclusions that can be drawn from our work are presented in the section V.

II. SYSTEM STRUCTURE AND WORKING PROCESS

This section introduces the telemetry system's structure and working procedures for data transmission between the ground and downhole instruments through seven-core armored cables. Fig. 2 is a cross-sectional view of the seven-core armored cable. The seven-core armored cable comprises seven cores, with the No. 7 core in the center and the No. 1 to No. 6 cores distributed on the periphery. The outermost layer of the logging cable is a steel wire braided armor to help the cable withstand the great tension caused by the gravity of itself and the downhole instruments and prevent the corrosive substances in the well from damaging the cable. The seven cable cores are not only used to transmit data but also need to power downhole tools. By appropriately
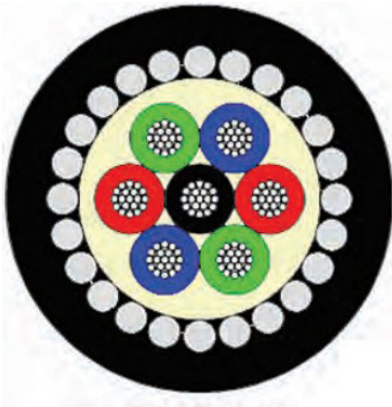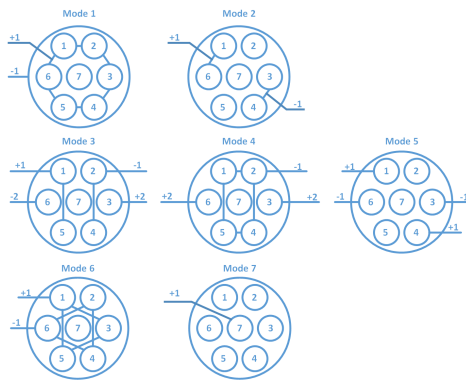
FIGURE 2. 7-core armored cable.

FIGURE 3. Seven transmission mode of 7-core armored cable.

combining the seven cores for transmission, the influence of crosstalk between each core during signal transmission and the interference between the power supply circuit and the signal transmission circuit can be reduced. Fig. 3 shows the seven transmission modes of the seven-core armored cable. We can choose the corresponding data transmission method according to different usage scenarios [18].

A. STRUCTURE OF THE TELEMETRY SYSTEM
The structure of the well-logging telemetry system is shown in Fig. 4. It includes a ground telemetry device, well-logging cables, and a downhole telemetry device. The ground telemetry device communicates with the computer through an Ethernet interface. On the other hand, the downhole telemetry device communicates with downhole tools through the downhole instrument bus (such as CAN Bus or Ethernet). Since the function of the ground telemetry device and the downhole telemetry device's function are only different in the transmission direction and transmission rate, their structures are similar, as shown in Fig. 5. It mainly includes three parts: Ethernet interface, FPGA for digital signal processing, and analog circuit.

B. WORKING PROCESS
The working process of the telemetry system includes the channel estimation stage and the data transmission stage.
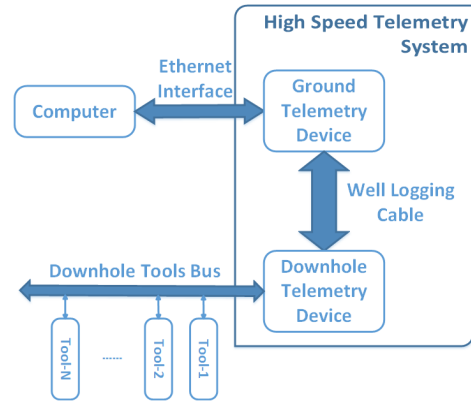

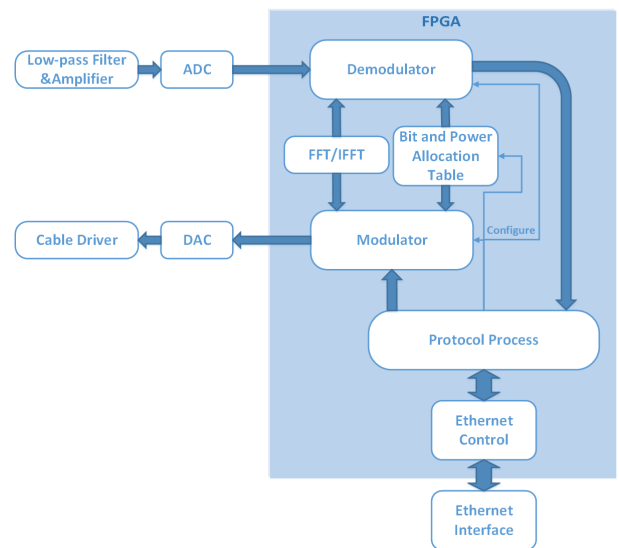**FIGURE 4.** Well logging telemetry system.

FIGURE 5. FPGA-based telemetry device.

Fig. 6 shows the process of the channel estimation stage. After turning on the ground and downhole devices' power, they will enter the channel estimation stage and use a specific single-frequency sinusoidal signal to start a handshake. After the two-way response, automatic gain training is started to ensure that the transmitted and received signals' amplitude is appropriate.

Then the system starts channel estimation, as shown in Fig. 7. The ground telemetry device first sends digital BPSK training sequences [19] and the downhole telemetry device trains the time domain equalizer according to the received training sequences. Next, the downhole telemetry device uses the 4QAM modulation of the specific sub-channel to send the tap coefficient of equalizer and data of equalized training sequences.The ground telemetry device analyzes each sub-channel's signal-to-noise ratio and allocates the appropriate power and number of bits to each sub-channel to optmize the transmission rate and bit error rate. After that, the ground telemetry device regenerates the training sequence according to the power allocation table and uses it as the long training
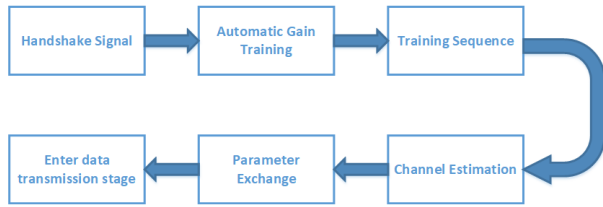
FIGURE 6. Working process.

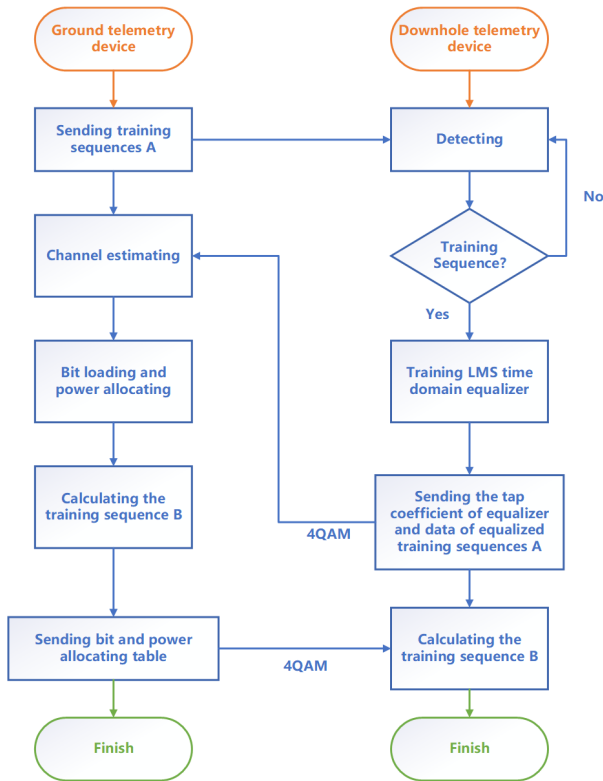**FIGURE 8.** Structure of transmit data.

FIGURE 7. Process of channel estimation.

sequence in the data transmission stage. Finally, the ground telemetry device sends the bit and power allocation table to the downhole device to complete the channel training stage.

Due to the harsh environment, the signal SNR received by the downhole telemetry device is lower than that received by the ground telemetry board, so it is used as a reference for bit allocation. In the whole process of channel estimation, the downhole telemetry device only undertakes the training task of the time-domain equalizer, while other more complex computing tasks are completed by the ground telemetry, which also helps to reduce the use of logic resources of FPGA on downhole telemetry device and reduce the heat dissipation pressure.

After finishing the channel estimation stage, the system enters the data transmission stage. At this stage, data is sent in bursts, and Fig. 8 shows the data frame structure. The preamble consists of ten repeated short training symbols (each sequence is 1/4 of the data symbol length) and two repeated long training symbols (each sequence has the same length
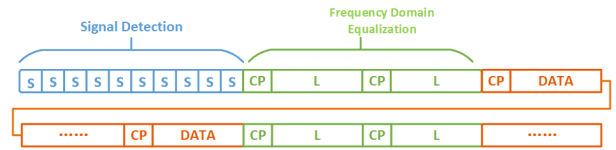
as the data symbol). At the receiver, short training symbols and long training symbols are used for symbol synchronization and channel estimation, respectively. When sending data continuously, the transmitter will periodically insert a long training sequence to track changes in the seven-core armored cable channel due to temperature and stretching factors.

When data needs to be downloaded, the computer's control software sends the data to the FPGA through the Ethernet interface. The data is compressed and modulated in the FPGA and then sent to the analog circuit. After the digital-analog conversion and amplification drive, it is sent to the logging cable and transmitted to the downhole telemetry device. The driver module should provide sufficient power and amplitude to drive the 7000m armored cable.

When the downstream signal reaches the downhole device through the logging cable, the long-distance cable channel will attenuate its high-frequency part by more than 30 dB. The received signal in the downhole device is first processed by the circuit of signal amplification and noise filtering to amplify the signal and suppress noise. The received signal is then converted into a digital signal through an analog-to-digital converter and sent to the FPGA. FPGA logic will demodulate it and recover the transmitted data.

We use FPGA chips to perform all data processing rather than using specific encoding or decoding chips or DSP chips. FPGA is a programmable chip, so we can modify or update the hardware algorithm in it for different specific application requirements, which makes the solution have better real-time performance, versatility, and flexibility. Therefore, FGPA is the critical chip in this architecture, and the algorithm in this FPGA is crucial to the entire telemetry system.

III. FPGA IMPLEMENTATION

As shown in Fig. 5, FPGA logic includes a modulator module and a demodulator module. The block diagram of the modulator is shown in Fig. 9. First, the data compression module compresses seismic wave data, while other kinds of data are not compressed. The scrambler then scrambles the data, and the Reed-Solomon (RS) encoder uses the RS [20] code to help the demodulator find and correct the error bits caused by noise or crosstalk. After that, the QAM constellation diagram module performs n-QAM (quadrature amplitude modulation) [21] constellation modulation on each sub-carrier according to the bit allocation table obtained in the channel training stage. Then, use inverse fast Fourier transform (IFFT) to achieve OFDM modulation. Finally, the modulator inserts a cyclic prefix (CP) in front of the frame to prevent the impacts
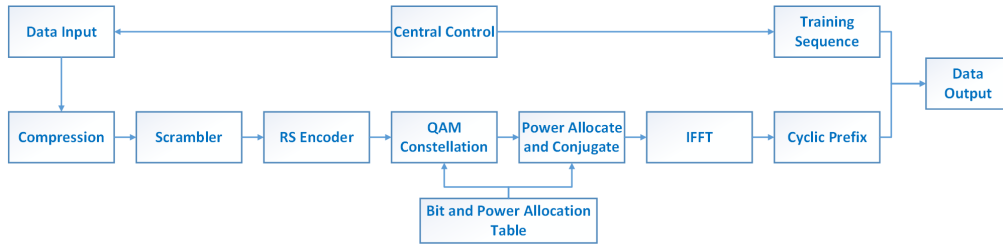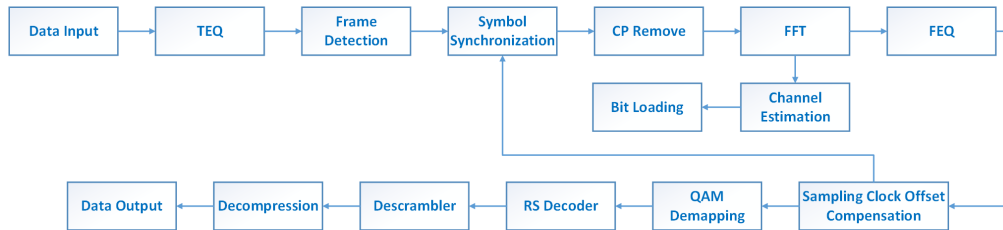
FIGURE 9. Block diagram of modulator.

FIGURE 10. Block diagram of demodulator.

of inter-symbol interference (ISI) and symbol synchronization errors.

Fig. 10 shows the block diagram of the demodulator. After converting the received signal into digital data and sending it to the FPGA, the frame detection and synchronization module determines whether a new data packet arrives by calculating the correlation between the received data and the short training sequence and finds the data packet's starting position. Then, a time-domain equalizer (TEQ) compensates for high-frequency signals to reduce inter-symbol interference. Next, the Fast Fourier Transform (FFT) is used to achieve OFDM demodulation. The frequency-domain equalizer (FEQ) will compensate for the amplitude and phase distortion of the received signal caused by the logging cable. Finally, the equalized data is sequentially sent to the QAM demapping module, RS decoder, descrambler, and data decompression module, and finally, the original data is restored.

A. DATA COMPRESSION MODULE

Seismic exploration is a widely used method in well logging [22]. The source frequency that excites artificial seismic waves is about tens of hertz, and the sampling period of the sensor is usually several kilohertz. That is, the sampling frequency is much greater than the frequency of seismic waves. Therefore, between the adjacent sampling points, the value collected by a particular sensor will not have much difference, which makes the data have much redundancy and is suitable for compression.

The data compression process is shown in Fig. 11. First, due to the correlation between adjacent seismic wave signals, one or more previous signals can be used to predict the next signal, and then the difference (prediction error) between the actual value and the predicted value can be coded, that is, linear prediction coding. The predicted value can be expressed

FIGURE 11. Procedure of compression.

as:

$$x_{predict} = a_1 x(n-1) \cdots + a_p x(n-p)$$
$$= \sum_{i=1}^{p} a_i x(n-i) \tag{1}$$

Because the implementation of linear predictive coding is complicated, especially calculating prediction coefficients is very difficult to implement on hardware. Therefore, we adopt the linear predictive coding with prediction order p = 1 and prediction coefficient a1 = 1, called differential coding. For input data:

$$x_1, x_2, x_3 \cdots x_n \tag{2}$$

The encoded data is

$$x_1, x_2 - x_1, x_3 - x_2 \cdots x_n - x_{n-1} \tag{3}$$

The process of entropy coding is shown in Fig. 12. Entropy coding, also known as statistical coding, is a lossless data compression coding based on the probability of data appearance's distribution characteristics. Due to seismic wave data characteristics, numerical values with smaller absolute values have a greater probability of appearing after differential encoding. Therefore, we can use entropy coding to compress differential coded data as follows:

1) If the differential coded data's value x is in the interval of $[-64, 63]$, the data can be encoded with one byte
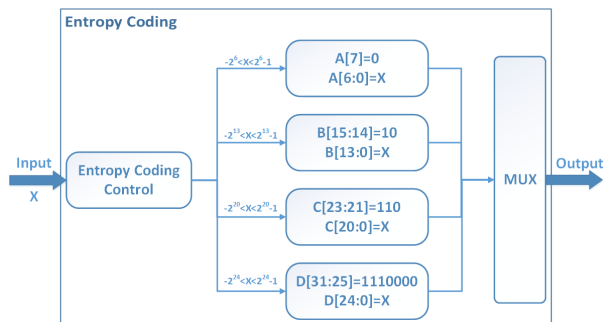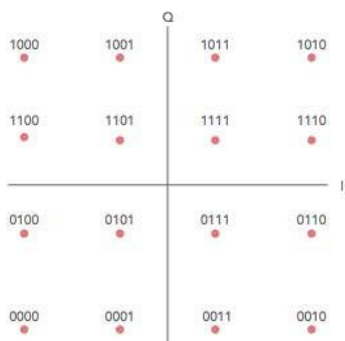
FIGURE 12. Block diagram of entropy coding.

FIGURE 13. QAM16 constellation.

FIGURE 14. QAM constellation module.

serial bitstream into the 8-bit shift register in turn and reads the bits allocated to the current subcarrier from the bit allocation table. When the number of bits in the shift register is the same as the data output by the RAM storing the bit allocation table, the data in the shift register and the output of the bit allocation table are sent to the QAM mapping sub-module.

The QAM mapping sub-module regards the bit allocation table's output value as the valid number of bits in the shift register's output data and maps the data with the corresponding nQAM constellation diagram.

C. POWER ALLOCATE AND CONJUGATE MODULE

After the QAM constellation module allocates the number of bits of each sub-channel, the Power allocate and conjugate module allocates the power of each sub-channel according to the power allocation table, and performs conjugate symmetric processing on the sequence. The architecture is shown in Fig. 15, We assume length of each sequence is N and the input data $x(n) = a(n) + ib(n)$, If the IFFT is performed on the $x(n)$ sequence, the transformed $X(n)$ can be expressed as

$$X(n) = \frac{1}{N} \sum_{k=0}^{N-1} x(k) e^{i\frac{2\pi nk}{N}} \tag{4}$$

If $x(n)$ is an ordinary complex sequence, then $X(n)$ will also be a complex sequence and cannot be transmitted on baseband. So, we have to extend the sequence $x(n)$ to make it conjugate symmetry. The extended $x'(n)$ and corresponding $X'(n)$ can be expressed as

$$x'(n) = \begin{cases} a(n) + ib(n), & n < N \\ a(0), & n = N \\ a(2N - n) - ib(2N - n), & 2N > n > N \end{cases} \tag{5}$$

$$X'(n) = \frac{1}{2N}\left(\sum_{k=0}^{N-1} (x(k)e^{i\frac{2\pi nk}{2N}} + (x(k)e^{i\frac{2\pi nk}{2N}})^*) \right) \tag{6}$$

Obviously $X'(n)$ is a real sequence and can be transmitted on baseband.

D. FRAME DETECTION AND SYNCHRONIZATION MODULE

Synchronization is one of the most fundamental tasks for any communication system. For OFDM-based communication systems, it is difficult to accurately demodulate the transmitted signal without accurate synchronization. We use ten short

$A[7 : 0]$. $A[6]$ is the sign bit of the differential data, $A[7] = 0$, $A[6 : 0] = x$;

2) Else if the differential coded data's value x is in the interval of $[-8192, 8191]$, the data can be encoded with two bytes $B[15 : 0]$. $B[13]$ is the sign bit of the differential data, $B[15 : 14] = 10$, $B[13 : 0] = x$;

3) Else if the differential coded data's value x is in the interval of $[-1048576, 1048575]$, the data can be encoded with three bytes $C[23 : 0]$. $C[20]$ is the sign bit of the differential data, $C[23 : 21] = 110$, $C[20 : 0] = x$;

4) Else if the differential coded data's value x is in the interval of $[-1677216, 16777215]$, the data can be encoded with four bytes $D[31 : 0]$. $D[24]$ is the sign bit of the differential data, $D[31 : 25] = 1110000$, $D[24 : 0] = x$;

The above method is suitable to be implemented by hardware algorithms and can compress the seimic wave data in the data stream in real-time.

B. QAM CONSTELLATION MODULE

The QAM constellation module selects the corresponding n-QAM constellation diagram to map the input data according to the bit allocation table. Fig. 13 shows the 16QAM constellation diagram, and Fig. 14 shows the QAM constellation module's architecture.

The data first enters the bit allocation sub-module to allocate bits on each sub-carrier. This sub-module puts the input
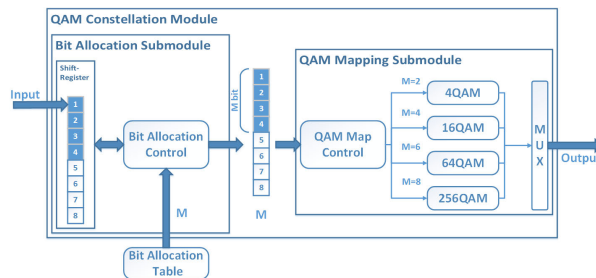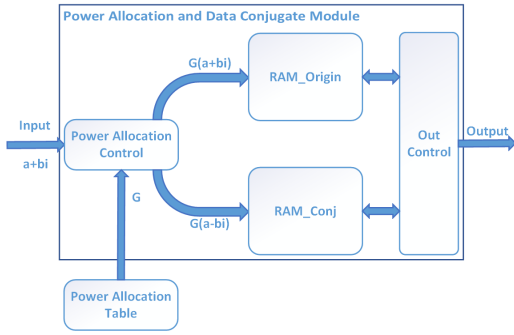
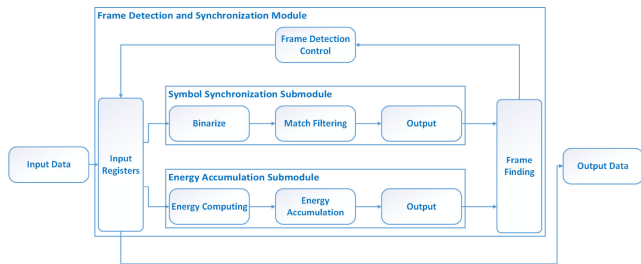**FIGURE 15.** Power allocate and conjugate module.

FIGURE 16. Frame detection and synchronization module.

training sequences in the preamble to achieve synchronization. Fig. 16 shows the architecture of frame detection and synchronization module.

The input data to be detected is buffered and enters the energy accumulation sub-module and the symbol synchronization sub-module. In the energy accumulation submodule, accumulate the energy within the symbol length window of the short training sequence. In the symbol synchronization sub-module, first binarize the input data to reduce the logic resource occupation, and then the binarized data and the expected short training sequence data are cross-correlated. After that, the results of these two sub-modules are sent to the frame finding module. When the output of the energy accumulation submodule is larger than the threshold and maintained, and the symbol synchronization module outputs the tenth peak with a short training sequence length as a cycle, it indicates that valid data has arrived and output the data in the registers.

E. TEQ MODULE

For long cable channels, the signal will be distorted due to its low-pass characteristics. This phenomenon causes that when the communication system continuously transmits symbols, the previous symbol will interfere with the subsequent symbols and making the communication less reliable, that is, inter-symbol interference (ISI).

Based on the periodicity of FFT, inter-symbol interference can be eliminated by adding a cyclic prefix. But for channels with a longer impulse response, a longer cyclic prefix is required, which means greater redundancy and will reduce the transmission rate.
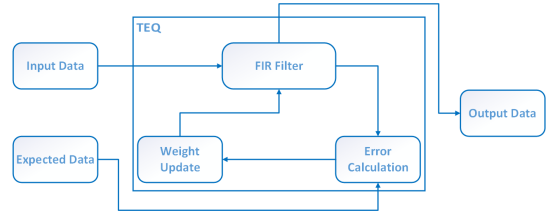

FIGURE 17. TEQ module.

In order to eliminate the inter-symbol interference under the condition of adding a shorter cyclic prefix, channel equalization can be used to shorten the impulse response length of the channel. Channel equalization can be performed in the time domain and the frequency domain, but the frequency domain equalization can only be performed after the Fourier transform of the signal. At this time, Inter-symbol interference has been aliased in the spectrum and cannot be eliminated, so we use time domain equalization before FFT to shorten the channel response.

In addition, due to the high-frequency attenuation of long cable channels, the energy difference between the low-frequency part and the high-frequency part is often greater than 30dB, which results in greater quantization noise in the high-frequency part after Fourier transform. Time-domain equalization can reduce the quantization noise of the high-frequency part signal by increasing the amplitude of the high-frequency part signal, thereby improving the SNR. The architecture of time-domain equalizer (TEQ) module is shown in Fig. 17.

In order to be able to adapt to channels of different lengths of cable, LMS algorithm with variable step size is used to train the time domain equalizer in channel training stage, Assuming that the FIR filter has M taps, tap coefficient matrix is w_n, the step factor is μ, the input signal is $x(n)$, and the expected signal is $d(n)$, then the error can be expressed as:

$$w_n = [w_n(0), w_n(1), \cdots, w_n(M)]^T \qquad (7)$$
$$x_n = [x(n), x(n-1), \cdots, x(n-M)]^T \qquad (8)$$
$$e(n) = d(n) - w_n^T x(n) \qquad (9)$$

And the tap coefficient matrix is updated to:

$$w_{n+1} = w_n + 2\mu e(n)x(n) \qquad (10)$$

After entering the transmission stage, use the tap coefficient matrix obtained in the channel training stage to equalize the received sequence.

F. FEQ MODULE

Frequency domain equalizer (FEQ) is used to compensate for signal distortion in amplitude and phase after passing through logging cable. Since the logging cable moves slowly in logging applications, we can treat this channel as a slow fading channel. Therefore, the module can use two repeated long training symbols to estimate the frequency domain response.
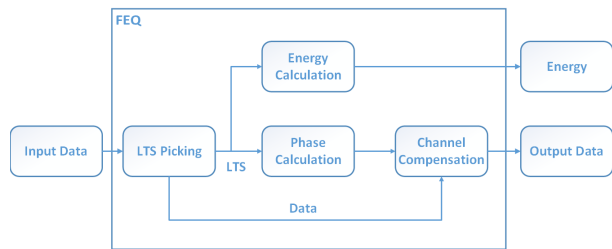
FIGURE 18. FEQ module.

We assume that R_{1LTS} and R_{2LTS} are the two received long training symbols, the average value R_{LTS} of the two received long training symbols can be expressed as:

$$R_{LTS} = \frac{R_{1LTS} + R_{2LTS}}{2} \tag{11}$$

The equalized data can be obtained by solving the following expressions:

$$H = \frac{R_{LTS}}{L_{LTS}} \tag{12}$$

$$R' = \frac{R}{H}$$
$$= \frac{R \times (R_{LTS}^* \times L_{LTS})}{\|R_{LTS}\|^2} \tag{13}$$

where L_{LTS} is the original long training symbol, H is the estimated value of the channel frequency domain response, R and R' are the data symbol before and after equalizing.

In order to make the algorithm suitable for hardware implementation and save logic resources, we set the data value in the original long training symbol to 1 or −1, so we can simplify the above expression to:

$$H = R_{LTS} \times L_{LTS}^* \tag{14}$$

$$R' = \frac{R \times H^*}{\|R_{LTS}\|^2} \tag{15}$$

The block diagram of FEQ we designed based on the above analysis is shown in Fig. 18. The LTS picking submodule first picks two long training symbols from the input data and calculates their average value. The average value of the long training symbols was then sent to the energy calculation submodule and the phase calculation submodule. The energy calculation submodule calculates each subcarrier's amplitude distortion and transmits it to the subsequent QAM demapping module. The phase calculation sub-module calculates equation (11) to obtain H and sends H to the phase compensation sub-module to compensate for signal phase distortion.

This module only corrects the distortion of phase, passes $\|R_{LTS}\|^2$ to the subsequent demapping module, and dynamically adjusts the judgment threshold of the constellation diagram, thereby avoiding the division structure. This method reduces the complexity of calculation and reduces the consumption of logic resources in FPGA.

G. SAMPLING CLOCK FREQUENCY OFFSET COMPENSATION MODULE

Since different clock sources are used between the signal transmitting and receiving devices, the sampling period of the transmitting and receiving devices will also be different, which results in the sample clock frequency offset(SFO).

Assuming that each OFDM signal has M sampling points, the symbol part has N_{sym} sampling point, the cyclic prefix part has N_{cp} sampling points, the sampling period of the transmitting device is T_s, and the sampling period of the receiving device is T_s', then the normalized SFO can be expressed as

$$\Delta_{T_s} = \frac{T_s' - T_s}{T_s} \tag{16}$$

When $(mM + N_{cp})T_s < t < (m+1)MT_s$, the mth transmitted OFDM symbol can be expressed as:

$$x_m(t) = \frac{1}{N} \sum_{k=0}^{N_{sym}-1} X_m(k) e^{i\frac{2\pi k(t-(mM+N_{cp})T_s)}{N_{sym}T_s}} \tag{17}$$

When $t = nT_s$, the nth sampling point of the mth transmitted OFDM symbol can be expressed as:

$$x_m(n) = \frac{1}{N} \sum_{k=0}^{N_{sym}-1} X_m(k) e^{i\frac{2\pi k(n-(mM+N_{cp}))}{N_{sym}}} \tag{18}$$

And the nth sampling point of the mth received OFDM symbol can be expressed as:

$$\begin{aligned} y_m(n) &= x((mM + N_{cp} + n)T_s') \\ &\approx x((mM + N_{cp})(1 + \Delta_{T_s})T_s + nT_s) \\ &\approx \frac{1}{N} \sum_{k=0}^{N_{sym}-1} X_m(k) e^{i\frac{2\pi kmM\Delta_{T_s}}{N_{sym}}} e^{i\frac{2\pi kn}{N_{sym}}} \end{aligned} \tag{19}$$

The frequency domain value of the lth subcarrier in the mth OFDM symbol can be calculated as follows:

$$\begin{aligned} Y_m(l) &= \frac{1}{N} \sum_{k=0}^{N_{sym}-1} X_m(k) e^{i\frac{2\pi kmM\Delta_{T_s}}{N_{sym}}} \sum_{n=0}^{N_{sym}-1} e^{i\frac{2\pi n(k-l)}{N_{sym}}} \\ &= \frac{1}{N} \sum_{k=l} X_m(k) e^{i\frac{2\pi kmM\Delta_{T_s}}{N_{sym}}} N \\ &= X_m(l) e^{i\frac{2\pi lmM\Delta_{T_s}}{N_{sym}}} \\ &= X_m(l) e^{iSl} \end{aligned} \tag{20}$$

$$S = \frac{2\pi mM\Delta_{T_s}}{N_{sym}} \tag{21}$$

So the impact of SFO on the frequency domain of the received signal is to rotate the phase of each sub-carrier in proportion to the sub-carrier number l. In order to compensate for the impact, we insert known pilots in OFDM symbols to estimate SFO.

Assuming a total of K pilots are inserted, the sub-carrier number of each pilot is $l_k(k = 1, 2, \cdots K)$, the rotated phase

of each pilot is $\theta_k(k = 1, 2, \cdots K)$, S can be estimated as:

$$S = \frac{\sum_{k=1}^{K} \theta_k}{\sum_{k=1}^{K} l_k} \qquad (22)$$

We can make the sum of the sub-carrier numbers of the pilots is power of 2, and the division in the expression can be implemented with register shift right.

When $S > 2\pi$, it means that the receiving sequence is advanced by one sampling period due to the impact of SFO, and we need to send a signal to the symbol synchronization module to delay the receiving sequence by one period, and vice versa.

Since the phase has been compensated according to the long training sequence in the FEQ module, what this module needs to compensate is the impact caused by SFO since the last long training sequence was received.

However, when the time between receiving two sets of long training symbols is not enough to delay or advance the received sequence by one sampling period, the situation of $S > 2\pi$ will not occur. Using the above method will not feed back the symbol synchronization module to advance or delay the receiving sequence by one cycle, and the FFT window will gradually deviate due to the influence of SFO, making it impossible to demodulate.

So while using the above method, we record the pth sub-carrier phase compensation value ϕ_0 when the FEQ module receives the first long training sequence, and compare it with the pth subcarrier phase compensation value ϕ' when the long training sequence is received later.

When the receiving sequence is advanced or delayed by one sampling point, the relationship between ϕ_0 and ϕ' can be expressed as

$$|\phi' - \phi_0| = \frac{2\pi p}{N_{sym}} \qquad (23)$$

In order to simplify the calculation, we select the $\frac{N_{sym}}{4}$th subcarrier and only record the sign information of the real and imaginary parts. When the received sequence is advanced or delayed by one sampling point, the phase change is $\frac{pi}{4}$. Therefore, the signs of the real part and the imaginary part have one and only one bit flip, and according to whether the sign of the real part or the imaginary part is flipped, the receiving sequence should be delayed or advanced by one sample point.

When the signs (r, i) of the real and imaginary parts meet the following conditions, the receiving sequence needs to be delayed by one sample point:

$$
\begin{aligned}
(+, +) &\rightarrow (-, +) \\
(+, -) &\rightarrow (+, +) \\
(-, -) &\rightarrow (+, -) \\
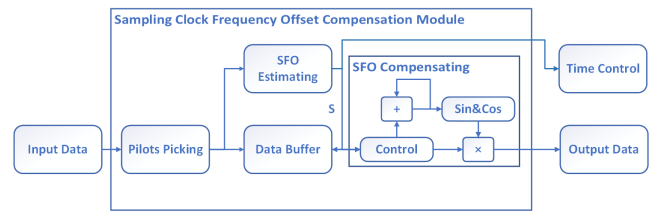(-, +) &\rightarrow (-, -)
\end{aligned} \qquad (24)
$$

FIGURE 19. Sampling clock frequency offset conpensation module.

And when the signs meet the following conditions, the receiving sequence needs to be advanced by one sample point:

$$
\begin{aligned}
(+, +) &\rightarrow (+, -) \\
(+, -) &\rightarrow (-, -) \\
(-, -) &\rightarrow (-, +) \\
(-, +) &\rightarrow (+, +)
\end{aligned} \qquad (25)
$$

The architecture of sampling clock frequency offset compensation module is shown in Fig. 19. When the data arrives, the pilot extraction submodule writes the data into the data buffer, and at the same time extracts the pilots with known subcarrier numbers and sends them to the SFO estimation module. The SFO estimation module will estimate the value of S according to the value of the pilots, determine whether to send a signal to the symbol synchronization module to retime the received sequence, and send S to the SFO compensation submodule. The SFO compensation submodule generates the compensation factor required by each subcarrier according to the value of S, and reads the data in the data buffer submodule to perform the compensation operation according to the generation timing of the compensation factor, and finally outputs the compensated data.

IV. EXPERIMENTS AND MEASUREMENTS

We have designed the prototype telemetry system based on Cyclone 10LP FPGA, and completed a series of measurements over 7000m 7-core armored cable. The 7km logging cable channel has severe attenuation of signals with a frequency greater than 250kHz, resulting in a low signal-to-noise ratio. In the low frequency band, because the two ends of the logging cable are coupled to the ground and underground telemetry device through the transformer, the low frequency signal with a frequency of less than 1kHz is seriously attenuated. Therefore, the cable channel can be regarded as a communication channel with 1-250kHz, and the OFDM parameters are used accordingly: the sampling frequency is 1024kHz, the FFT size is 1024, the third to 250 subchannels are used, and the subchannel interval is 1kHz.

Since Mode 3 and Mode 4 adopt differential transmission with asymmetric levels, it is difficult to implement and is not suitable for practical use, so these two modes are not used. Fig. 20 shows the amplitude-frequency response of the other five transmission modes on a 7km seven-core cable. Modes 1 and 2 have poor amplitude-frequency responses and
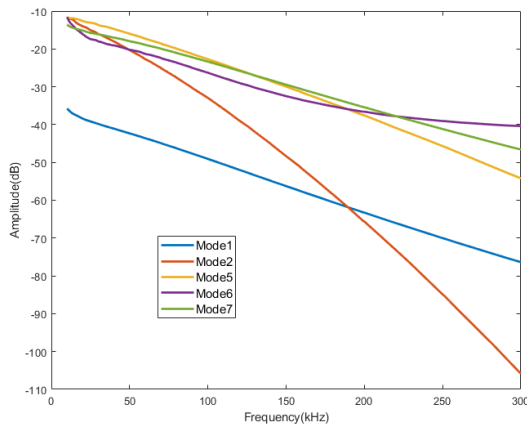
FIGURE 20. Amplitude frequency response of 5 transmission modes.

FIGURE 21. Block diagram of test system.

FIGURE 22. PCB of prototype telemetry device.

FIGURE 23. 7km armored cable.

are not suitable for transmission. Modes 5, 6, and 7 have similar responses, and mode 5 can combined with phantom power. Therefore, considering the compatibility with the old system and the transmission characteristics of the channel, we select the mode 5 to transmit data and supply power for the downhole instrument.

A. SEISMIC WAVE DATA COMPRESSION

We used the compression module described in section III to compress the three sets of real seismic data and calculate the compression ratio. The test results are shown in Table 1.

TABLE 1. Compression Rate Test.

Sets of data	Number of bytes before compression	Number of bytes after compression	Compression ratio
1	86114304	44027291	51.13%
2	86114304	46235854	53.69%
3	86114304	46286247	53.75%

The test results show that the three sets of seismic wave data's compression rate is less than 54%, and the module can effectively compress the seismic wave data.

B. COMMUNICATION ON 7km ARMORED CABLE

For the communication test, as shown in Fig. 21, we input the amplitude data of the sawtooth wave to the modulator. Fig. 22 shows the our prototype telemetry device's PCB. The Fig. 23 shows the 7-km armored cable we used. The modulated and demodulated data also can be observed in real time through the Signal Tap II debugging software in Quartus, as shown in Fig. 24.

1) BIT LOADING

For multi-carrier systems such as Orthogonal Frequency Division Multiplexing (OFDM), when the transmitter knows the channel state information, dynamically assigning the number of transmission bits and power to each subcarrier can significantly improve the system performance [23], [24], that
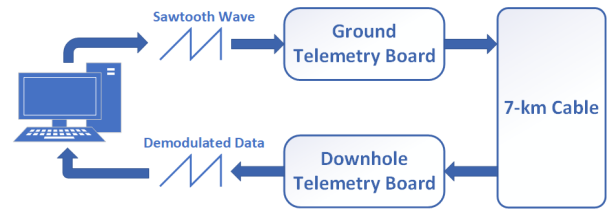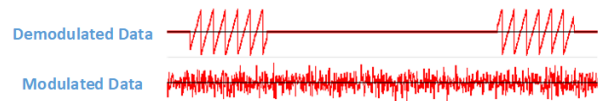

FIGURE 24. Data after modulation and demodulation (via signal tap II).

is, increase the transmission rate without increasing the bit error rate (BER).

According to the different signal-to-noise ratio (SNR) of each sub-channel and the required bit error rate, the number of bits allocated for each sub-channel can be expressed as

$$b(i) = \log_2(1 + \frac{SNR}{\Gamma + \gamma_{margin}}) \tag{26}$$

$$\hat{b}(i) = round(b(i)) \tag{27}$$

where $\hat{b}(i)$ is the number of bits allocated to each sub-channel, Γ is the SNR gap which is determined by the desired BER and coding method. For an uncoded, M-QAM communication system where the required bit error is 10^{-6}, the Γ is approximately 8.8dB. γ_{margin} is the system margin, which is the additional amount of noise that the system can tolerate under the requirement of BER.

After allocating the bits of each sub-channel, tune the power distribution to compensate for the impact caused by rounding and ensure the performance of the system.
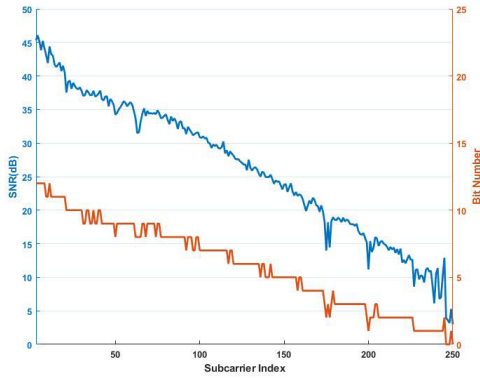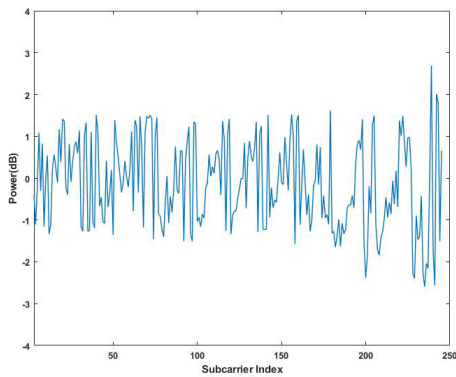
FIGURE 25. Estimated SNR and bit-loading scheme.

FIGURE 27. Correlation coefficient using the original received data.

FIGURE 26. Power distribution.
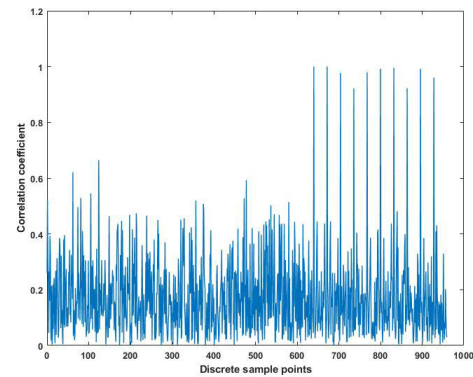
FIGURE 28. Correlation coefficient using the binarized received data.

Fig. 25 and 26 shows the signal-to-noise ratio, bit allocation number of each sub-channel and the power distribution obtained during the channel training stage.

It can be seen that when the frequency of the sub-channel is higher, the signal-to-noise ratio is lower, and the number of bits that can be carried under the same bit error rate is less. The subchannel at 250kHz can only transmit one bit, while the higher frequency subchannel cannot be used for transmission.

2) FRAME DETECTION AND SYNCHRONIZATION

The result of calculating the correlation coefficient using the original received data and the expected training sequence is shown in the Fig. 27. The result of calculating the correlation coefficient using the binarized received data and the expected training sequence is shown in the Fig. 28.

Obviously, no matter the original data or the binarized data, there are ten periodic peaks. Although the result of the calculation using the original data is better, it requires a lot of logic resources. When using the binarized data for calculation, although it is possible to misjudge the noise as a training sequence, there is an energy accumulation sub-module in the frame detection module as an auxiliary, so this will not happen.

Therefore, using the binarized data for symbol synchronization can save logic resources while not reducing the performance of the synchronization module.
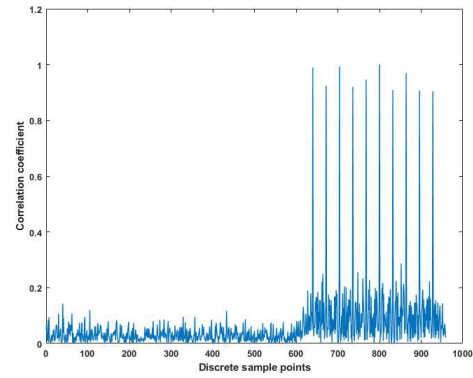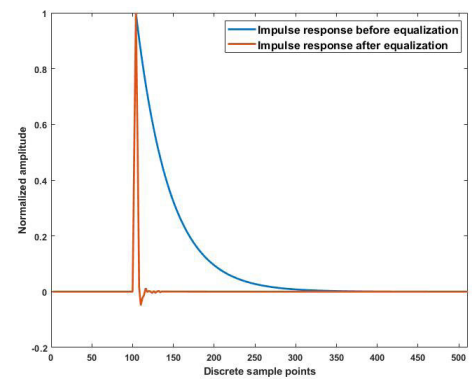

FIGURE 29. Impulse response before and after equalization.

3) TIME DOMAIN EQUALIZE

The impulse response of the channel and the impulse response equalized by the time domain equalizer are shown in the Fig. 29.

The original impulse response lasts about 200 sampling points, or 0.2us, and the FFT size is 1024, which means that a cyclic prefix with an FFT size of 20% must be added to eliminate inter-symbol interference. The equalized impulse response lasted only about 40 sampling points, accounting for 4% of the FFT size, and the required cyclic prefix length was greatly reduced.
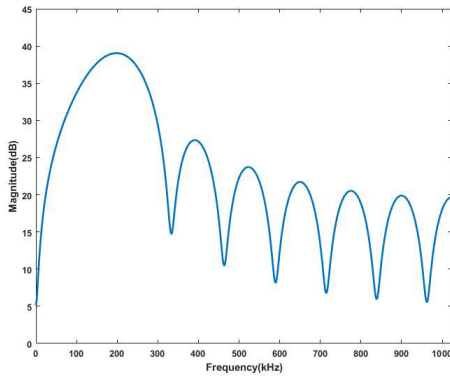
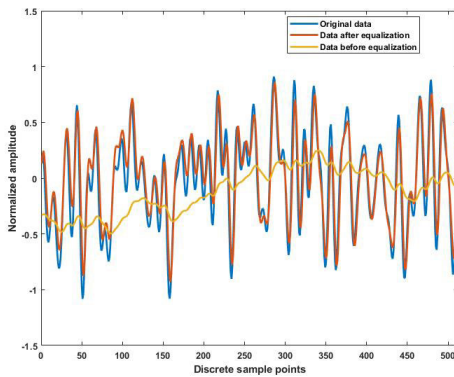**FIGURE 30.** Amplitude-frequency response of the time-domain equalizer.

FIGURE 31. Original signal, received signal and the equalized signal.

FIGURE 32. 16QAM constellation diagram before sampling clock offset compensation.

FIGURE 33. 16QAM constellation diagram after sampling clock offset compensation.

TABLE 2. Comunication rate test.

Test timers	Connection duration	Rate(kbps)	BER
1	2h	1392	0.2×10^{-9}
2	2h	1404	0.7×10^{-9}
3	2h	1421	1.2×10^{-9}
4	2h	1402	0.9×10^{-9}
5	2h	1412	1.3×10^{-9}

The Fig. 30 shows the amplitude-frequency response of the time-domain equalizer after training. Contrary to the low-pass characteristics of the channel, presenting the characteristics of high-pass.

The Fig. 31 shows the original signal, received signal and the equalized signal. The high-frequency signal attenuated by the cable is compensated by the equalizer.

4) SAMPLING CLOCK OFFSET COMPENSATION

In the test system, the deviation of the clock frequency between the transmitter and the receiver is 16*ppm*. We insert 4 pilots into each ofdm symbol, and the sub-carrier numbers of each pilot are 64, 128, 160, 196. The sum of sub-carrier numbers is $64 + 128 + 160 + 196 = 512$. Therefore, the division when estimating the value of S can be realized by shifting the register 9 bits to the right.

The QAM16 constellation diagram before and after sampling clock offset compensation is shown in the Fig. 32 and Fig. 33. The constellation diagram before equalization cannot be demapped because of SFO, and 16 constellation points can be clearly distinguished on the constellation after compensation.

After a long time test, the FFT window did not gradually deviate due to the influence of SFO, but converged at a fixed position, which shows that our retiming method based on pilot symbols is effective.
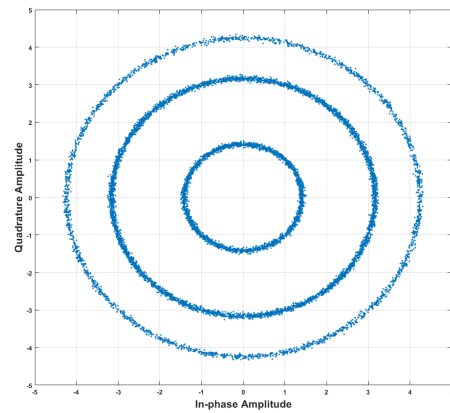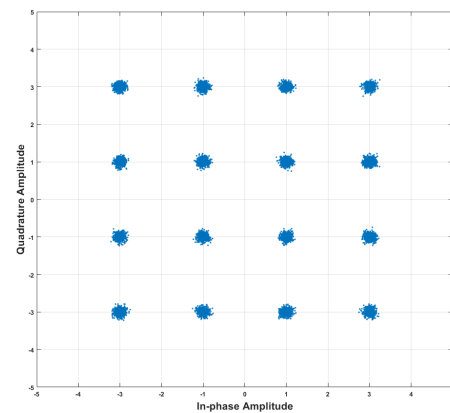
5) TRANSMISSION RATE

Table 2 shows the result of communication test. The communication rate of the system without compression is about 1.4Mbps while the bit error rate is less than 1.0×10^{-8}. Therefore, if we only transmit the seismic wave data, the effective data rate is up to 2.3Mbps.

Compared with some other well logging telemetry system in Table 3 [8], [9], The proposed telemetry system has a higher communication rate at the low bit error rate.

C. COMPARISON BETWEEN FPGA AND DSP

In the field of well logging, many high speed telemetry systems are implemented based on high-temperature DSP, such as CNPC Logging's EIlog system. Table 4 shows the

TABLE 3. Performance with other telemetry systems on 7km logging cable.

Telemetry system (Company)	Method	Transmission Mode	Communication rate(kbps)
CTS (Schlumberger)	AMI	5	100
WTS (ATLAS)	Manchester +AMI	2,5,7	229.16
[9]	Manchester II +AMI	2,5,7	230
EILog (CNPC Logging)	C-OFDM	5	430
MAXI-500 (Schlumberger)	QAM	-	500
LOGIQ (Halliburton)	ADSL	-	850
This Work	OFDM	5	1400-2300

TABLE 4. Performance of FPGA and DSP.

Parameters	Cyclone10 LP	OMAPL137-HT(300MHz)	OMAPL137-HT(476MHz)
Core Voltage(V)	1.2	1.2	1.3
Power Consumption(mW)	169.70	479.73	754.65
1024-point FFT Time(μs)	17.90	32.27	20.34
Processing Method	Parallel	Serial	Serial

power consumption and real-time performance comparison between the Cyclone 10 LP FPGA we used and the high-temperature DSP OMAPL137-HT commonly used in well logging applications [25], [26].

The data of FPGA in Table 4 is obtained from Timing Analyzer and Power Analyzer in Quartus. It can be seen that FPGA has some advantages in power consumption and real-time performance compared to DSP.

V. CONCLUSION

The limitations of telemetry techniques limit the coverage and distance of the geophysics application. In this paper, we propose a high-speed telemetry system for long-distance transmission. We successfully applied this system to transmit data on a 7000m armored cable. In addition, we have done various measurements and analyses on multiple stages of signal transmission and processing. The system is based on FPGA and compared to some traditional designs with digital signal processor, FPGA-based designs are less expensive, have more real-time performance, less power consumption and easier implementation.

Compared with our previous work shown in [16], the well logging telemetry system in this paper not only allocates the bits of each sub-channel, but also allocates the power of each sub-channel to maximize the utilization of channel bandwidth. The time domain equalization module is added to reduce the ISI and quantization noise, so that shorter cyclic prefix can be used in transmission and data redundancy can be

reduced.The sampling clock frequency offset compensation module, which was not considered before, was added to improve the stability and reliability of the system transmission. Meanwhile, the hardware algorithm was optimized to reduce the computational complexity. The channel equalization method is optimized so that the system can track the variation of channel characteristics and adjust the equalization parameters adaptively. The above improvements enable the current telemetry system to increase the transmission rate by 27% over the previous one, improve the reliability, and transmit data on actual cables instead of cable simulator.

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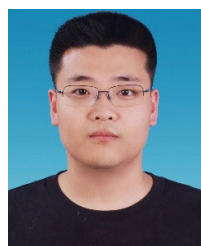
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KEHAN LI received the B.S. degree in electrical engineering and the M.S. degree in physical electronics from the University of Science and Technology of China, Hefei, China, in 2016 and 2019, respectively. His research interests include serial data processing of protocol, data compression, and high-speed data acquisition.

HONGWEI ZHAO (Graduate Student Member, IEEE) received the B.S. degree in physical electronics from the University of Science and Technology of China, Hefei, China, in 2017, where he is currently pursuing the Ph.D. degree with the State Key Laboratory of Particle Detection and Electronics. His research interests include long-distance data transmission, field-programmable gate array (FPGA) applications, and digital signal processing.

CHUAN WU received the B.S. degree in physical electronics from the University of Science and Technology of China, Hefei, China, in 2018, where he is currently pursuing the Ph.D. degree with the State Key Laboratory of Particle Detection and Electronics. His research interests include CAN bus communication, digital signal processing (DSP) applications, and digital signal processing.

KEZHU SONG (Member, IEEE) received the Ph.D. degree from the University of Science and Technology of China, in June 2001. He has been engaged in teaching and scientific research at the State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, where he is currently a Professor. His research interests include experimental physical instrument electronics, theoretical and technical research on data acquisition, transmission, and signal processing.

ZHUO CHEN received the B.S. degree in physical electronics from the University of Science and Technology of China, Hefei, China, in 2019, where he is currently pursuing the M.S. degree with the State Key Laboratory of Particle Detection and Electronics. His research interests include CAN bus communication, digital signal processing (DSP) applications, and digital signal processing.

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