

Received November 25, 2020, accepted December 11, 2020, date of publication January 6, 2021, date of current version January 19, 2021.

Digital Object Identifier 10.1109/ACCESS.2020.3048227

# A Study on the Optimized Ohmic Contact Process of AlGa<sub>N</sub>/Ga<sub>N</sub>-Si MIS-HEMTs

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This work was supported in part by the National Science Foundation of Shaanxi Province, China, under Grant 2018JQ6069, and in part by the China Postdoctoral Science Foundation, under Grant 2018M643733.

**ABSTRACT** AlGa<sub>N</sub>/Ga<sub>N</sub>-Si based MIS-HEMTs are considered as the popular candidates for application in the 5G communication system due to their competitive characteristics and low cost. Ohmic contact, as an important fabrication process, significantly affects the performance of the device. In this study, the ohmic contact process, including the SiN passivation layer etching, surface treatment, and barrier layer etching, was studied in detail in order to effectively optimize the device performance. It is observed that the sample with the SiN passivation layer etched by the magnetic neutral loop discharge (NLD) resulted in a lower contact resistance as compared to the reaction ion etching (RIE). The sample surface treated with the O plasma and pickled in the HCl:H<sub>2</sub>O = 1:10 liquid could effectively remove the pollutants and oxides from the surface, thus, correspondingly presenting a lower ohmic contact resistance as compared to the N<sub>2</sub> plasma. Meanwhile, an optimum etching depth was developed with the ICP process for 6 min with an etching speed of 1.6 nm/min. A contact resistance of 0.76 Ω · mm and square resistance of 274.63 ohm/sq were observed under the above-mentioned optimized ohmic contact process. The AlGa<sub>N</sub>/Ga<sub>N</sub>-Si MIS-HEMT with gate length of 0.5 μm, gate-source space of 1 μm, gate-drain space of 2.5 μm, and gate width of 100 μm was fabricated using the optimized process. A saturation current density of 794.30 mA/mm and the maximum transconductance of 16.86 mS were observed. The findings in this study provide the experimental basis for the manufacturing of AlGa<sub>N</sub>/Ga<sub>N</sub>-Si based MIS-HEMTs for RF applications.

**INDEX TERMS** AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT, Ohmic contact process.

## I. INTRODUCTION

Compared with the traditional III-V compounds of the GaAs and InP materials, the GaN material presents excellent characteristics, e.g., large bandgap width, high breakdown electric field, optimal thermal conductivity, high-temperature resistance, and effective radiation resistance. These characteristics satisfy the requirements of the RF high power amplifiers in mobile communications, radars, and satellites [1]. Currently, GaN based high electron mobility transistors (HEMTs) are developed on the SiC substrate for RF application. However, the large-scale market applications of the GaN-SiC device are limited by significant costs. The GaN devices based on the Si substrate exhibit characteristics, e.g., high breakdown voltage, low conduction resistance, and low energy consumption, along with a reduction in the cost, as compared with GaN-

SiC. Meanwhile, GaN-Si can be integrated with traditional Si technology for effective future integration. In addition, the gate leakage current seriously affects the efficiency of the GaN-Si HEMTs for RF application. Therefore, a thin film of insulator layer is deposited on the surface of the GaN epitaxy in order to form the metal-insulator-semiconductor (MIS) gate structure to effectively suppress the gate leakage current [2], [3]. For this reason, GaN-Si MIS-HEMTs are observed to be the most promising devices in RF application, especially for the upcoming 5G communication system [4], [5].

Ohmic contact, as an important fabrication process, significantly affects the performance of the GaN HEMTs devices. The literature studies have usually adopted the multi-layer metal structures such as Ti/Al/Ni/Au, Ti/Al/Pt/Au, Ti/Al/Pd/Au, Ti/Al/Mo/Au, and Ti/Al/Cr/Mo/Au [6]–[9], with a change in the metal ratio in each layer to obtain a stable ohmic contact. Wet etching and plasma treatment are

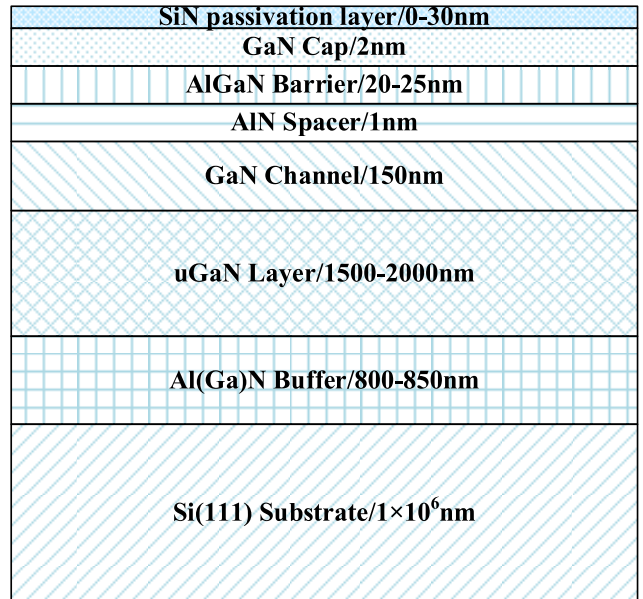
The associate editor coordinating the review of this manuscript and approving it for publication was Cheng Qian<sup>1</sup>.

commonly used techniques for surface treatment. Wet etching removes the pollutants and oxides on the sample surface by using the acid and alkali solutions [10]. The plasma treatment produces an enhanced extent of nitrogen vacancies on the surface [11]–[14], which reduces the height of the barrier to a certain extent. Surface etching can be adopted to reduce the thickness of the barrier layer of the source and drain regions to reduce the contact resistance [15], [16]. Meanwhile, different annealing temperatures and durations can influence the quality of the ohmic contact as well [17], [18]. It should be noted that the methods reported for improving the ohmic contact performance largely focus on GaN-SiC HEMTs. In contrast, only a few studies have focused on GaN-Si HEMTs, and especially the optimized ohmic contact process of the GaN-Si MIS-HEMTs needs to be studied in detail. In this respect, this study analyzes the ohmic contact process conditions of GaN-Si HEMTs in detail, such as SiN passivation etching, surface treatment, and barrier layer etching, in order to determine an optimized combination of these aspects for improving the ohmic contact performance of AlGaN/GaN-Si MIS-HEMTs.

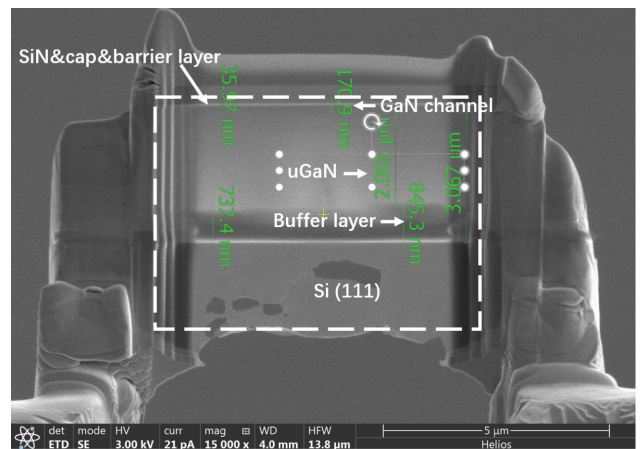
**II. EPITAXY PREPARATION**

High resistance Si (111) with a thickness of  $1 \times 10^6$  nm was chosen as the substrate for RF application. An AlN layer and two AlGaN layers were deposited on the Si substrate as the buffer layer to reduce the crystal and thermal mismatch between the Si substrate and GaN material. In addition, the buffer layer was doped with Fe for attaining high resistance. A 2000 nm uGaN epitaxial layer was grown on the surface of the buffer layer, on top of which a 150 nm GaN channel layer was grown further. A 1 nm thick AlN insertion layer was grown on the GaN channel to improve the two-dimensional electron gas (2DEG) of the device, followed by the growth of a 20 nm-thick undoped AlGaN barrier layer with Al composition of 25% [19]. Finally, a 2 nm thick GaN cap layer was grown on the surface of the barrier layer for protection. For RF application, the gate leakage current seriously affects the efficiency of the device. Therefore, a thin film of the SiN passivation layer with a thickness of 6 nm was deposited on the surface of the epitaxy by employing the LPCVD method, in order to form the isolated gate structure to suppress the gate leakage current. The process of SiN deposition is as follows: the samples were pickled in the HCl:H<sub>2</sub>O = 1:10 solution to remove the pollutant from the surface and were subsequently placed in a gas mixture (SiH<sub>2</sub>Cl<sub>2</sub> and NH<sub>3</sub>) using the LPCVD system for 80 s at 785 °C, deposited at a rate of 6 nm per minute using a chamber pressure of 300 mTorr. The schematic of the complete GaN-Si epitaxy structure is shown in Fig.1. The epitaxy was observed by Focused Ion Beam (FIB), and the scanning image is presented in Fig.2. It can be seen that the epitaxial growth is uniform, and the boundary between the layers is clear. The subsequent findings reported in the study about the device preparation are based on this epitaxy structure.

The HALL test was carried on the epitaxy, and the test results are shown in Table 1. The mobility is noted to be



**FIGURE 1.** The schematic of the complete GaN-Si epitaxy structure.



**FIGURE 2.** The schematic of the complete GaN-Si epitaxy structure.

**TABLE 1.** The Findings Obtained From Hall Test

Parameter	Mobility $[\text{cm}^2/\text{Vs}]$	Carrier density $[\text{cm}^{-2}]$	$R_s$ $[\text{ohm}/\text{sq}]$
Test result	1901.61	$1.862 \times 10^{13}$	169.97

$1901.61 \text{ cm}^2 / \text{Vs}$ , whereas the carrier density and square resistance ( $R_s$ ) of the epitaxy are  $1.862 \times 10^{13} \text{ cm}^{-2}$  and  $169.97 \text{ ohm}/\text{sq}$  respectively.

**III. DISCUSSION ON THE OHMIC CONTACT PROCESS**

Ohmic contact process comprises the lithography, SiN etching, metal deposition, and stripping/PDA steps. For lithography, AZ5214 was chosen as the positive photoresist applied on the samples at a rate of 4000 rpm for 30 s. For the photoresist thickness of about  $1.5 \mu\text{m}$ , baking the samples

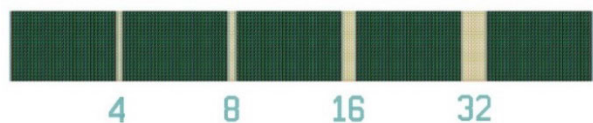


FIGURE 3. Layout of the TLM structure.

for 90 s at 95 °C to remove the solvent on the resist film led to enhanced adhesion of the resist to the wafer. Subsequently, Karl Suss MA6 was used for UV exposure for 6.5 s. After treatment for 45 s with the RZX-3038 developer, the samples were washed by using the DI liquor and dried by N<sub>2</sub>.

Subsequent to lithography, the SiN etching was used to form the ohmic contact region. Following this, the samples were handled for the surface treatment process in order to remove the surface oxide. Afterward, the ohmic contact metal structure Ti 20 nm/Al 130 nm/Ni 50 nm/Au 50 nm was grown. The metal was stripped with acetone and isopropanol, rinsed with DI, dried with N<sub>2</sub>, and finally rapidly thermal annealed for 30 s at 875 °C. During the Ohmic contact process, the parameters such as SiN etching, surface treatment, barrier etching significantly affect the quality of the ohmic contact. To study the effect of the different process conditions, several samples were prepared and the test results obtained from the TLM method were analyzed in detail.

The layout of the TLM cell is shown in Fig.3. The size of TLM is 100 μm \* 160 μm, and the distance between the TLM pads is 4/8/16/32 μm, respectively.

#### A. SiN PASSIVATION ETCHING

The removal of passivation before metallization is crucial to achieve the higher quality ohmic contact [20], [21], which can lower the height of the barrier. The etching process may cause damage on the surface used to grow metal. The damage includes surface flatness, change in the surface state, pollution, etc. Therefore, choosing an etching method leading to a low surface damage is vital for this process. The main method employed to etch the passivation layer is dry etching, which includes RIE (Reaction Ion Etching) and NLD (Magnetic Neutral Loop Discharge). RIE [22] is the dry etching process exhibiting characteristics of strong anisotropy and high selectivity. It is carried out in a vacuum system using the molecular gas plasma, and the ions induced chemical reaction is used to realize the anisotropic etching. Moreover, the ions can also remove the by-products from the surface. SF<sub>6</sub>, CHF<sub>3</sub>, and He have generally been used as the reactants. The gas decomposes to produce the active reaction components under the action of the radio frequency source and has physical and chemical effects with the etched material under the action of the self-bias electric field. Finally, the gas volatiles are produced to achieve the purpose of etching. However, the etching technology does not lead to a high selectivity and results in a greater degree of surface damage, along with pollution and inability to form a large extent of fine graphics. In the experiment, SF<sub>6</sub>, CHF<sub>3</sub>, and He are used as reaction gases to

TABLE 2. TLM Test Result for the Samples Generated With Different SiN Passivation Etching Processes

Sample	Contact resistance/[Ω·mm]	Square resistance/[ohm/sq]
1#	3.17	293.35
2#	1.56	274.14

etch the SiN passivation layer. SF<sub>6</sub> and CHF<sub>3</sub> are the supply source of element F and main gases used for etching Si-N and Si-O. O<sub>2</sub> is favorable for Taper Angle, also used for photoresist podzolic processes. NLD [23] represents a relatively new plasma source for the purpose of dry etching. The plasma can be generated using a high frequency electric field applied to a circular magnetic neutral line with a magnetic field strength of 0 in the vacuum chamber. The size and density of the plasma can be controlled by changing the current so as to produce plasma of various shapes. This method has the advantages of high etching rate, uniformity, high ionized density and low voltage discharge. The etching is completed under CF<sub>4</sub> (20 sccm) mixed with O<sub>2</sub> (2 sccm) atmosphere for 1 min. In case the simple fluorocarbon gas is selected, it is straight-forward to form the polymeric sidewall protection, which is not conducive to the etching process, and the addition of oxygen helps to remove the polymer. For other parameters, the temperature of the chamber is 30°C, and the power is 500 W, which leads to a low degree of damage to the samples as well as complete etching.

In order to study the effect of the different SiN etching processes, the samples were developed with RIE etching (sample 1#) and NLD (sample 2#). The samples were prepared as following: treatment with an O plasma at 200 W for 2 min, followed by etching using RIE and NLD, respectively. Subsequently, the samples were pickled with HCl:H<sub>2</sub>O = 1:10. Finally, the metal was grown and rapidly thermal annealed for 30 s at 875 °C to form the ohmic contact. The TLM test performed on the samples, and the averaged results are presented in Table 2.

As observed from Table 2, the contact resistance of sample 1# is 3.17 Ω · mm which is larger than the sample 2# (1.56 Ω · mm). The square resistance is observed to be 293.35 ohm/sq for the sample 1#, also larger than 274.14 ohm/sq for the sample 2#. SiN passivation etching decreases the thickness of the barrier to correspondingly reduce the ohmic contact resistance. On the other hand, based on the theories of the two etching methods mentioned earlier, it is noted that NLD has higher uniformity, strong anisotropy, and lower damage than RIE due to the reaction conditions, which can achieve a flatter etched surface than RIE. Therefore, etching SiN using the NLD method can attain a higher quality of the ohmic contact than with RIE.

To analyze the surface, the AFM images are obtained from sample 2# etched with NLD, as shown in Fig.4. Based on the AFM results, R<sub>a</sub> (arithmetic mean roughness) of sample 2# is 0.904 nm, whereas the R<sub>q</sub> (root mean square roughness) value is 0.00119 μm.

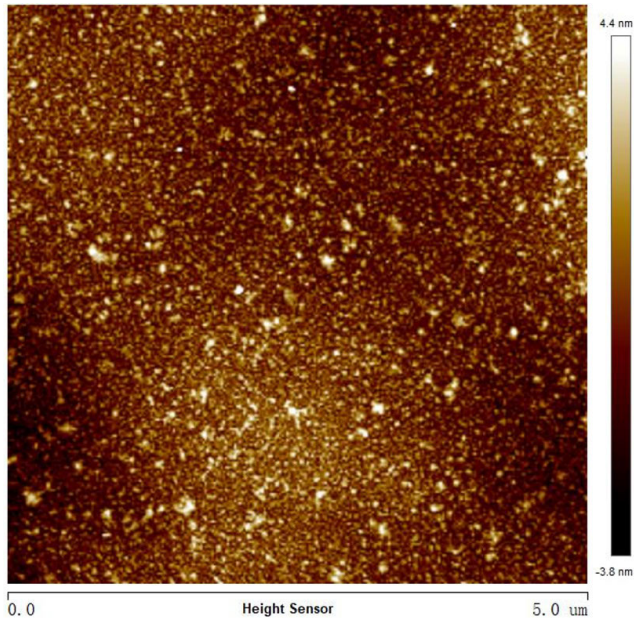


FIGURE 4. AFM image of sample 2# after SiN etching with NLD.

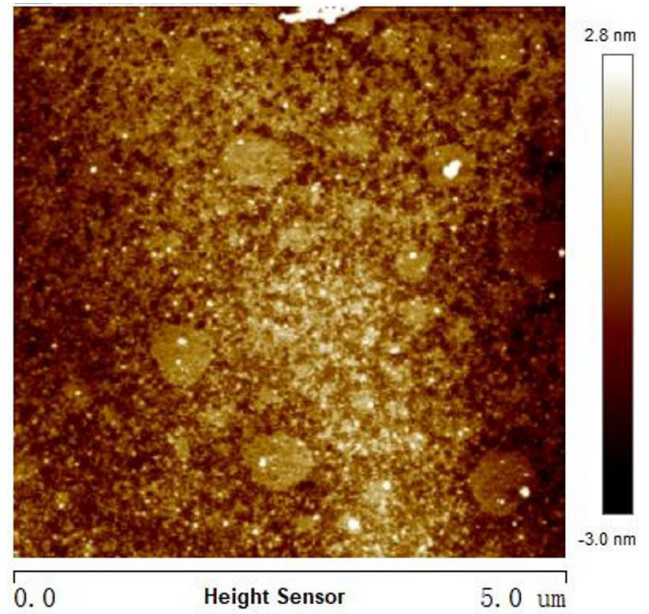


FIGURE 5. AFM image of sample 2# after surface treatment with wet method.

TABLE 3. TLM Test Results for the Samples Subjected to Different Surface Treatment Processes

Sample	Contact resistance/[ $\Omega \cdot \text{mm}$ ]	Square resistance/[ohm/sq]
2#	1.56	274.14
3#	2.89	290.25

**B. SURFACE TREATMENT**

In order to study the effect of the surface treatment process, the samples were prepared by the wet (O plasma and pickling in HCl:H<sub>2</sub>O = 1:10, as sample 2#) and dry (N<sub>2</sub> plasma, as sample 3#) methods. Surface treatment is employed to recover the damage caused by SiN passivation etching.

Wet etching is highly corrosive to the strain zones or chemical inhomogeneities on the defective surfaces, such as dislocations, impurities, etc. It can remove the contaminants on the material surface and reduce the surface state. Dry etching and N<sub>2</sub> plasma can react with Ga on the surface of GaN to generate GaN, thus, eliminating the non-stoichiometric ratio and improving the nitrogen deficiency of GaN after etching. Both treatment methods can improve the quality of the ohmic contact. The details of the processes are as follows: the samples were subjected to the O plasma at 200 W for 2 min before the ohmic contact. NLD was chosen for SiN passivation etching for 1 min. Subsequently, sample 2# was subjected to the O plasma at 200 W for 2 min, followed by pickling in HCl:H<sub>2</sub>O = 1:10 for a specific period of time. Sample 3# was treated with the N<sub>2</sub> plasma for surface treatment. Subsequently, the metal was grown and rapidly thermal annealed for 30 s at 875 °C to generate the ohmic contact. The TLM analysis was performed on the samples, and the averaged results are presented in Table 3.

Comparing the test data of the two samples, the contact and square resistance values of the sample 2# (1.56  $\Omega \cdot \text{mm}$  and 274.14 ohm/sq respectively) are smaller than those of the sample 3#. The HCl:H<sub>2</sub>O = 1:10 solution is noticed to remove the surface oxide to reduce the height and width of the barrier between the metal and semiconductor, together with the O plasma. After pickling, the Fermi level ( $E_F$ ) at the surface is observed to move near the conduction band edge. Pickling increases the nitrogen concentration on the surface, resulting in the movement of  $E_F$ . After the solution corrodes the oxidized layer, it also reacts with the AlGaIn surface to generate the passivation layer, thus, reducing the surface state and barrier height as well as alleviating the pinning effect, the factors responsible for improving the ohmic contact quality. In contrast, the N<sub>2</sub> plasma can recover the damage caused by the previous processes, e.g., mesa isolation and etching, thus, producing the flatter surface with the optimal condition to form the ohmic contact on the sample. The etch residues have been reported to be removed and the number of pinholes reduced after the N<sub>2</sub> plasma treatment [24]. The recovery on the surface may improve the properties of samples, thus, enhancing the quality of the ohmic contact. In addition to the etch residues and pinholes, the N<sub>2</sub> plasma can remove the pollutants and oxides formed on the surface, which lowers the barrier and forms a smaller contact resistance. However, the plasma-treated sample may be easily oxidized as the stoichiometry of the GaN is changed [10]. In addition, the nitrogen vacancy formed in the previous process receives nitrogen during the N<sub>2</sub> plasma process [22], which increases contact resistance. Therefore, the O plasma and pickling in the HCl:H<sub>2</sub>O = 1:10 solution as surface treatment can form the superior ohmic contact as compared to the N<sub>2</sub> plasma.

**TABLE 4.** TLM Test Results for the Samples Developed With Different Etching Depth

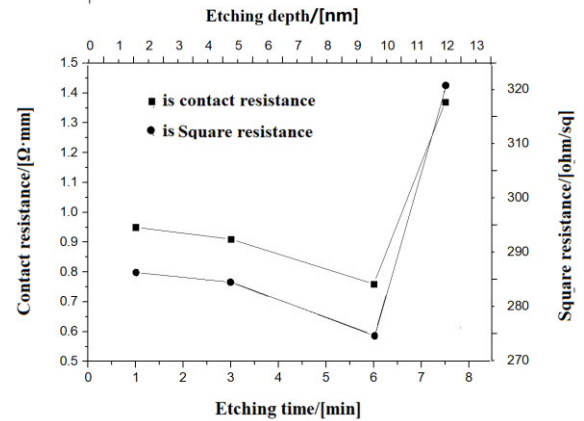
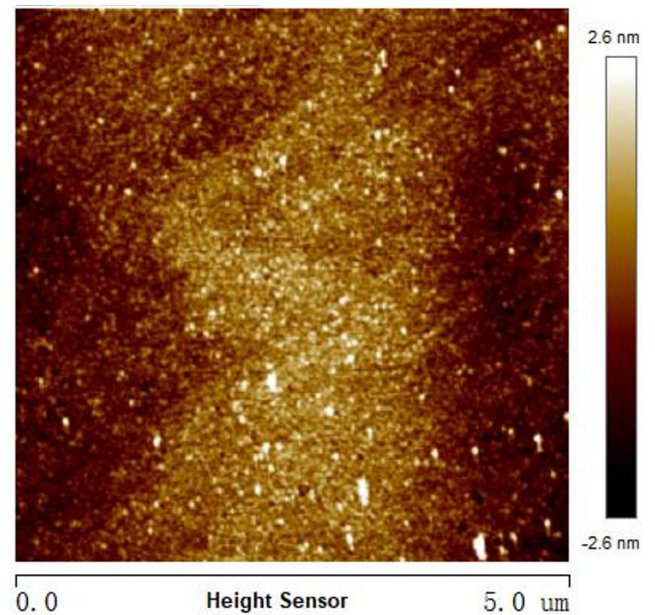
Sample	Contact resistance/ $[\Omega \cdot \text{mm}]$	Square resistance/ $[\text{ohm}/\text{sq}]$
4#	0.95	286.32
5#	0.91	284.53
6#	0.76	274.63
7#	1.37	320.81

The AFM image of sample 2# after wet etching (O plasma and pickling in  $\text{HCl}:\text{H}_2\text{O} = 1:10$ ) is shown in Fig.5.  $R_a$  (arithmetic mean roughness) of sample 2# after surface treatment is 0.694 nm, where  $R_q$  (root mean square roughness) is noted to be 1.09 nm. Compared with the result obtained from Fig.4., the surface roughness is observed to improve with O plasma and pickling in  $\text{HCl}:\text{H}_2\text{O} = 1:10$  as the surface treatment.

### C. CAP AND BARRIER LAYERS ETCHING

Overall etching of the ohmic contact area to reach the barrier layer can remove the surface oxides, thus, forming a new ohmic contact surface, reducing the thickness of the barrier layer, promoting the carrier tunneling and increasing the surface roughness, which facilitates the displacement reaction and reduces the effective barrier height [25]. In order to study the effect of the etching process, the samples were prepared with different etching depth using the following process steps: use of the NLD method to etch the SiN passivation for 1 min, followed by treatment with the O plasma at 200 W for 2 min. Subsequently, ICP was carried out on sample 4# for 1 min with etching depth of about 1.6 nm, sample 5# for 3 min with etching depth of about 4.8 nm, sample 6# for 6 min with etching depth of about 9.6 nm, and sample 7# for 7.5 min with etching depth of about 12 nm, respectively, with the etching speed of 1.6 nm/min. Following this, the samples were pickled in  $\text{HCl}:\text{H}_2\text{O} = 1:10$  for surface treatment. Subsequently, the metal was grown and rapidly thermal annealed for 30 s at 875 °C to form the ohmic contact. The TLM test has been performed on the samples, and the averaged result is presented in Table 4.

From Fig.6, it is observed that the contact resistance decreases on increasing the etching time from 0 to 6 min. This is due to the fact that the distance between the metal electrode and two-dimensional electron gas channel is reduced due to the thickness of the barrier layer of the etch source and drain area, thus, reducing the ohmic contact. The thinner barrier layer induces a reduction and subsequent depletion of 2DEG, thus, making the contact formation difficult [23]. In contrast, as the etching depth is increased beyond 6 min, the contact resistance is also increased, however, the consistency is noted to be non-uniform as the etching time increases beyond 7.5 min. The observed phenomenon takes place due to the fact that the depth might reach the channel layers due to the poor uniformity of the etching process. Based on this phenomenon, it can be concluded that an optimal etching depth is needed

**FIGURE 6.** The resistance curve for the surface etching process.**FIGURE 7.** The AFM of samples with ICP etching.

to form an effective ohmic contact. From the test results, the sample 6# with ICP etching for 6 min with etching depth of about 9.6 nm exhibits the smallest mean contact and square resistances of 0.76  $\Omega \cdot \text{mm}$  and 274.63 ohm/sq respectively, which indicated that ICP for 6 min at a rate of 1.6 nm/min leads to the growth of effective ohmic contact.

The surface roughness of the samples with ICP etching before pickling in  $\text{HCl}:\text{H}_2\text{O} = 1:10$  was tested with AFM. As shown in Fig.7,  $R_a$  (arithmetic mean roughness) is observed to be 0.653 nm, whereas  $R_q$  (root mean square roughness) is 0.875 nm. As compared with NLD etching, a lower surface roughness is observed.

## IV. DEVICE FABRICATION

The AlGaIn/GaN-Si MIS-HEMT was designed with gate length ( $L_g$ ) of 0.5  $\mu\text{m}$ , gate-source space ( $L_{gs}$ ) of 1  $\mu\text{m}$ ,

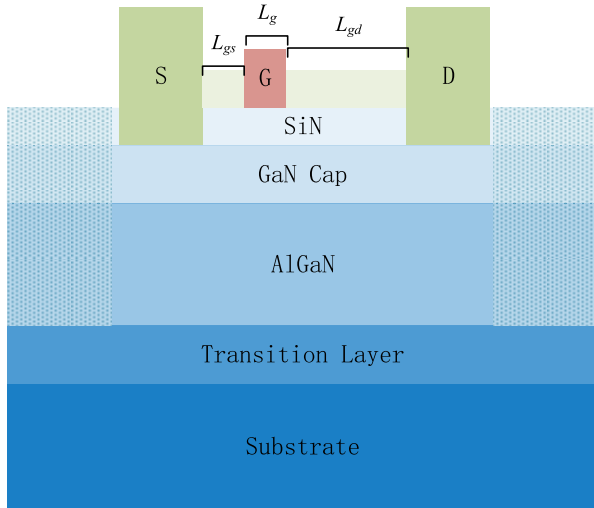


FIGURE 8. The structure diagram of GaN-Si HEMT.

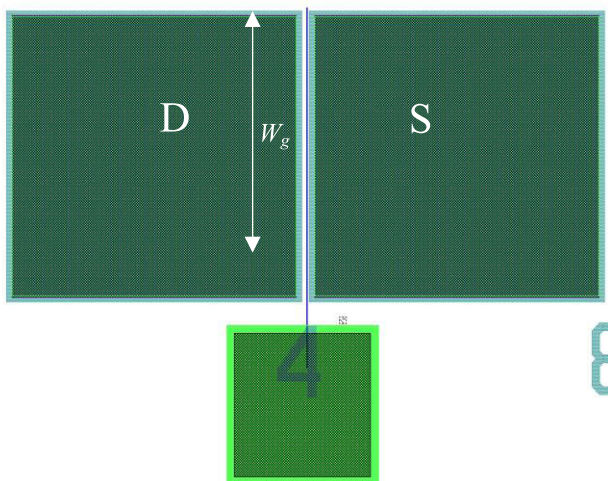
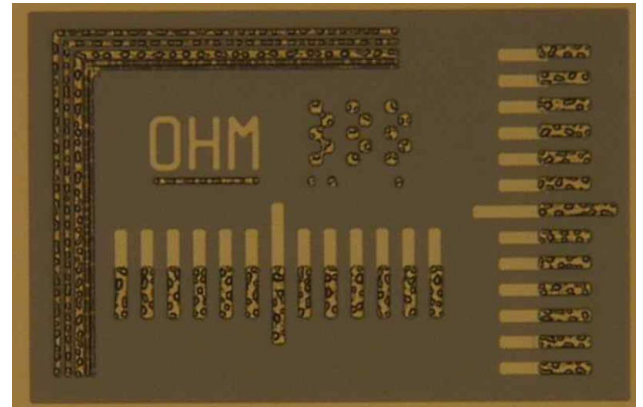
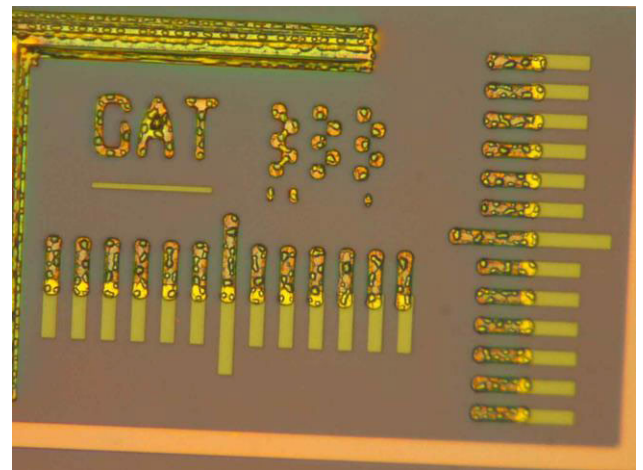


FIGURE 9. The layout of the designed device.

gate-drain space ( $L_{gd}$ ) of  $2.5 \mu\text{m}$ , which is shown in Fig. 8, and gate width ( $W_g$ ) is  $100 \mu\text{m}$  shown in the layout Fig. 9. It was fabricated by using the optimized process of SiN passivation layer etched by NLD, surface treatment with the O plasma and  $\text{HCl:H}_2\text{O} = 1:10$  liquid, cap, and AlGaIn barrier layers etched for 6 min at a rate of  $1.6 \text{ nm/min}$  with etching depth of about  $9.6 \text{ nm}$  by ICP and annealing at  $875 \text{ }^\circ\text{C}$ , as discussed above. Fig. 10 presents the optical microscopy images of the mask of the ohmic contact and gate metal, demonstrating that the relative position between the source-drain electrode and electrode growth is largely accurate. The gate-source and gate-drain spaces were tested to demonstrate a slight deviation from the design, as shown in Fig.11 (the measured values of  $L_{gs}$  and  $L_{gd}$  are  $0.7 \mu\text{m}$  and  $2.54 \mu\text{m}$  respectively). This is owing to the reason that the ohmic metal retracted about  $0.5 \mu\text{m}$  during the annealing step. Also, for the gate process, the precision error of the gate lithography



(a)



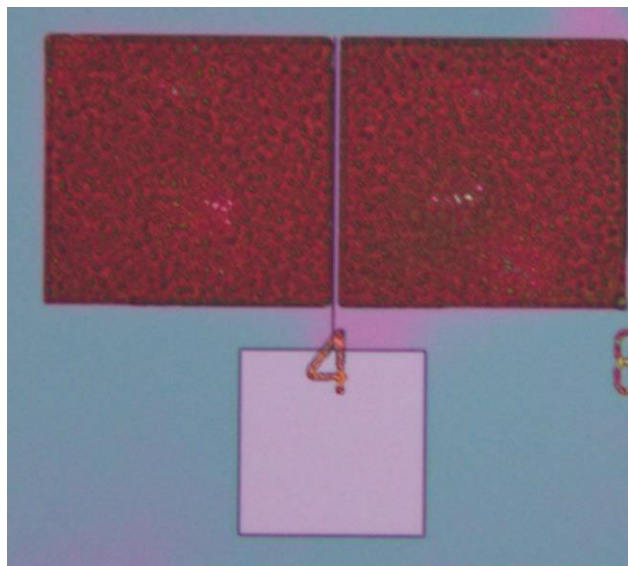
(b)

FIGURE 10. The optical microscopy images of the mask: (a) ohmic contact and (b) gate metal.

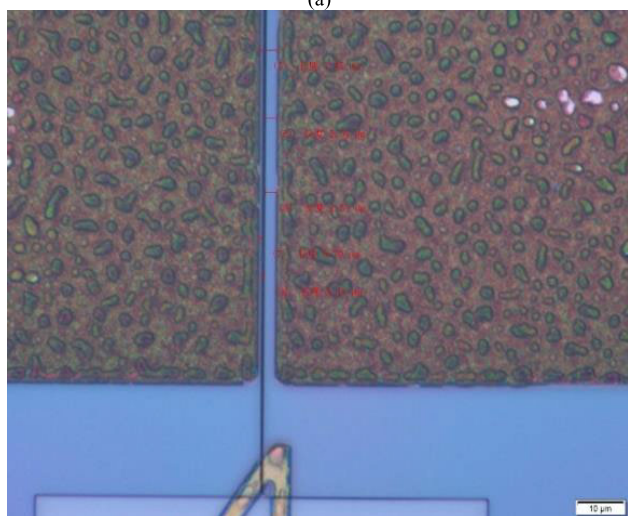
equipment and developer soaking time results in a deviation in the gate width as compared with the design size.

Fig.12 shows the gate leakage current as a function of gate voltage. The gate voltage ( $V_{gs}$ ) varied from  $-10 \text{ V}$  to  $8 \text{ V}$  with  $0.1 \text{ V}$  step, while the source-drain voltage ( $V_{ds}$ ) was  $0 \text{ V}$ . It is found that the gate current ( $I_g$ ) has a very low value of  $\sim 2.5 \times 10^{-11} \text{ A}$  (leakage current density is about  $2.5 \times 10^{-4} \mu\text{A/mm}$ ), with insignificant variation as  $V_{gs}$  increases from  $-10 \text{ V}$  to  $6 \text{ V}$ . On the other hand, a change is noted in  $I_g$  as the gate voltage is increased beyond  $6 \text{ V}$ . As the gate voltage ranges from  $-10 \text{ V}$  to  $-8 \text{ V}$ , the gate current shows a slight downward trend. It can be explained that as the gate voltage is closed to the threshold voltage, the device is open, and there is no obvious channel formed inside at the open voltage. Thus, as the gate voltage is applied, the electron tunneling directly from gate leads to a large leakage. However, in actual, the increase is less than an order of magnitude, as shown in the figure.

Fig.13 shows the variation of the drain current density with drain voltage.  $V_{ds}$  is varied from  $0$  to  $10 \text{ V}$ , whereas  $V_{gs}$  varies from  $-10 \text{ V}$  to  $0$  with a step of  $2 \text{ V}$ . It is noted the

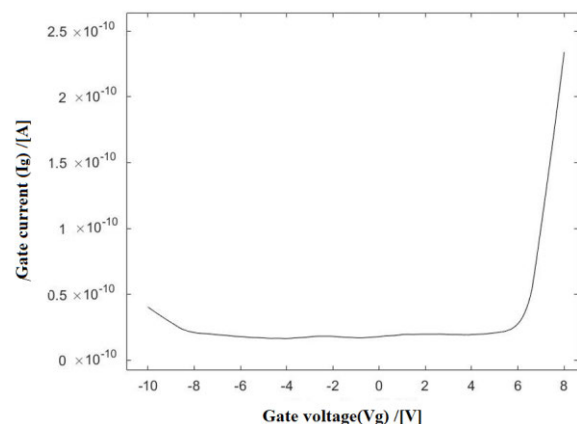


(a)



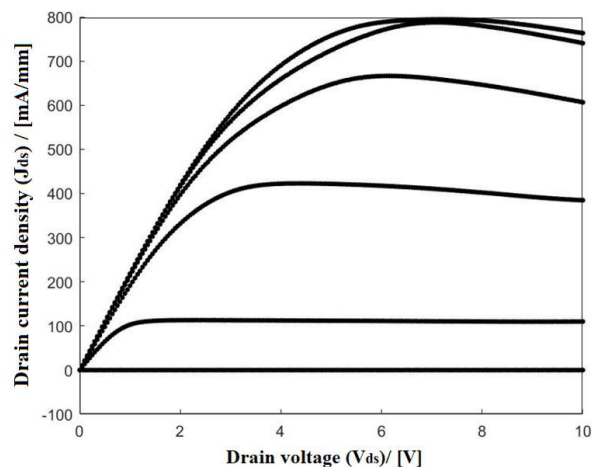
(b)

**FIGURE 11.** The optical microscopy images of the device: (a) complete view and (b) partial enlarged view.

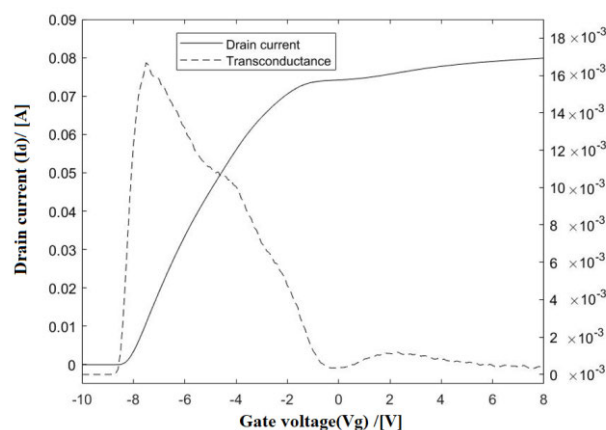


**FIGURE 12.** The gate leakage current as a function of gate voltage.

device presents a high saturation drain current density ( $J_{ds}$ ) of 794.30 mA/mm at a  $V_{gs}$  value of 0 V.



**FIGURE 13.** The drain current density as a function of drain voltage.



**FIGURE 14.** The transfer characteristics of the device.

Fig. 14 shows the transfer characteristics of the HEMT device. The device performance was measured as a function of  $V_{gs}$  varying from  $-10$  V to  $8$  V, with  $V_{ds}$  value of  $10$  V. The threshold voltage ( $V_{th}$ ) of  $-8$  V is noted, with the maximum transconductance ( $g_m$ ) of  $16.68$  mS at a  $V_{gs}$  value of  $-7.5$  V.

### V. CONCLUSION

In this study, the ohmic contact process of AlGaN/GaN-Si MIS-HEMT, including the SiN etching, surface treatment, cap and barrier layer etching, etc., has been studied in detail for attaining an optimized solution. For SiN passivation etching, the sample processed with the NLD method had a smaller contact resistance due to the lower surface damage and higher uniformity as compared to the RIE process. For the surface treatment process, compared with the  $N_2$  plasma, the O plasma together with pickling with  $HCl:H_2O = 1:10$  solution exhibited the better performance as the  $N_2$  plasma compensated the nitrogen vacancy on the surface. Also, the reduction in the barrier height was less than that under the pickling condition. Cap and barrier layer etching for 6 min with an etching speed of  $1.6$  nm/min improved the quality of the

ohmic contact and reduced the contact resistance effectively. The contact resistance of  $0.76 \Omega \cdot \text{mm}$  and a square resistance of  $274.63 \text{ ohm/sq}$  were obtained by the optimized ohmic contact process. The AlGaIn/GaN-Si MIS-HEMT with  $L_g$  of  $0.5 \mu\text{m}$ ,  $L_{gs}$  of  $1 \mu\text{m}$ ,  $L_{gd}$  of  $2.5 \mu\text{m}$ , and gate width of  $100 \mu\text{m}$  was fabricated by employing the optimized process. The device presented the saturation current density value of  $794.30 \text{ mA/mm}$  at a  $V_{gs}$  value of  $0 \text{ V}$ , whereas the maximum transconductance of  $16.68 \text{ mS}$  at a  $V_{gs}$  value of  $-7.5 \text{ V}$  was noted.

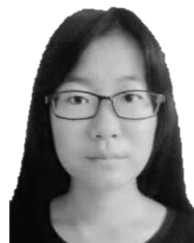
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