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An 18.39 fJ/Conversion-Step 1-MS/s 12-bit SAR ADC With Non-Binary Multiple-LSB-Redundant and Non-Integer-and-Split-Capacitor DAC

HSUAN-LUN KUO[1], CHIH-WEN LU[1,2], (Member, IEEE), AND POKI CHEN[3], (Member, IEEE)

[1]Department of Engineering and System Science, National Tsing Hua University, Hsinchu 30013, Taiwan, R.O.C.
[2]Institute of Lighting and Energy Photonics, National Chiao Tung University, Tainan 71150, Taiwan, R.O.C.
[3]Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology, Taipei 10607, Taiwan, R.O.C.

Corresponding author: Chih-Wen Lu (cwlu@mx.nthu.edu.tw)

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ABSTRACT A low-power 12-bit successive approximation register (SAR) analog-to-digital converter (ADC) with split-capacitor, nonbinary-weighted, and multiple-least-significant-bit (LSB)-redundant capacitor digital-to-analog converters (CDACs) is proposed. The proposed SAR ADC with nonbinary-weighted and multiple-LSB-redundant CDACs has an optimal mechanism for correcting the bit error decisions due to noise and incomplete digital-to-analog converter (DAC) switching settling. To reduce the total capacitance, all capacitor values of the 12-bit DAC were divided by 16, and a parallel-series capacitor scheme was used to implement these noninteger capacitors. The 12-bit SAR ADC prototype was fabricated using 0.18-μm 1P6M complementary metal oxide semiconductor technology. The maximal differential nonlinearity and integral nonlinearity were measured as $-0.4/0.54$ and $-0.81/0.89$ LSB, respectively, where 1 LSB $=$ 0.488 mV. The signal-to-noise-and-distortion ratio and effective number of bits were 69.51 dB and 11.25 bits, respectively, for the input frequency of 500 kHz and sampling rate of 1 MS/s. The proposed SAR ADC features an 18.39-fJ/conversion-step Figure-of-Merit (FoM) at the sampling rate of 1 MS/s.

INDEX TERMS SAR ADC, non-binary-weighted CDAC, multiple-LSB redundant CDAC.

I. INTRODUCTION

The Internet of Things (IoT) has developed rapidly in recent years. In general terms, IoT is a protocol that collects environmental data remotely, processes the data, and retrieves the processing results over the internet for further use. To sense environmental data in this context, analog-to-digital converters (ADCs) are indispensable. In the era of modern 5G access to the internet, IoT applications typically require wireless devices. Low power consumption is a key feature of wireless devices. The ADC resolutions required for different sensing elements are different. In sensor applications, the most widely used ADC resolution is 8–12 bits [1]–[6]. For electrocardiogram and electroencephalogram applications, a low-power ADC with 12-bit resolution and a sampling rate of 100k–1MS/s is required. For these specifications, a successive approximation register (SAR) ADC is suitable [7], [8].

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The charge-distributed SAR ADC architecture was introduced in 1975 [9]. This architecture typically has low power consumption, a medium speed sampling rate, and a medium-to-high resolution range. In a typical SAR ADC, the capacitor digital-to-analog converter (CDAC) accounts for a major portion of the total power consumption. In recent years, a few technologies have been proposed to reduce the power consumption of CDACs. For example, split-capacitor-array digital-to-analog converters (DACs) [10], monotonic switching [11], Vcm-based switching [12], the C-2C architecture [13], [14], series capacitors [12], [15]–[18], unit capacitance reduction [11], [19]–[22], and hybrid DACs [23]–[25] have been used to reduce the power consumption of DACs. The split-capacitor-array DAC architecture does not require precharging of the CDAC, which reduces the energy loss due to capacitor precharging. Because the total capacitance of a monotonic-switching DAC is half that of a typical DAC, the monotonic-switching architecture consumes less power than the split-capacitor-array DAC.

The monotonic-switching CDAC uses the set-and-down switching method. Therefore, the common-mode voltage of the comparator is gradually reduced, which causes the comparator dynamic offset problem. A few researchers have combined the split-capacitor technique with the monotonic- switching method to reduce power consumption and mitigate the comparator dynamic offset problem [26]. The total capacitance of a Vcm-based DAC is half that of a typical DAC. Therefore, the power consumption of a Vcm-based DAC is almost the same as that of a monotonic-switching DAC. However, an additional common-mode voltage is required for capacitor switching to maintain the comparator input voltage close to the common-mode voltage. The C-2C architecture can reduce power consumption more effectively than the aforementioned architectures [13], [14]. However, because of its large parasitic capacitance, achieving 12-bit performance with the C-2C architecture is challenging. Therefore, the C-2C architecture is typically used for 8–10-bit SAR ADCs.

A few correction schemes have been proposed to correct comparator error decisions and, by extension, to increase the effective bit of number (ENOB) of ADCs. Commonly used correction methods include binary-scaled error compensation [16], [26], [27], the nonbinary search algorithm [19], [28]–[30], and multiple least significant bit (LSB) redundancy [16] and [31]. The binary-scaled error compensation scheme uses a greater number of binary-weighted capacitors in a typical binary-weighted CDAC to obtain redundancy weights for error correction. In addition, the scheme requires an increase in the total DAC capacitance. The nonbinary search algorithm has a built-in correction mechanism to correct the erroneous decisions caused by incomplete DAC switching settling and comparator noise. Nonbinary CDACs have a higher number of redundancy weights than binary CDACs under the same search number. Therefore, nonbinary CDACs can correct a higher number of bit error decisions than binary CDACs. Furthermore, the nonbinary search architecture does not require an increase in the total DAC capacitance. The multiple LSB redundancy technique can correct bit error decisions that have occurred in the last few comparison cycles. However, for multiple LSB switching, the total DAC capacitance should be doubled.

In this study, we designed a prototype of a low-power 12-bit SAR ADC with split-capacitor, nonbinary-weighted, and multiple-LSB-redundant CDACs for IoT applications. The proposed SAR ADC features an 18.39-fJ/ conversion-step Figure-of-Merit (FoM) at a sampling rate of 1 MS/s.

The remainder of this paper is organized as follows. Section II introduces the proposed 12-bit SAR ADC. Section III describes the architecture and key building block implementation. Section IV summarizes the test results, and Section V provides the conclusions.

II. PROPOSED 12-BIT SAR ADC

The split-capacitor, nonbinary search, and multiple LSB redundancy techniques were used to develop the proposed 12-bit SAR ADC. In Section IIA, the search algorithm and architecture of the split-capacitor and nonbinary-weighted CDACs with redundant codes are introduced. The split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DACs are presented in Section IIB.

A. SPLIT-CAPACITOR AND NONBINARY-WEIGHTED CDACs WITH REDUNDANT CODES

CDACs are key components of high-speed, linear, and low-power-consumption SAR ADCs. The use of a nonbinary-weighted CDAC with redundant codes in SAR ADCs has been demonstrated to significantly improve the linearity of A/D conversion. The nonbinary search algorithm has a built-in correction mechanism that prevents bit error decisions due to incomplete DAC switching settling and comparator noise [27], [28]. Fig. 1(a) displays a schematic of a 4-bit nonbinary-weighted CDAC with one redundant code. An additional capacitor C_4 is added to the capacitor array to generate a redundant code. The capacitance ratios of C_4, C_3, C_2, C_1, C_0, and C_D are set to 6, 4, 2, 2, 1, and 1, respectively.

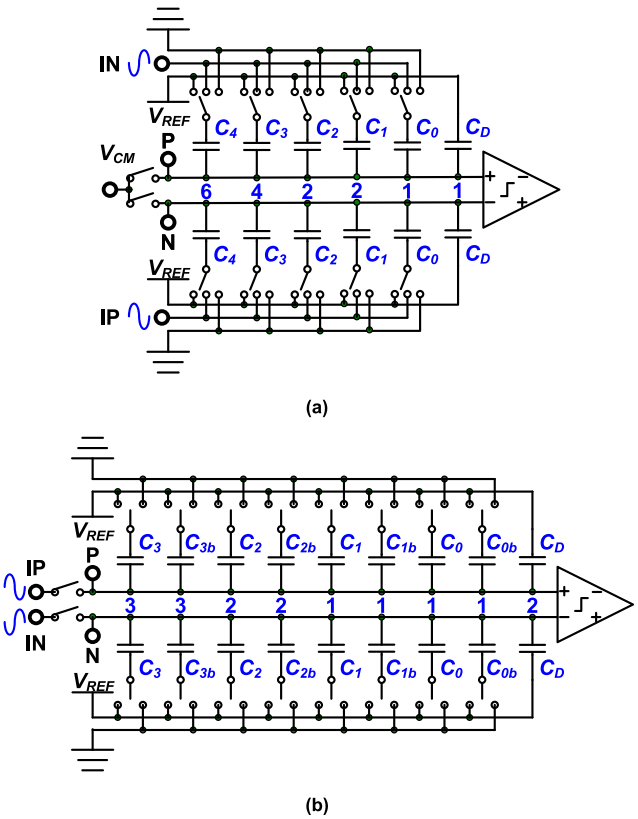


FIGURE 1. (a) Schematic of 4-bit nonbinary-weighted CDACs with one redundant code. (b) Schematic of 4-bit split-capacitor and nonbinary-weighted CDACs with one redundant code.

Because of the redundant code, the SAR ADC requires five search cycles to complete 4-bit A/D conversion. A few weight combinations of the five codes ($b_4b_3b_2b_1b_0$) can generate a correct quantization number. One of the weight arrangements is 6, 4, 2, 2, and 1 for these five codes. Thus, the quantization

number can be obtained from the mathematical operation $6\times b_4+4\times b_3+2\times b_2+2\times b_1+1\times b_0$. The redundant weights are 4, 2, 2, and 0 ($4+2+2+1+1-6=4$, $2+2+1+1-4=2$, $2+1+1-2=2$, and $1+1-2=0$).

The capacitor-splitting architecture of DACs facilitates energy-efficient switching [10]. Each capacitor of a DAC is split into two identical capacitors. During capacitor switching, the capacitor-splitting architecture utilizes charge in a more efficient manner than conventional capacitor arrays. By applying the capacitor-splitting scheme to the nonbinary-weighted CDAC with redundant codes, we ensure that the proposed SAR ADC achieves energy-efficient switching as well as an error bit correction mechanism for high-speed, linear, and low-power A/D conversion. Fig. 1(b) illustrates a schematic of the 4-bit split-capacitor and nonbinary-weighted CDACs with one redundant code. The capacitor C_{i+1} in Fig. 1(a) is split into two identical capacitors C_i and C_{ib}, where i ranges from 0 to 3. Capacitors C_0 and C_D in Fig. 1(a) are combined into one capacitor C_D, as depicted in Fig. 1(b). The capacitance ratios of C_3, C_{3b}, C_2, C_{2b}, C_1, C_{1b}, C_0, C_{0b}, and C_D in Fig. 1(b) are set to 3, 3, 2, 2, 1, 1, 1, 1, and 2, respectively. Although each capacitor is split into two capacitors, the number of codes does not change. The weight arrangement is also 6, 4, 2, 2, and 1 for the five codes, and the redundant weights remain as 4, 2, 2, and 0. Because the nonbinary-weighted DAC has a built-in correction mechanism, Figs. 2(a) and (b)–(d) describe the A/D conversion without error decision and with an error decision, respectively. A voltage equivalent to the quantified number between 8 and 9 but close to 9 is applied to the input of the 4-bit SAR ADC to explain the correction mechanism. Fig. 2(a) displays the A/D conversion without error decision. After five search cycles, the quantization number 9 ($=1\times 6+0\times 4+1\times 2+0\times 2+1\times 1$) is generated.

If an error decision occurs during the first search cycle, as depicted in Fig. 2(b), another digital code combination (01111) may be obtained to generate the correct quantization number of 9 ($=0\times 6+1\times 4+1\times 2+1\times 2+1\times 1$). However, the correction mechanism of the SAR ADC with the nonbinary-weighted DACs does not prevent bit error decisions from occurring in each search cycle, especially over the last few cycles.

For example, Figs. 2(c) and (d) illustrate the occurrence of one error decision in the fourth and the fifth cycles, respectively. For these two cases, quantization numbers of 10 (code: 10110) and 8 (code: 10100), respectively, were obtained after five search cycles.

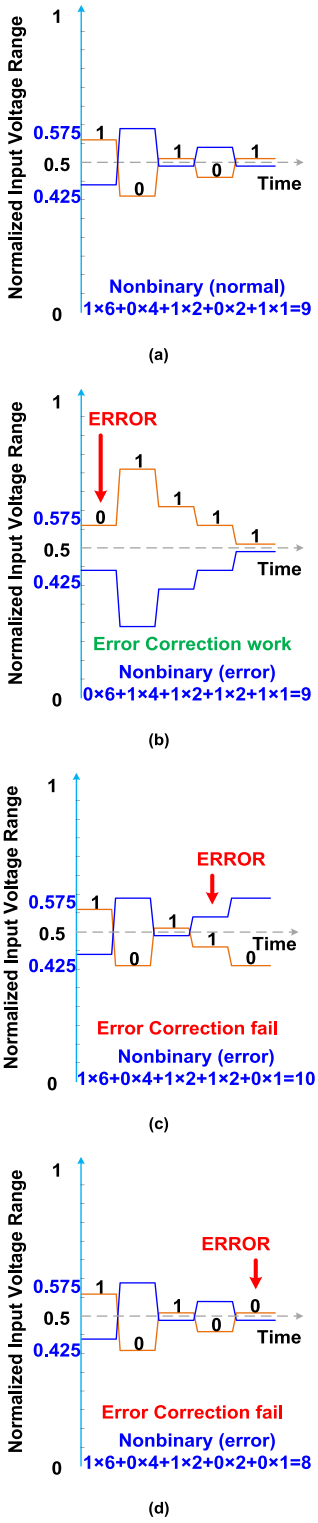


FIGURE 2. Nonbinary search algorithm to explain the correction mechanism (a) without error decision, (b) with an error decision during the first search cycle, (c) with an error decision during the fourth search cycle, and (d) with an error decision during the fifth search cycle.

B. SPLIT-CAPACITOR, NONBINARY-WEIGHTED, AND MULTIPLE-LSB-REDUNDANT DACs

To correct bit error decisions that have occurred over the last few cycles, the multiple LSB redundancy technique is applied to the split-capacitor and nonbinary-weighted CDACs.

Fig. 3 depicts a schematic of the proposed 4-bit split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DAC. The capacitance ratios of C_7 (C_{7b}), C_6 (C_{6b}), C_5 (C_{5b}), C_4 (C_{4b}), C_3 (C_{3b}), C_2 (C_{2b}), C_1 (C_{1b}), C_0 (C_{0b}), and C_D are 4, 3, 2, 1, 1, 1, 1, 1, and 2, respectively. Nine search cycles are required to complete the 4-bit A/D

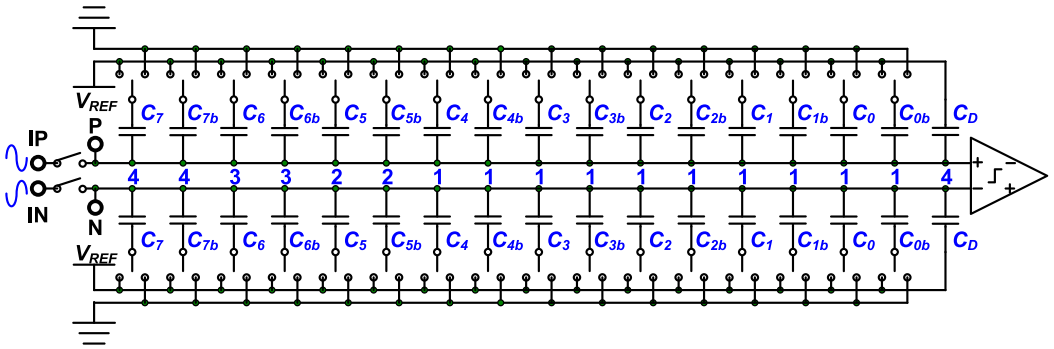


FIGURE 3. Schematic of the proposed 4-bit split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DACs.

conversion. In case of 4-bit quantization, the weight arrangement is 4, 3, 2, 1, 1, 1, 1, 1, and 1 for these nine search cycles. For this arrangement, the redundancy weights are 8, 6, 5, 5, 4, 3, 2, 1, and 0. Nonbinary-weighted and multiple-LSB-redundant DACs have a higher number of redundancy weights than nonbinary-weighted DACs without multiple LSB redundancy. Therefore, a higher number of bit error decisions can be corrected in nonbinary-weighted and multiple-LSB-redundant DACs than in nonbinary-weighted DACs without multiple LSB redundancy. Figs. 4(a)–(d) illustrate the nonbinary search algorithm to explain the correction mechanism with no decision error, error decision during the first search cycle, error decision during the third search cycle, and error decision during the seventh search cycle, respectively. All decision errors can be corrected. In the cases illustrated in Figs. 4(b)–(d), the input voltages were correctly quantized with the codes of 011110101 ($0\times4+1\times3+1\times2+1\times1+1\times1+0\times1+1\times1+0\times1+1\times1=9$), 100111101($1\times4+0\times3+0\times2+1\times1+1\times1+1\times1+1\times1+0\times1+1\times1=9$), and101010011($1\times4+0\times3+1\times2+0\times1+1\times1+0\times1+0\times1+1\times1+1\times1=9$), respectively. Fig. 4 verifies the effectiveness of the proposed split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DACs in terms of error decision correction.

The conventional ADC with non-binary coding and redundancy techniques, and the proposed ADC have been simulated for an input frequency of 100 kHz at a sampling rate of 1 MS/s, and a Gaussian noise model was introduced at the input of each comparator for simulation. Fig. 5(a) and (b) show the simulated output spectra of the conventional 12-bit ADC with non-binary coding and redundancy techniques, and the proposed 12-bit ADC under the condition of a noise value of 1.5 LSB and a DAC switching settling ratio of 99%. The ENOB of the conventional ADC is 10.45 bits, while the proposed ADC exhibits an ENOB of 11.05 bits. From the comparison of the simulated ADC output spectra, conventional ADCs with non-binary encoding and redundancy techniques are sensitivity to noise and incomplete DAC switching. However, the proposed ADC is immune to the noisy disturbance and incomplete DAC switching condition.

TABLE 1. Comparison of capacitor ratios and redundancies for different nonbinary-weighted schemes.

Item	This work		[16]		[28]		[9]	
Bit	W	R	W	R	W	R	W	R
b_{19}	1680	736	2048	278	1768	560	2048	0
b_{18}	1040	336	1024	278	1006	316	1024	0
b_{17}	592	192	512	278	572	178	512	0
b_{16}	336	112	256	278	324	102	256	0
b_{15}	192	64	256	22	184	58	128	0
b_{14}	112	32	128	22	104	34	64	0
b_{13}	64	16	64	22	60	18	32	0
b_{12}	32	16	32	22	34	10	16	0
b_{11}	16	16	16	22	20	4	8	0
b_{10}	11	10	16	6	10	4	4	0
b_9	7	7	8	6	6	2	2	0
b_8	4	6	4	6	4	0	1	0
b_7	2	6	2	6	2	0	-	-
b_6	1	6	1	6	1	0	-	-
b_5	1	5	1	5	-	-	-	-
b_4	1	4	1	4	-	-	-	-
b_3	1	3	1	3	-	-	-	-
b_2	1	2	1	2	-	-	-	-
b_1	1	1	1	1	-	-	-	-
b_0	1	0	1	0	1	0	1	0

W: Weight; R: Redundancy

The proposed 4-bit split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DAC can accordingly be extended to a 12-bit CDAC, as illustrated in Fig. 6. The capacitor ratios are highlighted on the circuit. Table 1 presents a comparison of the capacitor ratios and redundancies for different schemes. In [16], a 16-bit SAR ADC with binary-weighted and multiple-LSB-redundant DACs was described, whereas in [28], a 10-bit SAR ADC with nonbinary-weighted redundant DACs was described. And in [9], a conventional 10-bit SAR ADC was described. To compare the capacitor ratios and redundancies for different schemes, all SAR ADCs in Table 1 were designed to have a 12-bit resolution. Compared with the aforementioned two schemes, the proposed split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DAC had a higher number of redundancy weights and could correct higher numbers of bit error decisions.

To compare the mechanisms of various SAR ADC architectures for correcting the bit error decisions due

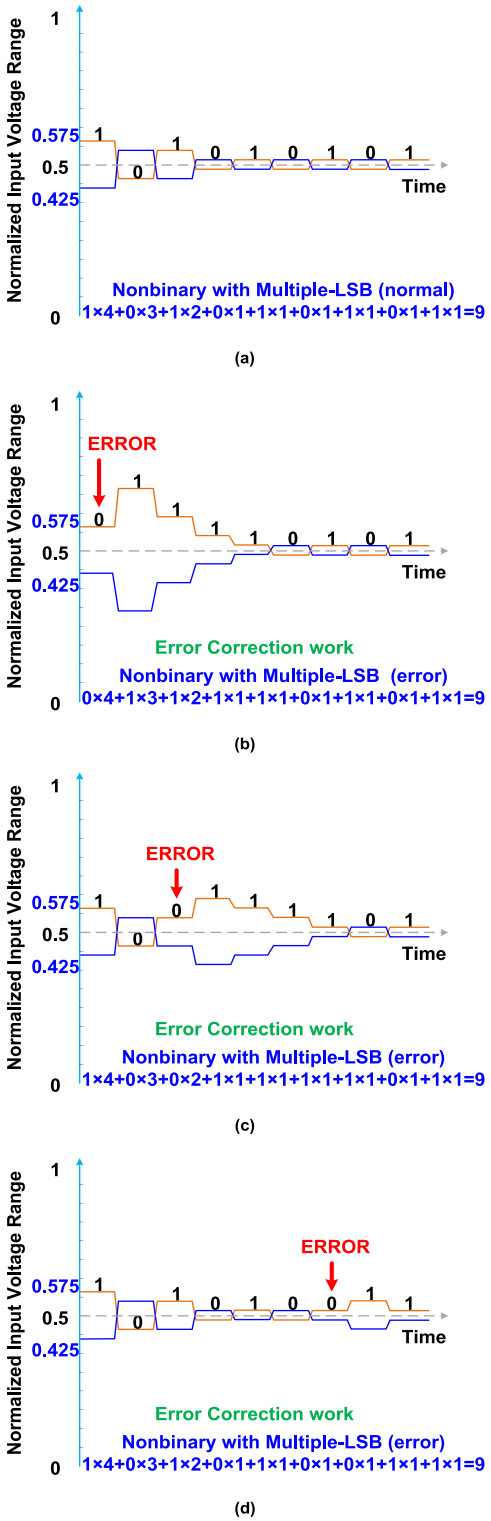


FIGURE 4. Nonbinary search algorithm to explain the correction mechanism for (a) no error decision, (b) an error decision during the first search cycle, (c) an error decision during the third search cycle, and (d) an error decision during the seventh search cycle.

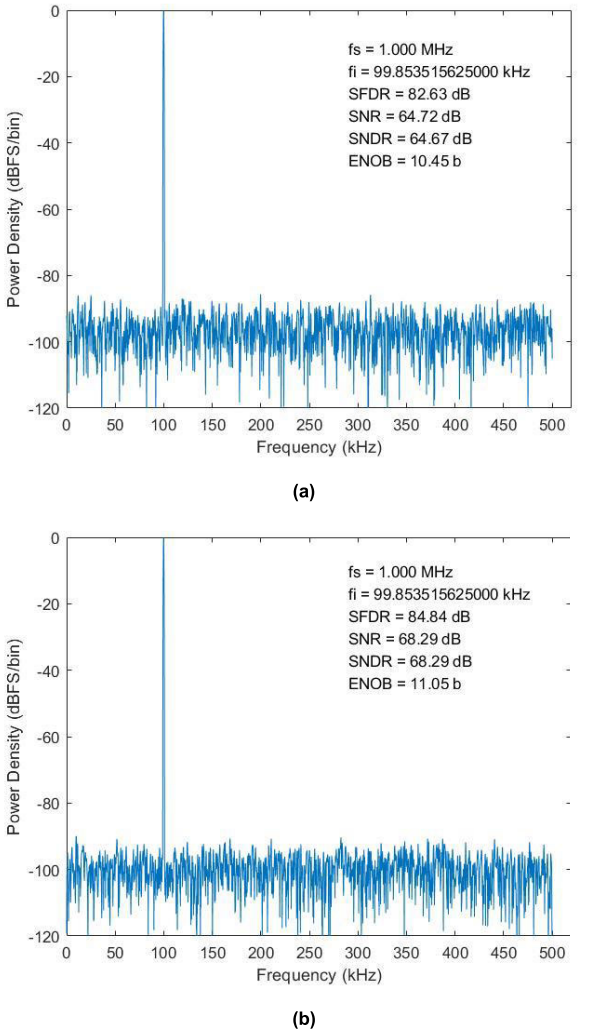


FIGURE 5. Simulated output spectra of (a) conventional 12-bit ADC with non-binary coding and redundancy techniques, and (b) proposed 12-bit ADC with a noise value of 1.5 LSB at a DAC switching settling ratio of 99% for input frequency of 100 kHz at a sampling rate of 1 MS/s.

to comparator noise and incomplete DAC switching settling, the proposed SAR ADC, a conventional SAR ADC with binary-weighted DACs [9], an SAR ADC with binary-weighted and multiple-LSB-redundant DACs [16], and an SAR ADC with nonbinary-weighted redundant DACs [28] were simulated. These different SAR ADC architectures were designed to have a 12-bit resolution, and the CDACs of these SAR ADCs were designed to have the same size. A Gaussian noise model was introduced at the input of each comparator for simulation. Fig. 7 shows the simulated ENOB values of the five SAR ADCs versus noise. The input frequency and sampling rate were 100 kHz and 1 MS/s, respectively. The ENOB values of all ADCs were almost identical for noise values smaller than 0.5 LSB.

However, the ENOB values of the conventional ADC [9] and the SAR ADCs described in [28] and [31] decreased when the noise was greater than 0.5 LSB. For example, for the noise value of 1 LSB, the ENOB values of [9], [28], and [31] are 11.01, 11.04, and 11.10 bits, respectively, and the ENOB values of [16] and the proposed SAR ADC are 11.30 and 11.32 bits, respectively. The proposed SAR ADC and the one

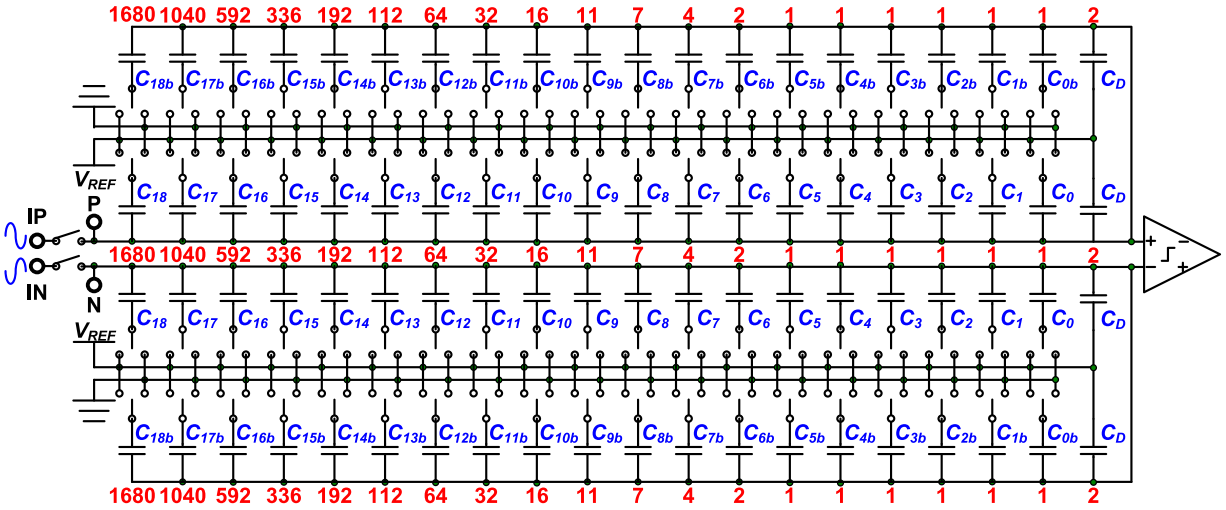


FIGURE 6. Schematic of the proposed 12-bit split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DACs.

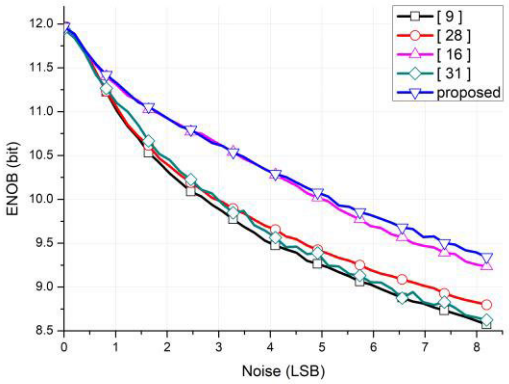


FIGURE 7. Plot of the simulated ENOB values versus noise for the proposed SAR ADC, a conventional SAR ADC with binary-weighted DACs [9], a SAR ADC with binary-weighted and multiple-LSB-redundant DACs [16], a SAR ADC with nonbinary-weighted redundant DACs [28], and a SAR ADC with one-LSB-redundant DACs [31].

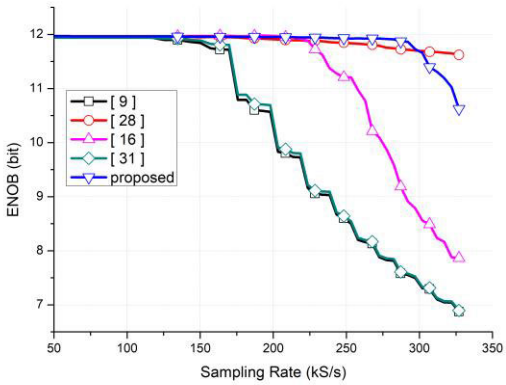


FIGURE 8. Simulated ENOB versus the sampling rate for the proposed SAR ADC, a conventional SAR ADC with binary-weighted DACs [9], a SAR ADC with binary-weighted and multiple-LSB-redundant DACs [16], a SAR ADC with nonbinary-weighted redundant DACs [28], and a SAR ADC with one-LSB-redundant DACs [31].

described in [16] were better in terms of noise immunity. The proposed SAR ADC and the one described in [16] employ multiple LSB redundancy, whereas the conventional ADC and the SAR ADCs described in [28] and [31] do not use the multiple LSB redundancy technique. Therefore, the proposed SAR ADC and the one described in [16] exhibited better performance in terms of noise immunity.

Moreover, the noise immunity of the proposed SAR ADC was better to that of the one described in [16] when the noise value was greater than 4 LSB. Fig. 8 displays the plot of the simulated ENOB values versus the sampling rate for these five ADCs. The ENOB of the conventional SAR ADC and the SAR ADC described in [31] decreased as the sampling rate increased from 175 kS/s. For the sampling rate of 200kS/s, the ENOB values of [9] and [31] are 9.83 and 9.91 LSB, respectively, and the ENOB values of [28], [16], and the proposed ADC are 11.91, 11.97, and 11.95 LSB, respectively. Because the proposed SAR ADC and the one described in [28] employ nonbinary-weighted redundant DACs, they have the mechanisms for correcting the bit error decisions caused by incomplete DAC switching settling. The proposed SAR ADC employs nonbinary-weighted and multiple-LSB-redundant DACs. Even when the sampling rate increased to 320 kS/s, the ENOB of the proposed SAR ADC was higher than 11 bits. In summary, among the SAR ADCs compared in this study, the proposed SAR ADC exhibited the optimal mechanism for correcting the bit error decisions caused by noise and incomplete DAC switching settling.

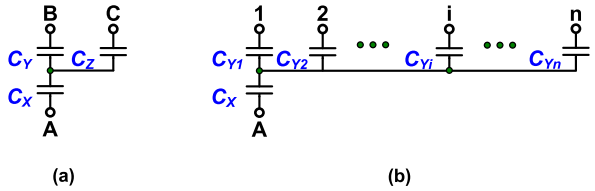
To reduce the total capacitance, all capacitor values of the 12-bit DAC were divided by 16. Table 2 lists the capacitor ratios of the 12-bit split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DAC, where the capacitor values of C'0–C'9 and CD are not integers.

A parallel-series capacitor scheme [15] was used to implement these noninteger capacitors in the present work.

TABLE 2. Capacitor ratios of the 12-bit split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DACs.

Cap. No.	Cap. size	Non-integer Cap. size
C_{18}	1680	105
C_{17}	1040	65
C_{16}	592	37
C_{15}	336	21
C_{14}	192	12
C_{13}	112	7
C_{12}	64	4
C_{11}	32	2
C_{10}	16	1
C_9	11	11/16
C_8	7	4/16 + 3/16
C_7	4	4/16
C_6	2	2/16
C_5	1	1/16
C_4	1	1/16
C_3	1	1/16
C_2	1	1/16
C_1	1	1/16
C_0	1	1/16
C_D	2	2/16

Cap.: capacitor



(a) (b)

FIGURE 9. Noninteger capacitors implemented by (a) three integer capacitors connected in parallel and in series or (b) multiple integrator capacitors connected in parallel and in series.

Noninteger capacitors can be implemented by using three integer capacitors connected in parallel and in series, as displayed in Fig. 9(a). The capacitance between Node A and Node B can be implemented using capacitors C_X, C_Y, and C_Z, and it can be expressed as follows:

$$C_{AB} = \frac{C_X \cdot (C_Y + C_Z)}{C_X + (C_Y + C_Z)} \times \frac{C_Y}{C_Y + C_Z} = \frac{C_X C_Y}{C_X + C_Y + C_Z} \quad (1)$$

For example, a capacitance of 11/16 units can be achieved by setting the capacitances of C_X, C_Y, and C_Z as 1, 11, and 4 units, respectively. The parallel-series capacitor scheme can be extended to a multiparallel-series capacitor scheme, as illustrated in Fig. 9(b). The capacitance between Node A and Node i can be expressed as follows:

$$C_{Ai} = \frac{C_X C_i}{C_X + \sum_{i=1}^{n} C_{Yi}} \quad (2)$$

Fig. 10 illustrates the use of the parallel-series capacitor scheme in the 12-bit split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DAC. The capacitor values are listed in Table 2. The capacitor C_9 was implemented using three capacitors, namely C'_{S1}, C'_{S2}, and C'_{S3}. The capacitance of C_9 was 11/16 units. This value was achieved by setting the capacitances of C'_{S1}, C'_{S2}, and C'_{S3} to 1, 11, and 4 units, respectively. The capacitance of C_8 was 7/16 units, which can be divided between two equivalent capacitors connected in parallel. According to Eq. (1), C'_{S1}, C'_{S2}, and C'_{S3} form a capacitance of 4/16 units for the first equivalent capacitor of C_8. According to Eq. (2), C'_{S4}, C'_{S5}, and C'_0–C'_7 form a capacitance of 3/16 units for the second equivalent capacitor of C_8. Capacitors C_0–C_7 can also be implemented using C'_{S4}, C'_{S5}, and C'_0–C'_7. The capacitor C_D (4/16 units) was implemented by connecting four unit capacitors in series.

C. REDUCING DAC WEIGHT MISMATCH AND PARASITIC EFFECT

To reduce the overall CDAC area without losing the advantages of multiple-LSB redundancy and non-binary-weighted redundancy technology, a non-integer capacitor technology was used, and the capacitor sizes were designed to a specific ratio. If a coupling capacitor is placed in the middle of a non-binary weighted capacitor array, the capacitor's weight will shift, resulting in capacitor mismatch.

Therefore, the capacitors placed after the coupling capacitor must be fine-tuned so that their capacitor weights match to the weight ratios required for both non-binary-weighted and multiple-LSB-redundant techniques. The improvement of the proposed non-integer capacitor technology over conventional non-integer capacitor technologies is discussed in Appendix.

III. ARCHITECTURE AND IMPLEMENTATION OF KEY BUILDING BLOCKS

Fig. 11 displays the architecture of the proposed 12-bit SAR ADC comprising a pair of bootstrapped switch circuits, CDAC, clock generator, comparator, and nonbinary-to-binary converter. The pair of bootstrapped switch circuits is used to sample and track differential input signals. The sampled voltages are stored on the CDAC. The comparator compares the sampled signals with the reference voltages generated by the CDAC and then quantizes the sampled signals. The CDAC comprises 19 switched-capacitor circuits (SCCs) and eight dummy capacitors (C'_D). The clock generator generates control signals for the CDAC and comparator for A/D conversion. Because the comparator outputs nonbinary codes (b_0–b_{19}), the nonbinary-to-binary converter converts the nonbinary codes into binary codes (d_0 –d_{11}).

The standard deviations of MOM (metal–oxide–metal) and MIM (metal-insulator-metal) capacitors are 0.652% and 0.105%, respectively [32]. The minimum capacitance of PDK provided by the foundry is 20 fF. Therefore, the CDAC includes a 20-fF MIM unit capacitor, resulting in a total capacitance of 10.24 pF for each side of the CDAC.

The sample-and-tracking circuit is one of the key analog building blocks associated with high-linearity A/D conversion in SAR ADCs. A bootstrapped switch circuit is typically used as the sample-and-tracking circuit to achieve high-linearity sampling [11], [33], [34]. The comparator is another key analog building block associated

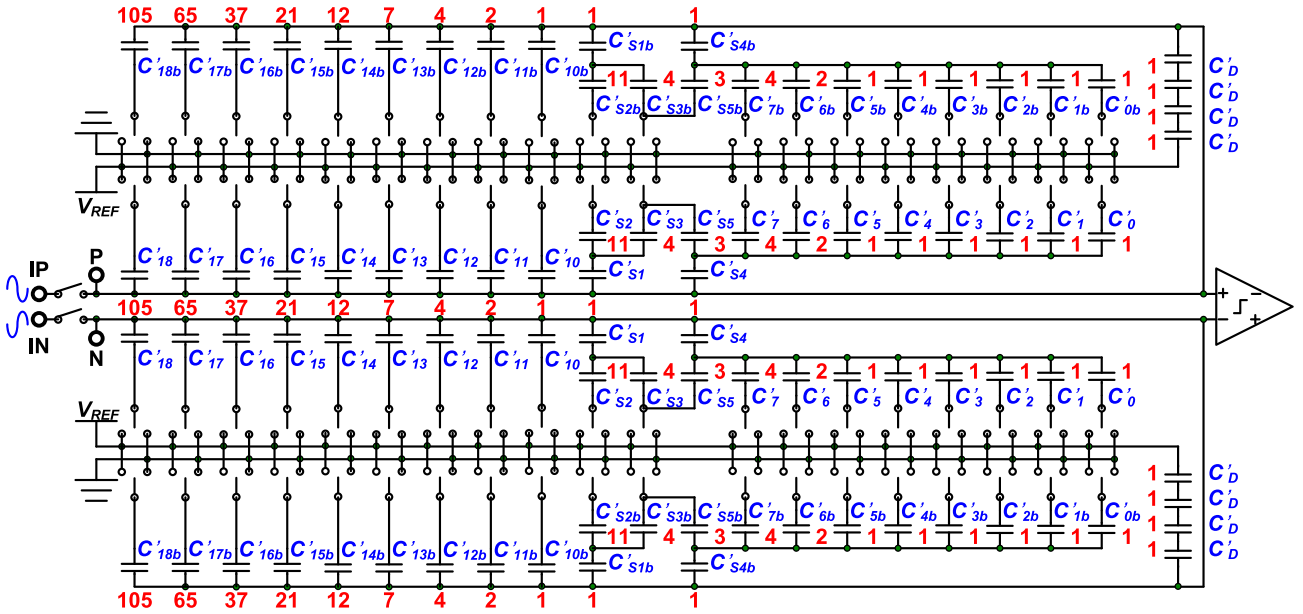


FIGURE 10. Proposed 12-bit split-capacitor, nonbinary-weighted, and multiple-LSB-redundant DACs with parallel-series capacitor implementation.

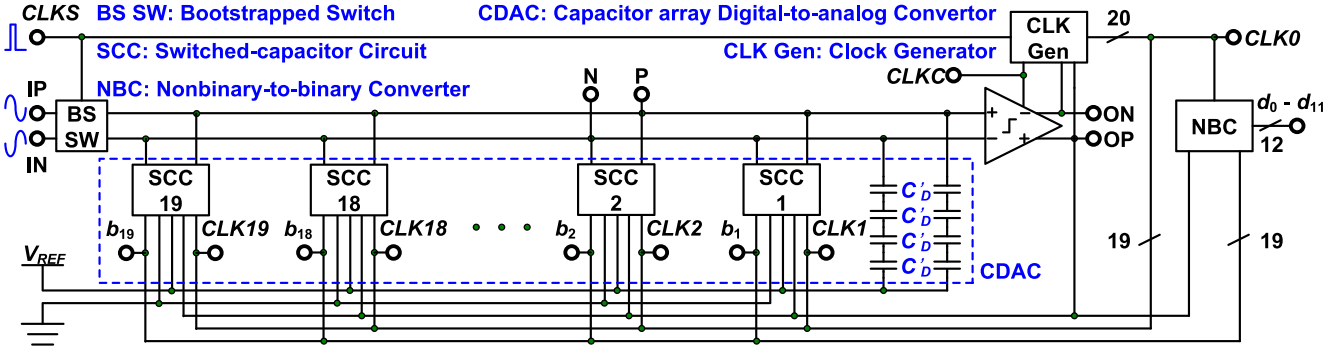


FIGURE 11. Architecture of the proposed 12-bit SAR ADC.

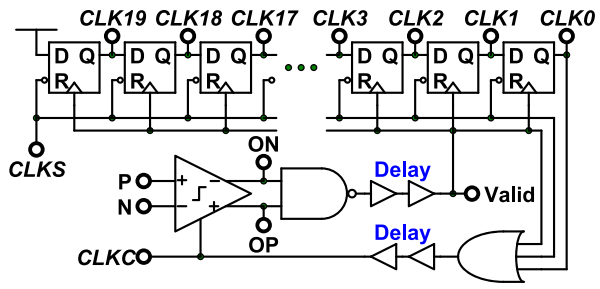


FIGURE 12. Asynchronous control circuit used to generate the clock control signals (CLK0–CLK 19) for switching the capacitor array.

with high-linearity A/D conversion. To reduce disturbance from the kickback noise, we used a two-stage comparator [35], [36]. In order to reduce the long conversion time required in the last few LSB bits due to the metastability, the resolution of the comparator operating on a 200-MHz clock is less than 1/8 LSB.

An asynchronous control circuit (Fig. 12) was used to generate the clock control signals, *CLK0* to *CLK 19*, for switching the capacitor array and a signal *CLKC* for controlling the comparator. A 38% duty cycle of *CLKS* was used to sample the input signals.

Figs. 13(a) and (b) depict the CDAC operation flowchart and the switched-capacitor circuit, respectively [15]. The bottom plates of C'_{i-1} are connected to the ground or the reference voltage V_{REF} by switching transistors $M_{3,i}$ and $M_{4,i}$ as well as $M_{7,i}$ and $M_{8,i}$, whereas the bottom plates of $C'_{(i-1)b}$ are controlled by $M_{1,i}$, $M_{2,i}$, $M_{5,i}$, and $M_{6,i}$. The SAR ADC executes one sampling cycle and 19 capacitor switching cycles for generating 20-bit nonbinary data. During the sampling phase, the sampling signal of *CLKS* is "high," and the signals *CLK0–CLK19* are "low." Multiplexers 1 and 2 output high and low voltages, respectively, to turn off transistors $M_{1,i}$, $M_{3,i}$, $M_{5,i}$, and $M_{7,i}$ and turn on transistors $M_{2,i}$, $M_{4,i}$, $M_{6,i}$, and $M_{8,i}$ of all the SCCs. The bottom plates of C'_i are connected to V_{REF}, and the bottom plates of C'_{ib} are connected to the ground. The differential voltages are sampled on the top plates of the capacitor array. Then, the comparator compares the voltages on these two top plates (V_p and V_n). If V_p is higher than V_n, the output nonbinary Most Significant Bit

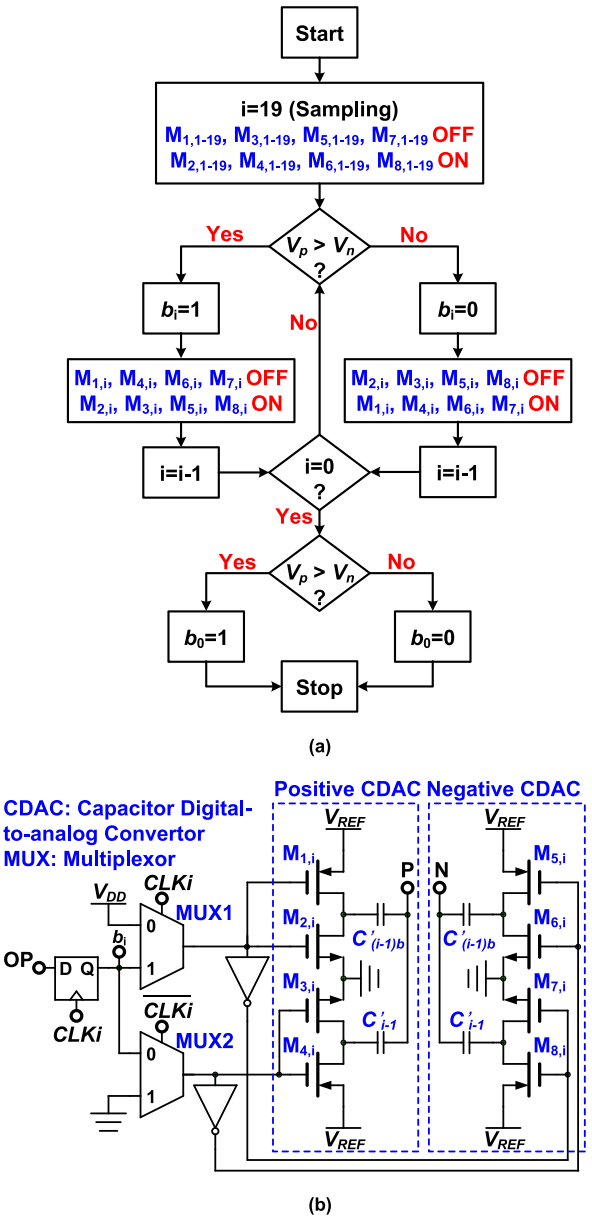


FIGURE 13. (a) Flowchart of CDAC operation and (b) the switched-capacitor circuit.

(MSB) b_{19} is "1." A valid signal generated by the comparator triggers the asynchronous control circuit (Fig. 12). Then, *CLK19* is "high." *CLK19* and b_{19} are connected to SCC 19. Both multiplexers output a high voltage to turn off transistors $M_{1,i}$, $M_{4,i}$, $M_{6,i}$, and $M_{7,i}$ and turn on $M_{2,i}$, $M_{3,i}$, $M_{5,i}$, and $M_{8,i}$ of SCC 19. The bottom plates of C'_{18} and C'_{18b} of the positive CDAC are connected to the ground, and the bottom plates of C'_{18} and C'_{18b} of the negative CDAC are connected to V_{REF}. For the first comparison, if V_p is smaller than V_n, the output nonbinary MSB b_{19} is "0." The connection of the capacitors is reversed. The bottom plates of C'_{18} and C'_{18b} of the positive CDAC are connected to V_{REF}, and the bottom plates of C'_{18} and C'_{18b} of the negative CDAC are connected to the ground. The capacitor switching cycles are repeated 19 times. After the 19th capacitor switching cycle, the comparator compares the 20th comparisons and outputs the nonbinary LSB b_0.

We designed a nonbinary-to-binary converter to convert 20-bit nonbinary codes (b_0–b_{19}) to 12-bit binary codes (d_0–d_{11}) (Table 1). The codes b_0–b_8 and b_{11}–b_{13} are binary, and the other codes are nonbinary. The 12-bit binary code can be obtained by decomposing a nonbinary code into several binary codes and summing all the binary codes. For example, the nonbinary code b_9 weighted to 7 can be decomposed into the binary codes 4, 2, and 1. Moreover, the nonbinary code b_{10} weighted to 11 can be decomposed into the binary codes 8, 2, and 1. The other nonbinary codes can be decomposed into several binary codes accordingly. Table 3 presents the decomposition results of the nonbinary codes. The final 12-bit binary codes (d_0–d_{11}) are obtained by summing the binary codes having the same weights.

For example, the code d_0 is obtained by summing b_0–b_6, b_9, and b_{10} from a summing circuit. The summing circuit outputs a sum (d_0) and three carriers (c_{01}, c_{02}, and c_{03}). The weights of c_{01}, c_{02}, and c_{03} are 2, 4, and 8, respectively. The code d_1 is obtained by summing b_7, b_9, b_{10}, and c_{01} from another summing circuit. This summing circuit outputs a sum (d_1) and two carriers (c_{11} and c_{12}). The weights of c_{11} and c_{12} are 4 and 8, respectively. The other codes d_2–d_{11} can be obtained accordingly. As presented in Table 3, the nonbinary-to-binary converter was designed with 11 multiple-input summing circuits and an OR gate [Fig. 14(a)]. Each summing circuit generates the corresponding digital output code and carriers. We constructed the multiple-input summing circuit with several full adders and half adders. Fig. 14(b) depicts a schematic of the nine-input summing circuit. This nine-input summing circuit outputs the sum (d_0) and the carriers (c_{01}, c_{02}, and c_{03}) by summing b_0–b_6, b_9, and b_{10}. Other summing circuits with different numbers of inputs can be designed accordingly.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

By using 0.18-μm 1P6M complementary MOS (CMOS) technology, we fabricated a prototype to validate the performance of the proposed 12-bit SAR ADC. Fig. 15 displays the photograph of a die with an ADC core area of 712 μm $\times$ 516 μm. The prototype ADC was tested under a sampling rate of 1 MS/s and a supply voltage of 0.95 V for digital circuits and 1.4 V for analog circuits. An external 1-V reference voltage was provided to the chip. Fig. 16 shows the power distribution of the proposed 12-bit SAR ADC. This 1-V reference voltage was stabilized by a 56-pF on-chip capacitor and three off-chip capacitors (100 pF, 10 nF, and 1 μF). Differential input signals were provided from a signal generator with band-pass filters. A pair of sinusoidal differential signals with a peak-to-peak amplitude of 2 V and frequencies 200 and 500 kHz was applied to the input terminals of the ADC chip to test its linear performance. Fig. 17 depicts the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the 12-bit SAR ADC. The maximal

TABLE 3. Conversion scheme of the nonbinary-to-binary converter.

Carry		c_{92}	c_{91}	c_{72}	c_{62}	c_{43}	c_{42}	c_{32}	c_{22}	c_{03}	c_{02}	c_{01}	
		c_{A1}		c_{81}	c_{71}	c_{52}	c_{51}	c_{41}	c_{31}	c_{12}	c_{11}		
						c_{61}				c_{21}			
1680	b_{19}		b_{19}	b_{19}		b_{19}			b_{19}				
1040	b_{18}	carry	b_{18}						b_{18}				
592	b_{17}			b_{17}			b_{17}		b_{17}				
336	b_{16}				b_{16}		b_{16}		b_{16}				carry
192	b_{15}					b_{15}	b_{15}						
112	b_{14}						b_{14}	b_{14}	b_{14}				
64	b_{13}						b_{13}						
32	b_{12}		sum					b_{12}					
16	b_{11}								b_{11}				
11	b_{10}									b_{10}		b_{10}	b_{10}
7	b_9										b_9	b_9	b_9
4	b_8										b_8		
2	b_7											b_7	
1	b_6												b_6
⋮	⋮												⋮
1	b_0												sum b_0
	Code	d_{11}	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0
Weight		2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 4. Performance summary of the proposed SAR ADC, [7], [16], [21], [29], and [35]–[39].

	This work	JSSC' 18 [37]	TCAS I' 18 [38]	TCAS I' 18 [39]	JSSC' 11 [29]	JSSC' 14 [21]	Access 18 [7]	JSSC' 07 [41]	VLSI s.' 17 [16]	Access 19 [40]
Resolution (bit)	12								16	18
Technology (nm)	180	40	40	180	130	180	130	180	55	130
Supply Voltage (V)	1.4	0.9	0.9	1.8	1.2	3.3	0.6	1.0	1.2	1.2
Sampling Rate (MS/s)	1	270	10	20	22.5	0.411	0.01	0.1	16	0.25
DNL (LSB)	0.54	0.81	0.5	0.51	-	0.83	-	0.66	-	0.76
INL (LSB)	0.89	1.1	0.6	1.01	-	1.62	-	0.68	2.3	0.94
ENOB (bit) @Nyquist	11.25	9.62	10.89	10.44	11.35	10.5	11.77	10.55	12.66	14.4
Power Cons. (μW)	44.78	4500	410	1770	3020	56	0.96	25	16300	5230
Area (mm^2)	0.367	0.074	0.041	1.61	0.059	0.013	0.126	0.63	0.55	4
Unit Cap. (fF)	20	5	0.6	16	0.88	1.5	51	-	7.75	1200
Total Cap. (pF)	10.24	1.3	1.2	16.4	3.6	0.096	6.681	-	1	76.8
FoM (fJ/conv.-step)	18.39	21.1	21.6	63.7	51.3	94	28	166.75	157.41	967.68
FoM(dB)	169.99	164.47	168.2	162.12	165.81	160.64	169.77	158.31	165	161.98

DNL and INL were measured as −0.4/0.54 and −0.81/0.89 LSB, respectively, with 1 LSB = 0.488 mV. The INL profile exhibited several points of discontinuity. This discontinuity was analyzed and is described in the following paragraph. Fig. 18 (a) illustrates the measured ADC output spectrum for an input frequency of 200 kHz and a sampling rate of 1 MS/s.

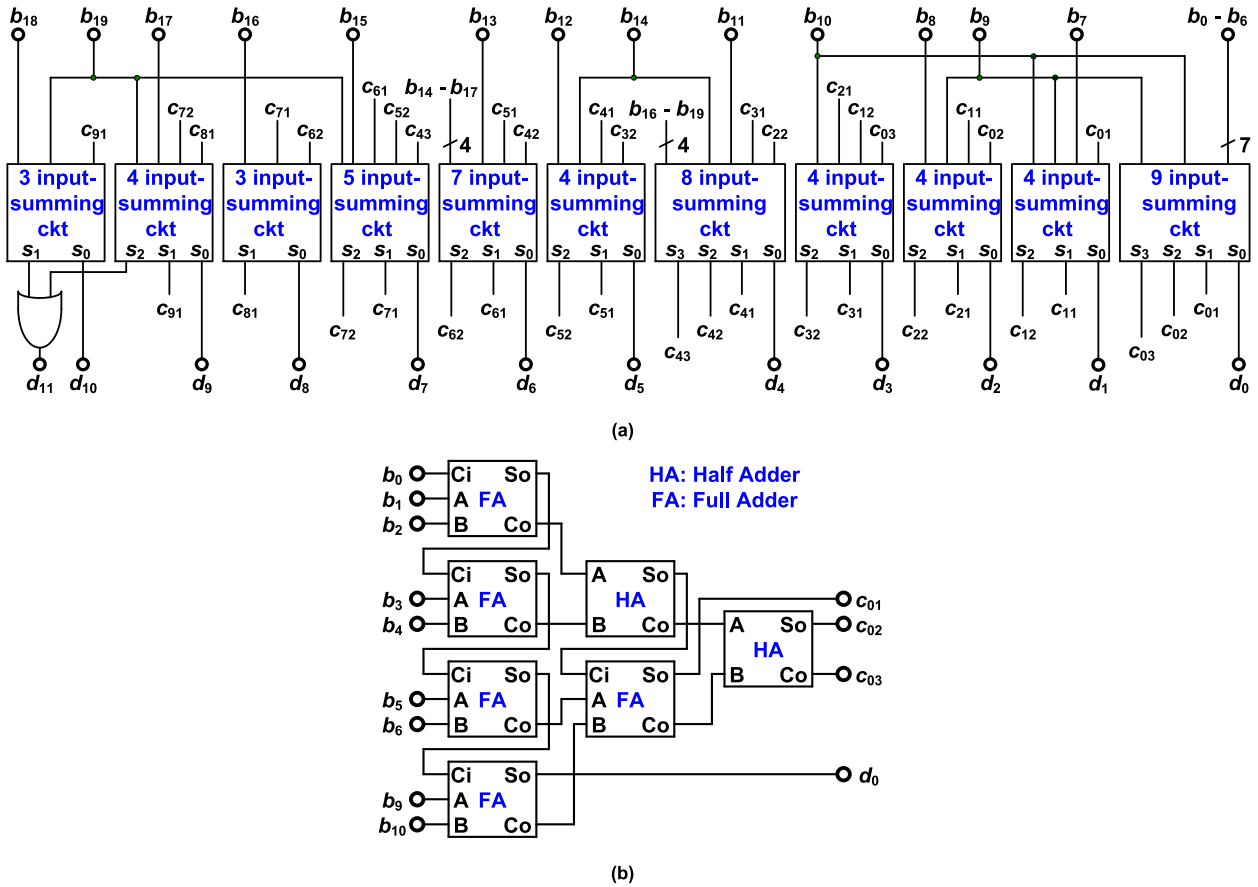


FIGURE 14. (a) Nonbinary-to-binary converter. (b) Schematic of the nine-input summing circuit.

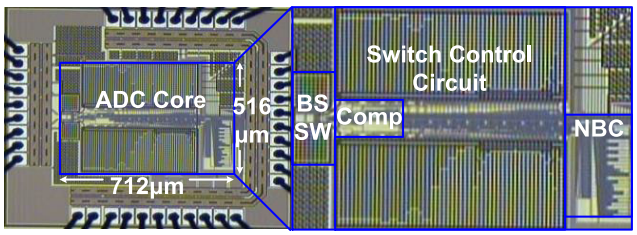


FIGURE 15. Die photograph of the proposed 12-bit SAR ADC.

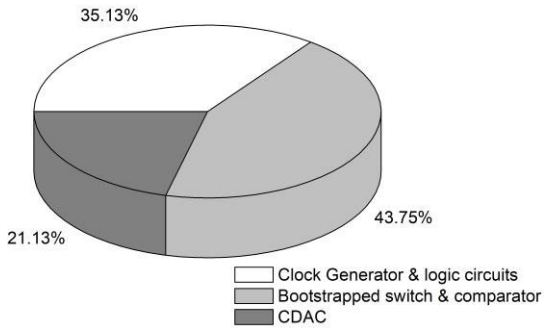


FIGURE 16. Power distribution of the proposed 12-bit SAR ADC.

The spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR), and signal-to-noise-and-distortion ratio (SNDR) at 200 kHz were 83.88, 69.51, and 69.44 dB, respectively. The resultant ENOB was 11.24 bits.

When the input frequency was increased to the Nyquist frequency, the proposed ADC maintained good dynamic performance. Fig. 18(b) shows the measured ADC output spectrum for an input frequency of 500 kHz and a sampling rate of 1 MS/s. At 500 kHz, the SFDR, SNR, and SNDR were 84.95, 69.51, and 69.51 dB, respectively, and the ENOB was 11.25 bits. Compare with the simulation result shown in Fig. 8, the measurement results show better ENOB performance at sampling rate of 1 MS/s. This is because the total capacitance of the CDAC used for the implemented SAR ADC is reduced by 8 times the total capacitance of the CDAC used for the simulation of Fig. 8.

Incomplete capacitor DAC switching settling, noise, and CDAC mismatch are the three main factors affecting the performance of A/D conversion. To demonstrate the error bit correction mechanism of the proposed SAR ADC and understand how these three factors affect the measured ADC performance, the proposed 12-bit SAR

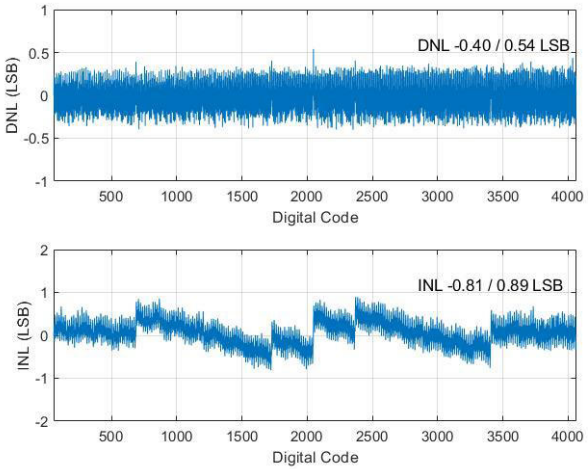
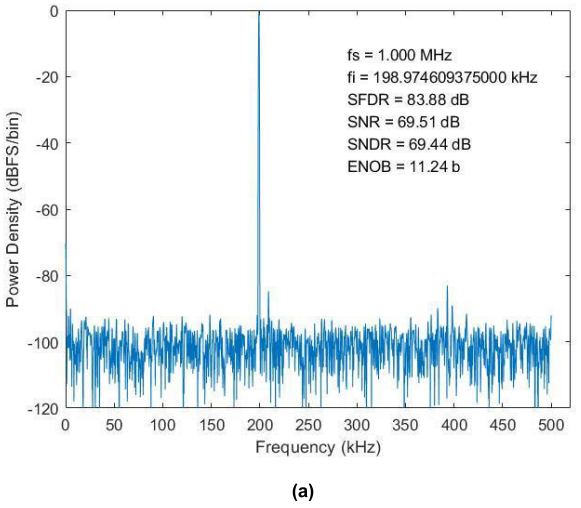
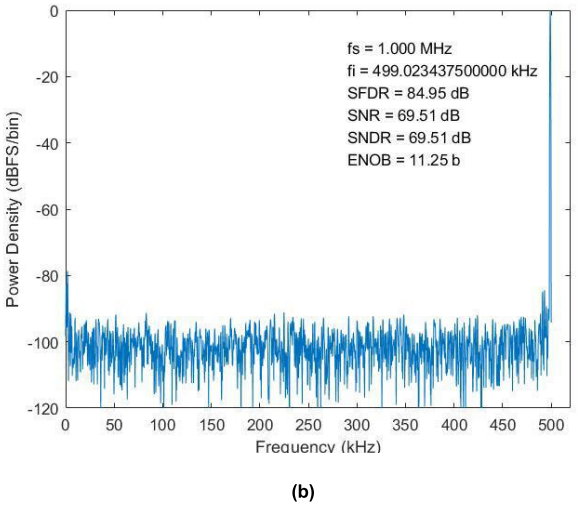


FIGURE 17. Measured DNL and INL of the proposed 12-bit SAR ADC.



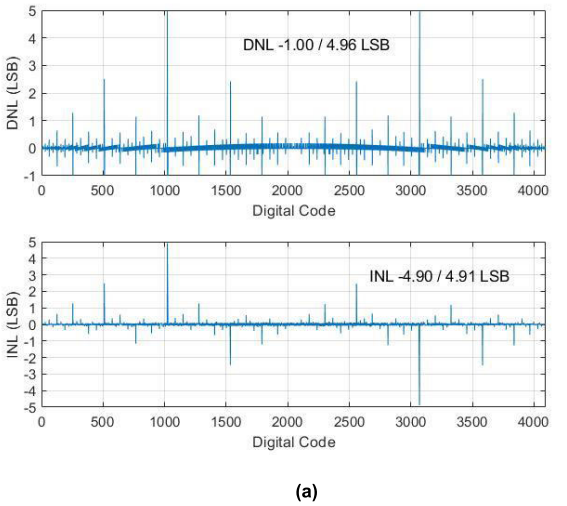
(a)



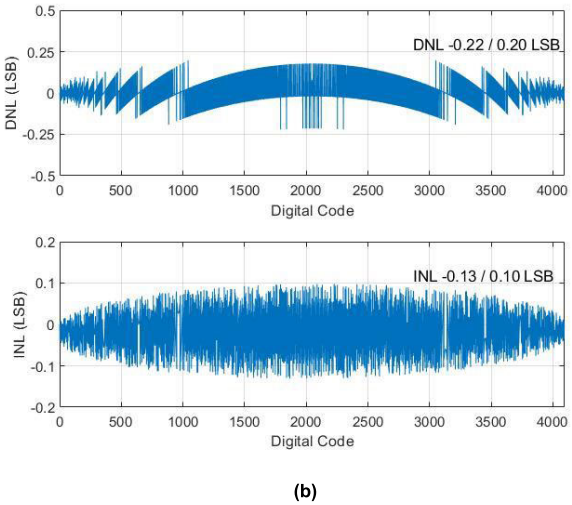
(b)

FIGURE 18. Measured ADC output spectra for input frequencies of (a) 200 and (b) 500 kHz at a sampling rate of 1 MS/s.

ADC and conventional 12-bit SAR ADC were simulated in the MATLAB software environment (MathWorks, MA, USA) by using the incomplete DAC switching settling and



(a)



(b)

FIGURE 19. Simulated DNL and INL of the (a) conventional 12-bit SAR ADC and (b) proposed 12-bit SAR ADC at a DAC switching settling ratio of 99.52 and 96.6%.

noise models. The conventional 12-bit SAR ADC was an ADC circuit with a fundamental binary search algorithm. Figs. 19 (a) and (b) display the simulated DNL and INL of the conventional SAR ADC under a conversion time of 63.7 time constants, which is equivalent to a DAC switching settling ratio of 99.52% and proposed 12-bit SAR ADC, respectively, at a DAC switching settling ratio of 96.6%. The maximal DNL and INL of the conventional SAR ADC were −1.00/4.96 and −4.90/4.91 LSB, respectively. The linearity of the conventional 12-bit SAR ADC was severely affected when DAC switching was incomplete. The proposed SAR ADC exhibited a good capability for correcting the bit error decisions due to incomplete DAC switching settling. Even when the settling ratio decreased to 96.6%, the proposed SAR ADC exhibited good performance with a maximal DNL of −0.22/0.20 LSB and a maximal INL of −0.13/0.10 LSB. A Gaussian-distributed noise model with a standard deviation of 4 LSB was applied to the input of the comparator of the conventional and proposed SAR ADCs.

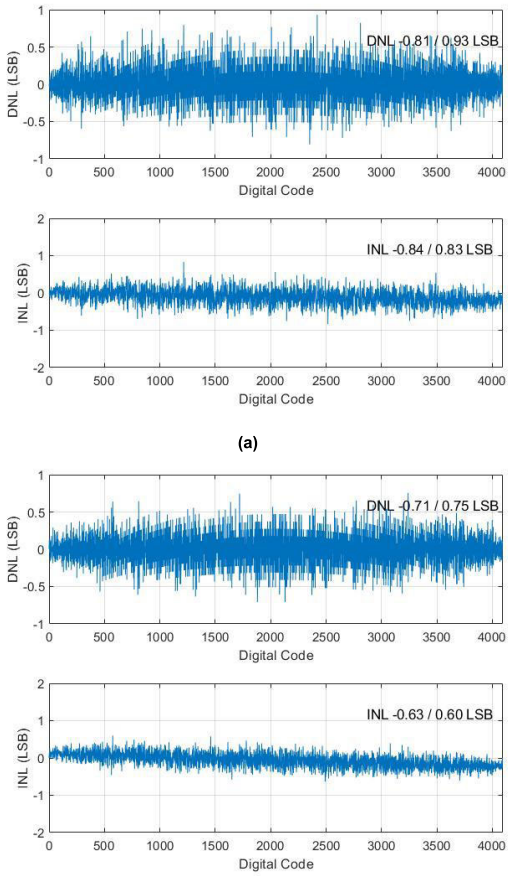


FIGURE 20. Simulated DNL and INL of the (a) conventional 12-bit SAR ADC and (b) proposed 12-bit SAR ADC. A Gaussian-distributed noise model with a standard deviation of 4 LSB was applied at the comparator input of the conventional and proposed SAR ADCs.

Figs. 20(a) and (b) display the simulated DNL and INL of the conventional and proposed 12-bit SAR ADCs, respectively. The maximal INL of the conventional SAR ADC was −0.84/0.83 LSB, whereas that of the proposed SAR ADC was only −0.63/0.60 LSB. This result indicates that the proposed SAR ADC corrected the bit error decisions due to comparator noise. The INL profiles depicted in Figs. 19 and 20 do not exhibit any points of discontinuity.

Therefore, incomplete capacitor DAC switching settling and noise were not the causes underlying the discontinuities in the measured INL profile. We inferred that the discontinuities in the measured INL profile were caused by several MSB capacitor mismatches. To understand how capacitor mismatch affects the ADC performance, the proposed 12-bit SAR ADC was simulated in the MATLAB software environment using 12 MSB mismatch capacitors and a Gaussian-distributed noise model with a standard deviation of 4 LSB. The changes in the capacitances of C_{18}, C_{17}, C_{16}, C_{15}, C_{14}, C_{13}, C_{12}, C_{11}, C_{10}, C_9, C_8, and C_7 were 0.06%, 0.01%, 0.02%, −0.02%, −0.05%, −0.05%, −0.05%, −0.05%, −0.05%, −0.05%, −0.05%, and −0.05%, respectively. Fig. 21 shows the simulated DNL and INL profiles.

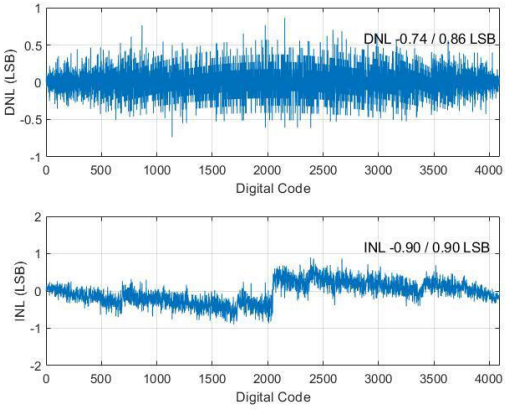


FIGURE 21. Simulated DNL and INL of the proposed 12-bit SAR ADC when using 12 MSB mismatch capacitors and a Gaussian-distributed noise model with a standard deviation of 4 LSB.

The simulated INL profile was very similar to the measured INL profile displayed in Fig. 17.

We concluded that capacitor mismatch caused the discontinuities in the measured INL profile and therefore reduced the linearity of A/D conversion. Table 4 summarizes the performance of the proposed SAR ADC, [7], [16], [21], [29], and [37]–[41]. Conventional binary-weighted CDACs were used for the SAR ADC of Ref. [41]. The ENOB of Ref. [41] is 10.55 bits under 0.1 MS/s sampling rate. Our SAR ADC features 11.25 bits at 1 MS/s sampling rate. Comparing with the linearity and conversion rate, our SAR ADC is better to the conventional SAR ADCs [41]. The proposed ADC featured an 18.39-fJ/conversion-step FoM, which is the smallest among the compared state-of-the-art SAR ADCs in Table 4. The die areas of the SAR ADCs have been included in the comparison table. These SAR ADCs were implemented through different CMOS technologies. The figure-of-merits are defined as:

$$FoM_W = \frac{Power}{2^{ENOB} \times f_{Sampling}} J/conv.-step \tag{3}$$

$$FoM_S = SNDR + 10\log\left(\frac{f_{Sampling}}{2 \times Power}\right) dB \tag{4}$$

V. CONCLUSION

This paper presents a 12-bit SAR ADC with split-capacitor, nonbinary-weighted, and multiple-LSB-redundant CDACs as well as parallel-series capacitor implementation. This design provides noise immunity and provides a mechanism for correcting the bit error decisions due to incomplete DAC switching settling by using the multiple LSB redundancy technique and nonbinary-weighted redundant DACs.

A prototype implemented using 0.18-μm 1P6M CMOS technology displayed a maximal DNL value, a maximal INL value, an SNDR, and an ENOB value of −0.4/0.54 LSB, −0.81/0.89 LSB, 69.51 dB, and 11.25 bits, respectively, for an input frequency of 500 kHz and a sampling rate of 1 MS/s. The A/D conversion linearity was mainly affected by capacitor mismatch. The proposed SAR ADC featured an

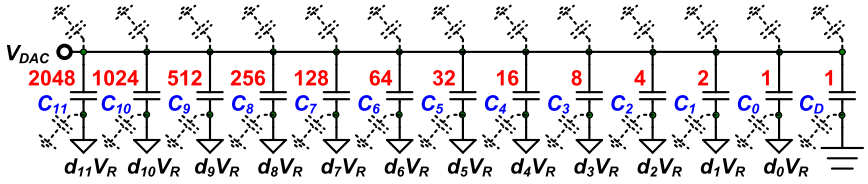


FIGURE 22. Schematic of conventional 12-bit binary CDAC.

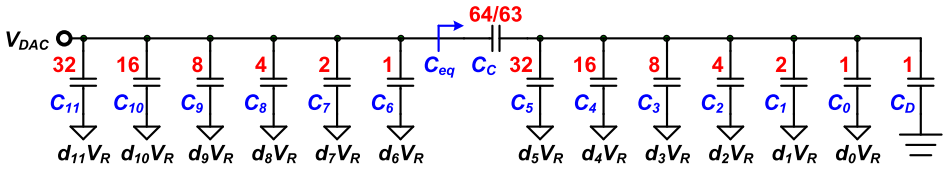


FIGURE 23. Schematic of a typical non-integer capacitor array where a coupling capacitor (C_C) is placed in the middle of a non-binary weighted capacitor array [18].

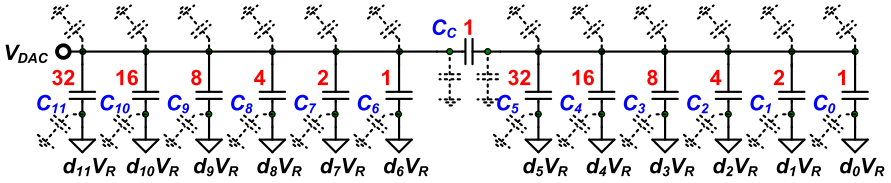


FIGURE 24. Alternative architecture to implement the non-integer capacitor array.

18.39-fJ/conversion-step FoM at the sampling rate of 1 MS/s, which is suitable for IoT applications.

APPENDIX

Fig. 22 illustrates a schematic of a conventional 12-bit binary CDAC. The capacitor array comprises a binary-weighted capacitor array and a dummy capacitor (C_D). The top plates of all capacitors are connected, and V_{DAC} represents the voltage at the top plate. The bottom plate of the dummy capacitor is connected to ground. The bottom plates of the binary-weighted capacitors are either connected to ground or the reference voltage V_R depending on their corresponding digital code d_i, where $i = 0$ to 11. After 12 switching steps for D/A conversion, V_{DAC} becomes

$$V_{DAC} = \frac{2048C \cdot d_{11} + 1024C \cdot d_{10} + \cdots 2C \cdot d_1 + C \cdot d_0}{2048C + 1024C + \cdots + 2C + C} \cdot V_R = \frac{V_R}{4096} \sum_{i=0}^{11} 2^i \cdot d_i \quad (5)$$

Equation (5) presents the output voltage of an ideal 12-bit DAC.

Fig. 23 displays a schematic of a typical non-integer capacitor array in which a coupling capacitor (C_C) is inserted between C_6 and C_5 [18]. After the D/A conversion switching, V_{DAC} becomes

$$V_{DAC} = \frac{\sum_{i=0}^{5} 2^i \cdot d_{i+6}}{\left(\sum_{i=0}^{5} 2^i\right) + 1} \cdot V_R + \frac{\frac{64}{63}}{\left(\sum_{i=0}^{5} 2^i\right) + \frac{64}{63}} \cdot \frac{\sum_{i=0}^{5} 2^i \cdot d_i}{\left(\sum_{i=0}^{5} 2^i\right) + 1 + \frac{\frac{64}{63} \cdot \sum_{i=0}^{5} 2^i}{\frac{64}{63} + \sum_{i=0}^{5} 2^i}} \cdot V_R = \frac{\sum_{i=0}^{5} 2^i \cdot d_{i+6}}{64} \cdot V_R + \frac{\sum_{i=0}^{5} 2^i \cdot d_i}{4096} V_R = \frac{V_R}{4096} \sum_{i=0}^{11} 2^i \cdot d_i \quad (6)$$

Because a non-integer coupling capacitor (64/63 unit capacitor) is inserted between two capacitor arrays, Equation (6) shows an error-free 12-bit D/A conversion. However, implementing the non-integer coupling capacitor is difficult. An alternative architecture to address this concern is illustrated in Fig. 24, where the value of the coupling capacitor becomes a unit capacitance, and the dummy capacitor (C_D) is removed. For this architecture, the converted voltage V_{DAC}

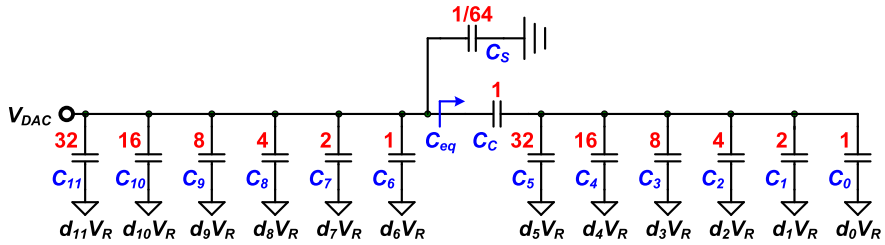


FIGURE 25. Schematic of a non-integer capacitor array with dummy capacitor C_S.

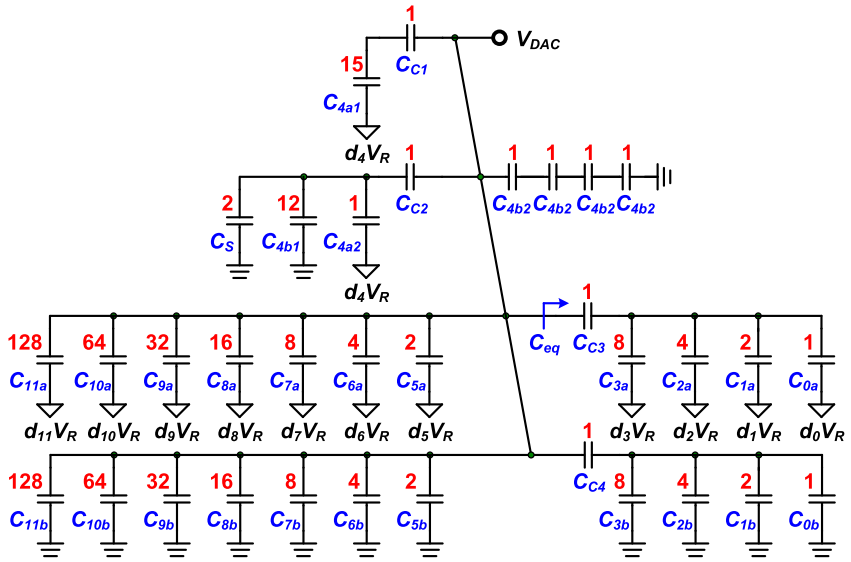


FIGURE 26. Schematic of a split and shifted C_C non-integer capacitor array with dummy capacitor C_S.

can be expressed as:

$$V_{DAC} = \frac{\sum_{i=0}^{5} 2^i \cdot d_{i+6}}{\left(\sum_{i=0}^{5} 2^i\right) + \frac{63}{64}} \cdot V_R + \frac{1}{\left(\sum_{i=0}^{5} 2^i\right) + 1} \cdot \frac{\sum_{i=0}^{5} 2^i \cdot d_i}{\left(\sum_{i=0}^{5} 2^i\right) + \frac{63}{64}} \cdot V_R = \frac{V_R}{4096} \sum_{i=0}^{11} 2^i \cdot d_i + \frac{V_R}{4096 \cdot 4095} \sum_{i=0}^{11} 2^i \cdot d_i \quad (7)$$

The first term on the right-hand side of (7) represents an ideal 12-bit D/A conversion, and the second term represents a D/A conversion gain error. The maximal error is 1 LSB when the $d_{11}d_{10}\cdots d_1d_0$ code is 111111111111.

To compensate for the weight mismatch and reduce the D/A conversion gain error, in this study, we added a dummy capacitor (C_S) connected between the left side of the coupling capacitor and ground (Fig. 25) and having 1/64 unit capacitance. For this proposed architecture, V_{DAC} can be expressed as

$$V_{\mathrm{DAC}} = \frac{\sum_{i=0}^{5} 2^i \cdot d_{i+6}}{1 + \sum_{i=0}^{5} 2^i} \cdot \mathrm{V_R} + \frac{1}{\frac{1}{64} + 1 + \sum_{i=0}^{5} 2^i} \cdot \frac{\sum_{i=0}^{5} 2^i \cdot d_i}{\frac{4033}{4097} + \sum_{i=0}^{5} 2^i} \cdot \mathrm{V_R} = \frac{V_R}{4096} \sum_{i=0}^{11} 2^i \cdot d_i \quad (8)$$

The proposed CDAC architecture effectively enhances the capacitor weight matching and exhibits an error-free D/A conversion. However, implementing a capacitor with 1/64 unit capacitance is also difficult. To facilitate the implementation of the non-integer dummy capacitor (C_D), the split-capacitor technique was used in the CDAC and a capacitor array with integer unit capacitances was constructed

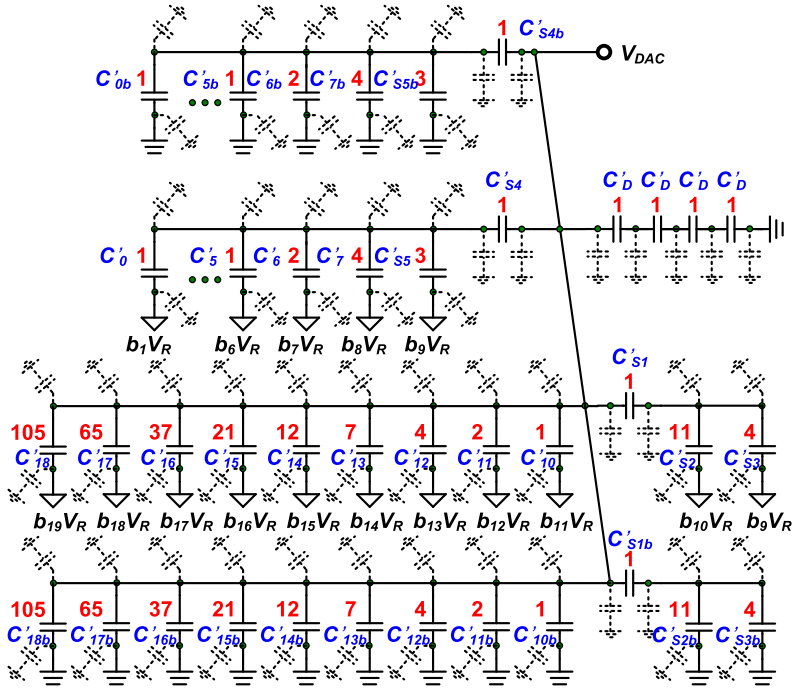


FIGURE 27. Proposed non-binary CDAC with a multiple-LSB technique.

to implement the 1/16 unit capacitor (Fig. 26). For this CDAC architecture, V_{DAC} can be expressed as:

$$V_{\mathrm{DAC}} = \frac{\sum_{i=0}^{7} 2^i \cdot d_{i+4}}{1+\sum_{i=0}^{7} 2^i} \cdot \mathrm{V_R} + \frac{1}{\frac{1}{16}+1+\sum_{i=0}^{7} 2^i} \cdot \frac{\sum_{i=0}^{3} 2^i \cdot d_i}{\frac{4081}{4097}+\sum_{i=0}^{3} 2^i} \cdot \mathrm{V_R} = \frac{V_R}{4096} \sum_{i=0}^{11} 2^i \cdot d_i \tag{9}$$

By using the split-capacitor technique, the proposed CDAC architecture also has an error-free D/A conversion. This architecture is not suitable for the binary CDAC architecture because the binary capacitor C_4 cannot be structured by several integer capacitors. However, it is suitable for the non-binary CDAC with a multiple-LSB technique. The proposed non-binary CDAC with a multiple-LSB technique is illustrated in Fig. 27. V_{DAC} can be expressed as

$$V_{\mathrm{DAC}} = \frac{\mathrm{V_R}\sum_{i=1}^{7} 2^i \cdot d_{i+5}}{512} + \frac{1}{512+\frac{1}{16}} \cdot \frac{\mathrm{V_R}\sum_{i=0}^{4} 2^i \cdot d_i}{15+\frac{8177}{8193}} = \frac{1}{2} \cdot \frac{V_R}{4096} \sum_{i=0}^{11} 2^i \cdot d_i \tag{10}$$

Equation (10) shows that the proposed CDAC architecture shows a perfect D/A conversion due to the elimination of the gain error caused by the series capacitor. The 1/4 C capacitor is used to allocate four sets of series capacitors, thus reducing the difficulty of 1/16 C implementation. This capacitor is also compatible with split-capacitor, non-binary, and multiple-LSB techniques, which is one of the contributions of this paper.

Fig. 22 displays a conventional 12-bit binary CDAC with parasitic capacitors occurring at the two plates of the capacitors where Δ is the parasitic capacitance weight compared with the unit capacitance. The D/A conversion voltage at the top plate of the CDAC can be expressed as

$$V_{\mathrm{DAC}} = \frac{\mathrm{V_R}\sum_{i=0}^{11} 2^i \cdot C \cdot d_i}{C \cdot (1+\Delta) + \sum_{i=0}^{11} 2^i \cdot C \cdot (1+\Delta)} = \frac{\mathrm{V_R}\sum_{i=0}^{11} 2^i \cdot d_i}{4096+4096\Delta} \tag{11}$$

Equation (11) reveals that the parasitic capacitors of the conventional binary CDAC reduce the converted voltage at the top of the CDAC but do not affect the conversion linearity. Fig. 24 illustrates a 12-bit split capacitor array with a unit bridge capacitor placed between a 6-bit MSB binary capacitor array and a 6-bit LSB binary capacitor array. Parasitic capacitance also occurs at the two plates of the capacitors. The converted voltage at the top plate of the CDAC can be

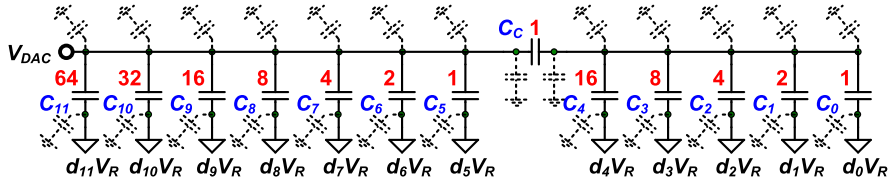


FIGURE 28. Schematic of a shifted C_C non-integer capacitor array with parasitic capacitors.

expressed as (12), as shown at the bottom of the page. The parasitic capacitors not only reduce the converted voltage but also affect the D/A conversion linearity. The converted voltage deviates from the ideal value because of the parasitic capacitances. The maximal deviation calculated using (12) is 63Δ. To reduce effect of parasitic capacitance, the position of the bridge capacitor can be shifted toward LSB binary capacitor array. Fig. 28 presents a 12-bit split capacitor array with a unit bridge capacitor placed between a 7-bit MSB binary capacitor array and a 5-bit LSB binary capacitor array. The converted voltage is expressed as (13), as shown at the bottom of the page. The total capacitance of the CDAC is doubled, but the maximal deviation is reduced to 31Δ. The calculation reveals that smaller LSB binary capacitor arrays have less parasitic capacitance effects. Fig. 27 illustrates the proposed CDAC architecture with parasitic capacitors.

$$
\begin{aligned}
V_{\mathrm{DAC}} &= \frac{\mathrm{V_R}\sum_{i=0}^{5} 2^i \cdot C \cdot d_{i+6}}{C\cdot(1+\Delta)+\sum_{i=0}^{5} 2^i \cdot C \cdot (1+\Delta)} + \frac{1}{1\frac{1}{64}\cdot(1+\Delta)+\sum_{i=0}^{5} 2^i \cdot (1+\Delta)} \cdot \frac{\mathrm{V_R}\sum_{i=0}^{5} 2^i \cdot C \cdot d_i}{\frac{63\frac{1}{64}}{63\frac{1}{64}+1} C\,(1+\Delta)+\sum_{i=0}^{5} 2^i \cdot C \cdot (1+\Delta)} \\
&= \frac{\mathrm{V_R}}{4096\cdot(1+\Delta)} \cdot \left[\sum_{i=0}^{11} 2^i \cdot d_i - \frac{\Delta}{1+\Delta}\sum_{i=0}^{5} 2^i \cdot d_i\right] \\
&\approx \frac{\mathrm{V_R}}{4096\cdot(1+\Delta)} \cdot \left[\sum_{i=0}^{11} 2^i \cdot d_i - \Delta\sum_{i=0}^{5} 2^i \cdot d_i\right] \qquad (12)
\end{aligned}
$$

$$
\begin{aligned}
V_{\mathrm{DAC}} &= \frac{\mathrm{V_R}\sum_{i=0}^{6} 2^i \cdot C \cdot d_{i+5}}{C\,(1+\Delta)+\sum_{i=0}^{6} 2^i \cdot C \cdot (1+\Delta)} + \frac{1}{1\frac{1}{32}\,(1+\Delta)+\sum_{i=0}^{6} 2^i \cdot (1+\Delta)} \cdot \frac{\mathrm{V_R}\sum_{i=0}^{4} 2^i \cdot C \cdot d_i}{\frac{127\frac{1}{32}}{127\frac{1}{32}+1} C\,(1+\Delta)+\sum_{i=0}^{4} 2^i \cdot C \cdot (1+\Delta)} \\
&= \frac{\mathrm{V_R}}{4096\cdot(1+\Delta)} \cdot \left[\sum_{i=0}^{11} 2^i \cdot d_i - \frac{\Delta}{1+\Delta}\sum_{i=0}^{4} 2^i \cdot d_i\right] \\
&\approx \frac{\mathrm{V_R}}{4096\cdot(1+\Delta)} \cdot \left[\sum_{i=0}^{11} 2^i \cdot d_i - \Delta\sum_{i=0}^{4} 2^i \cdot d_i\right] \qquad (13)
\end{aligned}
$$

$$
\begin{aligned}
V_{\mathrm{DAC}} &= \left[\frac{105C\cdot b_{19}+65C\cdot b_{18}+\ldots+2C\cdot b_{12}+C\cdot b_{11}}{512C\,(1+\Delta)}\right. \\
&\qquad \left. + \frac{1}{512\frac{1}{16}\,(1+\Delta)} \cdot \frac{11C\cdot b_{10}+7C\cdot b_9+\ldots+C\cdot b_1+C\cdot b_0}{\left(15+\frac{511\frac{1}{16}}{511\frac{1}{16}+1}\right) C\,(1+\Delta)}\right] \cdot \mathrm{V_R} \\
&= \frac{\mathrm{V_R}}{8192\cdot(1+\Delta)}\left[16\cdot(105b_{19}+\ldots+b_{11})+11b_{10}+\ldots+b_0-\frac{\Delta}{1+\Delta}(11b_{10}+\ldots+b_0)\right] \\
&\approx \frac{\mathrm{V_R}}{8192\cdot(1+\Delta)}\left[16\cdot(105b_{19}+\ldots+b_{11})+11b_{10}+\ldots+b_0-\Delta\,(11b_{10}+\ldots+b_0)\right] \qquad (14)
\end{aligned}
$$

The converted voltage is expressed as (14), as shown at the bottom of the previous page. The maximal deviation calculated through (14) is 31Δ. Because the position of the bridge capacitor is shifted toward the LSB binary capacitor array in the proposed CDAC architecture, the multiple-LSB technique does not cause considerable deviation. Therefore, the linearity concern caused by parasitic capacitances can be mitigated through careful layout. In this work, an ENOB of 11.25 bits was measured from the prototype. Therefore, compared with other architectures, the proposed SAR ADC architecture is competitive.

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HSUAN-LUN KUO was born in Tainan, Taiwan, in 1985. He received the B.S. and M.S. degrees from the Department of Electrical Engineering, National United University, Taiwan, in 2007 and 2010, respectively. He is currently pursuing the Ph.D. degree in engineering and system science with National Tsing Hua University (NTHU), Hsinchu, Taiwan. His research interests include analog-to-digital convertors and sensor front-end readout circuits design.

CHIH-WEN LU (Member, IEEE) received the B.S. degree in electronic engineering from the National Taiwan Institute of Technology, Taipei, Taiwan, in 1991, and the M.S. degree in electro-optics and the Ph.D. degree in electronic engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1994 and 1999, respectively.

From 1999 to 2001, he was an Assistant Professor with the Department of Electrical Engineering, Dayeh University, Taiwan. He joined National Chi Nan University (NCNU), Taiwan, in 2001, and was a Professor with the Department of Electrical Engineering, in 2010. He joined National Tsing Hua University, Hsinchu, in 2010, and was a Professor with the Department of Engineering and System Science. He joined National Chiao Tung University, Tainan, Taiwan, in 2020. He is currently a Professor with the Institute of Lighting and Energy Photonics. His research interests include analog/mixed-mode IC design and RFIC design.

Dr. Lu served as the Technical Program Chair for the 5th International Symposium on Next-Generation Electronics (ISNE 2016), in 2016 and the General Chair for the 13th IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC 2017), in 2017.

POKI CHEN (Member, IEEE) was born in Chia-Yi, Taiwan, R.O.C., in 1963. He received the B.S., M.S., and Ph.D. degrees from the Department of Electrical Engineering, National Taiwan University (NTU), Taipei, Taiwan, in 1985, 1987, and 2001, respectively.

From 1998 to 2001, from 2001 to 2006, and from 2006 to 2011, he was a Lecturer, an Assistant Professor, and an Associate Professor correspondingly with the Department of Electronic Engineering, National Taiwan University of Science and Technology (NTUST). He is currently a Professor with the Department of Electronic and Computer Engineering, NTUST. His research interests include analog/mixed-signal IC design and layout with special focus on time-domain signal processing circuits, such as time-domain smart temperature sensor, time-to-digital converter (TDC), digital pulse generator (DTC), time-domain ADC, and high accuracy DAC. He is also interested in creating innovative analog applications for FPGA platforms, such as FPGA smart temperature sensor and FPGA digital-to-time and time-to-digital converters. He has been serving as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS (VLSI) and IEEE ACCESS, since 2011 and 2013, respectively. He has been the Organizer of the IEEE International Conference on Intelligent Green Building and Smart Grid (IGBSG), since 2014. He serves as a keynote/invited speakers, a TPC members, and a session chair for various IEEE conferences, such as SOCC, VLSI-DAT, IFEEC, ISESD, NoMe TDC, ISNE, and ASID.