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A 25.1 dBm 25.9-dB Gain 25.4% PAE X-band Power Amplifier Utilizing Voltage Combining Transformer in 65-nm CMOS

VAN-SON TRINH, (Graduate Student Member, IEEE), AND JUNG-DONG PARK, (Senior Member, IEEE)
Division of Electronics and Electrical Engineering, Dongguk University, Seoul 04620, Republic of Korea

Corresponding author: Jung-Dong Park (jdpark@dongguk.edu)

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ABSTRACT We present an X-band two-stage power amplifier (PA) in 65-nm CMOS process using a transformer (TF)-based voltage combining technique (VTC) which achieves the highest figure of merit (FOM) among recently reported CMOS PAs. The PA architecture is constructed with two-stage push-pull amplifiers with a three-way voltage power combiner and splitter which play the main role to achieve outstanding performance. The power combining was applied in the voltage domain to increase the output device size aiming at boosting the output power of the CMOS PA. We constructed a compact two-stage PA with a push-pull structure with conjugate matchings at the input, inter-stage, and output with the capacitive neutralization technique to improve the power gain and drain efficiency. Working under a 1.2-V supply with DC quiescent current of 865-mA, the proposed PA achieved a maximum saturated output power of 25.1 dBm with a 1-dB power bandwidth of 3-GHz from 8.4-GHz to 11.4-GHz, a peak power added efficiency (PAE) of 25.4% at 10.2 GHz, a power gain of 25.9-dB at 9.5-GHz with a 3-dB gain bandwidth of 2-GHz (8.7-10.7 GHz). The total chip size is 0.9 mm^2, and the core size excluding pads is only 0.342 mm^2.

INDEX TERMS CMOS integrated circuits, power amplifier, transformer, X-band.

I. INTRODUCTION

Radar and wireless communication systems in X-band (8-12GHz) have been widely employed in various sectors both for military and civilian applications. X-band radars which operate in the wavelength of 2.5-4 cm are sensitive to small particles in the atmosphere, thereby suitable for short-range weather observation and monitoring [1]–[3]. X-band is also allocated for terrestrial and space communications with well-developed industrial products [4]–[6]. Particularly, Active Electronically Scanned Array (AESA) has been getting much attention recently owing to the potential usage in smart radar systems for aircraft vehicles [7], and electronically steered short-range weather radars suitable for low-cost civilian applications in X-band [8]. Therefore, the development of transmit/receive modules (TRMs) around the X-band is a popular research topic recently [9]–[12].

An efficient PA design is essential in RF transceiver design for low-cost AESA systems where a PA dominates the power consumption, spectra efficiency, and effective range coverage of the system. Even though an AESA system involves GaAs or GaN-based PAs for the higher output power and efficiency, it still requires a back-end module for the phase and magnitude control of the Tx/Rx signals which is typically realized in a highly-integrated silicon-based process with the driving capability higher than 20-dBm of the output power [13]. Moreover, it is always desirable to integrate a PA into a single CMOS chip for a lower cost and a reduced size in a low-cost short-range radar or communication systems as presented in [14], [15]. Therefore, designing high-performance CMOS PAs in X-band has gained intensive interests [16]–[25]. Nevertheless, PA design in a nanoscale CMOS process is a technically challenging task to attain overall high performance due to the serious second-order effects and reduced breakdown voltages between each node of the transistor.

In order to enhance the output power of the PA, stacking several FET devices to allow higher supply voltage is a preferred topology in silicon-on-insulator (SOI) CMOS PA design [19]. This method is partly applicable to a triple-well

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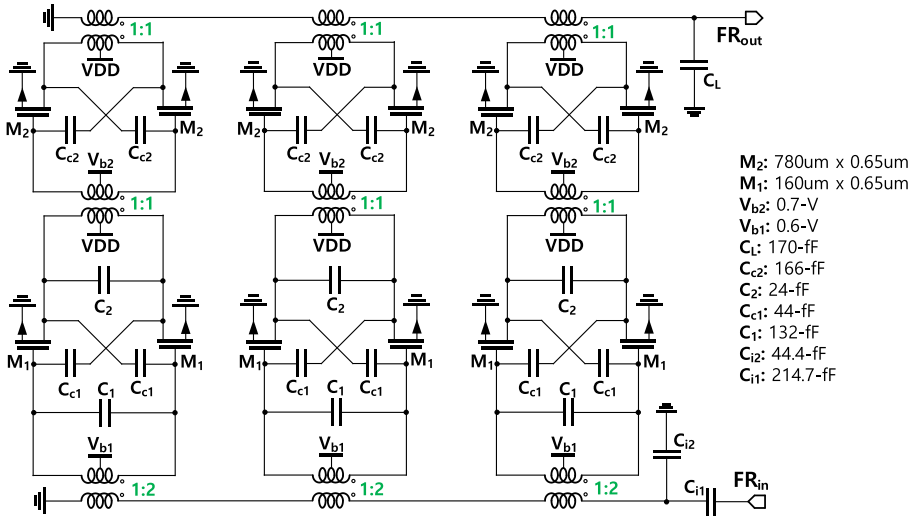


FIGURE 1. Complete schematic of the X-band CMOS two-stage PA using six-way voltage power combining/splitting architecture.

process in which the number of the stacked transistors is limited to barely two [22]. Another popular method to boost the PA's output power is to use power combining techniques. It is conventionally known that one cannot achieve a high output power from merely increasing the transistor size due to the unrealistic small optimum output resistance (R_{opt}) of the active device [26], [27]. The current combining technique (CCT) helps to increase the overall inductance of the passive components generated to resonate the capacitive parasitics at nodes of the transistors. However, it does not provide any transformation gain advantage of the overall resistance of the device [28], resulting in a poor output impedance matching when a large device size is used [17], [24], which results in a power efficiency degradation. By contrast, an m-way voltage power combining scheme provides an overall impedance transformation ratio of m^2-times for the load seen from the output of the transistors. Hence the voltage combining technique (VCT) can support the larger device size without incurring the tradeoff in output matching [28]. It should be noticed that the compact, high-efficiency push-pull structure widely used in a CMOS PA design can be considered as a PA with a two-way voltage power combiner. Despite the advantages of the VCT, the usage of high-way voltage power combiners (PCs) in X-band PA is still infrequent except for the PA's with four-way voltage PCs [20], [24].

Performance of a PA is typically assessed by its output power (P_{out}), power gain (G), power added efficiency (PAE), and its operating frequency (f_o), which is reflected through the commonly accepted figure-of-merit given as [29]:

$$FoM = P_{out} \cdot G \cdot PAE \cdot f_o^2 \tag{1}$$

In this paper, we demonstrate an X-band PA which attains an FoM of 85.0-dBm·Hz^2 which is the highest metric ever achieved among CMOS PAs around X-band to the best of our knowledge, and it is comparable to SiGe PAs. The PA is constructed from three ways of two-stage push-pull amplifiers whose output powers are combined in the voltage domain by a voltage power combiner (PC). Each differential pair of transistors is stabilized by using a couple of capacitors cross-connected between the drains and the gates to enhance the impedance matching capability. The conjugate impedance matching for the push-pull amplifiers using a transformer (TF) was carried out based on the analysis results in [30]. The proposed PA is fabricated in 65-CMOS and it works under a supply voltage of 1.2-V. On measurement, the PA achieves a maximum saturated output power (P_{sat}) of 25.1 dBm and a peak PAE of 25.4% at 10.2 GHz, a peak power gain of 25.9-dB at 9.5-GHz. The 3-dB gain bandwidth of the PA is 2-GHz recorded from 8.7-GHz to 10.7-GHz, while P_{sat} varied within 1-dB from 8.4-GHz to 11.4-GHz. The paper is organized as follows. Section II describes the designing details of the PA. Then, the measurement results are given in Section III followed by a conclusion in Section IV.

II. DESIGN OF THE SIX-WAY VOLTAGE COMBINING TWO-STAGE PA

The entire schematic of the proposed two-stage PA using six-way voltage power combining/splitting in X-band is illustrated in Fig. 1. The PA is composed of a power stage including three identical push-pull PA unit cells whose outputs are combined in voltage domain using a three-way differential-to-single-ended power combiner, three driving amplifiers (DAs) with push-pull configuration, and an input power splitter.

A. ARCHITECTURE CONSIDERATION

The popularity of transformer (TF)-based push-pull PAs in the microwave and millimeter-wave regime is owing to its compactness and high efficiency while it naturally implements a two-way power combining structure in voltage mode which boosts the output power of the push-pull PA by 3 dB compared with its single-ended counterpart. A large

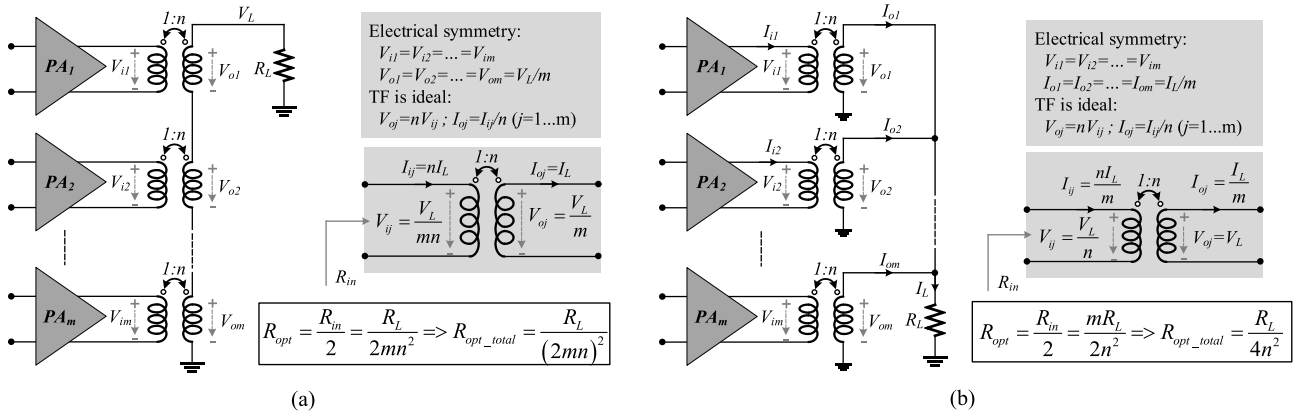


FIGURE 2. Transformer-based voltage combining technique (a) and current combining technique (b).

transformation ratio of the TF (i.e. $n > 1$) can be used to support a large device size and further boosts the output power of the PA. In our previous work, we employed a 1:2 TF at the output stage to obtain a high power-efficiency in the X-band PA design [22]. However, a large transformation ratio (n) typically results in a small mutual coupling factor (k) of the realized TF, which results in a degradation of its efficiency which is proportional to k^2 [30]. Moreover, it is difficult to implement a high-efficiency voltage mode power combiner with $n > 1$ because the long routing path of the secondary coil may reduce its self-resonance frequency (SRF), causing imbalances between the combined signals. For these reasons, TF units using $n = 1$ were used in this work.

To design a high output power PA, the use of power combining techniques including current combining technique (CCT) and voltage combining technique (VCT) were considered as presented in Fig. 2. An m-way differential-to-single-ended current mode power combiner based on ideal 1: n TFs supports an optimum resistance for each device of $R_{opt} = m \times R_L/2n^2$, where R_L is the load resistance with the typical value of 50 Ω [28]. When $n = 1$, this value becomes $R_{opt} = m \times R_L/2$. The denominator of 2 can be viewed as the effect of the two-way voltage combining push-pull structure. The effective R_{opt} of the total $2\times m$ number of devices connected in parallel is calculated to be $R_{opt\_total} = R_L/4$. This means that the use of CCT does not affect the optimal total device size. By contrast, an ideal m-way 1:1-TF-based voltage mode power combiner requires a total optimum device resistance of $R_{opt\_total} = R_L/(2\times m)^2$, supporting a larger output device size while remaining a good power matching at the load. As a reasonable voltage combining, a three-way power combining/splitting structure ($m = 3$) was chosen in this design to support an appropriately large device aiming at a high-efficiency layout realization of the output transistor.

The power combiner (PC) and splitter (PS) were implemented using the ultra-thick metal (UTM) layer for the primary coils and the combination of the two metal layers below the UTM for the secondary coils. A 3-D view of the combiner and splitter simulated on HFSS is shown in Fig. 3. As for the PC, the UTM is used for the primary coils to conduct the large

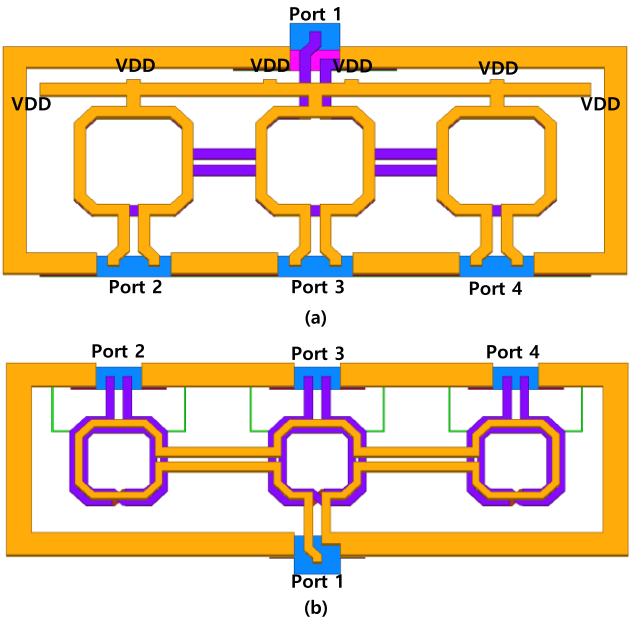
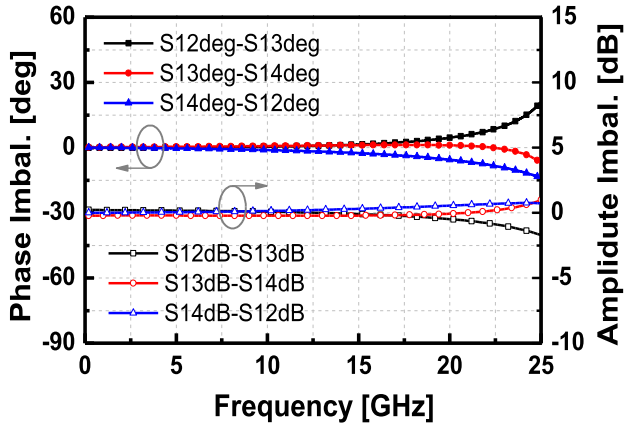


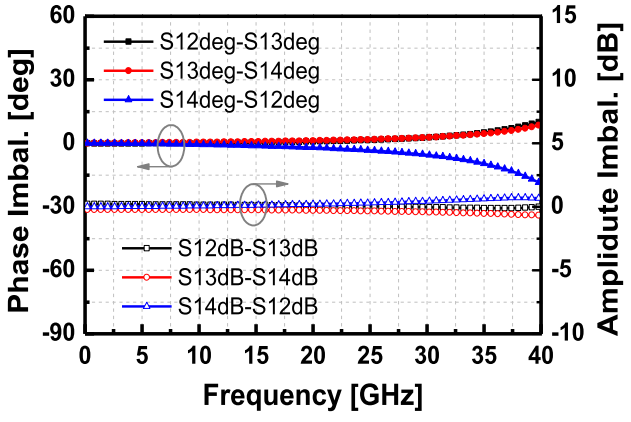
FIGURE 3. 3-D view on HFSS of the physical layout of power combiner (a) and power splitter (b).

quiescent drain currents of the output transistors. The supply voltage (VDD) was provided from several positions to reduce the parasitic series resistance between VDD and the drain of NMOS which can cause a serious voltage drop when the total bias current is large.

When we use the voltage combining/splitting technique, one of the concerns is to keep the electrical symmetry between the combined paths. If the combiner or splitter operates close to its SRF, it may cause an imbalance in amplitude and phase between signal paths which seriously degrades the combining efficiency. Thus, it is necessary to perform the EM simulation with HFSS to verify if there is no asymmetry issue in the designed structure. Fig. 4a shows the simulation results of the phase and amplitude imbalance of the power combining network. As illustrated in Fig. 4a, the imbalance between signal paths becomes serious when the frequency is larger than 20-GHz. The phase imbalance is smaller than 6°



(a)



(b)

FIGURE 4. Simulated phase/amplitude imbalances of the (a) output 3-way power combiner and (b) input 3-way power splitter.

and the amplitude imbalance is within 0.5-dB from 0.5-GHz to 20-GHz. Also, the simulation imbalances of the phase and the amplitude between signal paths for the input PS is shown in Fig. 4b, and the simulated results are also quite small in the X-band. The simulated results confirmed that the proposed three-way power combining/splitting architecture demonstrates electrically symmetric RF signal paths in the band of interest.

B. STABILIZING PUSH-PULL AMPLIFIERS

The proposed PA was built based on the push-pull amplifier structure which provides several important benefits of high efficiency and high output power while occupying a compact area. However, the differential two-port composed of two common source amplifiers is conditionally unstable in the low-frequency region due to the unwanted feedback caused by the gate-to-drain parasitic capacitor C_{gd}. One method to stabilize the differential pair of transistors is to use a resistor connected in series with a capacitor in the feedback path from the drains to the gates (RC-feedback) to intentionally increase the resistive loss for the stabilization [18], [22]. However, the drawback of this technique lies in its side effect on the degradation of power efficiency, preventing it from being widely used, especially at high frequencies. A feedback network using inductors was used to resonate out C_{gd} for a stabilized push-pull amplifier while attaining an improved efficiency owing to the high-quality factor of inductors realized at high frequency [31]. However, the large area occupancy of the inductive feedback is not appealing for architecture using a power combining technique, specifically at the low-frequency regime. A more common technique for the stabilizing task is to use a pair of capacitors cross-connected between the drains and the gates of the two active devices to neutralize the gate-to-drain parasitic C_{gd}. In this proposed PA design, we employed cross-connected couples of neutralizing capacitors (C_{neu}) to stabilize the push-pull amplifiers both in the power and the driving stages to attain an improved efficiency. The value of the neutralizing capacitor is ideally estimated to be the same as the C_{gd} of the transistor [32]. In designing the unit cell of the PA, C_{neu} was tuned around C_{gd} and the maximum available gain (G_{ma}) and the stability factor (K-factor) were investigated to determine the final value of C_{neu}. Fig. 5 shows the maximum available gain (G_{ma}), maximum stable gain (G_{ms}), and the stability factor (K) of the differential pair in the power stage with various values of C_{neu}. Herein, Δ was also examined to ensure its absolute value is less than unity. Without using a neutralization capacitor, the active differential pair is conditionally unstable with K <1 in the band of interest. It is noteworthy that the amplifier without C_{neu} becomes stable after a specific frequency of 77-GHz from the simulated K-factor versus frequency, which is also called knee frequency. When C_{neu} is involved, the knee frequency decreases as C_{neu} increases. However, when C_{neu} becomes even larger, it works as an AC-coupling capacitor, then the differential pair becomes the cross-coupled pair which is widely used in oscillator designs. In this case, the knee frequency of the differential pair increases as C_{neu} further increases. As shown in Fig. 5, when C_{neu} of 146-fF, 156-fF, and 166-fF is used, the knee frequency is reduced to around 15-GHz, 7-GHz, and 3-GHz, respectively. When C_{neu} equals 176-fF, the knee frequency is around 2.7-GHz. If C_{neu} further increases, the knee frequency was seen to be increased as we noticed. In this design, C_{neu} =166-fF was determined to achieve a stable condition in the X-band. This also makes the design less sensitive to the parasitic variations of the device. Similarly, C_{neu} =44-fF was chosen for the differential pair in the driving stage.

C. GATE BIAS VOLTAGE CONSIDERATION

When we design the output stage of the PA with the output PC, choosing an appropriate size of the active device and the matching network is crucial to achieving the desired output power with an enhanced power efficiency owing to its dominance in power consumption compared to the driving stage. The first mission is to choose the gate bias voltage for the output transistor since it is relatively independent of the active device size. The feasible range of output device size is determined by the load resistance and the power combining

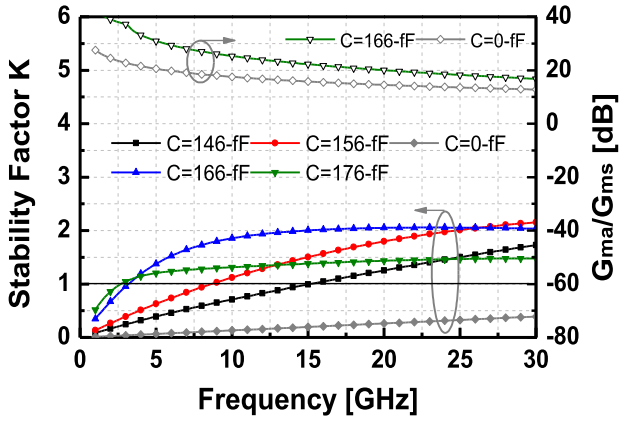


FIGURE 5. Simulated G_{ms}/G_{ma} and stability factor K versus frequency of several values of the neutralization capacitor (C_{neu}).

scheme. Hence, it is unrealistic to increase the output power by merely increasing the output device size considering the matching difficulty and bandwidth. Therefore, the gate bias for the output transistors should be chosen to achieve a good tradeoff between the maximum achievable output power and power efficiency.

We performed the harmonic balance (HB) simulation using Spectre to investigate the large-signal performances of the output transistor cell depending on the gate bias voltage. Fig. 6 shows the maximum output power (P_{sat}), the peak power added efficiency (PAE), the PAE at P_{in} =-10 dBm, and the quiescent current consumption of the differential two-port at the output stage versus the gate bias voltage (V_{bias}). In this simulation, the post-layout RC extraction was performed with Calibre. As can be seen, P_{sat} increases monotonously versus V_{bias}, and its increment becomes compressed in the large bias region. The peak PAE generally reduces when V_{bias} increases. However, the decrease is quite minor when V_{bias} is larger than 0.5-V, and the peak PAE keeps almost close to 70%. This means that when the input signal is large enough, the shape of the voltage waveform on the gate does not depend much on its DC bias voltage. The active devices operate as switches

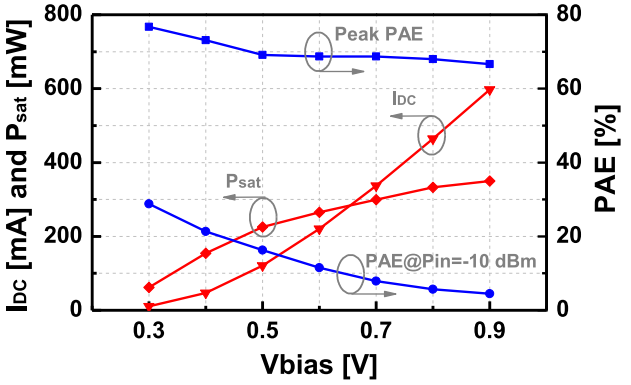


FIGURE 6. Simulated peak PAE, PAE at $P_{in} = -10$-dBm, saturated output power (P_{sat}) and DC current consumption (I_{DC}) of the output transistor differential amplifier versus the gate bias voltage (Vbias).

in the large-signal regime, which is inherently the working principle in switching PAs such as class $D^{+1/-1}$, $E^{+1/-1}$, $F^{+1/-1}$, particularly when the applied gate bias is small. However, the relative independence of the PAE from the gate bias voltage does not remain when the input power (P_{in}) is small. For example, at P_{in} =-10 dBm, the plot of the PAE drops drastically as V_{bias} increases. The large DC current consumption at the large gate bias makes the differential amplifier less efficient in the small-signal regime. Based on this experiment, the gate bias voltage of 0.7-V was chosen for the output transistor to achieve a good output power with a moderate level of DC current consumption and power efficiency at the small signals. Designing the gate bias voltage for the driving stage was also performed similarly to the power stage. The trend of the performance versus V_{bias} in the driving stage was similar to the power stage except that the output power criterion of the driving stage was mitigated compared with the power stage. Thus, V_{bias} equal to 0.6-V was chosen for the driving stage to further enhance the power efficiency with an improved gain.

D. DEVICE SIZING AND IMPEDANCE MATCHING

In the output stage, the TF-based power combiner has to transfer the 50-Ω output load to the optimum impedance of each differential pair to maximize the output power generated by the active device. The impedance seen from the load toward the active device should be also close to 50-Ω to minimize the return loss at the output port. From the calculation of the optimum resistance for the output transistor mentioned previously, the calculated R_{opt} of each transistor cell is 50/(2 × 3)=8.3-Ω, or R_{opt} of each differential pair amplifier is 16.6-Ω. This calculation is under the assumption that the TFs are ideal with the coupling factor of 1, and the inductances of the TF are resonated out by corresponding ideal capacitors.

In the real case, the winding coils composing the TF have their own resistive losses, and the mutual coupling factor is smaller than 1. Typically, a TF can be modeled by its low-frequency model with 5 parameters including L_1, L_2, R_1, R_2, and M standing for the primary and secondary inductances, the primary and secondary resistances, and the mutual coupling inductance, respectively [30]. The effective quality factors of the two TF coils at a specific frequency ω are defined to be $Q_1 = \omega L_1/R_1$ and $Q_2 = \omega L_2/R_2$. The mutual coupling factor is calculated by $k = (L_1L_2)^{1/2}/M$. Fig. 7a shows the impedance matching schematic of the output stage including the PC composing of three TFs, the 50-Ω load connected in parallel with a matching capacitor C_L and the output impedance of the differential amplifiers is modeled by a resistor in parallel with a capacitor. Since the electrical symmetry of the PC is already verified, we can assume that the three TFs of the PC are all identical, and the voltages at three input ports are all the same. Thus, the three input ports of the PC can be connected to form a single input port with the correspondingly scaled R and C in parallel as shown in Fig. 7b. Now the three-way PC can be characterized by an

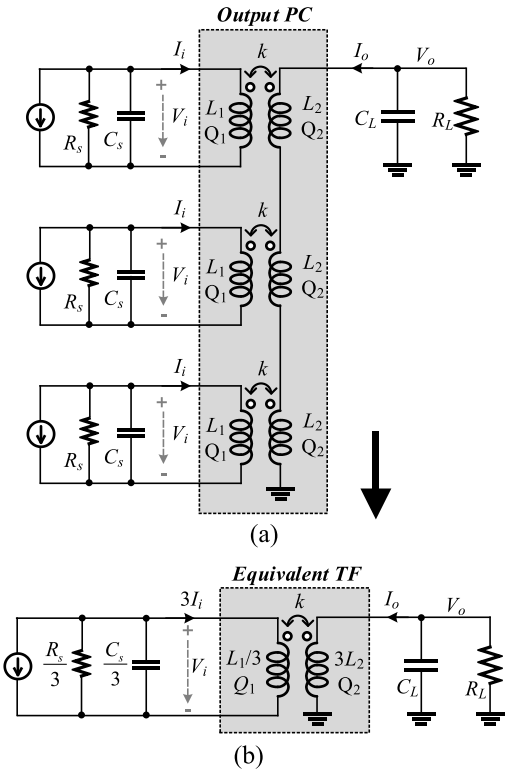


FIGURE 7. Schematic (a) and the equivalent TF model (b) of the output stage.

equivalent two-port TF whose primary inductance is reduced by three times and secondary inductance is tripled compared to those of the single unit TF composing of the original PC. With this equivalent TF model, we can choose its optimum source and load impedances given by [30]

$$\begin{cases} X_L = -\omega L_2, & X_S = -\omega L_1 \quad (2.1) \\ R_L = R_2\sqrt{1+k^2Q_1Q_2}, & R_S = R_1\sqrt{1+k^2Q_1Q_2} \quad (2.2) \end{cases}$$

where $Z_{s\_opt} = R_s + jX_s$ is the optimum source impedance and $Z_{L\_opt} = R_L + jX_L$ is the optimum load impedance.

It should be noticed that the calculated source impedance at the input side of the equivalent TF has to be tripled to get the optimal source impedance of each input port of the original three-way PC. Hence, the source impedance of each input port of the PC is $3\times Z_{sopt}$.

The characteristic parameters of the equivalent TF of the output PC extracted at 10 GHz are given in Table 1. As can be seen, the ratio between L_2 and L_1 is around 10, implying an equivalent turn-ratio of approximately three as expected. By using (2), the output PC was co-designed with an output

TABLE 1. Characteristic parameters of the equivalent TF of the output PC at 10-GHz.

L_1	L_2	Q_1	Q_2	k
80.5 pH	815 pH	8.1	5.9	0.76

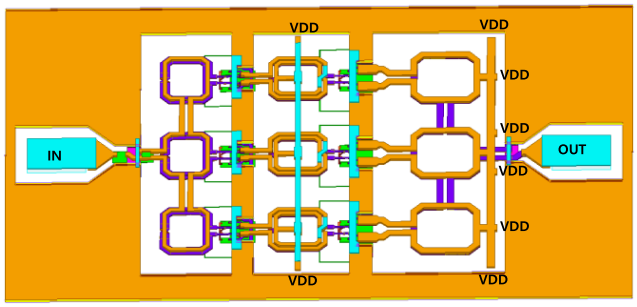


FIGURE 8. 3D HFSS physical structure of the whole PA.

active device with a gate width of 780-um so that the calculated optimum impedances at the input and output sides were close to their corresponding practical source and load. The synthesized optimum output resistance is around 50-Ω which allows us to simplify the output matching network which is only with a resonating capacitor connected in parallel to the load. A good impedance matching level was achieved at the load side with the simulated S_{22} of nearly -30 dB. Performing physical layout for such a big output transistor was also an important task, affecting the performance of the transistor cell. In this work, the fishbone layout structure was applied for the output transistor to reduce the gate parasitics as well as the harmful couplings between the gate and the other nodes [18]. In the simulation, the output stage can generate a saturated output power of 26.5-dBm to the 50-Ω load at 10-GHz.

The impedance matching formulas in (2) were also applied to design the driving stage as well as the input PS. Intuitively, the inter-stage TF size was designed such that its secondary inductance resonates out the gate capacitance of the output transistor. To give freedom in choosing the device size of the driving stage, a capacitor C_2 was employed to tune the capacitance at the input side. The device size of the driving stage was chosen in consideration of the linearity, the gain, and the power efficiency of the PA. The driving active device should be large enough to drive the power stage into the saturation region before its output power is compressed. Besides, a relatively large driving amplifier consumes a large DC power which degrades the overall power efficiency. Considering those issues, a suitable transistor size of 160-um was chosen for the driving stage, resulting in a simulated output 1-dB gain compression point (OP1dB) of 23.5-dBm at 10-GHz for the whole PA. The signal level processed by the input PS is small, thereby its efficiency is negligible to the whole PA design. Instead, the impedance matching for the input side is more problematic due to a relatively high impedance of the input gates. To enhance the impedance matching capability, low-quality MOS capacitors were shunted to the gate of the driving transistor to degrade the Q-factor of the resonator at the gates as well as to reduce the size of the input PS. Moreover, a pair of capacitors including C_{i1} and C_{i2} was used to transfer a relatively high input impedance seen from the PC to the 50-ohm source.

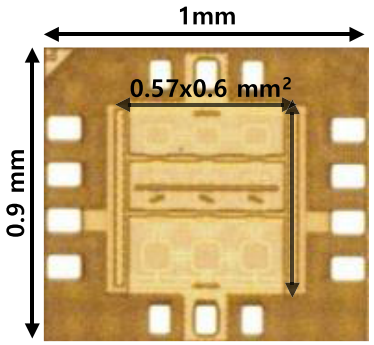


FIGURE 9. Photograph of the fully integrated PA chip.

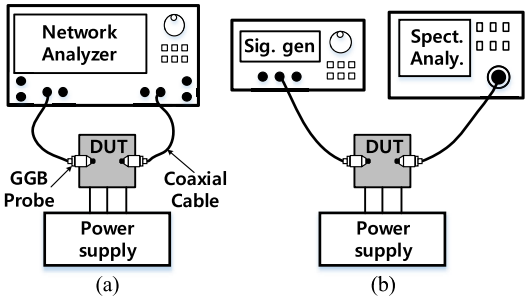


FIGURE 10. Measurement setup of the S-parameters (a) and large-signal performances (b).

To characterize the PA accurately, the whole physical layout of the PA was modeled in the EM simulation (HFSS). The 3-D structure of the proposed PA is illustrated in Fig. 8. The PA was fabricated on 65-nm CMOS, and a photograph of the chip is shown in Fig. 9. The chip size of the full PA including all DC and RF pads is 1×0.9 mm^2, and the core size is 0.6×0.57 mm^2.

III. MEASUREMENT RESULTS

Figure 10 shows measurement setups for S-parameters and large-signal performances of the X-band PA. In the measurement, the implemented PA consumed a DC quiescent current of 865 mA under 1.2-V supplying without an applied RF input. To measure the S-parameters, a vector network analyzer (VNA) Keysight N5224A (10 MHz to 43.5 GHz) was used combined with an on-wafer probe station. The cable connections and the RF-probes used in the measurement were calibrated with GGB CS-5 (calibration substrate). The simulated and measured S-parameters of the PA are shown in Fig. 11. The measurement and simulation results correspond to each other. On measurement, the PA achieves a peak gain of 25.9-dB at 9.5-GHz with a 3-dB gain bandwidth of 2-GHz recorded from 8.7-GHz to 10.7-GHz. In general, the measured S_{11} and S_{22} are shown to be better than the simulation results. In particular, a very good impedance matching level was demonstrated at the load with a measured minimum S_{22} of around -40 dB. This further verified the advantages of the VCT compared to CCT in terms of impedance matching performance. The isolation between the outputs and the input, i.e. S_{12}, was measured to be smaller than -50 dB.

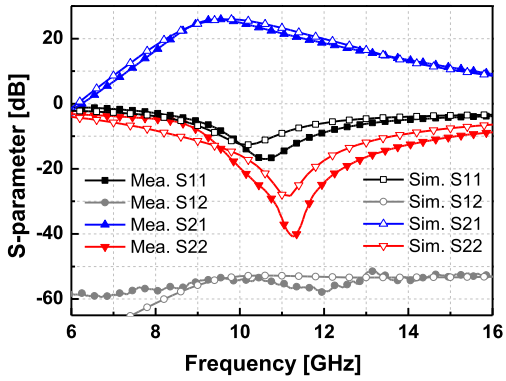


FIGURE 11. Simulated and measured S-parameters of the PA.

A signal generator Agilent 83623B (10-MHz–20-GHz) and a spectrum analyzer Agilent E4407B (9-kHz–26.5-GHz) were used to measure large-signal performances of the PA. The simulation and measurement performances including P_{sat}, power gain, and PAE of the PA versus the input power are shown in Fig. 12. The profiles of the measured power gain and P_{out} match quite well with the simulation results verifying the linearity of the fabricated PA. The measured PAE of the PA is almost identical to the simulation results at the small input signals. However, PAE is slightly degraded when the signal becomes larger in measurement, which indicates the limitation of the transistor model at the large signal domain.

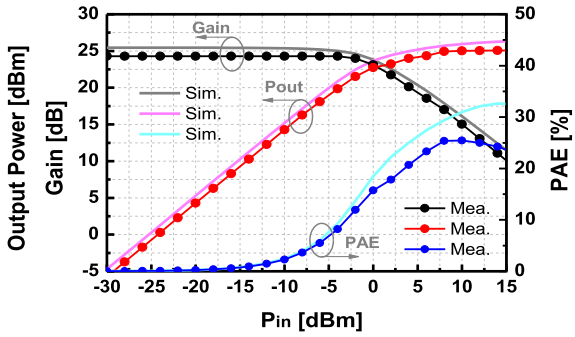


FIGURE 12. Simulated and measured output power (P_{out}), Gain and power added efficiency (PAE) versus input power (P_{in}) of the PA at 10-GHz.

The large signal performances of the PA were measured in the whole X-band with a frequency step of 0.2-GHz. Two tones with 20-MHz spacing were applied to the PA to measure the output third-order interception point (OIP3). The practical results of P_{sat}, OP1dB, OIP3, and peak PAE are presented in Fig. 13. In the measurement, the PA achieves a maximum P_{sat} of 25.1 dBm at 10.2-GHz with a peak PAE of 25.4% recorded at the same frequency. Also at 10.2-GHz, the PA achieved the highest measured OP1dB of 22-dBm and a peak OIP3 of 29 dBm. From 8.4-GHz to 11.4-GHz, the measured P_{sat} varied less than 1-dB from its peak value. Over the whole X-band, the measured P_{sat} is larger than 22.7-dBm, the OP1dB is higher than 19.6-dBm and the peak PAE is better than 16.1 %.

TABLE 2. Summary of state-of-art silicon-based PAs around X-band.

Ref.	Tech. (CMOS)	Combining Topology	Freq. (GHz)	V_{DD}/V_{CC} (V)	P_{sat} (dBm)	Gain (dB)	Peak PAE (%)	OP1dB (dBm)	Area (mm^2)	DC-Diss. [mW]	FoM
This	**65-nm CMOS**	**VCT6**	**8.7-10.7@10**	**1.2**	**25.1**	**25.9**	**25.4**	**22.0**	**0.9x1 0.57x0.6***	**1038**	**85.0**
[16]	90-nm CMOS	VCT2	5.2-13@8	2.8	25.2	18.5	21.6	22.6	0.7	NA	75.1
[17]	180-nm CMOS	VCT2-CCT3	7-10@9	3.3	27.1	11.2	22.7	24.2	0.88	1267	70.9
[18]	180-nm CMOS	VCT2	6.5-13@9.5	3.6	21.5	25.3	20.3	20.2	0.63	713	79.4
[19]	45-nm SOI	Stacked	9-15@12	4.8	22.8	9.8	21.8	21.9	0.22	NA	66.0
[20]	180-nm CMOS	VCT4	8.6-10.3@9.5	3.0	24.5	25	18	NA	1.2	960	81.6
[21]	180-nm CMOS	CCT2	7-12@10	3.6	23.8	14.5	25.8	17.6	0.47	691	72.4
[22]	65-nm CMOS	VCT2	8-11.4@9.5	1.2	20.5	24.4	24.5	15.2	0.48	347	78.3
[23]	180-nm CMOS	CCT2	7.4-8.3@8	1.8	18	19.2	22.6	14.9	0.43	NA	68.8
[24]	180-nm CMOS	CCT4-VCT2	10-12@11	5	29.6	11	15.5	28.2	2.1	4060	73.3
[25]	65-nm CMOS	VCT2	10	1.8	21.4	NA	33.3	21	NA	614	NA
[33]	130-nm SiGe	2-way CCT	8.6-11.2@10**	3	26.5	16.1	53.4	NA	0.81	15.6	79.9
[34]	180-nm SiGe	2-way VCT	7.2-10.2@10**	3.5	27	21	36	NA	0.95	578	83.5
[35]	130-nm SiGe	2-way CCT	8-12@10**	7.5	29.5	27.7	17.8	28.2#	2.66	NA	89.7
[36]	350-nm SiGe	2-way VCT	11-13@12	1.8	23.4	21.2	37.3	20.4	1.71	NA	81.9

$$FOM = P_{sat}(\text{dBm}) + Gain(\text{dB}) + 10\log\left(PAE[\%] \times f^2[\text{GHz}]\right)$$

* PA core only
** BW is defined as the frequency range of the power gain 1 dB lower than that at 10 GHz
# Estimated from figure

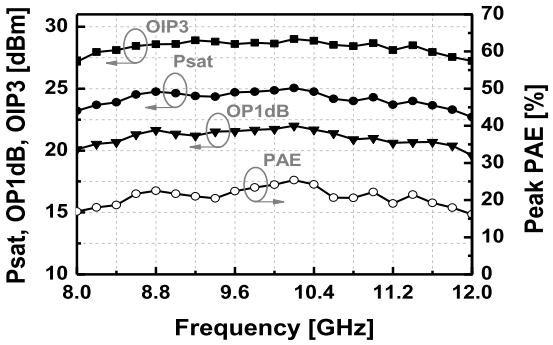


FIGURE 13. Measured P_{sat}, OP1dB, OIP3 and peak PAE of the PA in X-band.

The performance of the PA is summarized in Table 2 in comparison with other silicon-based PAs recently reported around X-band. The exhibited overall-high performance of the PA makes it become the highest FoM among the CMOS PAs, and even comparable to PA designs in SiGe.

IV. CONCLUSION

We presented a compact X-band CMOS power amplifier (PA) in 65-nm CMOS technology which achieved overall high performance with an outstanding figure of merit (FoM) of 85-dB compared with other reported silicon-based PAs in X-band. The push-pull architecture with the voltage mode power combiner and splitter with the compact and efficient impedance matching approach is the key factor in this design to improve the output power, efficiency, power gain as well as linearity. A six-way transformer (TF)-based power splitting/combining scheme combined with the push-pull architecture was developed and applied to achieve a high output power while still facilitating the output impedance matching. The PA used a two-stage architecture to ensure a high gain with good power efficiency. The equivalent TF with the established matching technique provided a useful design insight in co-designing the impedance matching network by choosing active device size to optimize the PA performance. The gate voltage bias for the transistors was selected based on a careful investigation of the large-signal performances of the active device. The implemented PA achieved a peak PAE of 25.4%, a maximum P_{sat} of 25.1-dBm, and the highest gain of 25.9 dB over the X-band.

ACKNOWLEDGMENT

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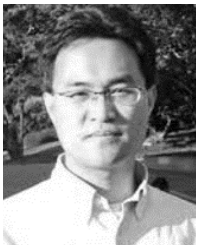
VAN-SON TRINH (Graduate Student Member, IEEE) received the Bachelor of Science degree from the Hanoi University of Science and Technology (HUST), Hanoi, Vietnam, in 2015. He is currently pursuing the Ph.D. degree in electronics and electrical engineering with Dongguk University, Seoul, Korea.

His current research interest includes various analog and RF integrated circuits.



JUNG-DONG PARK (Senior Member, IEEE) received the Bachelor of Science degree from Dongguk University, Seoul, South Korea, in 1998, the M.S. degree from the Gwangju Institute of Science and Technology (GIST), Gwangju, South Korea, in 2000, and the Ph.D. degree in EECS from the University of California, Berkeley, in 2012.

From 2000 to 2002, he worked with the Institute for Advanced Engineering (IAE), Yongin, South Korea, where he was involved with the design of 35 GHz radar/radiometer transceivers. From 2002 to 2007, he was a Senior Researcher with the Agency for Defense Development (ADD), Daejeon, South Korea, where he was responsible for the development of millimeter-wave (mmW) passive/active sensors and related mmW modules. From 2007 to 2012, he was with the Berkeley Wireless Research Center (BWRC), where he worked on silicon-based RF/millimeter-wave/terahertz circuits and systems. From 2012 to 2015, he worked with Qualcomm Inc., San Jose, CA, USA, where he designed various RF/analog integrated circuits. He is currently an Associate Professor with the Division of Electronics and Electrical Engineering, Dongguk University. His research interests include wireless communications, remote sensors, microwave electronics, analog, RF, mixed-signal, and millimeter-wave circuits.

Prof. Park was a recipient of the 2017 Most Frequently Cited Papers Award as a Lead Author at the 2017 IEEE Symposium on VLSI Circuits, Kyoto, from 2010 to 2016.