IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

IEEE POWER & ENERGY SOCIETY SECTION

Received November 15, 2020, accepted December 14, 2020, date of publication December 31, 2020,
date of current version January 25, 2021.

Digital Object Identifier 10.1109/ACCESS.2020.3047133

An Analytical Method to Determine the Optimal Switching of Modular Multilevel Converter in HVDC System

YONGHUI LI[1], JUN YANG[1], (Member, IEEE), SAN SHING CHOI[2], AND QIANG ZHAO[3]

[1]School of Electrical Engineering and Automation, Wuhan University, Wuhan 430072, China
[2]School of Electrical Engineering and Computer Science, Queensland University of Technology, Brisbane, QLD 4000, Australia
[3]Electric Power Research Institute of China, Beijing 100192, China

Corresponding author: Yonghui Li (liyonghui@whu.edu.cn)

This work was supported in part by the State Grid Corporation of China under Grant SGXJWL00JYJS1900575.

ABSTRACT The lifetime of the submodules (SMs) in a modular multilevel converter (MMC) is significantly impacted by its switching frequency. In this work, the determination of the switching frequency, to be applied to the nearest level modulation (NLM) method used in the SMs, is formulated as a linear integer optimization problem (LIOP). It is shown that there is an ideal minimum switching frequency under which all voltage constraints on the SMs are satisfied. As the loading level on the converter increases, additional switching events are generated and the solution of the LIOP is to yield the gating signals to ensure the voltage constraints are still met and the switching loss is reduced. The LIOP is approximated as a series of Lagrangian relaxation linear programming sub-problems. Each of the sub-problems is then shown to have integrality property and can be solved using the subgradient technique. The solution time is a polynomial function of the number of SMs and the number of voltage constraints in each arm of the converter. The quality of the solution is ε-optimal and the corresponding gating signals for each SM are generated by a proposed two-level coordinated control scheme. The feasibility of the proposed optimization method is demonstrated through simulation study performed on a practical 201-level $\pm$200kV/400MW MMC-HVDC system model constructed in a real-time digital simulator (RTDS) platform. Results of the simulation indicate that the tolerance on the voltage difference between any pair of SMs has to be adjusted when the MMC operates at the determined optimum switching.

INDEX TERMS Modular multilevel converter, nearest level modulation, switching frequency optimization, linear integer optimization problem, subgradient method.

I. INTRODUCTION

Modular multilevel converter (MMC) has gained increasing acceptance in high voltage direct current (HVDC) power transmission schemes [1]–[3]. MMC-HVDC has several advantages over conventional HVDC: it contributes to lower harmonic distortions, it allows independent control of real and reactive power flows on the ac side, it can achieve fast recovery after fault, it avoids the need to provide communications between converter stations for power regulation, the transmission corridor is significantly reduced when compared to HVAC transmission scheme of the same power transmission capacity, among others [3]–[5]. For these reasons, there are more than twenty installed and planned MMC-HVDC projects in China alone. For example, in order to provide alternative power supply routes for some islands in the eastern part of China, several 100-MW level pilot projects in Shantou, Zhoushan and Xiamen have been commissioned and put into successful commercial operation. Renewable energy sources, such as wind and solar power generators are also connected to terminals of these MMC-HVDC stations.

As can be seen from the literature on MMC-HVDC systems, the nearest level modulation (NLM) technique is most widely used among step-wise modulation methods [6]. Experimental and field testing results indicate that under rated power operating condition, the losses of a MMC-HVDC station are higher than those seen in conventional HVDC schemes [7]. The losses elevate the operating temperature of the converter which in turn increase the rate of reduction in the lifetime of the converter. In the MMC-HVDC scheme,

The associate editor coordinating the review of this manuscript and approving it for publication was Dragan Jovcic.

the converter valve consists of series connected submodules (SMs), and the losses in the valve typically account for more than 50% of the station's total loss [8]. The switching losses within the converter valve, which include those of the IGBT, are proportional to the SM switching frequency [9]. Due to thermal safety consideration, the switching frequency should be limited to below (say) 230 Hz [10], [11]. To optimize the switching frequency in order to increase the lifetime of the power converter and at the same time, ensure acceptable MMC-HVDC performance is a challenging task and has received much research interest.

Specifically, safe MMC-HVDC operations require the voltages across the SMs to be maintained within acceptable range. A change in the current flow through an arm of the converter, due to variations in the external grid operating conditions for example, will induce variations in the SM voltages. The gating signals to the SMs, and therefore the switching frequency, may have to be adjusted to ensure the voltages will still be within the acceptable range. A converter model constructed based on the average value of the SM voltages cannot take into account the differences between the voltages of the SMs during the switching period [12]. Therefore, such a model is unsuitable for use in the determination of the optimum switching frequency. Recognizing this shortcoming, much research attention has been directed toward designing methods to balance the SM voltages. The conventional method proposed in [1], [2] requires the SM voltages and the direction of the arm current flow to be monitored. Based on their voltage levels, the SMs are sorted into order which then determines the SMs to be switched in or out in each control period. Unfortunately this may result in excessively high switching frequency. To overcome this shortcoming, Tu *et al.* developed a reduced switching-frequency voltage balance algorithm [13] in which the number of the SMs in the on-state will change in accordance to a reference voltage. However, the possible occurrence of SM voltage deviation within each control period has not been considered. Wang *et al.* proposed an alternative algorithm which involves comparing the SM voltages against pre-set upper and lower voltage thresholds [14]. Unfortunately there could be situations whereby the voltage of an SM is just within the threshold levels in one control period, and the switching in of this SM in the next control period would cause the voltage across this SM to exceed the thresholds. Ilves *et al.* proposed a predictive sorting algorithm, with the view to achieve a trade-off between the switching frequency and voltage ripple by evenly distributing the estimated voltage change among all the SMs [15]. Similarly, a hybrid SM voltage prediction-based method was used in [16] to reduce the switching frequency. The effectiveness of this method depends strongly on the pre-set acceptable voltage deviation limit, with the result that the conventional sorting method used in [1], [2] has to be applied when the predicted SM voltage deviation is greater than the pre-set limit. With the same objective as in [15], [16], the authors of [10] had proposed a voltage balancing method in which additional SMs will be utilized to reduce both the switching frequency and the voltage deviations. In a later work, the authors of [17] proposed an alternative voltage-balancing scheme through tracking the difference between the maximum and minimum SM voltages in the converter and from which the number of SMs to be kept in reserve to balance the voltage difference is determined. In contrast to the above approaches, Hassanpoor *et al.* formulated the determination of the switching sequence of the SMs as the solving of an optimization problem [18]. In order to reduce the solution time to obtain the optimum switching sequence, a heuristic method named CTBoptimized was suggested. Generally for such a combinatorial optimization problem, heuristic method can find the feasible approximation solution within a reasonable time but the quality of the solution is difficult to assess [19].

From the above discussion, it is clear there is still considerable scope in investigating SM switching scheme for the NLM-based MMC. In this aspect, the present work aims to develop an analytical approach to determine the optimum switching sequence of the MMC, while meeting pre-specified voltage constraints concurrently. The paper is organized as follows. Steady-state analysis of the MMC-HVDC system is provided in Section II. In Section III, the mathematical formulation pertaining to the optimum switching is established in the form of a linear integer optimization problem (LIOP). The optimization is to be carried out in conjunction with meeting constraints developed from voltage quality considerations. In order to reduce the computation burden, a subgradient-based Lagrangian relaxation linear programming problem is re-formulated from the LIOP. A numerical technique to determine an ε-optimal solution for each control period is developed and incorporated into a proposed two-level switching control scheme in Section IV. Section V verifies the efficacy of the proposed approach through simulation study. The main findings are then summarized in Section VI.

II. STEADY STATE ANALYSIS OF MMC OPERATIONS

A. A BRIEF DESCRIPTION OF NLM METHOD

The topologies of a three-phase MMC and the associated half-bridge SM are shown in Figure. 1. At any time, the dc-side voltage U_{dc} can be maintained at an acceptable level through the appropriate switching on/off of the N series-connected SMs in each phase simultaneously. The switching pattern would depend on the power transfer level.

Without any loss of generality, phase "a" of the MMC under the inverter operating mode is considered herewith. Henceforth, the subscripts a, u and l are to indicate the respective quantities of phase a, the upper and lower arms of the MMC. Suppose the sinusoidal modulation signal is used. The number of SMs in the "ON" state, denoted as n_u and n_l of the upper and lower arms respectively, can be expressed as [20],

$$n_u(t) = N/2 - round[MN\sin(\omega t)/2] \quad (1)$$

$$n_l(t) = N/2 + round[MN\sin(\omega t)/2] \quad (2)$$

where the function round [y] returns with the nearest integer value to y. M is the MMC voltage modulation ratio which is defined as,

$$M = 2u_{vm}/U_{dc} \tag{3}$$

u_{vm} is the peak value of the MMC ac-side phase voltage $u_v(t)$.

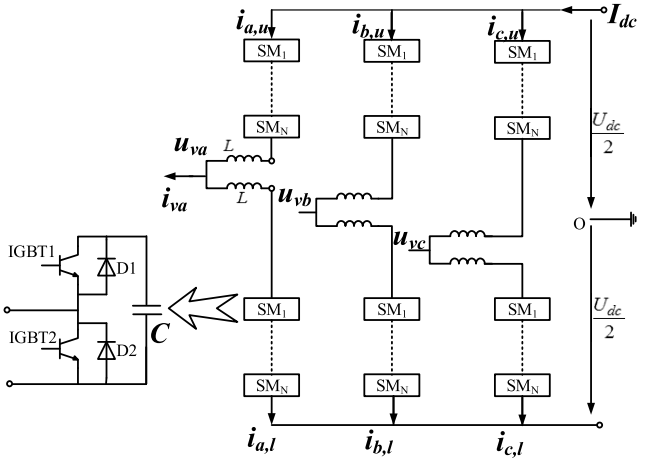

FIGURE 1. Topologies of the modular multilevel converter and that of the half-bridge submodule.

Denote the SM rated voltage as U_{c0}, from (1) and (2), $u_v(t)$ can be written in the stair-case form,

$$u_v(t) = [n_u(t) - n_l(t)]U_{c0}/2 = U_{c0}round[MN\sin(\omega t)/2] \tag{4}$$

The dotted line is the sinusoidal reference voltage. The stair-case $u_v(t)$ will intercept the reference voltage a number of times. The corresponding electrical angle at which an intercept occurs is denoted as θ_i. From (1) and (2), the total number of such intercepts N_θ in one power cycle can be shown to be

$$N_\theta = 4round[MN/2] \tag{5}$$

It can be seen from (5) that N_θ increases with the product MN. The maximum value of N_θ is $2N$ when $M = 1$. However, in order to maintain $u_v(t)$ to an acceptable quality level, M is typically between 0.8 and 0.9.

B. VOLTAGE ACROSS THE SM

Although various circulating current suppressing controllers (CCSCs) have been proposed for MMC [21]–[24], there still exit harmonic components in the arm currents $i_{x,y}$ where $x = a, b, c$ and $y = u, l$, particularly the dominant second-order harmonics. Again without any loss of generality, consider the upper arm current $i_{a,u}(t)$ in Figure. 1. This current contains the dc (I_{dc}), the fundamental (i_{va}) and the second-order ($i_{aZ,u}$) harmonics components:

$$\begin{aligned} i_{a,u}(t) &= I_{dc,u} + i_{va}(t) + i_{aZ,u}(t) \\ &= I_{dc}/3 + I_{vm}\sin(\omega t + \varphi)/2 + I_{aZ,u}\sin(2\omega t + \theta) \end{aligned} \tag{6}$$

In (6), ω, I_{vm} and φ are the power frequency, the peak value of the ac phase current and the power factor angle respectively. $I_{aZ,u}$ and θ are the magnitude and phase angle of the second-order harmonics current. The harmonics current is governed by the voltage difference between the arms and it circulates between the arms. $i_{aZ,u}$ cannot be expressed in a closed form.

The power loss P_{TON} of an IGBT in the on-state is given by

$$P_{TON} = V_{CE}I_{au,rms} \tag{7}$$

where V_{CE} is the forward voltage drop across the IGBT and $I_{au,rms}$ is the rms value of $i_{a,u}(t)$. In order to reduce the loss and to maintain the power quality on both the ac- and dc- sides to acceptable levels, the ratio of the rms value of the second-order harmonics current and $I_{au,rms}$ should not be greater than an upper bound α:

$$I_{aZ,rms}/I_{au,\mathrm{rms}} \leq \alpha \tag{8}$$

Typically $\alpha = 15\%$ [3]–[5].

If the j^{th} SM is in the "ON" state over the ith control period, the current flow $i_{a,u}(t)$ will induce a voltage change across this SM which is described by

$$U_{c,ij}(iT_c) = U_{c,ij}((i-1)T_c) + \frac{1}{C}\int_{(i-1)T_c}^{iT_c} i_{a,u}(t)dt \tag{9}$$

In (9), T_c is the control period of the power electronic devices controller and more shall be said about it in the next Section. $U_{c,ij}((i-1)T_c)$ is the voltage at the end of the previous control period. The voltage quality of $U_{c,ij}$ can be kept to acceptable level if the second-order harmonics current can be suitably controlled.

III. SM SWITCHING FREQUENCY OPTIMIZATION

A. PROBLEM FORMULATION

The main objective of achieving the optimum switching is to maximize the lifetime of the SM. The lifetime can be expressed in terms of the number of thermal cycles (N_f) the SM has undergone before the SM fails to function. N_f is significantly impacted by the average junction temperature of the IGBT, which in turn has certain non-linear relationships with the power losses generated in the SM. Among the various power losses, the IGBT switching loss is proportional to the switching frequency [9], [10]. Therefore, it would be most desirable if the switching frequency can be reduced while at the same time, the dc and ac voltage qualities can be maintained to acceptable levels. This would lead to a decrease in the switching loss and the IGBT junction temperature, and the lifetime of the SM can be expected to increase. Unlike the heuristic voltage balance approaches proposed in [13], [18], the present work propose to establish the mathematical framework under which the switching frequency can be optimized.

Consider one arm of the MMC station. Let N_{sw} denotes the total number of switching in all the SMs in the arm, within the period T_N of one power cycle. If N_{sw} is to be minimized,

then the objective function reflecting this design aim can be written as

$$MinN_{sw} = \sum_{i=0}^{T_N/T_c-1} \sum_{j=1}^{N} \left| x_{i+1,j} - x_{i,j} \right| \tag{10}$$

In (10), $x_{i,j}$ is an integer variable: it has the value of "1" if the j^{th} SM in the i^{th} control period is in the "ON" state. Conversely, $x_{i,j}$ would be "0" if the SM is in the "OFF" state. $x_{0,j}$ is the initial state of the j^{th} SM. Clearly the minimum value of the objective function depends on the combinations of $x_{i,j}$. Note that there are NT_N/T_c such integer variables in one power cycle. The design task becomes one of solving a combinatorial optimization problem.

With any SM switching pattern, however, it is also necessary to ensure the harmonic distortion level of $u_v(t)$ meets with stipulated quality standards while the SMs are more fully utilized. In order to do so, it is derived in [21] that the control period T_c should be selected to satisfy the bounds

$$\pi\sqrt{2MN}/T_N \le 1/T_c \le \pi MN/T_N \tag{11}$$

If $1/T_c$ is less than the upper bound, the voltage reference in Figure 2 will change by more than one level in some control periods. Thus at least two SMs will change their states. On the other hand, if $1/T_c$ is less than the lower bound, there will not be enough voltage levels to approximate the reference voltage such that some of the SMs may not change their states even in one power cycle.

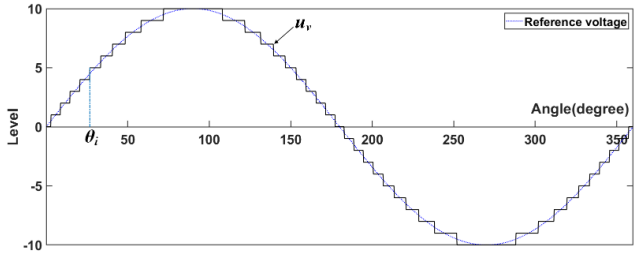

FIGURE 2. Illustrates a 21-level $u_v(t)$.

Equation (10) indicates that N_{sw} is obtained by summing up the number of changes in the ON/OFF states of all the SMs in all the control periods within the power cycle. Unlike all heuristic methods reported in the literatures, the objective function (10) provides a quantitative measure of the focus of the design study: that the number of switching is to be minimized.

Although the function (10) is nonlinear and non-differentiable, (10) can be transformed into a linear form through the introduction of an additional N_{TN}/T_c binary integer variables $x_{i,j+N}$, as follows:

$$MinN_{sw} = \sum_{i=0}^{T_N/T_c-1} \sum_{j=1}^{N} x_{i,j+N} \tag{12}$$

where $x_{i,j+N}$ satisfies,

$$\left| x_{i+1,j} - x_{i,j} \right| \le x_{i,j+N} \tag{13}$$

Equation (13) can in turn be expressed as linear equations (14) and (15):

$$x_{i+1,j} - x_{i,j} - x_{i,j+N} \le 0 \tag{14}$$

$$-x_{i+1,j} + x_{i,j} - x_{i,j+N} \le 0 \tag{15}$$

In the i^{th} control period and in view of (1), the objective function must satisfy the linear equality constraint

$$n_{u,i} = \sum_{j=1}^{N} x_{i,j} \tag{16}$$

If the control period T_c is sufficiently short, the number of SMs in the ON-state ($n_{u,i}$) may not change until the electrical angle θ_i shown in Figure 2 changes in the next control period. However, as shown by (9), as the current flow through an SM changes, the voltage across the SM will vary. In response to this, the gating signals to the SM will have to be adjusted in order to avoid excessive levels of voltage imbalance and circulating current. Therefore, the individual value of $x_{i,j}$ may have to change within a control period. A closer analysis is therefore warranted, as follows.

Consider firstly the voltage $U_{c,ij}$ across the j^{th} SM in the i^{th} control period. If the SM is in the ON-state, i.e., $x_{i,j} = 1$, then $U_{c,ij}$ will differ from that of the previous control period. Based on (9) and noting that the control period T_c is typically very short, the difference in the voltage across the SM over two consecutive control periods can be approximated by the constant coefficient c_i given by (17):

$$c_i = \frac{1}{C} \int_{(i-1)T_c}^{iT_c} i_{a,u}(t)dt \approx \frac{T_c}{C} i_{a,u}((i-1)T_c) \tag{17}$$

Denote the initial voltage across the j^{th} SM as $U_{c,1j}(0)$. From (17), $U_{c,ij}$ is then given by

$$U_{c,ij} = U_{c,1j}(0) + \sum_{i=1}^{i} c_i x_{i,j} \tag{18}$$

It has been shown in [18] that $U_{c,ij}$ will be within acceptable level if $U_{c,ij}$ does not deviate from its rated value U_{c0} by more than the amount $dU_{c,0}$,

$$\left| U_{c,ij} - U_{c0} \right| \le dU_{c0} \tag{19}$$

Typically, $d = 0.1$ [1]–[3]. Substituting (18) into (19), the linear voltage inequality constraint (19) can be expressed in terms of $x_{i,j}$ as follows:

$$U_{c,1j}(0) + \sum_{i=1}^{i} c_i x_{i,j} - (1+d)U_{c0} \le 0 \tag{20}$$

$$-U_{c,1j}(0) - \sum_{i=1}^{i} c_i x_{i,j} - (1-d)U_{c0} \le 0 \tag{21}$$

Henceforth, $x_{i,j}$ are termed the binary integer decision variables because different sequence of gating signals will cause $U_{c,ij}$ to deviate from its rated value in varied ways. The deviations will impact the amount of the circulating current flow between the SMs. Indeed, the constraint (8)

alluded to earlier is to reflect the need to restraint the level of the circulating current.

Therefore in this work, it is proposed that in order to impose a limit on the magnitude of the circulating current, the difference in the voltages across any two SMs in the i^{th} control period shall be kept to within the tolerance β_{Uc0}, i.e.,

$$\left|U_{c,il} - U_{c,im}\right| \leq \beta U_{c0} \quad 1 \leq (l, m) \leq N \tag{22}$$

As will be illustrated in Section V, the choice of the value of β will depend on the power transfer level through the MMC. Under light power transfer condition, larger value of β can be selected.

Substituting (18) into (22), the voltage difference constraint (22) can be expressed in terms of the integer decision variables $x_{i,j}$ as,

$$U_{c,1l}(0) + \sum_{i=1}^{i} c_i x_{i,l} - U_{c,1m}(0) - \sum_{i=1}^{i} c_i x_{i,m} - \beta U_{c0} \leq 0 \tag{23}$$

$$-U_{c,1l}(0) - \sum_{i=1}^{i} c_i x_{i,l} + U_{c,1m}(0) + \sum_{i=1}^{i} c_i x_{i,m} - \beta U_{c0} \leq 0 \tag{24}$$

The above derivation allows the problem formulation to be stated mathematically as follows: the determination of the optimum switching of the SMs involves solving a linear integer optimization problem (LIOP). It can be seen from (10) and (12) that there are $2NT_N/T_c$ binary integer decision variables $x_{i,j}$ which must meet the T_N/T_c linear equality constraints given by (16), as well as the $(4 + N(N-1))\, NT_N/T_c$ linear inequality constraints given by (14), (15), (20), (21), (23) and (24).

As far as the authors are aware, this is a new approach to determine the optimum switching of a MMC-HVDC system in which practical operational constraints on the circulating current and SM voltage level have also been taken into consideration.

B. IDEAL SWITCHING FREQUENCY

Next, consider the inequality relationship

$$|a - b| \leq |a| + |b| \tag{25}$$

The equality relationship in (25) will be satisfied only when $ab \leq 0$. It therefore follows that the objective function (10) will have the lower bound shown on (26):

$$\sum_{i=0}^{T_N/T_c-1} \left| \sum_{j=1}^{N} (x_{i+1,j} - x_{i,j}) \right| \leq \min N_{sw} = \sum_{i=0}^{T_N/T_c-1} \sum_{j=1}^{N} \left| x_{i+1,j} - x_{i,j} \right| \tag{26}$$

Substituting (16) into the left hand side of (26), one obtains

$$\sum_{i=0}^{T_N/T_c-1} \left| n_{u,i+1} - n_{u,i} \right| \leq \min N_{sw} = \sum_{i=0}^{T_N/T_c-1} \sum_{j=1}^{N} \left| x_{i+1,j} - x_{i,j} \right| \tag{27}$$

Equation (27) shows that the lower bound equals to the sum of the absolute values of the difference in the number of SM in the ON-state within two consecutive control periods and over one cycle of the power frequency. If the voltage inequality constraints (19) and (22) are not considered, $\left|n_{u,i+1} - n_{u,i}\right| = 0$ between two θ_i, and $\left|n_{u,i+1} - n_{u,i}\right| \geq 1$ if the next control period reaches a new θ_i. Therefore, if the total number of θ_i shown in Figure 2 is N_θ, as given by (5), the ideal number of switching $N_{sw,ideal}$ in one power cycle will be independent of T_c, *viz.*,

$$N_{sw,ideal} = N_\theta \tag{28}$$

Whence the ideal average switching frequency f_{sw} of each SM is

$$f_{sw} = N_\theta / (NT_N) \tag{29}$$

Bearing in mind the presence of the second-order harmonics current as shown in (6), this ideal switching frequency can be achieved only under certain light load conditions when the SM voltage quality is acceptable. As the power transfer level increases, however, the arm current $i_{a,u}(t)$ will increase too. The variation of the voltage across a SM from one control period to the next control period, denoted as c_i in (17), will assume a larger value. In order to satisfy the voltage constraints (20) and (21), the SM may not be able to maintain at the "ON" state for as long a duration as when under the light power transfer condition. Hence, there will be additional switching events and the switching frequency will increase. A careful simulation study must be carried out to arrive at an acceptable trade-off between acceptable voltage quality and the switching frequency.

The problem formulation given in this Section has two advantages over the reported heuristic methods. First, the physical meaning of the objective function (10) is obvious. The optimum switching frequency is reached once the total number of switching is minimized, subject to the constraints pertaining to the circulating current and the SM voltage deviation. This is in contrast to the heuristic approaches where no explicit objective function has been given and hence, the solution may vary with the heuristic rules. Second, the optimal switching frequency can be evaluated analytically for both off-line and on-line applications. There are well-established methods to determine the optimal solution of the LIOP, for example, the optimization toolbox of MATLAB can be used. On the other hand, none of the heuristic methods can verify the generated gating signals are indeed optimal.

IV. OPTIMAL SWITCHING CONTROL SCHEME

A. DETERMINATION OF THE OPTIMAL SWITCHING

Section III provides sufficient information from which a mathematical framework can be developed to determine the optimal switching of the MMC, in the form of the optimal $x_{i,j}$. A series of gating signals are generated for $i_{a,u}(t)$ based on the determined $x_{i,j}$. However, numerical optimization techniques, such as the branch-and-bound (B&B) method, have exponential time complexity and in this instance, can

only be used for the off-line planning and analysis studies of the MMC-HVDC system. As pointed out in Section I, heuristic methods have been widely used to determine the switching strategy for on-line applications [19], although it is unclear if the determined switching strategy is indeed optimum. Faced with these dilemma, various endeavors have been made in the past few decades to obtain the approximate optimal solution for such combinatorial problem. Among the possible numerical techniques to determine the approximate optimal solution to the LIOP such as the linear relaxation method [25], random rounding method [26] and Chvátal-Gomory cutting plane method [27], the subgradient method based on Lagrangian relaxation is simple, robust and can be readily applied [28], [29]. Most importantly, subgradient method has a solid theoretical foundation and that the near-optimal or feasible solution for the LIOP can be obtained in polynomial time.

For the MMC-HVDC system, the gating signals for the IGBT must be generated within one control period. Unfortunately, the computational burden of the formulated LIOP (10) is such that this is not possible, based on the current state of development of digital signal processing technology, if the calculation window is as large as one power cycle. An effective approach adopted in the present work to reduce the calculation time is to divide the original LIOP into T_N/T_c integer programming (IP) sub-problems. Such divide and conquer approach has also been widely used in the field of on-line management systems. Based on the problem formulation discussed in Section III, the optimal solution for each of the IP problem can be found but in order to further accelerate the calculation, the IP problem is reformulated into one in which an approximate optimum solution can be found. The main challenge lies in the integrality property of the approximate solution. This approach and the issue of integrality of the solution are dealt with next, as follows.

Let the optimal solution for each of the IP problems be N_{IP}. The IP problem can be approximated by relaxing the binary decision variables to a real value between 0 and 1. For the i^{th} control period, this approximation can be represented as a linear programming (LP) problem for which the optimal solution is N_{LP}:

$$(\text{LP})N_{LP} = \min FX \tag{30}$$

$$s.t.\ AX \leq B \tag{31}$$

$$GX \leq HX \in [0, 1]^{2N} \tag{32}$$

In the LP problem, $X = (x_1, \ldots, x_{2N})^{\mathrm{T}}$, $F = (O_{1\times \mathrm{N}}, I_{1\times \mathrm{N}})$ where O and I represent the zero and identity matrices respectively. Matrices A, B, G and H are obtained from the constraints discussed in Section III. The details are shown in the Appendix.

LP could provide a lower bound solution for the IP problem [25]. If $N_{LP} \neq N_{IP}$, there will be an integrality gap between the LP and IP solutions. Some rounding methods have to be used to round off the fractional element in the decision variables X to a proper integer. This may increase the complexity of the computational process. To mitigate this, it is proposed the constraints (31) be added to (30) with the introduction of a non-negative Lagrangian multiplier vector Λ. The Lagrangian relaxation linear programming (LRLP) problem is thus obtained from the LP problem (30)

$$(LR\text{LP})N_{LRLP} = \min FX + \Lambda(AX - B)$$

$$s.t.\ GX \leq HX \in [0, 1]^{2N} \tag{33}$$

It is shown in the Appendix that G is a total unimodular matrix. This special mathematical structure indicates that all the decision variables for (33) will be integers and the derived LRLP problem will have the integrality property. Thus the rounding process can be avoided. The quality of the solution depends on the value of the augmented Lagrangian term $\Lambda(AX\text{-}B)$ in the new objective function. $\Lambda(AX\text{-}B)$ is the difference in the optimum solution values obtained from the IP and that of the LRLP. If $\Lambda(AX - B) = 0$, the LRLP problem will lead to the optimal solution of the IP problem, i.e., $N_{LRLP} = N_{IP}$. Otherwise, the LRLP would provide an ε-optimal solution for each of the IP problems where $N_{LRLP} - N_{IP} = \varepsilon > 0$.

B. SUBGRADIENT SOLUTION TECHNIQUE FOR THE LRLP PROBLEM

As the term $\Lambda(AX\text{-}B)$ in (33) is not differentiable when the number of SMs in the ON-state changes, the subgradient search technique described in [30] can be used to determine the optimal solution of the LRLP. Again, taking the upper arm of phase a as an example, this calculation process involves the following 5 steps:

Step one: In each control period, the arm current $i_{a,u}(t)$ and the corresponding SM voltages $U_{c,ij}(t)$ are monitored. According to the ac reference voltage, the number of n_u can be calculated from (1). In addition, the initial Lagrangian multiplier vector $\Lambda(0)$ in (33) is set to 0.

Step two: Based on (17), all the SM voltages at the end of this control period $U_{c,ij}(t + T_c)$ can be estimated:

$$U_{c,ij}(t + T_c) \approx U_{c,ij}(t) + i_{a,u}(t)T_c/C \tag{34}$$

If any pair of the predicted SM voltages does not satisfy the voltage difference tolerance constraint (22), the SM which has the higher voltage will be switched off if the SM is charging. Conversely, the SM with the lower voltage will be switched off if it is discharging. The corresponding equality constraints, expressed in the form shown in the Appendix as (A.9) and (A.10) will be added to (33).

Step three: At the k^{th} iteration, solve the LRLP problem (33). The solutions $N_{LRLP}(k)$ and $X(k)$ are stored. $S(k) = AX\text{-}B$ is then a subgradient vector.

Step four: If every element of $S(k)$ is 0 or if k reaches the pre-set iteration limit, the optimal or ε-optimal solution is found from the minimum N_{LRLP} among all the k stored N_{LRLP} values. This is because N_{LRLP} does not decrease monotonously with k[25]. The first N values of X corresponding to the minimum N_{LRLP} will be used as the gating signals sent to the SMs.

Step five: If every element of $S(k)$ is not 0 or if k has not reached the iteration limit, update the Lagrangian multiplier vector Λ, using the general updating equation provided in [25]

$$\Lambda(k+1) = \max(O, 2\Lambda(k)S(k)) \tag{35}$$

Return to Step three.

The flow chart showing the above five steps is included on Figure 3.

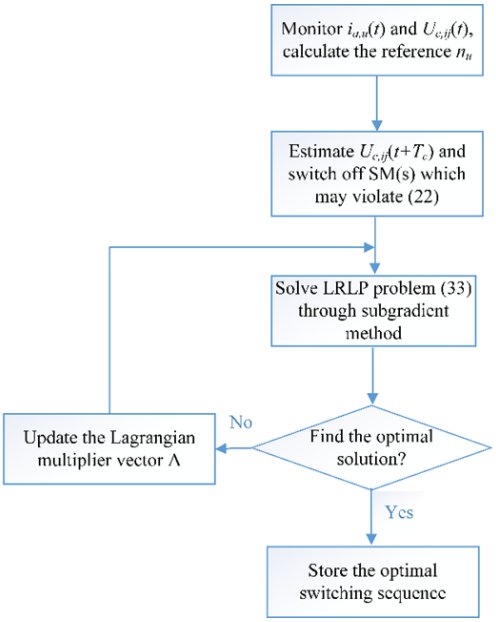

FIGURE 3. Flow chart showing the computational procedure of solving the LRLP problem via the subgradient method.

Compared to the heuristic methods reported in the literatures, the above subgradient solution approach is based on a theoretical analysis of finding an optimal or ε-optimal solution of the original IP problem. Although it is essentially a first order optimization method, a near-optimal solution for the LRLP problem can be found after a few iterations. If l pairs of the SM voltage differences are greater than the pre-set tolerance βU_{dc0}, the subgradient method will involve up to $O(2kN(2N+1+l))$ arithmetic operations [31]. This polynomial time approach will permit the real-time application of the generated switching signals for the SMs, as shown next.

C. TWO-LEVEL COORDINATED OPTIMAL SWITCHING CONTROL SCHEME

The above development permits a new two-level coordinated control strategy to generate and adjust the gating signals of the MMC-HVDC. The strategy involves control actions at the station and at the device levels of the MMC.

Figure 4 shows the two-level optimal switching control scheme whereby the station-level control scheme includes the well-documented CCSC for the MMC [4], [21], [22]. The current i_s and the voltage u_s at the point of common coupling (PCC) in the figure can be used to track the real and

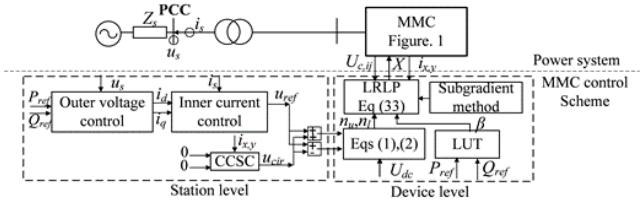

FIGURE 4. Schematic of the proposed two-level coordinated optimal mmc switching control scheme.

reactive power references P_{ref} and Q_{ref}. The outer voltage control loop will generate the d-q axis reference current signals i_d and i_q for the inner current loop. Through the feed-forward control method, the d and q components can be decoupled and the corresponding voltage reference signal u_{ref} can be generated. In addition, in order to eliminate the second-order harmonics circulating currents among the three phase legs of the converter station, the signal corresponding to the average arm current of each phase leg is sent to the CCSC. Similar to the inner current control loop, another voltage reference signal u_{cir} is generated to produce the zero d and q axes reference voltage signals to eliminate the harmonic currents.

The reference signals u_{ref} and u_{cir} are combined to form the inputs to the "Device-level" control scheme. Using (1) and (2), n_u and n_l for each control period will be determined for the upper and lower arms of the MMC. Based on the measured arm current $i_{x,y}$ and the voltages $U_{c,ij}$ across the SMs, the LRLP block will determine the optimal X of each control period using the subgradient method. The optimal or ε-optimal gating signal X is then sent to all the SMs.

In addition, the voltage difference tolerance β must be carefully selected such that the inequality (8) will be satisfied. A straightforward method would be to adjust β on-line until the second-order harmonics current level in $i_{x,y}$ is acceptable. However, this is computationally expensive. Instead it is proposed that a series of off-line simulation be carried out at pre-selected power transfer levels. The purpose of these studies is to determine the maximum value of β such that the resulting second-order harmonics current satisfies (8). A look-up table (LUT) can then be constructed based on the maximum values of β obtained at these pre-selected power transfer levels. The LUT is incorporated in Figure 4 such that the maximum value of β at any given power transfer level can be determined through the interpolation of the data-set contained in the LUT. In this way, the resulting LRLP solution will yield the minimum switching frequency at the given power transfer level.

V. ILLUSTRATIVE EXAMPLES

A. SYSTEM PARAMETERS

The intent of this Section is to demonstrate the proposed scheme can achieve the real-time optimal switching of the MMC-HVDC. In order to do so, a 201-level NLM-based ±200kV/400MW point-to-point MMC-HVDC project in China is studied through steady state and real-time dynamic

simulations. The circuit parameters for the two identical conversion stations are listed in Table 1. The results of the simulation study presented in this Section will be those pertaining to the upper arm of phase "a" of the MMC, operating under the inverter mode.

TABLE 1. Main circuit parameters of the two-terminal ±200 kV MMC-HVDC system.

Rated capacity S_N (MVA)	400
External equivalent ac source voltage (kV)	230
External equivalent ac source inductance (mH)	1
Transformer ratio	230/205
Transformer reactance on the secondary side (Ω)	0.01+j0.15
Number of SMs per arm N	200
SM rated voltage U_{c0} (kV)	2
SM capacitor C (F)	0.013
Arm inductance (mH)	90
dc bus rated voltage U_{dc} (kV)	±200
dc cable length (km)	15
SM voltage deviation ratio d	0.1
Second-order harmonics current ratio α	0.15
Voltage modulation ratio M	0.9
MMC control period T_c (μs)	100
Power period T_N (s)	0.02
IGBT module	ABB5SNA1200E250100

B. COMPARISON OF THE STEADY STATE RESULTS USING THE B&B AND PROPOSED METHODS

Suppose the MMC-HVDC system initial power transfer level P is 250MW, the station dc bus voltage U_{dc} and the terminal voltage U_{c0} of each of the SM at the initial time are maintained at the rated values. From the values of M, N and T_N listed in Table 1, the acceptable range of the control period T_c obtained from (11) should be between 33μs and 300μs. In the following analysis, T_c is selected at the value of 100μs. As T_c is short, the voltage variation coefficient c_i over each control period can be evaluated using (17). Without considering the second-order harmonics in the arm current, Table 2 compares the optimal solutions of the LIOP problem obtained using the B&B method with that using the subgradient method discussed in Section IV. The iteration limit used in the latter method is set to 3. An Inter®Core^{TM}i7-6700 CPU@3.4GHz with 16GB RAM computer was used in carrying out the steady state simulation. The simulation tool is MATLAB.

Without considering any voltage constraints and using (29), it can be readily seen that the ideal number of switching per power cycle $N_{sw,ideal}$ is 360, yielding the ideal switching frequency of 90 Hz. However, Table 2 shows that this lower bound can only be achieved if the voltage difference tolerance β is greater than 0.045. In fact, Table 2 shows that when β is decreased to 0.025, both optimization methods have resulted in the corresponding switching number N_{sw} being more than 600 and the switching frequencies of over 150Hz. The consequence would be an increase in the IGBT switching loss when compared to the case of $\beta = 0.045$. N_{sw} obtained by the subgradient method is slightly higher than the more accurate optimal solution yielded by the B&B method. This is due to the rounding effect generated in (A.12) when SMs of very similar voltage levels are rounded to the same integers. The difference in N_{sw} is less than 3% when $\beta = 0.025$.

TABLE 2. Comparison of the optimal switching solutions obtained using the B&B and proposed method AT P = 250MW and d = 0.1.

β	Method	N_{sw}	f_{sw}(Hz)	Solution time (s)
0.025	B&B	608	152	59.39
	subgradient	626	156.5	3.28
0.035	B&B	466	116.5	57.51
	subgradient	474	118.5	3.23
0.045	B&B	360	90	56.86
	subgradient	360	90	3.22

It is interesting to note from Table 2 that the solution time of the subgradient method is some 18 times less than that based on the B&B method. As discussed in the Appendix, the voltage difference inequality constraints will be activated only when the voltage difference of any pair of SMs are greater than the pre-set tolerance. The approximation used in (A.5) has reduced the search space significantly in the optimization search process. This accounts for the much reduced solution time.

From this steady state study, the subgradient method is shown to be able to generate solution of great accuracy and is computationally efficient. However, the second-order harmonics circulating currents have yet to be considered. The feasibility of the determined optimal switching scheme must be verified from the real-time dynamic simulation of the MMC-HVDC scheme, as follows.

C. REAL-TIME DYNAMIC SIMULATION OF OPTIMAL SWITCHING

In order to verify the efficacy of the on-line optimal switching control scheme discussed in Section IV, a point to point MMC-HVDC benchmark platform is constructed based on the real-time digital simulator (RTDS). Similar like the control scheme shown in Figure. 4, high performance digital processor PXI-8106 is selected as the system level controller. Field-programmable gate arrays (FPGA) PXI-7833R will sample the SM voltages and generate the optimal switching signals for each arm. The detailed platform parameters are given in Table 1. The simulation step is 100μs.

The results of dynamic simulation based on the proposed method are compared with those obtained using the heuristic CTBoptimized solution approach. CTBoptimized has the computational complexity of $O(NlogN)$ and details of this method can be found in [18].

In this study, suppose the maximum allowable SM voltage ripple is to be kept to less than 2.5% of the SM rated voltage, that is, 50V in this example. Figure 5 shows the simulation results obtained by the CTBoptimized method whereby it can be seen from Figure 5a that the SM voltage ripple is indeed

less than 50V. The figure shows that there are 8012 switching events in 10 cycles. So the average switching frequency determined using the CTBoptimized method is about 200 Hz. As the SM voltage deviation is well constrained, further harmonic analysis also confirms the level of the second-order harmonics level in the arm current shown in Figure 5b satisfies (8).

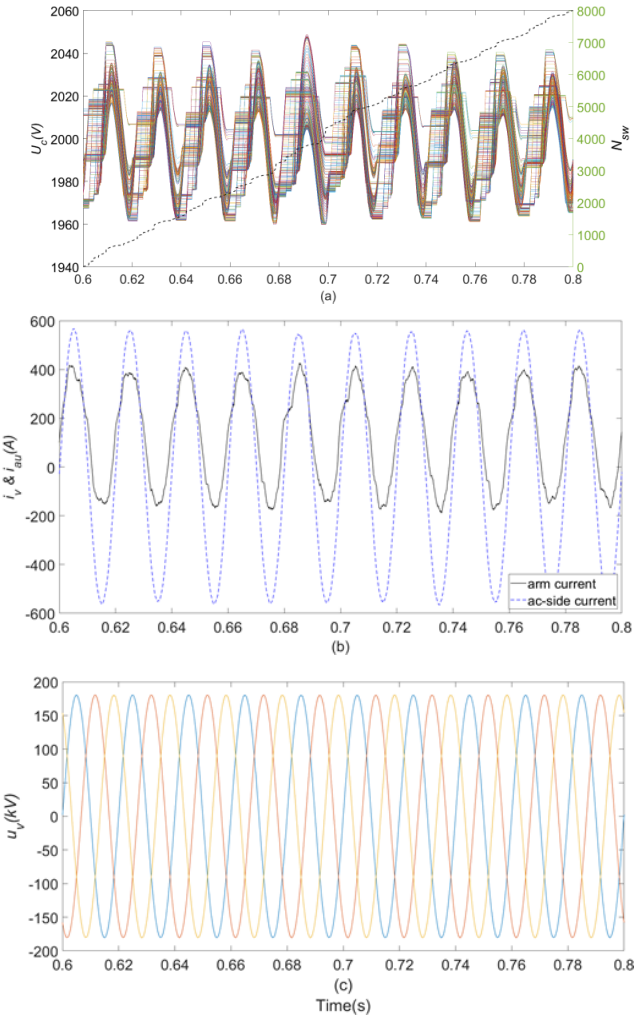

FIGURE 5. Simulation results obtained by the CTBoptimized method: (a) SM voltages U_C and switching number N_{SW}; (b) MMC ac-side phase "a" current i_V and arm current i_{au}; (c) MMC ac-side phase voltages u_V.

If the voltage difference tolerance β is selected as 0.025, Figure 6 shows the simulation results obtained by the proposed subgradient solution method. It can be seen from Figure 6a that the SM voltages U_c are constrained to between 1950V and 2050V. The voltage ripple is also less than the stipulated limit of 2.5% in this case. The total number of switching N_{sw} is 7376, to yield the average switching frequency of 184.4 Hz. Compared to the CTBoptimized method, although the proposed subgradient method requires a longer solution time, it does yield the optimal solution of lower switching frequency while still meeting the SM voltage and second-order harmonics current limits.

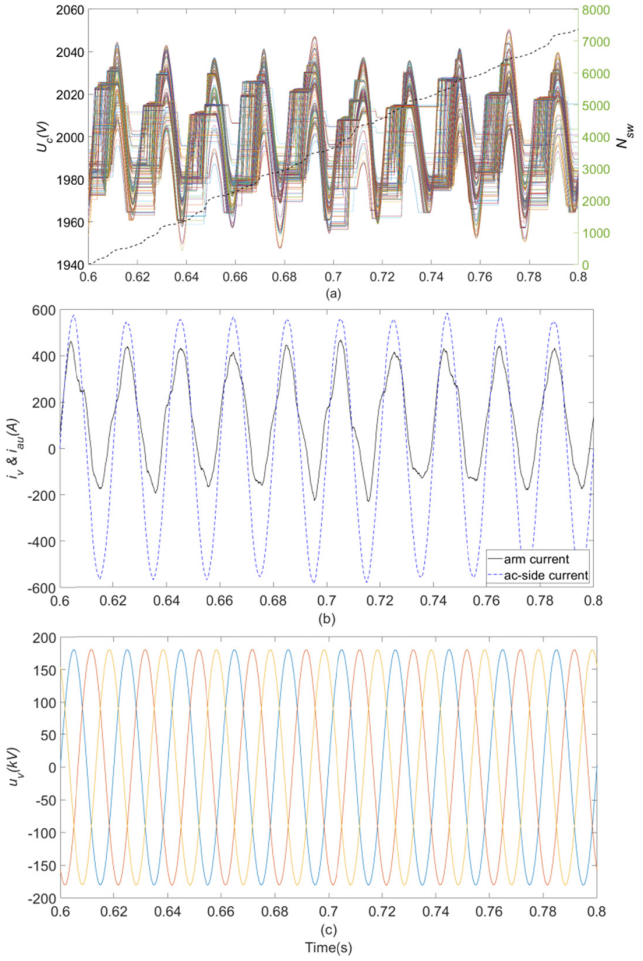

FIGURE 6. Simulation results obtained by the subgradient method: (a) SM voltages U_C and switching number N_{SW}; (b) MMC ac-side phase "a" current i_V and arm current i_{au}; (c) MMC ac-side phase voltages u_V.

The switching frequency determined using the subgradient method is higher than that obtained in the steady state study. This is because the steady-state study does not consider the presence of the second-order harmonics current, whereas by imposing the constraint in the voltage difference between the SMs through the design parameter β, the harmonic level has been restrained to the acceptable level. The voltage constraints are met and the circulating currents are reduced by the CSCC effectively. As shown in Figure 6b, the MMC ac-side current i_v portrays an almost constant amplitude.

Figure 7 shows the arm currents i_{au}, the MMC ac-side current i_v and the number of switching N_{sw} obtained by the subgradient method, when the voltage difference tolerance β is 0.03, 0.045 and 0.05. The number of switchings (switching frequency) in the three cases decreases from 6017 (150.43 Hz) to 5105 (127.63 Hz). However, the arm current and the MMC ac-side current are highly distorted by the circulating current caused by the unbalanced phase leg voltages when $\beta = 0.05$. The second-order harmonics current ratio is greater than the allowable 15%.

From the dynamic simulation results, it can be concluded that by increasing β, the switching frequency and the

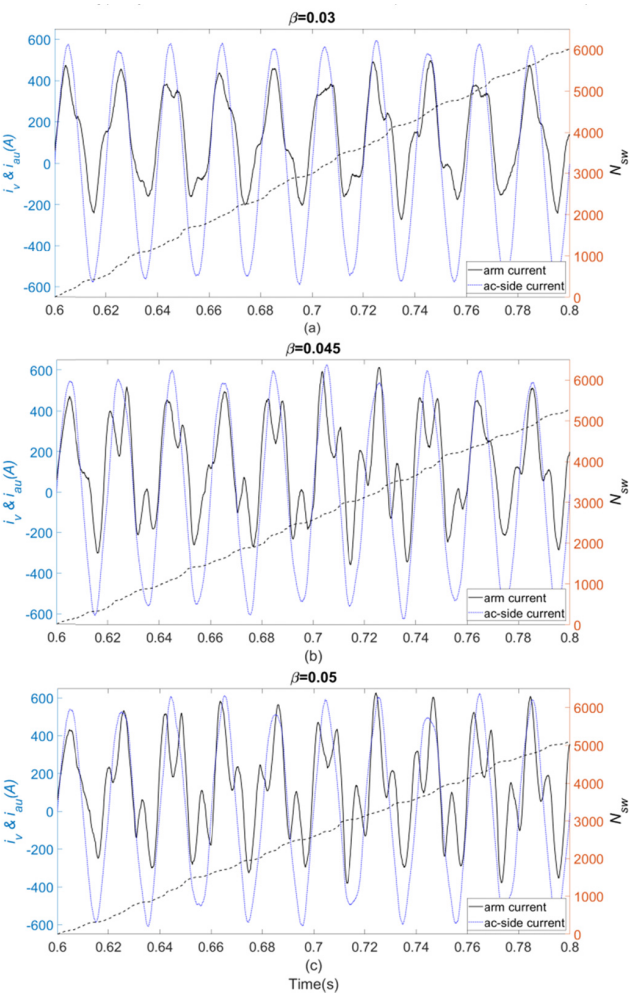

FIGURE 7. Arm current, MMC ac-side phase "a" current and switching number obtained by the subgradient method under different voltage difference tolerance: (a) $\beta = 0.03$; (b) $\beta = 0.045$; (c) $\beta = 0.05$.

switching losses will decrease but at the expense of an increase in the level of the second-order harmonics current. A trade-off between the two conflicting factors can be reached by adjusting β until the ratio of the second-order harmonics current to the arm current ratio is observed to be just less than the pre-specified limit α, as described by (8). For example, suppose when $P = 250$ MW, the maximum acceptable β was found to be 0.045 and the optimal switching frequency was about 131.85 Hz. As the power transfer level increases, the possible voltage difference between any pair of SMs will increase so that β will have to be adjusted to a smaller value. Under light power transfer conditions, on the other hand, the switching frequency can be set close to the ideal switching frequency by selecting a larger β.

D. MMC VALVE LOSSES EVALUATION

The main losses in the MMC are the IGBT turn-on and turn-off losses, and the diode turn-off losses. The total loss, which is the real power difference on the dc and ac sides of the converter valve, can be extracted from the dynamic simulation result. Consider the MMC-HVDC system operates under the light (115 MW), median (250 MW) and heavy (400 MW) power transfer conditions. The IGBT module, with data taken from [32], is assumed to operate at 125°C junction temperature in the simulation. Table 3 summarizes the maximum allowable voltage difference tolerance β, the optimal average switching frequency f_{sw} and the valve power losses ΔP.

TABLE 3. Comparison of the MMC valve total losses per station.

P (MW)	β	f_{sw}(Hz)	ΔP(MW)
115	0.05	95.86	1.5
250	0.045	131.85	2.8
400	0.035	168.51	4.2

The simulation results shown in Table 3 verify that the optimal switching frequency will be very close to the ideal frequency 90 Hz when $\beta = 0.05$ under the light power transfer condition. When the MMC operates under the rated 400 MW power transfer condition, β is chosen as 0.035 in order to guarantee the second-order harmonics current meets with α of 0.15 or less. The SM average switching frequency increases to 168.51 Hz. Although the switching frequency is optimized at each power condition, it is observed that the total valve loss per station is still higher than 1% of the transferred power.

For the purpose of power system operational planning, the results shown on Table 3 can be used to determine the optimum β such that the switching frequency can be minimized while the second-order harmonics current is kept to acceptable level. This will enhance the operational safety and the lifetime of the SM.

VI. CONCLUSION

Unlike existing heuristic methods, an analytical method to obtain the near-optimal switching for the NLM-based MMC-HVDC system has been proposed. The switching frequency can be optimized by solving a LIOP. Analysis shows that there will be an ideal minimum switching frequency when the power transfer level is low and there is no necessity to apply any constraints on the SM voltages in the optimization solution process. At higher power transfer level, however, the voltage difference between the SMs must be constrained to acceptable level even as the SM average switching frequency increases.

It is a time-consuming task to find an accurate optimal solution for the LIOP. In view of this, the present investigation also shows that to find the ε-optimal gating signals for a given power transfer level, the LIOP can be approximated as a series of LRLP problems which have integrality property. The integer decision variables can be generated by the subgradient method in polynomial time. The dynamic simulation results generated by the real-time digital simulator (RTDS) platform show that the voltage tolerance parameter β plays an important role in finding the optimal switching frequency. The setting value of β must be reduced when the power transfer level increases. This will necessitate higher average switching frequency in order to reduce the second-order harmonics current

caused by the unbalanced phase leg voltages. Notwithstanding these encouraging findings, the impacts of the variations in the parametric values of the main circuit parameters of the MMC-HVDC system on the optimal switching frequency would be a fruitful area for future work.

APPENDIX

The inequalities (14) and (15) can be incorporated into (31) such that A and B are given by

$$A = \begin{pmatrix} I_{N\times N} & -I_{N\times N} \\ -I_{N\times N} & -I_{N\times N} \end{pmatrix} \tag{A.1}$$

$$B = \begin{pmatrix} X(0) & -X(0) \end{pmatrix}^T \tag{A.2}$$

In (A.2), $X(0)$ is the initial decision variable vector obtained from the previous control period.

Defining G and H in (32) as,

$$G = (G_1; G_2; G_3)^T, H = (H_1; H; H_3)^T \tag{A.3}$$

where

$$G_1 X = H_1 \tag{A.4}$$

$$G_2 X = H_2 \tag{A.5}$$

$$G_3 X \le H_3 \tag{A.6}$$

From (16), (A.4) can be written as,

$$G_1 = \begin{pmatrix} G_{11} & G_{12} \end{pmatrix} = \begin{pmatrix} I_{1\times N} & O_{1\times N} \end{pmatrix} \tag{A.7}$$

$$H_1 = n_{u,i} \tag{A.8}$$

The voltage difference tolerance constraints given in (23) and (24) will be activated only when the voltage difference between any two SMs is greater than the pre-set value βU_{c0}. If l constraints are activated, the $N(N-1)$ inequality constraints in one control period can be simplified to l equalities. In (A.5), G_2 and H_2 can be written as

$$G_2 = \begin{pmatrix} G_{21} & G_{22} \end{pmatrix} = \begin{pmatrix} I_{l\times N} & O_{l\times N} \end{pmatrix} \tag{A.9}$$

$$H_2 = (O_{l\times 1}) \tag{A.10}$$

From (20) and (21), (A.6) can be simplified to

$$G_3 = \begin{pmatrix} G_{31} & G_{32} \end{pmatrix} = \begin{pmatrix} I_{N\times N} & O_{N\times N} \\ -I_{N\times N} & O_{N\times N} \end{pmatrix} \tag{A.11}$$

$$H_3 = \begin{cases} [floor(\dfrac{(1+d)U_{c0} - u_{c,ij}(0)}{c_i})_{1\times N}, O_{1\times N}]^T, & if\ c_i \ge 0 \\ [floor(\dfrac{u_{c,ij}(0) - (1-d)U_{c0}}{-c_i})_{1\times N}, O_{1\times N}]^T, & if\ c_i < 0 \end{cases} \tag{A.12}$$

In (A.12), the function floor[y] rounds y to the nearest integer towards $+\infty$.

From (A.7) to (A.12), G and H are $(1+l+2N)\times 2N$ and $2N \times 1$ integer matrices respectively. G can be written as,

$$G = \begin{pmatrix} G_1 \\ G_2 \\ G_3 \end{pmatrix} = \begin{pmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \\ G_{31} & G_{32} \end{pmatrix} = \begin{pmatrix} I_{1\times N} & O_{1\times N} \\ I_{(l+N)\times N} & O_{(l+N)\times N} \\ I_{N\times N} & O_{N\times N} \\ -I_{N\times N} & O_{N\times N} \end{pmatrix} \tag{A.13}$$

Suppose g is an $m \times m$ submatrix of G. The determinant of g, $Det(g)$, will be 0 if one of columns of g is selected from G_{12}, G_{22} and G_{32}. $Det(g)$ will be either 1 or -1 if all rows and columns of g are selected from G_{21} or G_{31}. $Det(g)$ will be 0 if one of columns of g has two opposite-sign non-zero entries (1 and -1). If all rows and columns of g are selected from G_{11} and G_{21}, g_{1j} which is 1 will be the only no-zero entry in the j^{th} column. The determinant of g can be expressed as,

$$Det(g) = (-1)^{1+j} Det(I_{(m-1)\times(m-1)}) = (-1)^{1+j} \tag{A.14}$$

$Det(g)$ in (A.14) will be 1 or -1 when j is odd or even.

From the above, the determinant of G will be 0 or ± 1. That is, G is a total unimodular matrix. Therefore, only integer solutions can satisfy (A.3). The proposed LRLP problem given in (33) has integrality property.

REFERENCES

[1] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.
[2] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.
[3] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1631–1656, Dec. 2017.
[4] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.
[5] M. Kurtoğlu, F. Eroğlu, A. O. Arslan, and A. M. Vural, "Recent contributions and future prospects of the modular multilevel converters: A comprehensive review," *Int. Trans. Electr. Energy Syst.*, vol. 29, no. 3, p. e2763, Mar. 2019.
[6] P. M. Meshram and V. B. Borghate, "A simplified nearest level control (NLC) voltage balancing method for modular multilevel converter (MMC)," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 450–462, Jan. 2015.
[7] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.
[8] Z. Zhang, Z. Xu, and Y. Xue, "Valve losses evaluation based on piecewise analytical method for MMC–HVDC links," *IEEE Trans. Power Del.*, vol. 29, no. 3, pp. 1354–1362, Jun. 2014.
[9] H. Wang, Z. He, G. Tang, X. Zhang, and J. Cao, "Analytical approximate calculation of losses for modular multilevel converters," *IET Gener., Transmiss. Distrib.*, vol. 9, no. 16, pp. 2455–2465, Dec. 2015.
[10] Z. Li, F. Gao, F. Xu, X. Ma, Z. Chu, P. Wang, R. Gou, and Y. Li, "Power module capacitor voltage balancing method for a ±-350-kV/1000-MW modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 3977–3984, Jun. 2016.
[11] F. Hahn, M. Andresen, G. Buticchi, and M. Liserre, "Thermal analysis and balancing for modular multilevel converters in HVDC applications," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1985–1996, Mar. 2018.
[12] J. Peralta, H. Saad, S. Dennetiere, J. Mahseredjian, and S. Nguefeu, "Detailed and averaged models for a 401-level MMC–HVDC system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1501–1508, Jul. 2012.
[13] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.
[14] S. Wang, T. Liu, X. Huang, and Y. Yu, "Capacitor voltage balancing control with reducing the average switching frequency in MMC," *J. Eng.*, vol. 2019, no. 16, pp. 2375–2380, Mar. 2019.
[15] K. Ilves, L. Harnefors, S. Norrga, and H. P. Nee, "Predictive sorting algorithm for modular multilevel converters minimizing the dpread in the submodule capacitor voltages," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 440–449, Jan. 2015.

[16] J. Qin and M. Saeedifard, "Reduced switching-frequency voltage-balancing strategies for modular multilevel HVDC converters," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2403–2410, Oct. 2013.
[17] Y. Luo, Z. Li, L. Xu, X. Xiong, Y. Li, and C. Zhao, "An adaptive voltage-balancing method for high-power modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2901–2912, Apr. 2018.
[18] A. Hassanpoor, A. Roostaei, S. Norrga, and M. Lindgren, "Optimization-based cell selection method for grid-connected modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2780–2790, Apr. 2016.
[19] G. Ausiello, P. Crescenzi, and G. Gambosi, *Complexity and Approximation: Combinatorial Optimization Problems and Their Approximability Properties*, 2nd ed. Berlin, Germany: Springer, 1999, ch. 10, sec. 1, pp. 322–325.
[20] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3702–3713, Aug. 2013.
[21] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 298–306, Jan. 2011.
[22] S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An improved control system for modular multilevel converters with new modulation strategy and voltage balancing control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 358–371, Jan. 2015.
[23] D. Samajdar, T. Bhattacharya, and S. Dey, "A reduced switching frequency sorting algorithm for modular multilevel converter with circulating current suppression feature," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10480–10491, Nov. 2019.
[24] S. Yang, P. Wang, Y. Tang, M. Zagrodnik, X. Hu, and K. J. Tseng, "Circulating current suppression in modular multilevel converters with even-harmonic repetitive control," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 298–309, Jan. 2018.
[25] M. L. Fisher, "Comments on—The lagrangian relaxation method for solving integer programming Problems," *Manage. Sci.*, vol. 50, no. 12, pp. 1872–1874, Dec. 2004.
[26] A. Federgruen and G. van Ryzin, "Probabilistic analysis of a generalized bin packing problem and applications," *Oper. Res.*, vol. 45, no. 4, pp. 596–609, Aug. 1997.
[27] I. Aliev and A. Letchford, "Iterated Chvátal-gomory cuts and the geometry of numbers," *SIAM J. Optim.*, vol. 24, no. 3, pp. 1294–1312, Jan. 2014.
[28] K. Holmberg, "Experiments with primal–dual decomposition and subgradient methods for the uncapacitatied facility location problem," *Optimization*, vol. 49, nos. 5–6, pp. 495–516, Jan. 2001.
[29] C. Lin, H. Wei, W. Hou, and J. Tan, "Linear inequalities convex transformation for optimal reactive power flow model based on MISOCP relaxations," *IET Gener., Transmiss. Distrib.*, vol. 12, no. 7, pp. 1589–1594, Apr. 2018.
[30] C. Araya-Sassi, P. A. Miranda, and G. Paredes-Belmar, "Lagrangian relaxation for an inventory location problem with periodic inventory control and stochastic capacity constraints," *Math. Problems Eng.*, vol. 2018, pp. 1–27, Oct. 2018.
[31] G. Nemhauser, A. Kan, and M. Todd, *Optimization*. Amsterdam, The Netherlands: Elsevier, 1989, pp. 130–133, ch. 2, sec. 7.
[32] B. Backlund, U. Schlapbach, and R. Fischer. (2009). *Application Note: Applying IGBTs*. [Online]. Available: http://www.abb.com

YONGHUI LI received the B.E. and M.Sc. degrees in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 1994 and 1998, respectively, and the Ph.D. degree in power engineering from Nanyang Technological University (NTU), Singapore, in 2006.

From 2006 to 2008, he was a Transmission Planning Engineer of SP Power Grid, Singapore. Since 2008, he has been an Associate Professor with the School of Electrical Engineering and Automation, Wuhan University, Wuhan. His research interests include power quality and power system planning.

JUN YANG (Member, IEEE) received the Ph.D. degree from the Huazhong University of Science and Technology, China, in 2006. He joined Wuhan University, Wuhan, China, where he is currently a Professor. His research interests include power system security, electrical vehicles, and smart grid.

SAN SHING CHOI received the B.E. and Ph.D. degrees in electrical engineering from the University of Canterbury, Christchurch, New Zealand, in 1973 and 1976, respectively. He was with the New Zealand Electricity Department, Wellington, New Zealand, the National University of Singapore, Singapore, the State Energy Commission of Western Australia, Perth, WA, Australia, and Nanyang Technological University, Singapore. He is currently an Adjunct Professor with the Curtin University of Technology, Perth, and the Queensland University of Technology, Brisbane, QLD, Australia. His research interests include power system control, renewable, and energy storage systems.

QIANG ZHAO graduated from Northeast Electric Power University, China. He joined the China Electric Power Research Institute, Beijing, China, where he is currently an Engineer. His research interests include power systems and smart grid.