IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received December 10, 2020, accepted December 28, 2020, date of publication December 31, 2020, date of current version January 11, 2021.

Digital Object Identifier 10.1109/ACCESS.2020.3048387

An Interleaved Zero-Voltage Zero-Current Switching High Step-Up DC-DC Converter

BINXIN ZHU, (Senior Member, IEEE), SHIHUAN CHEN, YAO ZHANG, AND YU HUANG
Hubei Provincial Research Center on Microgrid Engineering Technology, College of Electrical Engineering and New Energy, China Three Gorges University, Yichang 443002, China

Corresponding author: Shihuan Chen (chenshihuan88@163.com)

This work was supported in part by the National Natural Science Foundation of China under Grant 51707103, and in part by the Natural Science Foundation of Hubei Province under Grant 2020CFB754.

ABSTRACT An interleaved zero-voltage zero-current switching (ZVZCS) high step-up DC-DC converter is proposed for modern photovoltaic power generation systems. The proposed converter can achieve high voltage conversion gain without operating under extreme duty cycles. The voltage conversion gain can be readily adjusted by selecting different numbers of the diode-capacitor multiplier (DCM) cells in the circuit at the design stage. Moreover, with the passive snubber circuit in the proposed converter, all power switches and diodes in the DCMs can achieve zero-voltage turn-off and zero-current turn-on, which effectively reduces switching losses and increases the overall converter efficiency. The operational principles and analysis of the performance analysis with two DCMs are presented for demonstrative purpose. The effectiveness of the proposed ZVZCS DC-DC converter is validated using an 800W experimental prototype.

INDEX TERMS Interleaved, passive snubber circuit, ZVZCS, high step-up, high efficiency.

I. INTRODUCTION

Photovoltaic (PV) technology has gained a growing research interest over the past decade due to the ever-increasing energy consumption supplied by fossil fuels and the resulting environmental issues [1]–[4]. In a typical PV power generation system, the output voltage of the PV panels is usually limited up to 50V, while it needs to be stepped up to about 380–760V so as to meet the requirement of the inverters for grid connection. As conventional DC/DC converters such as the boost converter cannot achieve such a high voltage gain, an inverter with a transformer is generally needed. This increases the size and cost of the entire system and does not follow the recent rising trend towards high-frequency, high-efficiency, and light-weighted PV systems.

High-gain DC-DC converters have thus received much research attention especially for PV applications [5]–[9]. It is well known that in order to lower the capital cost and increase the energy conversion efficiency of the system, it is necessary to increase the switching frequency of the converter. However, there are insurmountable difficulties for high-power converters to work with high switching frequency at present [10]–[13]. The major reasons are the considerable switching losses and increased electromagnetic interference (EMI), which in turn lead to the decrease of the overall efficiency and increase of the volume and weight of the radiator [14], [15]. To solve the problems, soft-switching techniques are indispensable and widely adopted in practical applications. Various snubber circuits are designed to decrease the switching loss and mitigate the EMI problems of the electronic devices [16]–[27].

The snubber circuits can be generally categorized as the active and the passive types based on whether the active switches that can achieve soft switching are used. A variety of active schemes have been proposed in existing works [16]–[22]. For example, a novel soft-switching full-bridge converter with an additional secondary switch and a non-dissipative energy recovery snubber is proposed in [16]. The converter can achieve zero-voltage zero-current switching for all of the primary switches and the rectifier diodes within the entire load range. This circuit like the converter discussed in [17] has a complex topology with the high number of components. More importantly, this converter has an additional diode in the main power path resulting in high conduction losses. A zero-voltage-transition (ZVT) non-isolated bidirectional converters are presented in [18]. The auxiliary circuit is composed of a coupled inductor, a converter main inductor and two auxiliary switches, leading

The associate editor coordinating the review of this manuscript and approving it for publication was Huai-zhi Wang.

to a complex control method. In [19]–[22], soft switching of the main power switches is achieved by utilizing various resonance active schemes. Although the switching loss can be significantly reduced and the overall efficiency can be effectively increased such schemes are expensive and less reliable since additional components for active snubber circuits are needed. Furthermore, the auxiliary active switch itself also makes the control and drive scheme more complicated. In contrast, for the passive soft switching schemes, only passive components are used. Hence, the corresponding circuits are easier to design, more reliable, and more cost-effective. These advantages make the passive soft switching an attractive approach in various applications [23]–[27].

In this connection, a novel zero-voltage zero-current switching (ZVZCS) high step-up DC-DC converter with passive snubber circuit has been proposed in this paper on the converter proposed in [28]. The passive snubber circuit includes two absorption capacitors, two small inductors, and five auxiliary diodes, so that all power switches and diodes in the diode-capacitor multipliers (DCMs) can achieve zero voltage turn-off and zero current turn-on. This feature can reduce the turn-off and turn-on losses and thus overall efficiency of the converter is effectively increased.

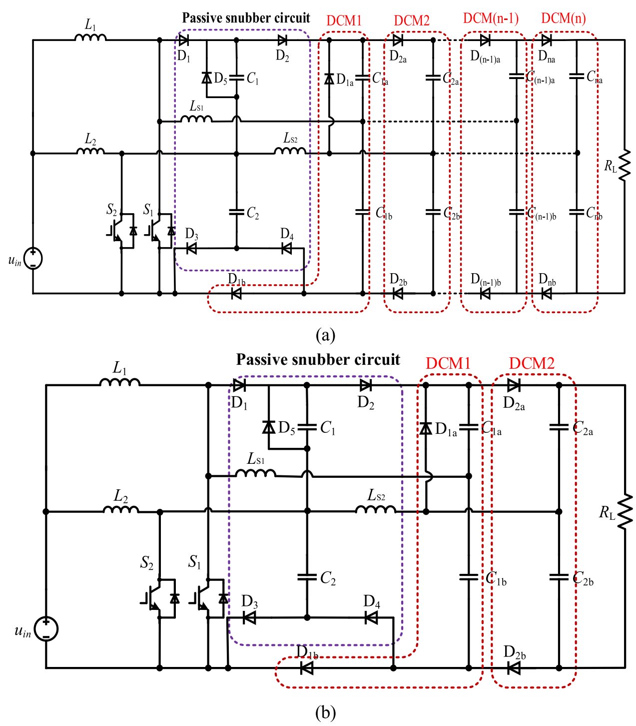


FIGURE 1. Topologies of the proposed converter: (a) with *n* DCM; (b) with 2 DCMs.

II. PERFORMANCE ANALYSIS

A. OPERATIONAL PRINCIPLES

The general topology of the proposed ZVZCS high step-up DC-DC converter with a passive snubber circuit and n DCMs are shown in Fig. 1(a). In the figure, u_{in} and R_L represents the input voltage source and the load, respectively. Capacitors C_1 and C_2, diodes D_1, D_2, D_3, D_4, and D_5, as well as inductors L_{S1} and L_{S2} constitute the passive snubber circuit for the switches S_1 and S_2. Furthermore, each DCM cell consists of two capacitors C_{ia} and C_{ib}, and two diodes D_{ia} and D_{ib}, where $i = 1, 2, \ldots, n$ denotes the index of the DCM.

In order to simplify the analysis, we first present the operational principle of the proposed converter with two DCMs as shown in Fig. 1(b), since the procedure can be readily extended for the configuration with more DCMs. In addition, the following assumptions are made to facilitate the analysis, i.e.,

(i) The capacitors of C_{1a}, C_{1b}, C_{2a}, and C_{2b}, and the inductors of L_1 and L_2 are assumed to be large enough so that the voltages u_{in}, u_{C1a}, u_{C1b}, u_{C2a}, u_{C2b}, and u_o as well as the inductor currents i_{L1} and i_{L2} can be considered constant during normal operation.

(ii) All devices are ideal, i.e., the effects of parasitic parameters are negligible.

(iii) An interleaved strategy is adopted to control the switching of S_1 and S_2. The duty cycles of the two switches are $D_{S1} > 0.5$, $D_{S2} > 0.5$.

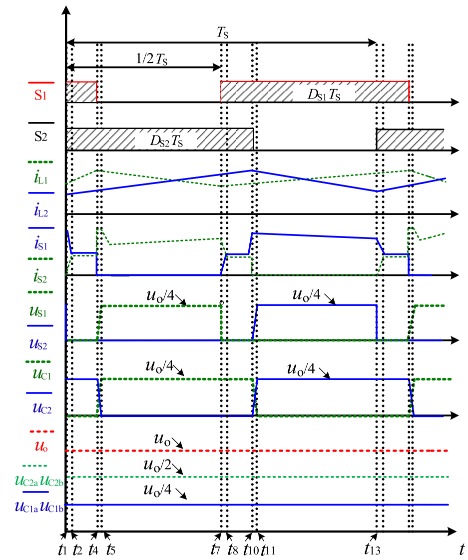


FIGURE 2. Key waveforms during one switching period.

Fig. 2 shows the key waveforms of the proposed converter during one switching period T_S, including the on-off states S_1 and S_2 of the switches, the inductor currents i_{L1} and i_{L2}, switch currents i_{S1} and i_{S2}, switch voltage u_{S1} and u_{S2}, voltages u_{C1} and u_{C2} of the capacitors in the snubber circuit, output voltage u_o, and voltages u_{C1a}, u_{C1b}, u_{C2a}, and u_{C2b} of the capacitors in the DCMs. According to the on-off states of the switches, the operation of the converter can be divided into twelve modes during one switching period and the equivalent circuits for different modes are depicted in Fig. 3. The descriptions of the modes are given as follows.

Mode 1 [$t_1 - t_2$]: The switches S_1 and S_2 are both working in the ON-state. At the moment of conduction of the

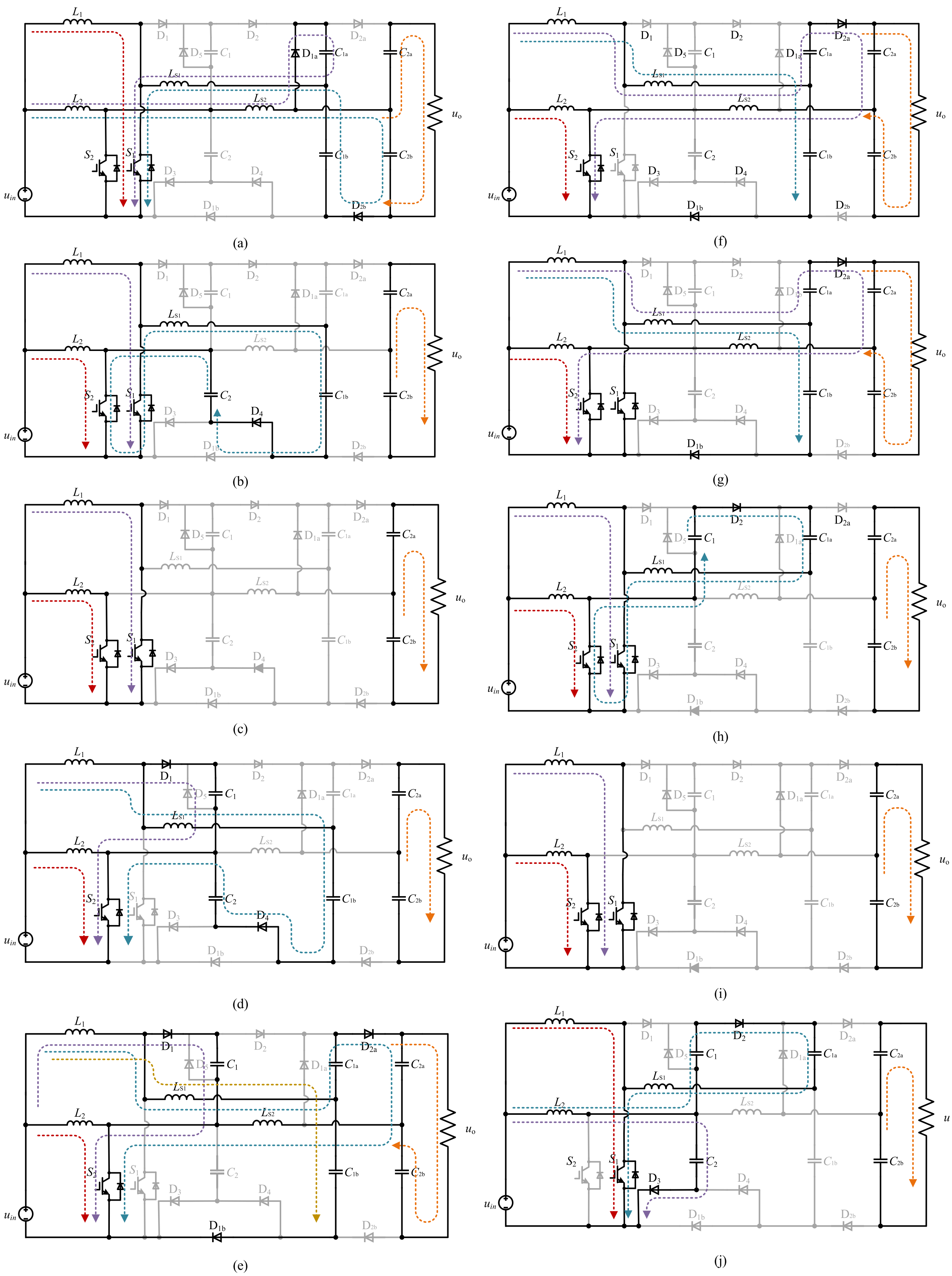
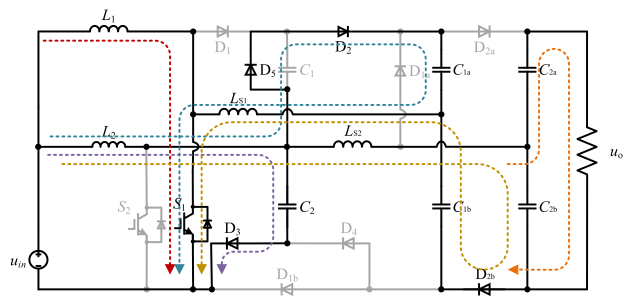
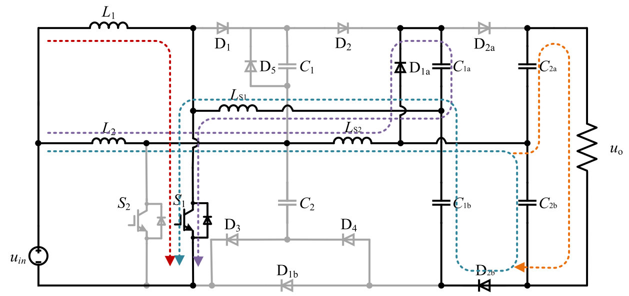


FIGURE 3. Equivalent circuit of the twelve modes of the proposed converter:(a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5; (f) Mode 6; (g) Mode 7; (h) Mode 8; (i) Mode 9; (j) Mode 10; (k) Mode 11; (l) Mode 12.



(k)



(l)

FIGURE 3. ***(Continued.)*** **Equivalent circuit of the twelve modes of the proposed converter:(a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5; (f) Mode 6; (g) Mode 7; (h) Mode 8; (i) Mode 9; (j) Mode 10; (k) Mode 11; (l) Mode 12.**

switch S_2, since the current of L_{S2} cannot change suddenly, the energy in the inductor L_{S2} will discharge through the loop circuit as shown in Fig.3(a). The switch S_2 is turned on with zero-current.

Mode 2 [$t_2 - t_3$]: Due to the discharge of the capacitor C_{1b} in the above process, the voltage u_{C2} of capacitor C_1 is greater than the voltage u_{C1b} of capacitor C_{1b}, diode D_4 is turned on at t_2. At this time, C_2, C_{1b} and L_{S1} form a resonance unit, C_2 is discharged, meanwhile C_{1b} and L_{S1} are charged, capacitors C_{2a} and C_{2b} are discharged to the output end, and all diodes except D_4 are turned off.

Mode 3 [$t_3 - t_4$]: When capacitor C_2 is discharged and capacitor C_{1b} is charged until $u_{C2} = u_{C1b}$, inductor L_{S1} current drops to zero, diode D_4 is turned off at t_3, input voltage source is charged to inductor L_1 and L_2 through switch S_1 and S_2, respectively. The capacitors C_{2a} and C_{2b} are discharged to the output end, and all diodes are OFF.

Mode 4 [$t_4 - t_5$]: Switch S_1 is turned OFF at t_4, during the short period of turning off, C_1 controls the voltage rising rate, which achieves zero-voltage turn-off. At this time, diode D_1 is turned on, part of the current of inductor L_1 charges the capacitor C_1 through diode D_1, and then flows back to the input voltage source through S_2, and the other part flows back to the input voltage source through L_{S1}, C_{1b}, D_4, C_2 and S_2. In this process, L_{S1} and C_{1b} are charged, meanwhile C_2 is discharged; capacitors C_{2a} and C_{2b} are discharged to the output end, and all diodes except D_1 and D_4 are turned off.

Mode 5 [$t_5 - t_6$]: The voltage u_{C1} of capacitor C_1 has not yet risen to u_{C1b}, part of the current of inductor L_1 continues to charge the capacitor C_1 through diode D_1, capacitor C_2 is discharged to $u_{C2} = 0$, diode D_4 is turned off at t_5, and the other part of the current of inductor L_1 passes through inductor L_{S1} when passing through the node between C_{1a} and C_{1b}, and part of it flows back to the input voltage source through C_{1a}, D_{2a}, C_{2a}, L_{S2} and S_2. In this process, L_{S1} and C_{2a} are charged, C_{1a} is discharged, and inductor L_{S2} is reversely charged; the second part of the current flows back to the input voltage source through R, C_{2b}, L_{S2} and S_2. In this process, C_{2b} is discharged and L_{S2} is reversely charged; the third part of the current, when passing through the node between C_{1a} and C_{1b}, flows through C_{1b}, D_{1b}, and then the input voltage source. At this stage, C_{1b} is being charged.

Mode 6 [$t_6 - t_7$]: When C_1 and C_{1b} are charged to $u_{C1} = u_{C1b}$, C_1 is fully charged, diode D_1 is turned off at t_6, other behaviour is the same as Mode 5. This state ends at t_7.

Mode 7 [$t_7 - t_8$]: The switches S_1 and S_2 are both working in the ON-state. At the moment of conduction of the switch S_1, since the current of L_{S1} cannot change suddenly, the energy in the inductor L_{S1} will discharge through the loop circuit as shown in Fig. 3(g). The switch S_1 is turned on with zero-current.

Mode 8 [t_8-t_9]: Due to the discharge of the capacitor C_{1a} in the above process, the voltage u_{C1} of the capacitor C_1 is higher than the voltage u_{C1a} of the capacitor C_{1a}, diode D_2 is turned on at t_8. At this time, C_1, C_{1a}, and L_{S1} form a resonance unit, capacitor C_1 is discharged, meanwhile capacitor C_{1a} is charged, and inductor L_{S1} is reversely charged. The capacitors C_{2a} and C_{2b} are discharged to the output end, and all diodes except D_2 are turned off.

Mode 9 [$t_9 - t_{10}$]: When capacitor C_1 is discharged and capacitor C_{1a} is charged until $u_{C1} = u_{C1a}$, the current of the inductor L_{S1} drops to zero, diode D_2 is turned off at t_9, input voltage source is charged to inductors L_1 and L_2 through S_1 and S_2, respectively. The capacitors C_{2a} and C_{2b} are discharged to the output end, and all diodes are OFF.

Mode 10 [$t_{10} - t_{11}$]: Switch S_2 is turned OFF at t_{10}, during the short period of turning off, C_2 controls the voltage rising rate, which achieves zero-voltage turn-off. At this time, diode D_3 is turned on, part of the current of inductor L_2 charges capacitor C_2 through diode D_3, and then flows back to the input voltage source, and the other part flows back to the input voltage source through L_{S1}, C_{1a}, D_2, C_1 and S_1. In this process, C_{1a} is charged, L_{S1} is reversely charged and C_1 is discharged; capacitors C_{2a} and C_{2b} are discharged to the output end, and all diodes except D_2 and D_3 are turned off.

Mode 11 [$t_{11} - t_{12}$]: When capacitor C_1 discharges to u_{C1} =0, diode D_2 turns off. At this time, the voltage u_{C2} of capacitor C_2 has not yet risen to u_{C1a}, while D_3 is in ON state, charging capacitor C_2. When $u_{C2} = u_{C1a}$, diodes D_5 and D_2 are turned on at t_{11}, the first part of the current of inductor L_2 continues to charge capacitor C_2 through diode D_3; the second part charges inductor L_{S1} and capacitor C_{1a} through diodes D_5 and D_2; the third part flows back to the input voltage source through L_{S2}, C_{2b}, D_{2b}, C_{1b}, L_{S1} and S_1; the fourth part flows back to the input voltage source through L_{S2}, C_{2a}, R, D_{2b}, C_{1b}, L_{S1} and S_1. In this process, L_{S2}, C_{1a}

and C_{2b} are charged and L_{S1} is reversely charged, capacitors C_{1b} and C_{2a} are discharged.

Mode 12 [$t_{12} - t_{13}$]: When the current of inductor L_{S1} is equal to the current of inductor L_2, capacitor C_2 is fully charged, and diodes D_2, D_3, and D_5 are turned off. When capacitors C_{1a} and C_{2b} are charged and capacitor C_{1b} is discharged to $u_{c2b} = u_{c1a} + u_{c1b}$, diode D_{1a} is turned on at t_{12}, and the current of inductor L_2 passes through L_{S2} and a part of it flows back to the input voltage source through D_{1a}, C_{1a}, L_{S1}, and S_1. When the other part of the current flows through the node between C_{2a} and C_{2b}, on the other hand, part of which flows back to the input voltage source through C_{2b}, D_{2b}, C_{1b}, L_{S1} and S_1. Another part flows back to the input voltage source through C_{2a}, R, D_{2b}, C_{1b}, L_{S1} and S_1.

B. VOLTAGE GAIN

By applying the volt-second balance approach to the inductors L_1 and L_2 and considering $D = D_{S1} = D_{S2}$, the following relationships can be obtained in the steady state, i.e.,

$$\begin{cases} u_{in} \cdot D = (u_{C1b} - u_{in}) \cdot (1-D) \\ u_{in} \cdot D = (u_{C2a} - u_{C1a} - u_{in}) \cdot (1-D) \end{cases} \tag{1}$$

$$\begin{cases} u_{in} \cdot D = (u_{C1a} - u_{in}) \cdot (1-D) \\ u_{in} \cdot D = (u_{C2b} - u_{C1b} - u_{in}) \cdot (1-D) \end{cases} \tag{2}$$

From (1) and (2), we obtain the expressions of the capacitor voltages and the output voltages as functions of the input voltage and the duty cycle, i.e.,

$$\begin{cases} u_{C1a} = \dfrac{u_{in}}{1-D} \\ u_{C1b} = \dfrac{u_{in}}{1-D} \end{cases} \tag{3}$$

$$\begin{cases} u_{C2a} = u_{C1a} + u_{C1b} \\ u_{C2b} = u_{C1a} + u_{C1b} \end{cases} \tag{4}$$

Therefore:

$$u_o = u_{C2a} + u_{C2b} = 2(u_{C1a} + u_{C1b}) = \frac{4u_{in}}{1-D} \tag{5}$$

Based on (5), the voltage conversion ratio M can be obtained as:

$$M = \frac{u_o}{u_{in}} = \frac{4}{1-D} \tag{6}$$

By extending the above analysis for a converter with n DCMs, we can readily obtain a generic expression of the voltage conversion ratio:

$$M = \frac{u_o}{u_{in}} = \frac{2n}{1-D} \tag{7}$$

C. VOLTAGE STRESS OF THE SEMICONDUCTOR DEVICES

The voltages of the switches S_1 and S_2 and the diodes D_{1a}, D_{1b}, D_{2a}, and D_{2b} are expressed as u_{S1}, u_{S2}, u_{D1a}, u_{D1b}, u_{D2a}, and u_{D2b} respectively. Using (3), we have:

$$u_{S1} = u_{C1b} = \frac{u_{in}}{1-D} \tag{8}$$

$$u_{S2} = u_{C1a} = \frac{u_{in}}{1-D} \tag{9}$$

$$u_{D1b} = \frac{u_{in}}{1-D} \tag{10}$$

$$u_{D1a} = u_{D2a} = u_{D2b} = \frac{2u_{in}}{1-D} \tag{11}$$

Similarly, for n DCMs, the voltage stress on S_1, S_2, D_{1a}, D_{1b}, D_{2a}, and D_{2b} are

$$\begin{cases} u_{S1} = u_{C1b} = \dfrac{u_{in}}{1-D} \\ u_{S2} = u_{C1a} = \dfrac{u_{in}}{1-D} \end{cases} \tag{12}$$

$$\begin{cases} u_{D1b} = \dfrac{u_{in}}{1-D} \\ u_{D1a} = u_{D2a} = \cdots = u_{Dna} = u_{Dnb} = \dfrac{2u_{in}}{1-D} \end{cases} \tag{13}$$

D. INPUT CURRENT RELATIONSHIP

As the inductor currents i_{L1} and i_{L2} are continuous and their current ripples are neglected, we only consider the DC components I_{L1} and I_{L2} for further analysis. Similarly, by neglecting the current ripple, the DC component I_{in} of the input current i_{in} is considered. In addition, we denote the peak currents of the diodes by I_{D1ap}, I_{D2ap}, I_{D1bp}, and I_{D2bp}, respectively, while I_{D1a}, I_{D2a}, I_{D1b}, and I_{D2b} are the average currents of D_{1a}, D_{2a}, D_{1b}, and D_{2b}, respectively. Again, applying the ampere-second balance principle to C_{1a} and C_{1b} yields:

$$\begin{cases} (I_{L2} - I_{D2bp})(1-D)T_S = (I_{L1} - I_{D1bp})(1-D)T_S \\ I_{D1bp}(1-D)T_S = I_{D2bp}(1-D)T_S \end{cases} \tag{14}$$

According to (14), one obtains

$$I_{L1} = I_{L2} = \frac{I_{in}}{2} \tag{15}$$

Which means that the input current is evenly shared between the two inductors. The same conclusion can be obtained by analysing the proposed converter with n DCM.

E. CURRENT STRESS OF THE SEMICONDUCTOR DEVICES

To analyse the current stress, we denote the average output current by I_o. Ampere-second balance is applied to the capacitor C_{2a}, C_{2b}, and it gives:

$$\begin{cases} (I_{Dap} - I_o)(1-D)T_S - I_o DT_S = 0 \\ (I_{Dbp} - I_o)(1-D)T_S - I_o DT_S = 0 \end{cases} \tag{16}$$

Using (14) and (16), the peak current of diodes can be expressed as:

$$I_{D1ap} = I_{D2bp} = I_{D1bp} = I_{D2ap} = \frac{I_o}{1-D} \tag{17}$$

In modes 6 and 12, the following current relationships apply:

$$\begin{cases} I_{D2ap} + I_{D1bp} = I_{L1} \\ I_{D1ap} + I_{D2bp} = I_{L2} \end{cases} \tag{18}$$

From (17) and (18), the average inductor currents can be calculated as:

$$I_{L1} = I_{L2} = \frac{2I_{\rm o}}{1-D} \tag{19}$$

Hence, the average currents of the diodes equal the output current, i.e.,

$$I_{\rm D1a} = I_{\rm D2b} = I_{\rm D1b} = I_{\rm D2a} = I_{\rm o} \tag{20}$$

Next, denote the average currents of the switches by I_{S1} and I_{S2}, respectively. By analysing the operational principles of the converter, the currents flowing through the switches in each switching mode can be obtained as:

$$i_{S1} = \begin{cases} I_{L1} \cdots\cdots\cdots\cdots\cdots (2D-1)T_S \\ 0 \cdots\cdots\cdots\cdots\cdots\cdots (1-D)T_S \\ I_{L1}+I_{L2} \cdots\cdots (1-D)T_S \end{cases} \tag{21}$$

$$i_{S2} = \begin{cases} I_{L2} \cdots\cdots\cdots\cdots\cdots (2D-1)T_S \\ I_{L2}+I_{D2ap} \cdots\cdots (1-D)T_S \\ 0 \cdots\cdots\cdots\cdots\cdots\cdots (1-D)T_S \end{cases} \tag{22}$$

From (21) and (22), the average currents of the switches can be expressed as:

$$\begin{cases} I_{S1} = \dfrac{2I_{\rm o}}{1-D} \\ I_{S2} = \dfrac{2DI_{\rm o}}{1-D} + I_{\rm o} \end{cases} \tag{23}$$

By extending the above analysis to the proposed converter with n DCM cells, it produces the relationships between the switch currents and the output current, i.e.,

$$I_{\rm D1a} = I_{\rm D1b} = I_{\rm D2a} = I_{\rm D2b} = \cdots = I_{\rm Dna} = I_{\rm Dnb} = I_{\rm o} \tag{24}$$

$$\begin{cases} I_{S1} = \dfrac{nI_{\rm o}}{1-D} \\ I_{S2} = \dfrac{2DI_{\rm o}}{1-D} + (n-1)I_{\rm o} \end{cases} \tag{25}$$

III. EXPERIMENTAL VERIFICATION

In order to verify the outcome of the theoretical analysis presented in the previous section, an 800W experimental prototype with two DCMs is established. The specifications of the prototype are given in Table 1.

Fig. 4(a) shows the waveforms of $u_{\rm gs1}$, $u_{\rm gs2}$, $u_{\rm in}$, and $u_{\rm o}$, the voltage conversion gain is about 9.7 when the duty cycle is 0.6, which is close to that calculated from (6). Fig. 4(b) shows the current waveforms of L_1 and L_2. It can be observed that the DC components of $i_{\rm L1}$ and $i_{\rm L2}$ are about 10A, and this is close to that calculated using (19). In addition, Fig. 4(c) shows the waveforms of $u_{\rm C1a}$, $u_{\rm C1b}$, $u_{\rm C2a}$, and $u_{\rm C2b}$. The average values of $u_{\rm C1a}$, $u_{\rm C1b}$, $u_{\rm C2a}$ and $u_{\rm C2b}$ are about 100, 100, 200 and 200V, respectively, which is consistent with (3) and (4).

To verify the effectiveness ZVZCS feature of the proposed converter, the waveforms during the period of switching are shown in Fig. 5. For comparison, Figs. 5(a) and (c) show the waveforms of the switches S_1 and S_2 during turn-off and turn-on in hard switch state, while Figs. 5(b) and (d) show

TABLE 1. Specifications of the Experimental Prototype.

Parameter	Values
Input voltage ($u_{\rm in}$)	40V
Output voltage ($u_{\rm o}$)	400V
Output power ($P_{\rm o}$)	800W
Switching frequency (f_s)	50kHz
Switch (S_1, S_2)	GP4055D
Diodes (D_1, D_2, D_3, D_4, D_5, D_{1a}, D_{1b}, D_{2a}, D_{2b})	STTH15L06D
Capacitors (C_{1a}, C_{1b}, C_{2a}, C_{2b})	10μF
Capacitors (C_1, C_2)	0.047μF
Inductors (L_1, L_2)	300μH
Inductors (L_{S1}, L_{S2})	2.6μH

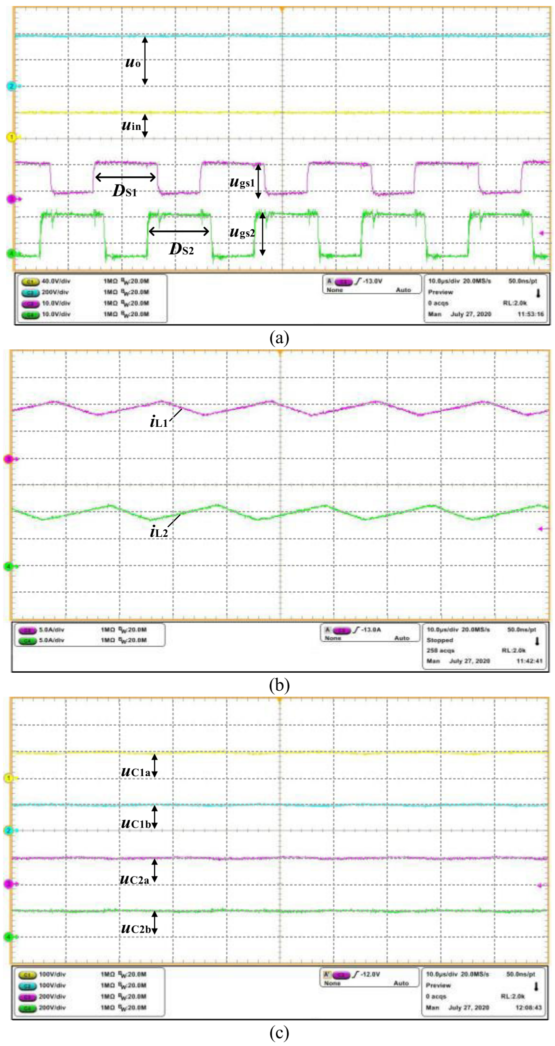


FIGURE 4. The waveforms of the experimental prototype: (a) Duty cycle, input voltage, output voltage; (b) Inductor currents; (c) Voltage across capacitors.

the waveforms of the switches S_1 and S_2 under the ZVZCS condition, respectively. Obviously, with the introduction of the passive snubber circuit, the overlap of the voltage and the

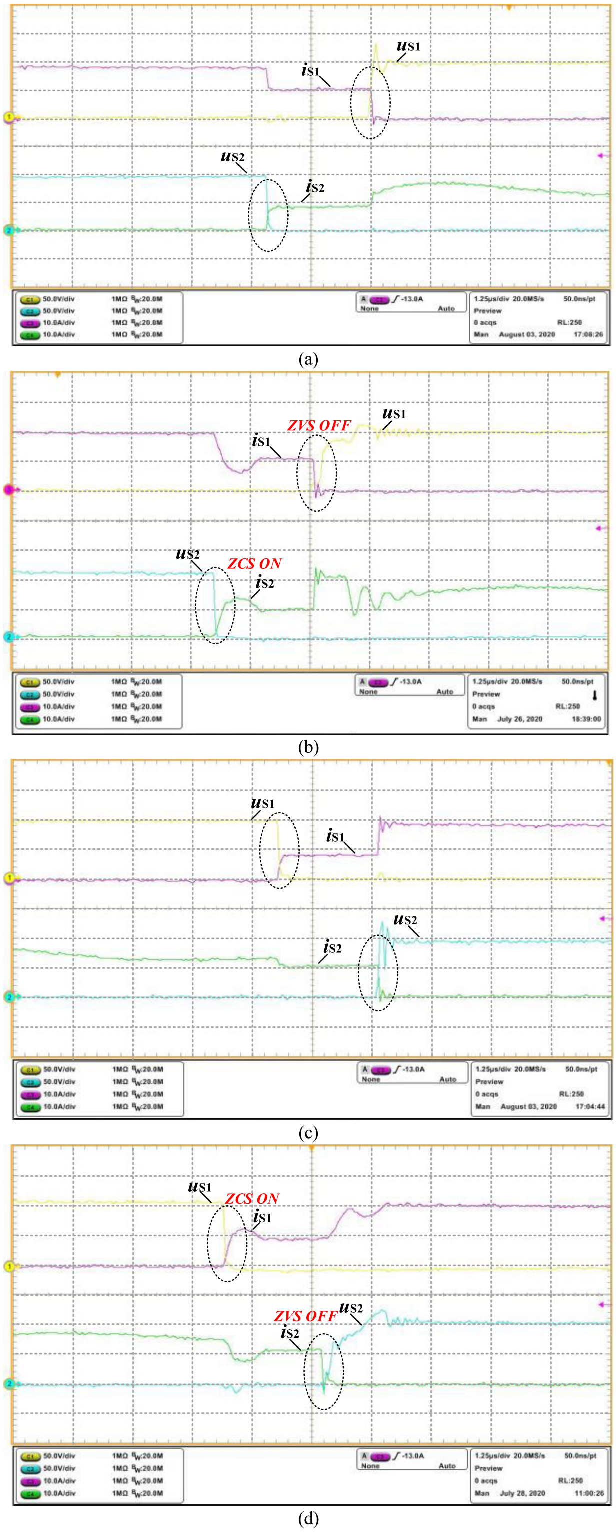


FIGURE 5. The voltage and current waveforms of S_1 and S_2: (a) S_1 turn off in hard switch state and S_2 turn on in hard switch state; (b) S_1 at the ZVS OFF state and S_2 at the ZCS ON state; (c) S_1 turn on in hard switch state and S_2 turn off in hard switch state; (d) S_1 at the ZCS ON state and S_2 at the ZVS OFF state.

current areas is almost zero. Therefore, the overall efficiency of the proposed converter is increased significantly. In addition, the transient during the on-off process has been greatly

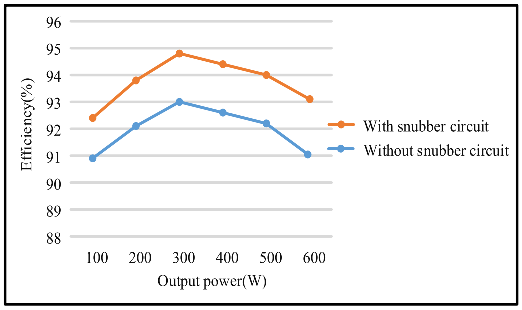


FIGURE 6. Efficiency curve.

improved with alleviated voltage and current oscillation. This can help to reduce the EMI and enhance the stability of the converter.

Next, by adjusting the output power, the efficiency curves of the converter under different loading conditions are obtained and shown in Fig. 6. Here, the efficiencies of the converter with and without the passive snubber circuit are compared. It can be seen from Fig. 6 that the highest efficiency reaches 94.8% with the snubber circuit, while this value is only 93% without the snubber circuit. Hence, the conversion efficiency of the proposed converter has been effectively improved by using the snubber circuit.

IV. LOSSES ANALYSIS

Detailed theoretical power analysis can be concluded as follows:

i. The conduction loss of the switches is denoted as P_{CON}, which can be calculated by multiplying the forward voltage drop v_{F} by the average current I_{s}. The loss can be expressed as follows:

$$P_{\mathrm{CON}} = v_{\mathrm{F}}(I_{\mathrm{S1}} + I_{\mathrm{S2}}) = 9\mathrm{W} \tag{26}$$

ii. The conduction loss in a diode is calculated by multiplying the forward voltage drop (v_{F}) of the diode by the average diode current. The average currents of $\mathrm{D_{1a}}$, $\mathrm{D_{1b}}$, $\mathrm{D_{2a}}$, and $\mathrm{D_{2b}}$ are equal to 1A. Therefore,

$$P_{\text{D-CON}} = 4v_{\mathrm{F}} \cdot I_{\mathrm{D}} = 3.8\mathrm{W} \tag{27}$$

Due to the low reverse recovery current in STTH15L06D, the reverse recovery loss could be ignored.

iii. The loss in the capacitor occurs due to the equivalent series resistance (ESR) of the capacitor. The capacitor currents can be estimated as follows:

$$\begin{cases} I_{C1a(rms)} = \sqrt{\left(\dfrac{I_{L1}}{2}\right)^2 (1-D) + \left(\dfrac{I_{L2}}{2}\right)^2 (1-D)} = 2.24\mathrm{A} \\ I_{C1b(rms)} = \sqrt{\left(\dfrac{I_{L2}}{2}\right)^2 (1-D) + \left(\dfrac{I_{L1}}{2}\right)^2 (1-D)} = 2.24\mathrm{A} \\ I_{C2a(rms)} = \sqrt{I_o^2 (1-D) + \left(\dfrac{I_{L1}}{2} - I_o\right)^2 (1-D)} = 1.14\mathrm{A} \\ I_{C2b(rms)} = \sqrt{I_o^2 (1-D) + \left(\dfrac{I_{L2}}{2} - I_o\right)^2 (1-D)} = 1.14\mathrm{A} \end{cases} \tag{28}$$

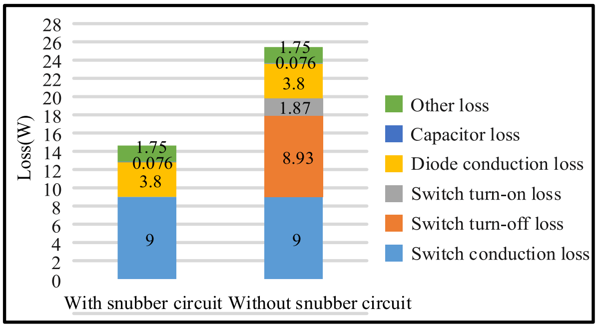


FIGURE 7. Losses distribution.

The ESR of capacitor is 6mΩ. Therefore, the capacitor loss can be calculated as follows:

$$\begin{aligned} P_C &= P_{C1a} + P_{C1b} + P_{C2a} + P_{C2b} \\ &= \left(I^2_{C1a(rms)}+I^2_{C1b(rms)}+I^2_{C2a(rms)}+I^2_{C2b(rms)}\right) ESR \\ &= 0.076\text{W} \end{aligned} \tag{29}$$

iv. The other losses include the wire loss, magnetic component loss, and the loss of the passive snubber circuit. The wire loss is about 0.4W, which takes up 0.1% of total power. The magnetic component loss mainly includes the wire and core loss of the inductor. According to the measurement, the actual inductance is about 300μH and its conduction resistance is about 18.2mΩ. The conduction loss of L_1 is thus

$$P_{L1\text{-CON}} = I^2_{L1} \cdot R_L = 0.455\text{W} \tag{30}$$

Based on B_{pk}-Peak AC flux density curve, the core loss of L_1 can be estimated by

$$P_{L1\text{-core}} = P \cdot V = 0.22\text{W} \tag{31}$$

and the losses of the two inductors can be calculated by

$$P_{L1} = P_{L1\text{-CON}} + P_{L1\text{-core}} = 0.675\text{W} \tag{32}$$

$$P_L = P_{L1} + P_{L2} = 1.35\text{W} \tag{33}$$

Furthermore, the specific calculation of the snubber loss is shown in (34). Obviously, compared with other losses, the loss of passive snubber circuit can be ignored.

$$\begin{cases} P_{C1} = I^2_{C1(rms)} \cdot R_{C1} = 0.01W \\ P_{C2} = I^2_{C2(rms)} \cdot R_{C2} = 0.01W \\ P_{D\text{-snubber}} = v_F \cdot (I_{D1} + I_{D2} + I_{D3} + I_{D4} + I_{D5}) = 0.095W \\ P_{L\text{-snubber}} = \left(I^2_{LS1} + I^2_{LS2}\right) \cdot R_L = 0.03W \\ P_{\text{snubber}} = P_{C1} + P_{C2} + P_{D\text{-snubber}} + P_{L\text{-snubber}} = 0.145W \end{cases} \tag{34}$$

The sum of the losses of the inductors and the wires are denoted other losses, i.e.,

$$P_{\text{other}} = P_L + P_{\text{wire}} = 1.75\text{W} \tag{35}$$

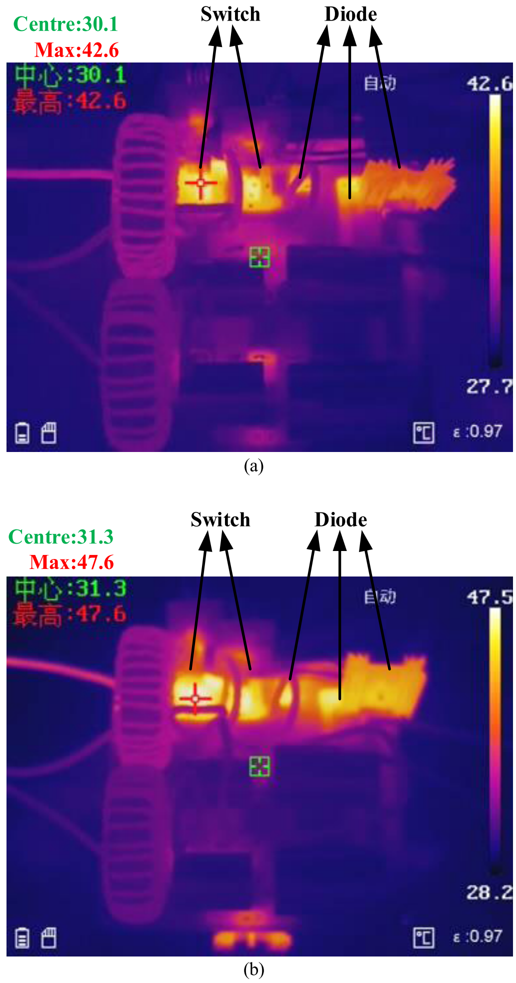


FIGURE 8. Thermal image: (a) With passive snubber circuit; (b) Without passive snubber circuit.

Next, the efficiency of the converter can be calculated by

$$\eta = \frac{P_o(100\%)}{P_o + P_{CON} + P_{D\text{-CON}} + P_C + P_{\text{other}}} = 96.47\% \tag{36}$$

The turn-off and the turn-on losses of the switches S_1 and S_2, without the proposed passive snubber circuit, should be included. Other losses are similar. The turn-off and turn-on losses of switches S_1 and S_2 can be expressed as follows:

$$\begin{aligned} P_{SW} &= \frac{u_{S1} I_{S1} \left(t_{t-\text{off}} + t_{t-\text{on}}\right)}{2T_S} + \frac{u_{S2} I_{S2} t_f \left(t_{t-\text{off}} + t_{t-\text{on}}\right)}{2T_S} \\ &= 10.8\text{W} \end{aligned} \tag{37}$$

where $t_{t-\text{off}}$ is equal to the turn-off delay time $t_{d(\text{off})}$ plus the falling time t_f, and $t_{t-\text{on}}$ is equal to the turn-on delay time $t_{d(\text{on})}$ plus the rising time t_r.

Then, the overall efficiency of the converter without the passive snubber circuit is

$$\eta = \frac{P_o(100\%)}{P_o + P_{CON} + P_{SW} + P_{D\text{-CON}} + P_C + P_{\text{other}}} = 94\% \tag{38}$$

Fig. 7 shows the calculated power losses of the proposed converter. The calculated losses are consistent with the measurements and this verified the effectiveness of the proposed converter.

Furthermore, Fig. 8(a) and Fig. 8(b) show the thermal images with and without the passive snubber circuit, respectively. The two images are taken by operating the circuits with the same duration for proper comparison. It can be observed that the maximum switching temperature with the passive snubber circuit is about 42.6°C, while the maximum switching temperature without snubber circuit is 47.6°C. The thermal images have also shown the effectiveness of the analysis.

V. CONCLUSION

This paper proposes an interleaved zero-voltage zero-current switching (ZVZCS) high step-up DC-DC converter. The operational principles and the performance characteristics of the converter are presented in a comprehensive manner. The effectiveness of the proposed converter with the passive snubber circuit is validated using an 800W experimental prototype. By comparing it with the topology without the snubber circuit, theoretical analysis and experimental results show the proposed scheme is superior to the conventional topology without the snubber circuit. The proposed converter has the following salient advantages: 1) The proposed passive snubber circuit is easier to design, reliable, and cost-effective. The conversion efficiency of the converter is significantly improved by the proposed passive snubber circuit. 2) The improvement of the overall efficiency is beneficial to the improvement of the switching frequency of the converter, at the same time, it reduces the size and weight of the passive components in the circuit, leading to reduced power density of the converter. 3) The conversion gain can be flexibly designed by adjusting the number of the diode-capacitor multipliers.

REFERENCES

[1] D. Xu, Q. Wu, B. Zhou, C. Li, L. Bai, and S. Huang, "Distributed multi-energy operation of coupled electricity, heating, and natural gas networks," *IEEE Trans. Sustain. Energy*, vol. 11, no. 4, pp. 2457–2469, Oct. 2020.

[2] H. Wang, Y. Liu, B. Zhou, C. Li, G. Cao, N. Voropai, and E. Barakhtenko, "Taxonomy research of artificial intelligence for deterministic solar power forecasting," *Energy Convers. Manage.*, vol. 214, Jun. 2020, Art. no. 112909.

[3] L. Xi, L. Zhang, Y. Xu, S. Wang, and C. Yang, "Automatic generation control based on multiple-step greedy attribute and multiple-level allocation strategy," *CSEE J. Power Energy Syst.*, early access, Nov. 20, 2020, doi: 10.17775/CSEEJPES.2020.02650.

[4] L. Xi, J. Wu, Y. Xu, and H. Sun, "Automatic generation control based on multiple neural networks with actor-critic strategy," *IEEE Trans. Neural Netw. Learn. Syst.*, early access, Jul. 14, 2020, doi: 10.1109/TNNLS.2020.3006080.

[5] L. Müller and J. W. Kimball, "High gain DC–DC converter based on the Cockcroft–Walton multiplier," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6405–6415, Sep. 2016.

[6] B. Zhu, Z. Wei, Y. Chen, H. Wang, and D. M. Vilathgamuwa, "Multiple input-terminal voltage multiplier circuit," *IEEE Trans. Ind. Appl.*, vol. 56, no. 5, pp. 5075–5082, Sep. 2020.

[7] B. Zhu, S. Hu, G. Liu, Y. Huang, and X. She, "Low-voltage stress buck-boost converter with a high-voltage conversion gain," *IEEE Access*, vol. 8, pp. 95188–95196, 2020.

[8] B. Zhu, F. Ding, and D. M. Vilathgamuwa, "Coat circuits for DC–DC converters to improve voltage conversion ratio," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3679–3687, Apr. 2020.

[9] S. Miao and J. Gao, "A family of inverting buck-boost converters with extended conversion ratios," *IEEE Access*, vol. 7, pp. 130197–130205, Sep. 2019.

[10] C. Wang, S. Xu, W. Shen, S. Lu, and W. Sun, "A single-switched high-switching-frequency quasi-resonant flyback converter," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8775–8786, Sep. 2019.

[11] A. Knott, T. M. Andersen, P. Kamby, J. A. Pedersen, M. P. Madsen, M. Kovacevic, and M. A. E. Andersen, "Evolution of very high frequency power supplies," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 386–394, Sep. 2014.

[12] E. Chung, K.-H. Lee, Y. Han, and J.-I. Ha, "Single-switch high-frequency DC–DC converter using parasitic components," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3651–3661, May 2017.

[13] J. Li, F. B. M. van Horck, B. J. Daniel, and H. J. Bergveld, "A high-switching-frequency flyback converter in resonant mode," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8582–8592, Nov. 2017.

[14] G. Zhang, J. Zeng, W. Xiao, S. S. Yu, B. Zhang, and Y. Zhang, "A self-protected single-stage LLC resonant rectifier," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Sep. 21, 2020, doi: 10.1109/JESTPE.2020.3024893.

[15] G. Zhang, H. Chen, S. S. Yu, and Z. Li, "Novel method to operation conditions identification of high-order power converters," *J. Adv. Res.*, vol. 28, pp. 175–181, Feb. 2021.

[16] L. Yi, H. Zhu, B. Wang, L. Fang, W. Ma, and X. Liang, "A novel full-soft-switching full-bridge converter with a snubber circuit and couple inductor," in *Proc. IEEE 10th Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Jun. 2019, pp. 60–64.

[17] Y. Xi and P. K. Jain, "A forward converter topology employing a resonant auxiliary circuit to achieve soft switching and power transformer resetting," *IEEE Trans. Ind. Electron.*, vol. 50, no. 1, pp. 132–140, Feb. 2003.

[18] M. R. Mohammadi and H. Farzanehfard, "A new family of zero-voltage-transition nonisolated bidirectional converters with simple auxiliary circuit," *IEEE Trans. Ind. Electron.*, vol. 63, no. 3, pp. 1519–1527, Mar. 2016.

[19] J.-Y. Lin, S.-Y. Lee, C.-Y. Ting, and F.-C. Syu, "Active-clamp forward converter with lossless-snubber on secondary-side," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7650–7661, Aug. 2019.

[20] J.-Y. Lin, P.-J. Liu, and C.-Y. Yang, "A dual-transformer active-clamp forward converter with nonlinear conversion ratio," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4353–4361, Jun. 2016.

[21] E. Adib and H. Farzanehfard, "Analysis and design of a zero-current switching forward converter with simple auxiliary circuit," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 144–150, Jan. 2012.

[22] P. Jang and B.-H. Cho, "Two-switch forward converter with reset winding and an auxiliary active-clamp circuit for a wide input voltage range," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4491–4502, Jun. 2017.

[23] S. Sharifi, M. Jabbari, and H. Farzanehfard, "A new family of single-switch ZVS resonant converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4539–4548, Jun. 2017.

[24] G. Tibola, E. Lemmen, J. L. Duarte, and I. Barbi, "Passive regenerative and dissipative snubber cells for isolated SEPIC converters: Analysis, design, and comparison," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9210–9222, Dec. 2017.

[25] B. Zhu, Q. Zeng, Y. Chen, Y. Zhao, and S. Liu, "A dual-input high step-up DC/DC converter with ZVT auxiliary circuit," *IEEE Trans. Energy Convers.*, vol. 34, no. 1, pp. 161–169, Mar. 2019.

[26] X. Yu, J. Su, S. Guo, S. Zhong, Y. Shi, and J. Lai, "Properties and synthesis of lossless snubbers and passive soft-switching PWM converters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3807–3827, Apr. 2020.

[27] M. Mohammadi, E. Adib, and M. Rouhollah Yazdani, "Family of soft-switching single-switch PWM converters with lossless passive snubber," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3473–3481, Jun. 2015.

[28] B. Zhu, L. Ren, and X. Wu, "Kind of high step-up DC/DC converter using a novel voltage multiplier cell," *IET Power Electron.*, vol. 10, no. 1, pp. 129–133, Jan. 2017.

BINXIN ZHU (Senior Member, IEEE) was born in Anhui, China, in 1986. He received the B.S. degree from the Hefei University of Technology, Hefei, China, in 2008, and the Ph.D. degree from Chongqing University, Chongqing, China, in 2013, both in electrical engineering. In 2014, he joined the College of Electrical Engineering and New Energy, China Three Gorges University, China, as a Lecturer. In 2016, he became an Associate Professor and a Group Leader of the Power Electronics Group. His research interests include high power and high step-up dc-dc converters.

SHIHUAN CHEN received the bachelor's degree from Hubei Polytechnic University, Hubei, China, in 2019. He is currently pursuing the master's degree in electrical engineering with China Three Gorges University, Yichang, China. His research interests include high power, high step-up, and high efficiency dc-dc converters.

YAO ZHANG is currently pursuing the bachelor's degree in electrical engineering with China Three Gorges University, Yichang, China. His research interest includes power electronics.

YU HUANG received the bachelor's degree from the Taiyuan University of Science and Technology, Shanxi, China, in 2018. He is currently pursuing the master's degree in electrical engineering with China Three Gorges University. His research interests includes wide voltage conversion ratio dc-dc converter used in photovoltaic power generation systems.