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Predictive Nearest-Level Control Algorithm for Modular Multilevel Converters With Reduced Harmonic Distortion

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ABSTRACT Owing to the low number of submodules (SMs) in modular multilevel converters (MMCs), especially in medium-voltage applications, the output current and voltage generated by conventional nearest-level control (NLC) methods contain evident distortions. Previously, various hybrid and level-increased NLC methods have been proposed to improve the output voltage quality, but such measures wither increased the complexity or did not regulate all the control objectives simultaneously. To further enhance the output performances of MMCs containing low numbers of SMs, an improved predictive NLC (I-PNLC) method combining NLC and model predictive control (MPC) is proposed, where the output and circulating currents are regulated with the corresponding predicted references, and the output voltage is controlled by the added voltage correction. The proposed I-PNLC not only reduces the output current and voltage total harmonic distortion (THD) considerably but also avoids additional complexity in the control system design. The results of simulations and an experiment are presented to verify the proposed approach, in addition to a comparison of the evaluations of conventional NLC methods.

INDEX TERMS Modular multilevel converter, nearest-level control (NLC), nearest-level modulation, level-increased NLC, output voltage, predictive control.

I. INTRODUCTION

Modular multilevel converters (MMCs) have garnered extensive interest since their invention by Marquardt in 2003 [1]. Compared with the conventional voltage-source converter (VSC) topologies, MMCs have advantages with regard to their modular structures, flexible expendabilities, transformerless configuration, ease of assembly, scalabilities, low switching losses, and substantially improved output waveforms [2]–[5]. The modularity characteristic ensures decreased production cost and simple maintenance, while the scalability characteristic allows voltage rating adjustments by changing the number of submodules (SMs) [6]. An indispensable characteristic of the MMC is its high reliability [7], which allows operation despite the presence of faulty SMs via fault-tolerant methods [8]–[10]. Furthermore, when the number of SMs is considerably high, the MMC outputs increased voltage, resulting in a nearly ideal sinusoidal waveform with reduced filtering requirement. Because of these prominent advantages, MMCs have the best potential converter topologies in high- and medium-voltage applications as direct current transmission systems [5], [11], flexible alternating current transmission systems [12], motor drives [13], static synchronous compensators [14], renewable energy systems [15], and energy storage systems [16], among others.

Despite their distinctive benefits and extensive potential application prospects, MMCs require complicated control strategies than other multilevel converters for appropriate operation. This is because, in addition to the correct phase and magnitude of the output current and voltage, the balance between the capacitor voltages and circulating current suppression needs to be guaranteed concurrently [3], [4], [17]. Appropriate control techniques are therefore indispensable for MMCs owing to the effects on the overall quality, filtering requirement, switching frequency, and power losses. Among the various types of modulation methods for MMCs, pulse width modulation (PWM) and staircase modulation are the most commonly used [18]–[21]. In the PWM methods,

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phase-shifted and level-shifted carriers (PSCs and LSCs) are the two main realizations for MMCs [22]–[25]. Owing to merits, such as low total harmonic distortion (THD) in the output voltage, PWM is primarily used in medium-voltage applications, where the MMCs contain a few SMs. However, these PWM methods have some limiting features, such as high switching frequencies, high switching losses, and complicated implementation processes, in addition to unsatisfactory transient performances [26]–[28]. Furthermore, when the numbers of SMs increase, the PWM methods require extensive hardware resources for implementation. This is the same problem in the model predictive control (MPC) despite the MPC method offers an excellent dynamic performance and straightforward implementation [29]–[31].

Meanwhile, the conventional nearest-level control (NLC) method offers simple implementation and low switching frequency characteristics regardless of the number of SMs [32], [33], which render the NLC the most practical modulation method for MMCs. Unfortunately, conventional NLC techniques generate lower output performances than the PSC PWM method with a low number of SMs, as applied in medium-voltage applications. Furthermore, a large voltage ripple of the corresponding SM capacitor and high root-mean-square (rms) value of the circulating current are other problems in the conventional NLC method. Therefore, to achieve adequate output quality, the conventional NLC method is primarily used in high-voltage applications when the MMC contains a lot of SMs.

In an effort to further enhance the output current and voltage harmonic characteristics, one upper SM and one lower SM were operated in the PWM condition in [34] to increase the resolution ratio of the staircase waveform. This hybrid modulation lowered the harmonics and improved the THDs in the output currents and voltages. However, the voltage levels still remain similar to those of the conventional NLC method, the modular characteristic is eliminated, and the assembly is impractical. The level-increased NLC method presented in [35] used the $round_{0.25}(x)$ function instead of the traditional $round_{0.5}(x)$ function, where the decimal fraction of x is rounded to the next higher integer when it exceeds 0.25 or rounded down to the nearest integer otherwise. This is equivalent to adding an offset to the arm voltage references. However, the average number of inserted SMs is not constant at N, resulting in changes to the average SM capacitor voltages. To address this problem, an improved level-increased NLC was introduced in [36] that changed the offset value twice within a fundamental period and allowed maintaining the average number of inserted SMs at N; hence, the average voltage of the SM capacitors did not deviate. The level-increased NLC improved the output voltage performance by increasing the output voltage level; however, the circulating current was not suppressed, and the improved level-increased NLC was based on changing the offset phase to regulate the circulating current. The NLC approach in [37] included an additional second-order harmonic control term with the references of the upper and lower arm voltages. The low-frequency circulating current components are eliminated, but the efficiency of this scheme was affected by the sampling time and magnitude of the harmonic control term.

In [38], a limit controller was used to regulate the circulating current, and the limit controller modified the number of inserted SMs from the conventional NLC method to decrease the circulating current ripple. However, this adjustment to the number of SMs might degrade the output voltage performance. Another NLC approach [39] used deadbeat control to reduce the circulating current peak-to-peak value. A recent NLC method proposed in [40] defined the number of inserted SMs according to the output voltage level selection condition and circulating current regulation, thereby significantly improving the output performance and circulating current controllability. Unlike the previous NLC methods, the predictive NLC (PNLC) method, presented in [41], achieved the current-control objectives using the corresponding predicted references. The PNLC method is independent of the number of SMs and inherits the combined benefits of the predictive control and NLC methods. However, the inserted SM number in the conventional PNLC was according to the difference between the predicted reference and measured values, resulting in a non-nearest level or undesirable level transitions. Additionally, the staircase approximation error due to the voltage references in real applications is a discrete-time quantized signal that might produce undesirable level transitions. These undesirable level transitions increase the *dv/dt* of the output voltage, causing undesirable transitions between neighboring output voltage levels, which could cause voltage and current distortions and increase the corresponding THDs.

To resolve this problem and enhance the output performance of the MMC, the effective improved PNLC (I-PNLC) approach is proposed in this paper. Based on the analysis of the conventional PNLC and MPC, the principle and implementation of the proposed I-PNLC are described. First, the conventional PNLC method is implemented to define the temporary numbers of inserted SMs in the upper and lower arms. To avoid delays due to even one sampling instant in any digital control system, which might deteriorate the performance of the control system, a delay compensation technique is applied. Second, a predefined condition for output voltage correction is generated; this corresponding condition leads to possible combinations of the inserted SM numbers in the upper and lower arms. To select the optimal number of inserted SMs in the upper and lower arms from all possible combinations, the MPC technique is employed using a simple cost function. The proposed I-PNLC method enhances the output performance with low corresponding THDs compared with the conventional NLC and PNLC methods and regulates the other control objectives well under both low and fundamental modulation index operations. The efficacy of the proposed I-PNLC approach is carefully validated by simulations and experiments; moreover, the conventional NLC and PNLC methods, and various control schemes are also realized for comparison purposes.

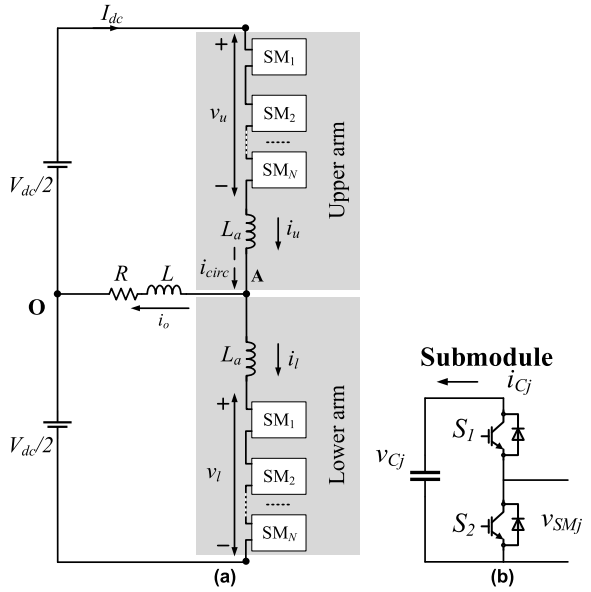

FIGURE 1. (a) Single-phase MMC arrangement and (b) structure of the half-bridge SM.

The remainder of this manuscript is organized as follows. The mathematical models of the single-phase MMC and conventional NLC methods are discussed in Section II. Section III introduces and analyzes the proposed I-PNLC method. The simulations and experimental validations are presented in Section IV, and the conclusions are presented in Section V.

II. CONVENTIONAL NLC AND PNLC METHODS

A. MATHEMATICAL MODEL OF MMC

The configuration of the one-phase leg of the MMC is illustrated in Fig. 1(a). The two arms are called the upper and lower arms, as shown. One arm comprises an arm inductor L_a and N series-connected half-bridge SMs, and each SM is formed using two series insulated gate bipolar transistors and a capacitor, as shown in Fig. 1(b); here, v_u and v_l are the output voltages of the upper and lower arms, respectively, and i_u and i_l represent the upper and lower arm currents, respectively, with i_o being the output current and V_{dc} the dc-link voltage.

The mathematical equations governing the dynamic behavior of the MMC are obtained using Kirchhoff's voltage law as follows:

$$\frac{V_{dc}}{2} - v_u(k) - L_a\frac{di_u(k)}{dt} - Ri_o(t) - L\frac{di_o(k)}{dt} = 0, \quad (1)$$

$$-\frac{V_{dc}}{2} + v_l(k) + L_a\frac{di_l(k)}{dt} - Ri_o(k) - L\frac{di_o(k)}{dt} = 0. \quad (2)$$

The upper and lower arm currents can be expressed from Fig. 1(a) as

$$i_u(k) = i_o(k) + \frac{i_{circ}(k)}{2}, \quad (3)$$

$$i_l(k) = -i_o(k) + \frac{i_{circ}(k)}{2}, \quad (4)$$

where i_{circ} is the circulating current that is calculated as

$$i_{circ}(k) = \frac{i_u(k) + i_l(k)}{2}. \quad (5)$$

Adding (1) and (2), and subtracting (1) from (2), the dynamic behavior of the MMC can be expressed as

$$\frac{di_o(k)}{dt} = \left(\frac{1}{2L + L_a}\right)[v_l(k) - v_u(k) - 2Ri_o(k)], \quad (6)$$

$$\frac{di_{circ}(k)}{dt} = \left(\frac{1}{2L_a}\right)[V_{dc} - v_u(k) - v_l(k)]. \quad (7)$$

B. CONVENTIONAL NLC AND PNLC METHODS

The control structure of the conventional NLC approach is illustrated in Fig. 2(a). The upper arm voltage reference v_u^* and lower arm voltage reference v_l^* are divided with the nominal value of the SM capacitor voltage V_C^*; the inserted SM numbers associated with the nearest voltage levels are generated using the $round_{0.5}(x)$ function. A voltage sorting algorithm is then employed to balance the capacitor voltage and produce the switching signals from the generated SM number. The inserted SM numbers in the upper and lower arms can be expressed as

$$N_{u\_final}^* = round_{0.5}\left(N\frac{v_u^*}{V_C^*}\right), \quad (8)$$

$$N_{l\_final}^* = round_{0.5}\left(N\frac{v_l^*}{V_C^*}\right), \quad (9)$$

where

$$v_u^* = \frac{V_{dc}}{2}[1 - Mcos(2\pi f_o t)], \quad (10)$$

$$v_l^* = \frac{V_{dc}}{2}[1 + Mcos(2\pi f_o t)]. \quad (11)$$

To facilitate understanding, an example of the arm voltage reference and its corresponding output voltage for an SM number of seven ($N = 7$) is depicted in Fig. 3(a), in addition to a modulation index of one ($M = 1$) in a single period of time T_o resulting from the conventional NLC method. The output voltage v_o^{round} has the highest number of levels $N + 1$, with a step size of V_C^* and maximum possible error of $0.5V_C^*$. The upper and lower arm step voltages v_u^{round} and v_l^{round} are symmetrical about the vertical $y = V_{dc}/2$ line. Thus, all the transition instants of v_u^{round} and v_l^{round} are aligned (two such pairs are shown by the black lines in Fig. 4(a)), and the total inserted SM numbers in the upper and lower arms are always equal to N.

It should be noted that the conventional NLC has the most straightforward implementation, along with a reduction in the switching losses, compared with other carrier-based modulation techniques. However, the conventional NLC exhibits the poorest output performance, with high THD in output current and voltage. Furthermore, the conventional NLC method causes high amplitudes of the circulating current and capacitor voltage ripples. Therefore, the conventional NLC method is recommended for use in an MMC containing a relatively high number of SMs to obtain adequate output performance.

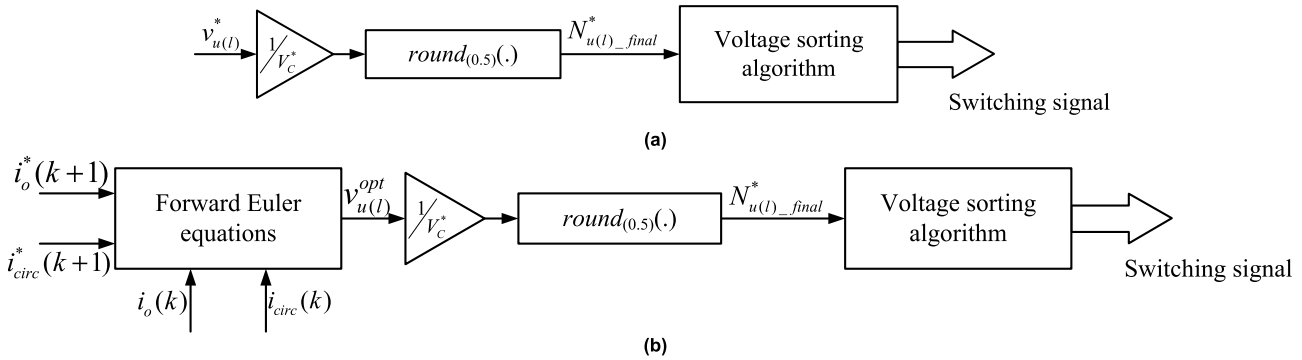

FIGURE 2. (a) Conventional NLC and (b) conventional PNLC.

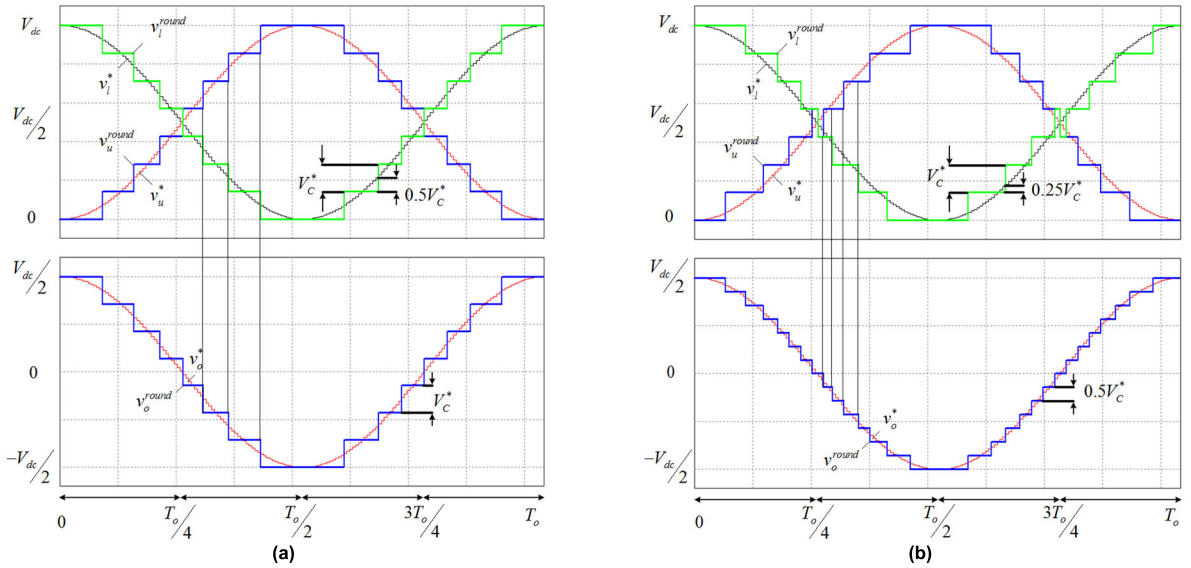

FIGURE 3. Basic principles of the conventional (a) NLC and (b) PNLC.

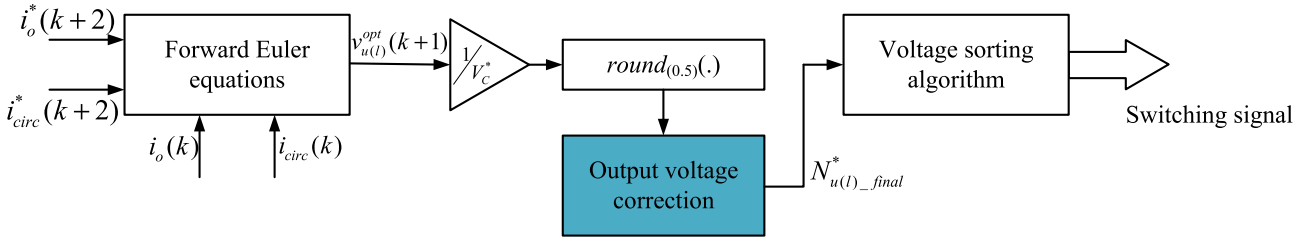

FIGURE 4. Control diagram of the proposed I-PNLC.

The conventional PNLC method inherits the benefits of predictive control as well as the NLC approach, as presented in Fig. 2(b). Instead of using the conventional upper and lower arm references, the optimal upper and lower arm voltages are generated by applying the predicted output and circulating current references. The model of the output and circulating currents in the discrete-time domain are respectively deduced from (6) and (7), based on Euler approximation [42], as

$$i_o(k+1) = \left(\frac{T_s}{2L+L_a}\right)[v_l(k) - v_u(k)] + \left(1 - \frac{2RT_s}{2L+L_a}\right) i_o(k), \quad (12)$$

$$i_{circ}(k+1) = \left(\frac{T_s}{2L_a}\right)[V_{dc} - v_l(k) - v_u(k)] + i_{circ}(k). \quad (13)$$

The optimal voltages corresponding to the upper and lower arms are deduced from (12) and (13) by replacing $i_o(t+T_s)$ and $i_{circ}(t+T_s)$ with their corresponding reference values $i_o^*(t+T_s)$ and $i_{circ}^*(t+T_s)$, respectively. Thus, the optimal

upper and lower arm voltages can be expressed as

$$v_u^{opt} = \frac{V_{dc}}{2} - \frac{A+B}{2}, \tag{14}$$

$$v_l^{opt} = \frac{V_{dc}}{2} + \frac{A-B}{2}, \tag{15}$$

where

$$A = \frac{2L+L_a}{T_s}\left[i_o^*(k+1) - i_o(k)\right] + 2Ri_o(k), \tag{16}$$

$$B = \frac{2L}{T_s}\left[i_{circ}^*(k+1) - i_{circ}(k)\right]. \tag{17}$$

The final numbers of SMs in the upper and lower arms are generated in a manner similar to the conventional NLC using the $round_{0.5}(x)$ function. However, unlike the conventional NLC, the total SM numbers in the upper and lower arms are not always equal to N but vary among N, $N-1$, and $N+1$. As shown in Fig. 3(b), the vertical symmetry of the resulting steps v_u^{round} and v_l^{round} are disrupted, thereby causing a misalignment of the level transitions. This results in $2N+1$ output voltage levels with reduced step heights of $0.5V_C^*$ via $2N+1$ PWM. Therefore, in addition to the regulation of the output and circulating currents, the output voltage levels are increased to $2N+1$, resulting in improved output performance compared with that of the conventional NLC approach.

Nevertheless, the number of inserted SMs in the conventional PNLC is selected based on the difference between the predicted references and values of the output and circulating currents, which result in non-nearest or undesirable level transitions and staircase approximation errors. These undesirable level transitions increase the *dv/dt* in the output voltage, causing undesirable transitions among the adjacent output voltage levels, which could lead to voltage and current distortions and increase the corresponding THDs.

III. PROPOSED I-PNLC METHOD

To enhance appropriate output performance of the MMC, the I-PNLC is proposed herein as a modification of the conventional PNLC method. The entire I-PNLC scheme is outlined in Fig. 4. A substantial time delay exists unavoidably in any digital control system, which might deteriorate the operation of the system. Thus, for effective practical implementation of the I-PNLC, delay compensation techniques such as in [43], [44] should be applied by shifting the model in (12) and (13) forward by one-step as follows:

$$i_o(k+2) = \left(\frac{T_s}{2L+L_a}\right)\left[v_l(k+1) - v_u(k+1)\right] + \left(1 - \frac{2RT_s}{2L+L_a}\right) i_o(k+1), \tag{18}$$

$$i_{circ}(k+2) = \left(\frac{T_s}{2L_a}\right)\left[V_{dc} - v_l(k+1) - v_u(k+1)\right] + i_{circ}(k+1). \tag{19}$$

The optimal upper and lower arm voltages at the $k+1$ sampling instant can be obtained from (18) and (19) by replacing $i_o(k+2)$ and $i_{circ}(k+2)$ with their respective reference values $i_o^*(k+2)$ and $i_{circ}^*(k+2)$. Accordingly, the optimal upper and lower arm voltages are derived as

$$v_u^{opt}(k+1) = \frac{V_{dc}}{2} - \frac{A'+B'}{2}, \tag{20}$$

$$v_l^{opt}(k+1) = \frac{V_{dc}}{2} + \frac{A'-B'}{2}, \tag{21}$$

where

$$A' = \frac{2L+L_a}{T_s}\left[i_o^*(k+2) - i_o(k+1)\right] + 2Ri_o(k+1), \tag{22}$$

$$B' = \frac{2L}{T_s}\left[i_{circ}^*(k+2) - i_{circ}(k+1)\right]. \tag{23}$$

The temporarily inserted SM numbers in the upper and lower arms are defined as

$$N_{u\_temp}^* = round_{0.5}\left(N\frac{v_u^{opt}(k+1)}{V_C^*}\right), \tag{24}$$

$$N_{l\_temp}^* = round_{0.5}\left(N\frac{v_l^{opt}(k+1)}{V_C^*}\right). \tag{25}$$

These temporarily inserted SMs in the upper and lower arms $N_{u(l)\_temp}^*$ are generated using (24) and (25), similar to the conventional PNLC. However, these $N_{u(l)\_temp}^*$ are not the final values, but are modified to enhance the output current and voltage qualities without affecting the circulating current controllability. To solve the undesirable-level problem, the temporarily inserted SMs in the upper and lower arms $N_{u(l)\_temp}^*$ are adjusted according to the differences between the previous output voltage levels *level_old* and temporary output voltage levels at the current sampling instant *level_temp*.

$$level_{old} = N_{l\_final\_1}^* - N_{u_{final_1}}^* + N + 1, \tag{26}$$

where $N_{u\_final\_1}^*$ and $N_{l\_final\_1}^*$ are the final numbers of inserted SMs at the previous sampling instant.

$$level_{temp} = N_{l\_temp}^* - N_{u_{temp}}^* + N + 1, \tag{27}$$

$$\Delta level = level_{temp} - level_{old}. \tag{28}$$

To guarantee smooth transitions among the neighboring output voltage levels, the absolute value of the difference between the previous and current output voltage level should be less than or equal to one. Therefore, three conditions regarding $\Delta level$ are generated, as shown in Fig. 5. For instance, if $\Delta level > 1$, instead of using the temporary SM numbers directly in the upper and lower arms, as acquired using (24) and (25), respectively, $N_{u\_temp}^*$ and $N_{l\_temp}^*$ are modified by adding one to $N_{u\_temp}^*$ or subtracting one from $N_{l\_temp}^*$. Two possible combinations of inserted SMs in the upper and lower arms ($M_{u1} = N_{u\_temp}^* + 1, M_{l1} = N_{l\_temp}^*$ and $M_{u1} = N_{u\_temp}^*, M_{l1} = N_{l\_temp}^* - 1$) are thus generated. These two combinations can result in changes to the output voltage levels, which decrease the differences between the previous and generated output voltage levels.

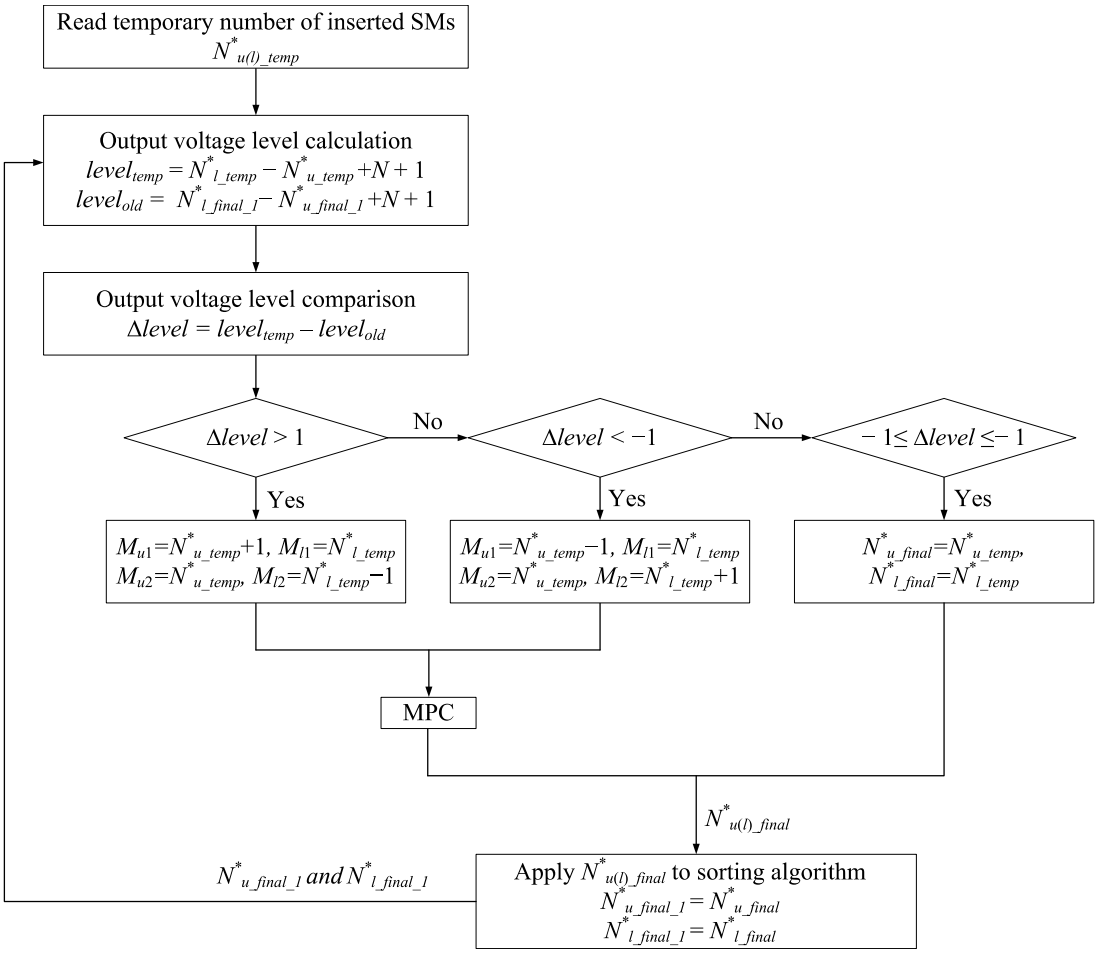

FIGURE 5. Block diagram for output voltage correction.

It is noted that there are many possible number combinations to adjust the values of $N^*_{u\_temp}$ and $N^*_{l\_temp}$. However, $N^*_{u\_temp}$ and $N^*_{l\_temp}$ should vary in the range of 0 to N. Therefore, the number of inserted SMs in the upper and lower arms after adjustment cannot be negative or exceed N. Additionally, having only one possible change in $N^*_{u\_temp}$ or $N^*_{l\_temp}$ instead of changing both guarantees controllability of the circulating current and no increase in the switching loss. To guarantee circulating current controllability, the changes in $N^*_{u\_temp}$ and $N^*_{l\_temp}$ are followed by an analysis, as in [42]. The optimal inserted SM number needs to be selected from among possible combinations $M_{u(l)1}$ or $M_{u(l)2}$. The MPC technique is employed using a simple cost function J, which contains the output and circulating current terms.

$$J = \left|i^*_o(k+2) - i_o(k+2)\right| + \lambda\left|i^*_{circ}(k+2) - i_{circ}(k+2)\right|, \quad (29)$$

where λ is a weighting factor of the cost function that is obtained using the method in [44], [46], resulting in $\lambda = 0.05$. The flow chart of the MPC part is depicted in Fig. 6(a).

The final acquired number of inserted SMs in the upper and lower arms $N^*_{u\_final}$ and $N^*_{l\_final}$ are applied to the voltage sorting algorithm [20] to balance the capacitor voltages, as shown in Fig. 6(b). The output signals are generated using the arms' current directions and the sorted capacitor voltages. When the arm current is negative (i.e., the capacitor is discharged), the SMs with the highest voltages are inserted; conversely, the SMs with the lowest voltages are inserted for positive arm currents.

Compared with the conventional control schemes, the proposed I-PNLC achieves better output performance by limiting the output voltage level transitions to one to eliminate the undesirable levels. The control of the circulating current is guaranteed via the MPC technique to select the optimal SM numbers in the upper and lower arms from among the two possible combinations. Compared with the conventional PNLC, although the MPC part is added to the control, the additional number of cost function evaluations is only two for each sampling instant. Hence, the computational load is not heavy.

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

Simulations were realized using the PSIM software to assess the suitability and efficacy of the proposed I-PNLC method. The single-phase MMC in the simulation contains seven SMs

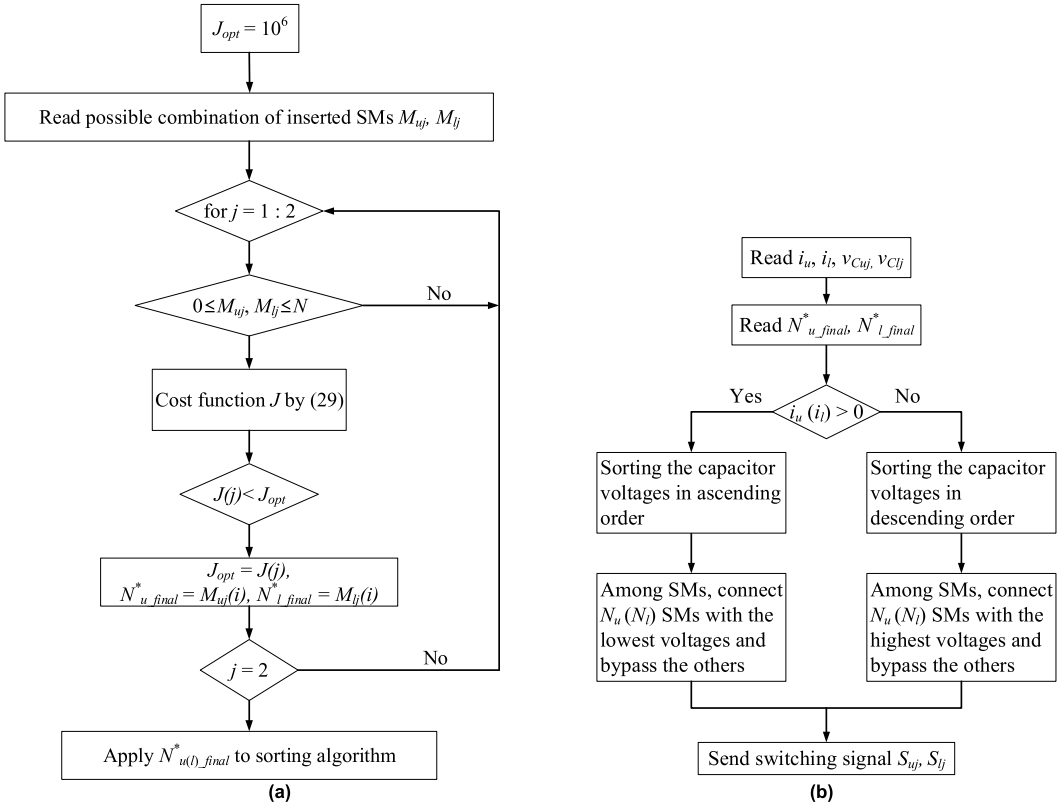

FIGURE 6. (a) Flowchart for the MPC part and (b) SM capacitor voltage sorting algorithm.

TABLE 1. Simulation parameters.

Parameter	Simulation
DC-link voltage V_{dc} (V)	7000
SMs per arm N	7
SM capacitor voltage V_C (V)	1000
SM capacitance C (mF)	2.2
Arm inductance L_a (mH)	4
Load inductance L (mH)	10
Load resistance R (Ω)	20
Output frequency f_o (Hz)	60
Rated MMC kVA S (kVA)	700
Sampling frequency f_{sp} (kHz)	10

per arm ($N = 7$), along with the parameter configuration given in Table 1. For a full assessment, comparisons between the proposed control scheme as well as the conventional NLC and PNLC methods, the level-increased NLC with circulating harmonic current suppression based on deadbeat control approach in [39], and the reduced computational burden MPC approach in [45] were obtained via simulations. The sampling frequency exerts a significant impact on the control performance of predictive control. A high sampling frequency enables obtaining high performance of the system but requires a fast control processor to ensure large numbers of needed calculations. This leads to increased system cost, which poses a challenge for practical implementation in industrial applications. Alternatively, the performance of the system deteriorates with a small sampling frequency. Therefore, the sampling frequency was set to 10 kHz in both the simulations and experiments, which is suitable for the output performance of the system and the clock frequency of a digital signal processor (DSP).

Figs. 7(a)–(e) illustrate the simulated results of the output current and voltage under steady-state operation using the conventional NLC, conventional PNLC, the level-increased NLC with circulating harmonic current suppression based on deadbeat control [39], the reduced computational burden MPC [45], and proposed I-PNLC methods, respectively. With reference to Fig. 7(a), the output current obtained by the conventional NLC method contains evident distortion, which results in a non-smooth sinusoidal waveform. Meanwhile, it can be seen that there are eight levels ($N + 1$) in the output voltage. The corresponding THDs of the output current and voltage are 3.58% and 9.15%, respectively. Compared with the conventional NLC scheme, the THDs of the output current and voltage yielded by the conventional PNLC are reduced to 1.21% and 8.7%, respectively. The output current is thus well regulated with the conventional PNLC. Although the number of levels of output voltage from the conventional PNLC increases to fifteen ($2N + 1$), the corresponding THD is still relatively high because of the generation of undesirable output level transitions, resulting in high dv/dt and high harmonic component magnitudes. Meanwhile, the level-increased with

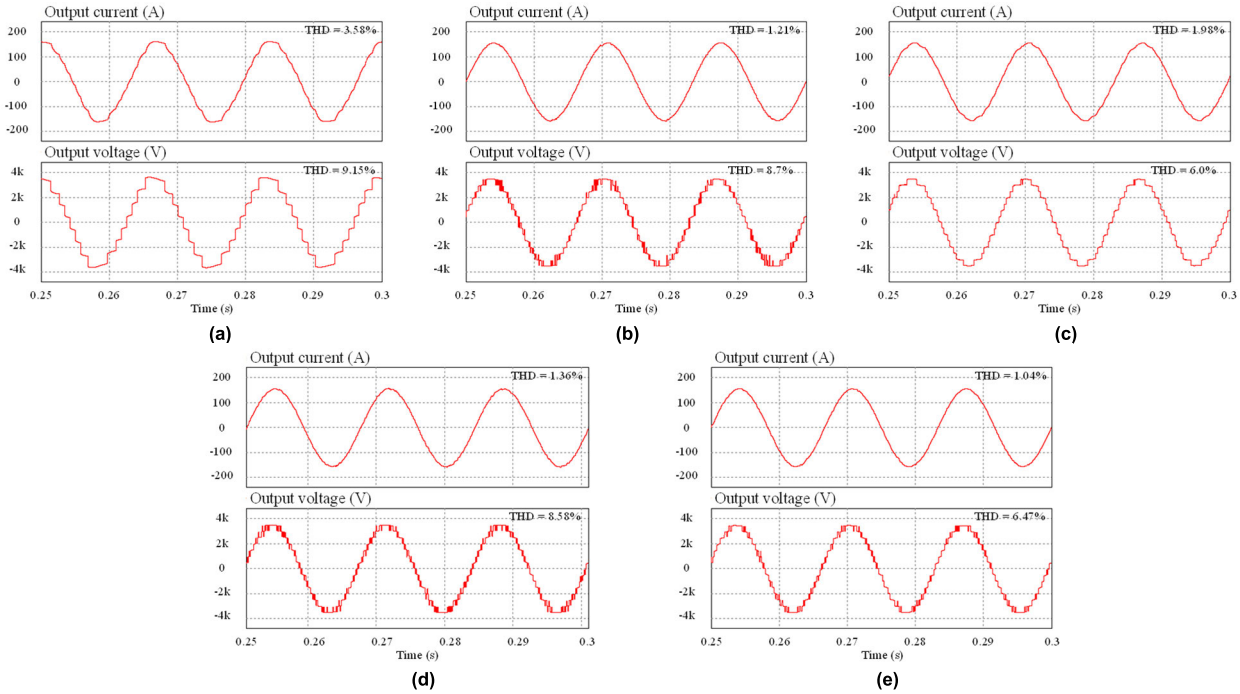

FIGURE 7. Steady-state performances of the output current and voltage obtained by (a) conventional NLC, (b) conventional PNLC, (c) level-increased NLC with circulating harmonic suppression based on deadbeat control, (d) reduced computational burden MPC, and (e) proposed I-PNLC from simulations.

circulating harmonic current suppression based on deadbeat control produced the lowest THD of the output voltage at 6.0% since the magnitude of high-frequency components in output voltage is low. The corresponding output current has a sinusoidal form with corresponding THD at 1.98%. The reduced computational burden MPC method has the quite same output performance as the conventional PNLC scheme with a slight difference between THDs of output current and output voltage. However, the output current and voltage acquired by the proposed I-PNLC are significantly improved compared with the two conventional schemes and approaches in [39] and [45]. The corresponding THDs of the output current and voltage are considerably low at 1.04% and 6.47%, respectively. It can be seen apparently that the output current is well controlled with a sinusoidal wave, whereas the output voltage contains fifteen $(2N + 1)$ levels without any undesirable level transitions. The comparison of the normalized output voltage levels between the conventional PNLC and the proposed I-PNLC is shown in Fig. 8. It is observed that the undesirable level transitions from the conventional PLNC, represented by the red lines, are eliminated completely.

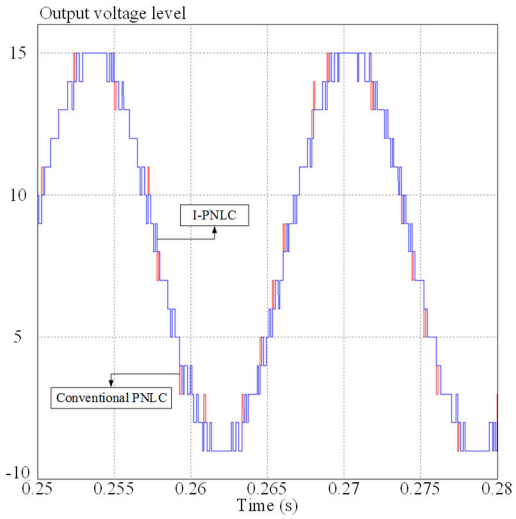

FIGURE 8. Normalized output voltages obtained by conventional PNLC and proposed I-PNLC.

Figs. 9(a)–(e) present the waveforms of the SM capacitor voltages and circulating currents obtained by the conventional NLC, conventional PNLC, the level-increased NLC with circulating harmonic current suppression based on deadbeat control, the reduced computational burden MPC, and proposed I-PNLC approach, respectively. The SM capacitor voltage deviation obtained via the conventional NLC, as shown in Fig. 9(a), is notably large owing to unregulated circulating currents, resulting in low-frequency circulating current components, especially the second harmonic component. This also causes high rms values of the circulating currents (approximately 66.24 A). Meanwhile, the SM capacitor voltages obtained by the remaining approaches are maintained close to the nominal values of 1 kV for both cases, with ignorable deviations. Furthermore, the low-frequency components in the circulating current from both

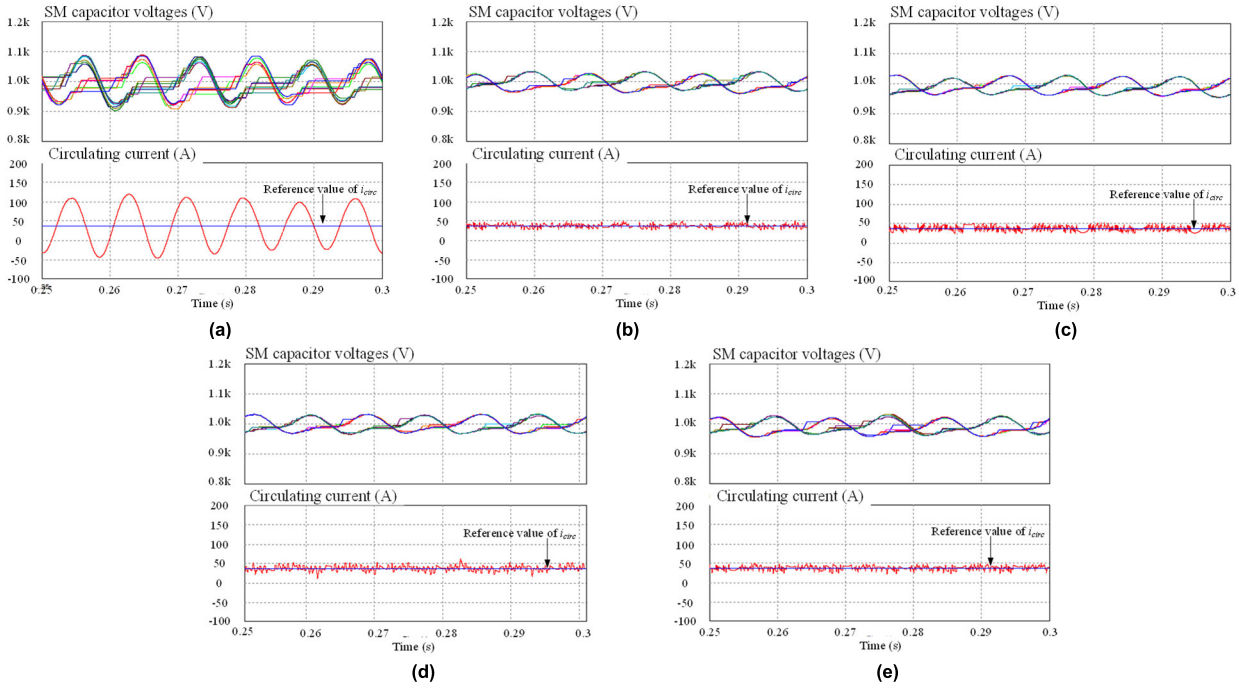

FIGURE 9. Steady-state performances of the SM capacitor voltages and circulating currents obtained by (a) conventional NLC, (b) conventional PNLC, (c) level-increased NLC with circulating harmonic suppression based on deadbeat control, (d) reduced computational burden MPC, and (e) proposed I-PNLC from simulations.

PNLC schemes, the level-increased NLC with circulating harmonic current suppression based on deadbeat controller, and the reduced computational burden MPC are entirely removed, whereas the magnitudes of the remaining high-frequency components are low, as described in Figs. 9(b) – (e). The rms values of circulating current from the four control schemes are almost the same at approximately 38 A with a slight difference in peak-to-peak values. This means that the proposed I-PNLC does not deteriorate the circulating current controllability compared with the conventional PNLC and other methods, whereas the output current and voltage are significantly improved.

The dynamic performances of the five control schemes are shown in Figs. 10(a)–(e). The MMC was first controlled to generate 110 A of output current, equivalent to a modulation index of 0.6 ($M = 0.6$). At $t = 0.3$s, the modulation index increased to 1 ($M = 1$). First, it can be seen that under low-modulation-index operation, the output currents obtained by the conventional PNLC, the level-increased NLC with circulating harmonic current suppression based on deadbeat controller, the reduced computational burden MPC, and proposed I-PNLC have higher qualities than that of the conventional NLC method, as depicted in Figs. 10(a)–(e). The voltage levels obtained by the five control schemes are increased, equivalent to the rise of the modulation index. Meanwhile, the SM capacitor voltages are maintained at nominal values, with lower deviations, and the magnitudes of the circulating currents are reduced as well. It can be apparently observed that the conventional NLC method exhibits the poorest dynamic performance for the circulating current, as seen in Fig. 10(a). The circulating currents obtained by the conventional NLC method presents a considerably high peak-to-peak value after the change to the modulation index, compared with the result under steady-state operation in Fig. 9(a). Nevertheless, the conventional PNLC, the level-increased NLC with circulating harmonic current suppression based on deadbeat controller, the reduced computational burden MPC, and proposed I-PNLC show better dynamic performances, where the circulating currents are tracked rapidly with the changes to the reference circulating current without any overshoots.

TABLE 2. Experimental parameters.

Parameter	Simulation
DC-link voltage V_{dc} (V)	150
SMs per arm N	3
SM capacitor voltage V_C (V)	50
SM capacitance C (mF)	2.2
Arm inductance L_a (mH)	4
Load inductance L (mH)	10
Load resistance R (Ω)	20
Output frequency f_o (Hz)	60
Rated MMC kVA S (kVA)	0.15
Sampling frequency f_{sp} (kHz)	10

B. EXPERIMENTAL RESULTS

A downscaled single-phase MMC prototype with parameters as given in Table 2 was setup under laboratory conditions, as presented in Fig. 11(a), to confirm the proposed analysis and control method. Fig. 11(b) shows a photograph of the

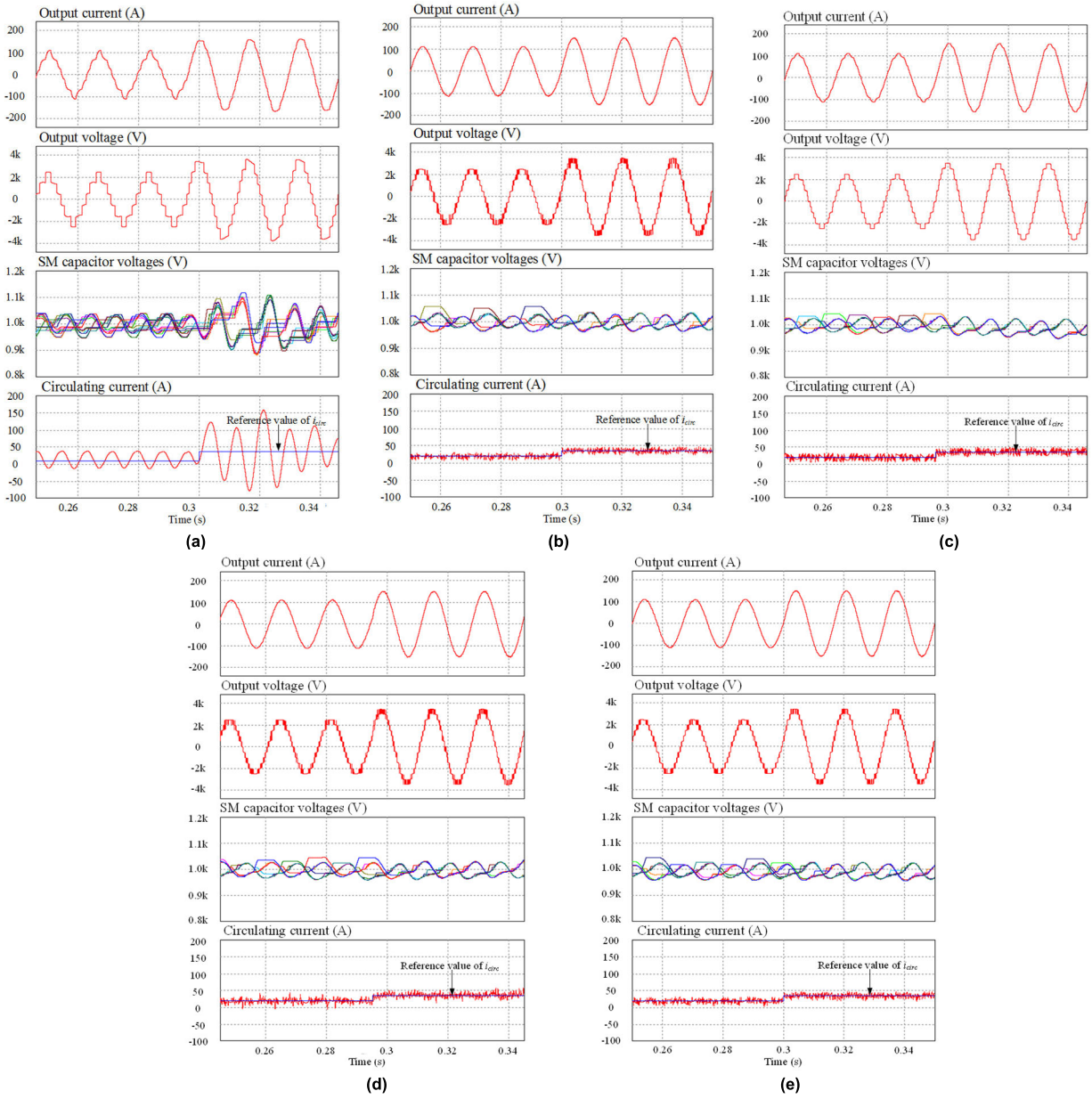

FIGURE 10. Dynamic performances of the output currents, output voltages, SM capacitor voltages, and circulating currents obtained by (a) conventional NLC, (b) conventional PNLC, (c) level-increased NLC with circulating harmonic suppression based on deadbeat control, (d) reduced computational burden MPC, and (e) proposed I-PNLC from simulations.

MMC circuit and control board hardware. In the following experiment, the conventional NLC, conventional PNLC, and proposed I-PNLC methods are assessed and compared. A DSP TMS320F28335 was employed to implement the control algorithms and generate the output signals. The arm currents and SMs capacitor voltages were sensed using current and voltage sensors respectively and sampled every T_{sp} seconds (100 μs).

Figs. 12(a)–(e) show the steady-state performances of the output currents and voltages of the conventional NLC, conventional PNLC, and proposed I-PNLC methods, respectively. The experimental waveforms appear to match the simulated outcomes. In Fig. 13(a), the output currents and voltages THDs are presented. It is observed that owing to the lower SMs compared to the simulations, the THDs of the output currents and voltages from the conventional NLC are high, reaching 8.22% and 18.2%, respectively. The output current in Fig. 12(a) contains considerable distortion, whereas the output voltage comprises four levels $(N + 1)$ with a step size of $V_C^* = 50$V, as explained in Fig. 4(a). It can be observed that the harmonic contents of the output voltage from the corresponding frequency spectrum are relatively high, indicating low voltage quality.

The output currents obtained by the conventional PNLC, the reduced computational burden MPC, and proposed

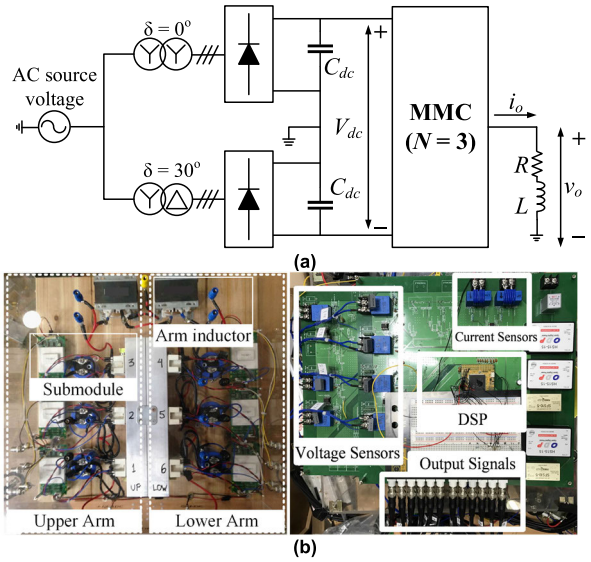

FIGURE 11. Experimental configuration of the single-phase MMC laboratory prototype: (a) circuit diagram; (b) MMC circuit and control board hardware.

I-PNLC are regulated adequately compared with the conventional NLC and the level-increased NLC with circulating harmonic current suppression based on deadbeat control. The corresponding THDs reach 4.08%, 3.05%, and 2.90%, respectively, as illustrated in Fig. 13(b), (d), and (e). Meanwhile, the THD of output current obtained by the level-increased NLC with circulating harmonic current control based on deadbeat control is relatively high at 6.13%, as shown in Fig. 13(c). Apparently, the output currents obtained from the conventional PNLC, the reduced computational burden MPC and the proposed I-PNLC approach the trend of a sinusoidal waveform better than the conventional NLC and the level-increased NLC with circulating harmonic current control based on deadbeat control. It is observed that the output voltage levels obtained by the conventional PNLC, the level-increased NLC with circulating harmonic current suppression based on deadbeat controller, the reduced computational burden MPC, and proposed I-PNLC increase from four to seven, matching the number $2N + 1$. However, it is noted that the output voltage obtained from the conventional PNLC contains large distortions and undesirable level transitions and that the corresponding THD reaches 17.0%. Although this output voltage THD is lower than that of the conventional NLC, it is relatively high, indicating poor voltage quality.

Conversely, the output voltage obtained by the proposed I-PNLC approach presents lower THD at 10.3% (reduced from 43.4% and 39.4% compared with the conventional NLC and conventional PNLC, respectively, and equivalent to the reduced computational burden MPC), as shown in Fig. 13(e). The elimination of undesirable level transitions of the proposed I-PNLC method results in reduced ripple in the waveforms and reduced filtering requirements under the same operating conditions. Furthermore, the application of the proposed I-PNLC results in significantly improved operating characteristics of the MMC compared with the conventional PNLC and especially the conventional NLC method. Equivalent to the simulation results, the THD value of output voltage obtained by the level-increased NLC with circulating harmonic current suppression based on deadbeat control approach is the lowest with 9.43%. However, in comparison with the proposed I-PNLC method, this difference is trivial.

Regarding the behaviors of the SM capacitor voltages, Fig. 14(a)–(e) present the capacitor voltage waveforms of the corresponding upper SM1 and lower SM3 obtained from the conventional NLC, conventional PNLC, the level-increased NLC with circulating harmonic current suppression based on deadbeat controller, the reduced computational burden MPC, and proposed I-PNLC methods, respectively. The capacitor voltage waveforms from the five control schemes are close to the nominal value of $V_C^* = 50$V. However, the presence of considerably large ripples in the SM capacitor voltage obtained from the conventional NLC is noticeable owing to the circulating current not being regulated, as shown in Fig. 14(a). Meanwhile, the capacitor voltages obtained from the remaining control schemes are balanced well, with negligible deviations. Similar to the simulation results, the circulating current obtained from the conventional NLC contains low-frequency components, resulting in high peak-to-peak values, as shown in Fig. 14(a). The conventional PNLC, the level-increased NLC with circulating harmonic current suppression based on deadbeat controller, the reduced computational burden MPC, and proposed I-PNLC present better circulating current suppression performances. The low-frequency components in the circulating currents from both PNLC schemes are entirely removed, whereas the magnitudes of the remaining high-frequency components are negligible, as depicted in Fig. 14(b) – (e). However, due to the low number of SMs in the experimental MMC prototype, the number of redundant inserted SMs is limited. The level-increased NLC with circulating harmonic current suppression based on deadbeat control uses a deadbeat controller to modify the number of inserted SMs acquired by the method in [39]. When the number of SMs is very low, the modified number of inserted SMs might not be sufficient to regulate the circulating current, resulting in higher peak-to-peak value compared with the PNCL, the reduced computational burden MPC and the proposed I-PNLC approaches, as shown in Fig. 14(c).

Figs. 15(a) – (e) present the dynamic performances obtained from the five control schemes, where the MMC was operated under the step change of the modulation index from 0.5 to 1. Owing to the lack of output and circulating current regulations, the conventional NLC exhibits low dynamic performance compared with both PNLC schemes. Meanwhile, the remaining approaches exhibit better dynamic performances of the output and circulating currents. Furthermore, under low modulation index operation, the output current quality from the conventional NLC and the level-increased NLC with circulating harmonic current suppression

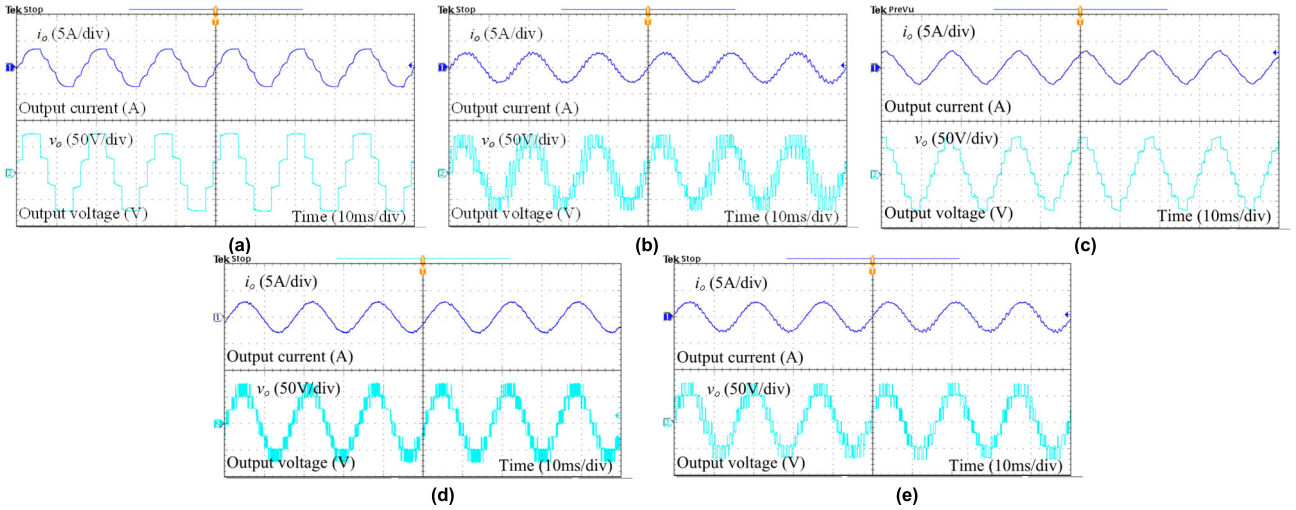

FIGURE 12. Steady-state performances of output currents and voltages obtained by (a) conventional NLC, (b) conventional PNLC, (c) level-increased NLC with circulating harmonic suppression based on deadbeat control, (d) reduced computational burden MPC, and (e) proposed I-PNLC from experiments.

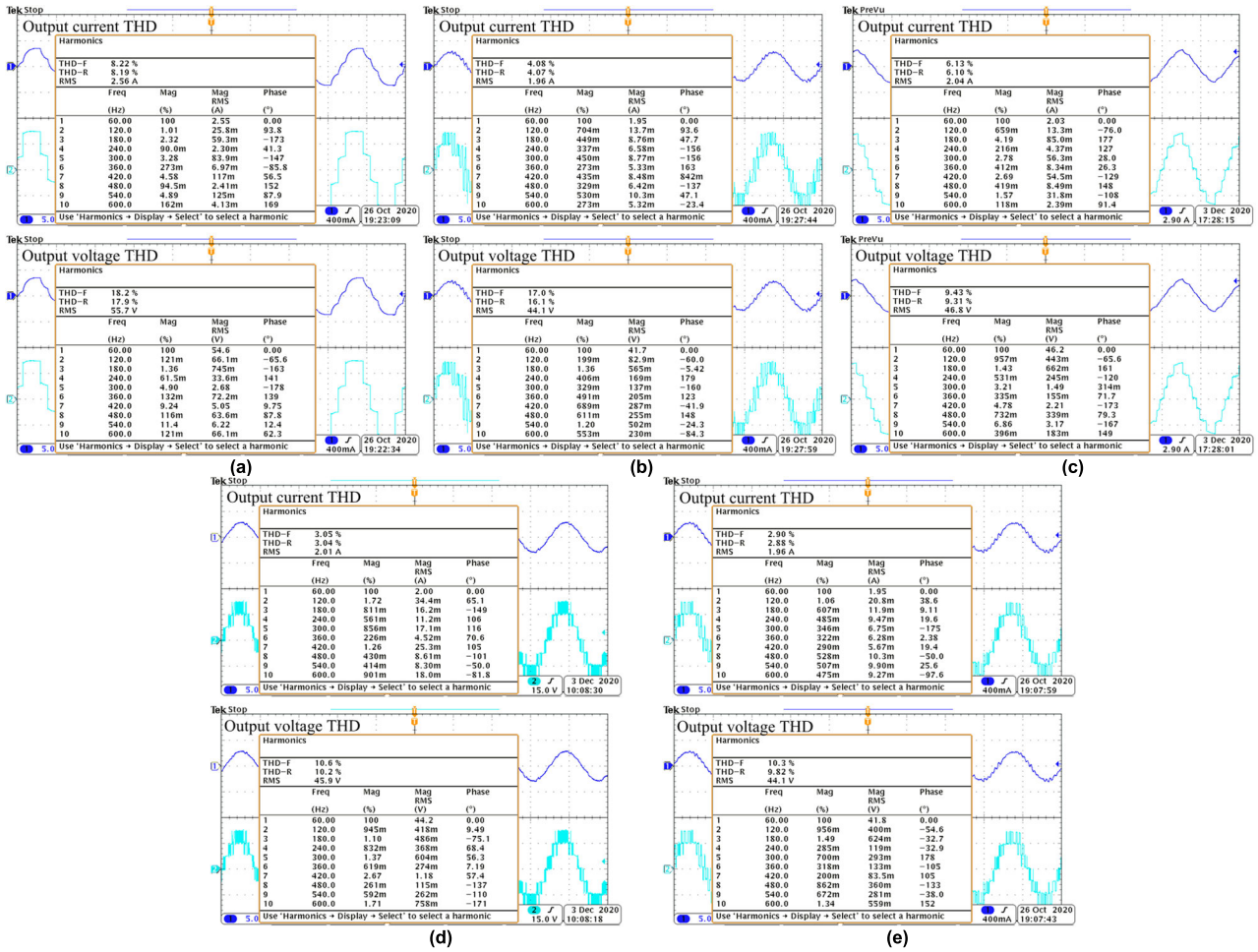

FIGURE 13. Corresponding THDs of output currents and voltages for Fig. 12 obtained by (a) conventional NLC, (b) conventional PNLC, (c) level-increased NLC with circulating harmonic suppression based on deadbeat control, (d) reduced computational burden MPC, and (e) proposed I-PNLC from experiments.

based on deadbeat control are inadequate because the low output voltage level results in high *dv/dt*, as shown in Fig. 15(a) and (c). The output voltage obtained from the conventional PNLC contains several undesirable output voltage transitions, resulting in evident distortion, as shown in Fig. 15(b). On the other hand, the proposed I-PNLC presents a higher

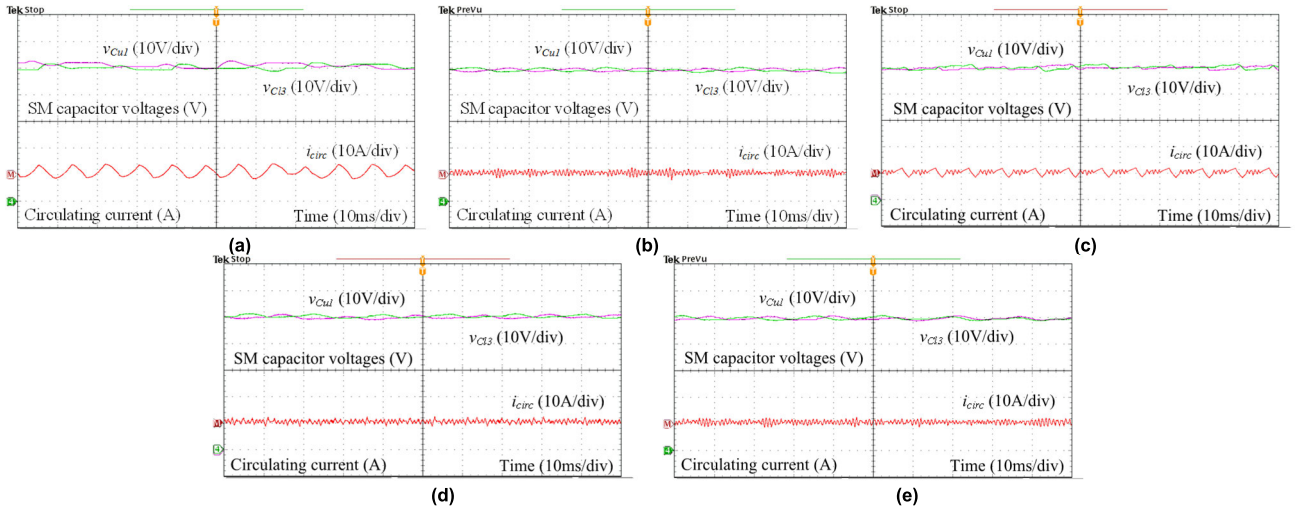

FIGURE 14. Steady-state performances of SM capacitor voltages and circulating currents obtained by (a) conventional NLC, (b) conventional PNLC, (c) level-increased NLC with circulating harmonic suppression based on deadbeat control, (d) reduced computational burden MPC, and (e) proposed I-PNLC from experiments.

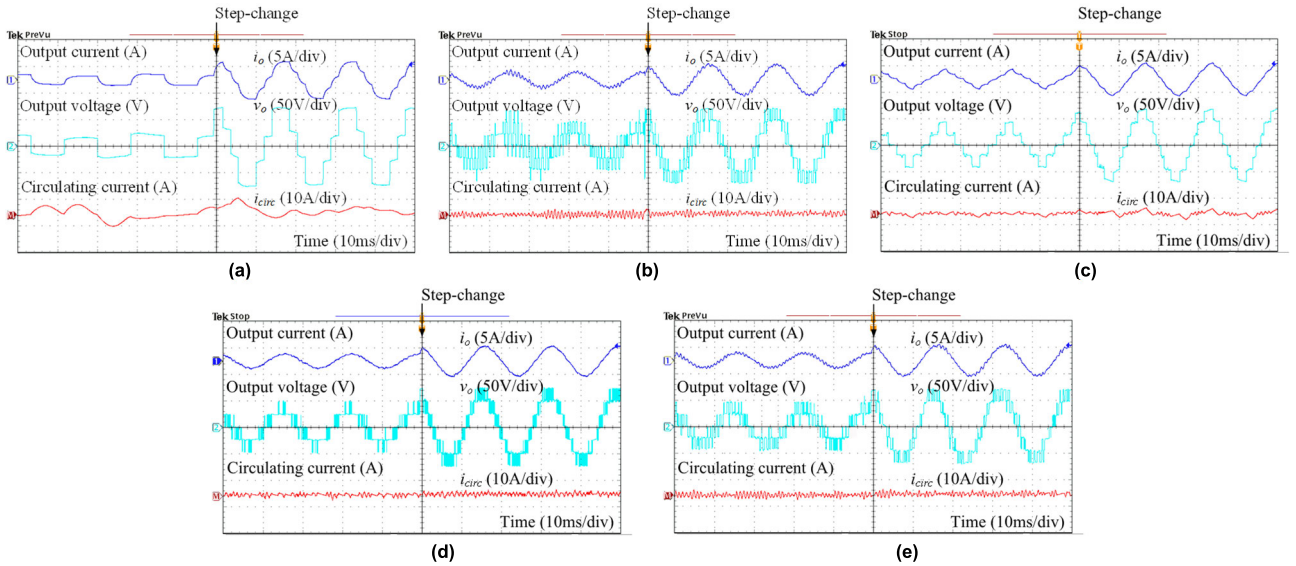

FIGURE 15. Dynamic performances of output currents, output voltages, and circulating currents obtained by (a) conventional NLC, (b) conventional PNLC, (c) level-increased NLC with circulating harmonic suppression based on deadbeat control, (d) reduced computational burden MPC, and (e) proposed I-PNLC from experiments.

quality of output voltage than the conventional schemes at both low- and high-modulation-index operations. The output voltage correction ensures that there are no approximation errors or undesirable level transitions.

The THDs obtained by the five control schemes, including simulation and experimental results, are summarized in Table 3. Apparently, the experimental results are very identical with those acquired in the simulations. The simulation and experimental results provide satisfactory performance in the sinusoidal output current, sufficient output voltage, the balance of SM capacitor voltages, and suppressed circulating currents for the proposed I-PNLC method under both steady-state and transient-state operations. From the comparison between the proposed I-PNLC approach and various control schemes, it can be noticed that the proposed I-PNLC is effective and significantly enhances the output performance compared with the conventional NLC and PNLC methods. In terms of the conventional PNLC, the proposed I-PNLC eliminates unnecessary level transitions to get better THDs in output current and output voltage. This results in an ignorable rise in switching transition number and corresponding switching losses compared with the effectiveness of the proposed I-PNLC. Regarding the level-increased NLC with circulating harmonic current suppression based on deadbeat control, the proposed I-PNLC method significantly improve the output current performance, especially on the low number

TABLE 3. THD comparison between proposed I-PNLC and various control schemes including simulation and experimental results.

		Conventional methods				Proposed I-PNLC
		Conventional NLC	Conventional PNLC	Level-increased NLC with circulating harmonic current suppression	Reduced computational burden MPC	
Simulation	Output current THD (%)	3.58	1.21	1.98	1.36	1.04
	Output voltage THD (%)	9.15	8.7	6.0	8.58	6.47
Experiment	Output current THD (%)	8.22	4.08	6.13	3.05	2.9
	Output voltage THD (%)	18.2	17.0	9.43	10.6	10.3

of SMs and low modulation index operation. Although the THD value of output voltage obtained by the level-increased NLC with circulating harmonic current suppression based on deadbeat control is lower than the proposed I-PNLC. This difference is trivial. In comparison with the reduced computational burden MPC, the proposed I-PNLC improves the output performance not too much. However, The computational burden of the proposed method is better than the reduced computational burden MPC, where the number of control actions of the proposed method is only two per sampling instant compared with five. Moreover, the number of control actions of the method in the reduced computational burden MPC increases when the number of SMs increases.

V. CONCLUSION

In MMC systems, the output current and voltage, in addition to the circulating current and capacitor voltage balancing control, should always be achieved simultaneously. This paper presents an I-PNLC method combining the PNLC and MPC approaches. The added output voltage correction by the MPC enhances the output voltage by altering the inserted SM numbers appropriately from the PNLC scheme. Owing to this output voltage correction, the approximation errors and undesirable voltage level transitions are eliminated, resulting in reduced THDs of the output current and voltage. The proposed I-PNLC method was verified through simulations and experiments, which confirm the excellent overall performance compared with the conventional NLC control schemes.

REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf.*, Bologna, Italy, vol. 3, Jun. 2003, pp. 272–277.
[2] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.
[3] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.
[4] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.
[5] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan. 2015.
[6] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 316–324, Jan. 2011.
[7] Q. Yang, J. Qin, and M. Saeedifard, "A postfault strategy to control the modular multilevel converter under submodule failure," *IEEE Trans. Power Del.*, vol. 31, no. 6, pp. 2453–2463, Dec. 2016.
[8] M. Aleenejad, H. Mahmoudi, and R. Ahmadi, "Unbalanced space vector modulation with fundamental phase shift compensation for faulty multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7224–7233, Oct. 2016.
[9] M. Aleenejad, H. Mahmoudi, P. Moamaei, and R. Ahmadi, "A new fault-tolerant strategy based on a modified selective harmonic technique for three-phase multilevel converters with a single faulty cell," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3141–3150, Apr. 2016.
[10] M. Aleenejad, H. Mahmoudi, and R. Ahmadi, "Multifault tolerance strategy for three-phase multilevel converters based on a half-wave symmetrical selective harmonic elimination technique," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7980–7989, Oct. 2017.
[11] G. J. Kish, M. Ranjram, and P. W. Lehn, "A modular multilevel DC/DC converter with fault blocking capability for HVDC interconnects," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 148–162, Jan. 2015.
[12] Z. Liu, J. Lu, Z. Ou, M. Ma, C. Yuan, X. Xiao, and H. Wang, "The start control strategy design of unified power quality conditioner based on modular multilevel converter," in *Proc. Int. Electric Mach. Drives Conf.*, Chicago, IL, USA, May 2013, pp. 933–937.
[13] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
[14] H. Mohammadi P and M. T. Bina, "A transformerless medium-voltage STATCOM topology based on extended modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1534–1545, May 2011.
[15] V. Yaramasu, A. Dekka, M. J. Durán, S. Kouro, and B. Wu, "PMSG-based wind energy conversion systems: Survey on power converters and controls," *IET Electr. Power Appl.*, vol. 11, no. 6, pp. 956–968, Jul. 2017.
[16] T. Soong and P. W. Lehn, "Assessment of fault tolerance in modular multilevel converters with integrated energy storage," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4085–4095, Jun. 2016.
[17] M. Mehrasa, E. Pouresmaeil, S. Zabihi, and J. P. S. Catalao, "Dynamic model, control and stability analysis of MMC in HVDC transmission systems," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1471–1482, Jun. 2017.
[18] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[19] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.
[20] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.
[21] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, "An improved pulse width modulation method for chopper-cell-based modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3472–3481, Aug. 2012.
[22] R. Naderi and A. Rahmati, "Phase-shifted carrier PWM technique for general cascaded inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1257–1269, May 2008.
[23] Y. Li, Y. Wang, and B. Q. Li, "Generalized theory of phase-shifted carrier PWM for cascaded H-bridge converters and modular multilevel converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 589–605, Jun. 2016.
[24] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, and V. G. Agelidis, "Circulating current control and evaluation of carrier dispositions in modular multilevel converters," in *Proc. IEEE ECCE Asia Downunder*, Melbourne, VIC, Australia, Jun. 2013, pp. 332–338.
[25] B. P. McGrath, C. A. Teixeira, and D. G. Holmes, "Optimized phase disposition (PD) modulation of a modular multilevel converter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4624–4633, Sep. 2017.
[26] M. H. Nguyen, S. S. Kwak, and T. Kim, "Phase-shifted carrier pulse-width modulation algorithm with improved dynamic performance for modular multilevel converters," *IEEE Access*, vol. 7, pp. 170949–170960, Nov. 2019.
[27] D. Zhou, S. Yang, and Y. Tang, "Model-predictive current control of modular multilevel converters with phase-shifted pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4368–4378, Jun. 2019.
[28] J. Bocker, B. Freudenberg, A. The, and S. Dieckerhoff, "Experimental comparison of model predictive control and cascaded control of the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 422–430, Jan. 2015.
[29] A. Dekka, B. Wu, V. Yaramasu, R. L. Fuentes, and N. R. Zargari, "Model predictive control of high-power modular multilevel converters—An overview," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 168–183, Mar. 2019.
[30] M. H. Nguyen and S. S. Kwak, "Improved indirect model predictive control for enhancing dynamic performance of modular multilevel converter," *Electronics*, vol. 9, no. 9, p. 1405, Aug. 2020.
[31] M. H. Nguyen and S. S. Kwak, "Switching loss balancing technique for modular multilevel converters operated by model predictive control method," *Electronics*, vol. 8, no. 10, p. 1175, Oct. 2019.
[32] S. Kouro, R. Bernal, H. Miranda, C. A. Silva, and J. Rodriguez, "High-performance torque and flux control for multilevel inverter fed induction motors," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2116–2123, Nov. 2007.
[33] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 298–306, Jan. 2011.
[34] Y. Wang, C. Hu, R. Ding, L. Xu, C. Fu, and E. Yang, "A nearest level PWM method for the MMC in DC distribution grids," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9209–9218, Nov. 2018.
[35] P. Hu and D. Jiang, "A level-increased nearest level modulation method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1836–1842, Apr. 2015.
[36] L. Lin, Y. Lin, Z. He, Y. Chen, J. Hu, and W. Li, "Improved nearest-level modulation for a modular multilevel converter with a lower submodule number," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5369–5377, Aug. 2016.
[37] D. Wu and L. Peng, "Characteristics of nearest level modulation method with circulating current control for modular multilevel converter," *IET Power Electron.*, vol. 9, no. 2, pp. 155–164, Feb. 2016.
[38] X. Chen, J. Liu, S. Ouyang, S. Song, and H. Wu, "A modified circulating current suppressing strategy for nearest level control based modular multilevel converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Cincinnati, OH, USA, Oct. 2017, pp. 1817–1822.
[39] X. Chen, J. Liu, S. Song, and S. Ouyang, "Circulating harmonic currents suppression of level-increased NLM based modular multilevel converter with deadbeat control," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11418–11429, Nov. 2020.
[40] M. H. Nguyen and S. S. Kwak, "Nearest-level control method with improved output quality for modular multilevel converters," *IEEE Access*, vol. 8, pp. 110237–110250, Jun. 2020.
[41] F. Zhang and G. Joos, "A predictive nearest level control of modular multilevel converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Charlotte, NC, USA, Mar. 2015, pp. 2846–2851.
[42] Z. Gong, P. Dai, X. Yuan, X. Wu, and G. Guo, "Design and experimental evaluation of fast model predictive control for modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3845–3856, Jun. 2016.
[43] P. Cortes, J. Rodriguez, C. Silva, and A. Flores, "Delay compensation in model predictive current control of a three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 1323–1325, Feb. 2012.
[44] J. Rodríguez and P. C. Estay, *Predictive Control of Power Converters and Electrical Drives*. Hoboken, NJ, USA: Wiley, 2012.
[45] B. Gutierrez and S.-S. Kwak, "Modular multilevel converters (MMCs) controlled by model predictive control with reduced calculation burden," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9176–9187, Nov. 2018.
[46] M. H. Nguyen and S. S. Kwak, "Simplified indirect model predictive control method for a modular multilevel converter," *IEEE Access*, vol. 6, pp. 62405–62418, Oct. 2018.

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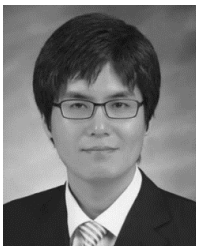

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