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Transmission Lines-Based Impedance Matching Technique for Broadband Rectifier

SUMIN DAVID JOSEPH[1], YI HUANG[1], (Senior Member, IEEE), AND SHAWN S. H. HSU[2], (Member, IEEE)

[1]Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool L69 3GJ, U.K.
[2]Department of Electrical Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan

Corresponding authors: Yi Huang (yi.huang@liverpool.ac.uk) and Shawn S. H. Hsu (shhsu@ee.nthu.edu.tw)

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ABSTRACT A high-efficiency compact broadband rectifier is developed for wireless energy harvesting. A novel three-stage impedance matching technique is utilized in a broadband rectifier design to achieve high conversion efficiency with a compact size. In the rectifier, a low loss impedance matching technique is initiated by employing a linearly tapered transmission line for controlling the impedance curve at the required input power level, followed by two stages to make a circular impedance curve for wideband impedance matching. Both theoretical analysis and numerical simulations of the proposed rectifier are performed. For validation, a prototype is fabricated and demonstrated a broadband performance with a fractional bandwidth (FBW) of 74% (from 1.12 to 2.43 GHz) and power conversion efficiency of more than 50% at a 5 dBm input power level. Moreover, the rectifier can reach an efficiency of more than 50% extending from 0.97 to 2.55 GHz (FBW = 90%) at the input power of 10 dBm, which is the highest bandwidth reported under this condition. This low complexity design is suitable for realizing broadband rectifiers for wireless energy harvesting (WEH) applications.

INDEX TERMS Broadband rectifier, energy harvesting, impedance matching, rectenna, transmission lines, wireless power transmission.

I. INTRODUCTION

Wireless power transmission and energy harvesting using rectennas have gained much interest in the recent years due to the increasing demand for various applications such as low-power electronics, wireless chargers, medical devices, and IoT (Internet of Things) [1]. Several literatures demonstrated the possibility of utilizing the power from various radio frequency (RF) transmitters including, FM, TV, cellular, and Wi-Fi systems to operate low-power electronics [2], [3]. However, the complex propagation settings, broadcasting schedules and changing demands of these transmissions result in variable nature of the time-/space-varying ambient RF power. Thus, it is necessary to harvest RF energy from a large frequency spectrum to ensure the required power for various real-life applications [4]. Broadband or multiband rectennas are therefore needed [5]. Due to the non-linearity of diodes, also the varying input impedance with both the input power and the operating frequency making the broadband matching difficult, the RF to DC conversion efficiency reduces considerably in broadband rectennas compared to narrow band rectennas. There are only few broadband rectennas reported with good conversion efficiency [5]–[7].

To address this problem, several approaches (such as the resistance compression network, stacked RF harvester and the resistance-controlled DC–DC converter) have been reported for realizing high performance broadband or multiband rectennas [8]–[11]. Resistance compression networks (RCNs) are introduced to reduce the sensitivity and nonlinearity of rectennas. Moreover, the large variation of load impedance can be compressed using this technique which results in a smaller variation of the input impedance [8]. A broadband rectifier based on a branch-line coupler was presented in [9]. Even though the coupler added an insertion loss of 0.9 dB and took up a reasonably large circuit area, a fractional bandwidth of 21.5% was realized. A non-uniform transmission line-based octave band rectifier exhibited a broad bandwidth ranging from 470 to 860 MHz at 10 dBm input power with efficiency over 60% [10]. In [11], a compact broadband rectifier with efficiency over 30% from 870 MHz to 2.5 GHz was presented based on two cascaded L-section reactive elements. The rectifier achieved a wide bandwidth by introducing several lumped elements for impedance matching. Source pull simulation was used in [12], to find the

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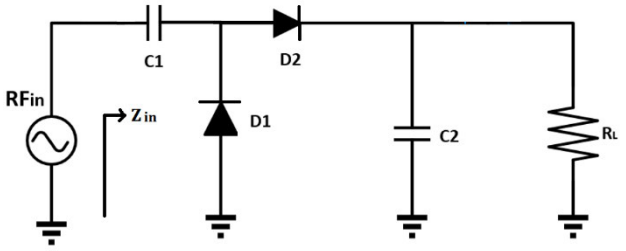

FIGURE 1. Schematic diagram of the reference voltage doubler configuration.

optimum load impedance for realizing a 58% fractional bandwidth (FBW) with more than 50% efficiency. Most of the previously proposed broadband rectifiers not only demand complex matching procedures but also reduce the efficiency because of the loss introduced by the circuit components. Thus, more efforts are required to develop a highly efficient, robust, flexible, and simple broadband rectifier for wireless energy harvesting applications.

In this paper, a broadband rectifier is realized by employing a novel transmission lines-based impedance matching technique. In this proposed rectifier, a voltage doubler topology is combined with a tapered line; a short circuit stub and a pair of open stubs are employed to widen the frequency bandwidth and maintain high efficiency. The detailed design procedure and theoretical analysis are presented in Section II. Measured results of the fabricated rectifier and analysis of its performance are addressed in Section III. Comparison of the proposed rectifier performance with other broadband designs is made in this section. Finally, conclusions are drawn in Section IV highlighting the achievements of this work.

II. PROPOSED BROADBAND RECTIFIER DESIGN

Schottky diodes are key elements for the rectification of RF signals in WEH and WPT scenarios because of their fast-switching properties and low threshold voltage [13]. But the capacitive nature of Schottky diodes imposes difficulties in impedance matching. Adopting complex circuits with lumped elements to realize broadband matching results in the reduction of power conversion efficiency. Different topologies with the diodes are introduced for implementing broadband rectifiers. The single series topology has the advantage of low biasing requirement, but the low breakdown voltage limits the power handling capabilities, which will be harmful for the broadband performance [14]. Moreover, this topology can only provide a narrow bandwidth. To improve the power handling capabilities, multi-diode rectifiers such as charge pump rectifiers with two or more diodes can be used [15]. But it affects the performance at low input voltage due to the loss factor and also increases the complexity. In this design, a voltage doubler configuration with two diodes is selected which offers the benefit to maintain a minimum circuit complexity while achieves low-power performance.

Fig. 1 shows the schematic diagram of a typical voltage doubler configuration. The rectifier consists of capacitors *C1* and *C2* which have the function of storing the energy rectified

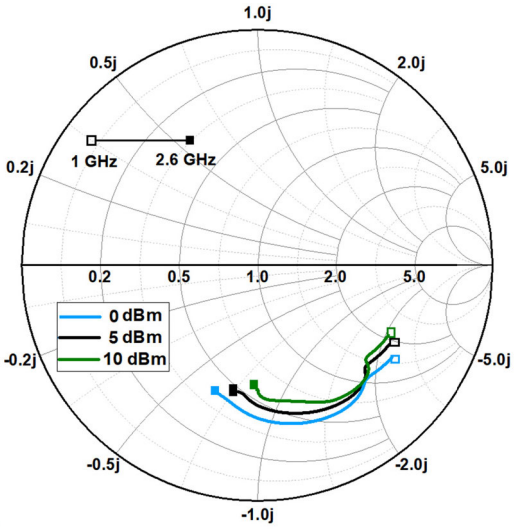

FIGURE 2. Input impedance Z_{in} of reference voltage doubler at different input power levels.

by the rectifying elements *D1* and *D2*. Schottky diodes HSMS 2850 from Avago have been selected in this voltage doubler rectifier design due to its low threshold voltage and junction capacitance [16]. The rectifier is designed to operate from $f_l = 1.0$ to $f_h = 2.6$ GHz (to cover the UK GSM-1800/4G, 3G/UMTS-2100, and WLAN-2.4 GHz bands) with a load impedance of 1 kΩ. The vital factor for the design of a broadband rectifier is the impedance matching circuit. Due to the nonlinearity of the rectifier, the input impedance Z_{in} depends on the operating frequency range f_{req}, input power P_{in}, load resistor R_L and the nonlinear impedance of the diode Z_d.

$$Z_{in} = f(f_{req}, P_{in}, R_L, Z_d) \tag{1}$$

Fig. 2 shows the input impedance Z_{in} of the reference doubler design over the frequency band f_l to f_h at three different power levels by using the Harmonic Balance (HB) simulation in Advanced Design System (ADS). It can be observed that the rectifier has a large capacitance over the entire operating band. Resistive and capacitive impedance of the rectifier is decreasing with frequency at the different input power levels. Furthermore, the low input power levels appear to be more difficult to match than the high input power levels. For easy analysis, we define the mid frequency of the operating frequency band as $f_m = (f_l + f_h)/2$. At f_l, f_m and f_h, the diode input impedance of reference design at a 5 dBm input power level (P_{in}) can be observed as $Z_{in}(f_l) = 105.7 - 115.5\text{j}\ \Omega$, $Z_{in}(f_m) = 39.50 - 83.4\text{j}\ \Omega$ and $Z_{in}(f_h) = 30.16 - 42.75\text{j}\ \Omega$.

To overcome the losses due to the lumped elements in complex broadband impedance matching circuits and to maintain a high efficiency performance, a novel transmission lines-based impedance matching technique is introduced. Fig. 3 shows the schematic diagram of the proposed broadband rectifier comprising of the three-stage matching process. Impedance matching is achieved by employing the three-stage process which consists of a tapered microstrip line,

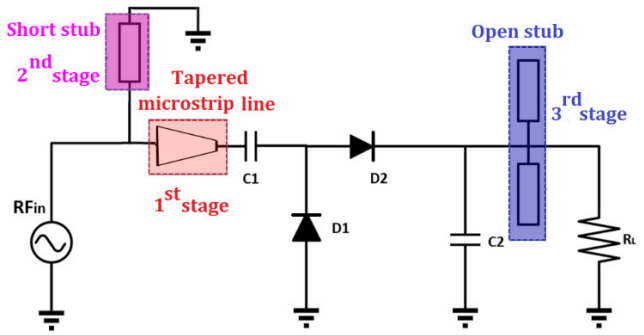

FIGURE 3. Schematic of the proposed broadband rectifier.

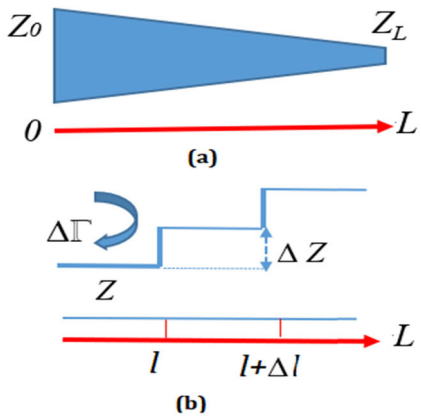

FIGURE 4. (a) Linearly tapered transmission line (b) Model of an incremental impedance step in line.

a short circuit stub and a pair of open stubs in DC pass filter. The proposed rectifier is suitable for a wide range of operating frequencies and load impedances.

A. DESIGN OF THE 1st STAGE

A linearly tapered microstrip line is utilized in the 1st stage of broadband realization. A tapered microstrip line is intended to make input impedance symmetric with respect to the real axis (resistance axis) and to maintain the mid frequency $Z_{in1}(f_m) \approx 25\ \Omega$. Instead of having a stepped impedance transformer, the linearly tapered impedance transformer helps to improve the bandwidth. Fig. 4(a) shows a linearly tapered transmission line connecting to a source with an impedance of Z_0 at the input and connecting to Z_L at the output. Considering a multisection tapered transmission line is made up of many small sections of length Δl as in Fig. 4(b), the incremental reflection coefficient can be expressed as

$$\Delta\Gamma = \left|\frac{((Z+\Delta Z)-Z)}{((Z+\Delta Z)+Z)}\right| \approx \frac{\Delta Z}{2Z} \tag{2}$$

In order to reduce the reflections, it is required to consider a very small Δl. As $\Delta l \rightarrow 0$, the exact differential can be estimated as in [17]

$$d\Gamma = \frac{d(ln(Z/Z_0))dZ}{2dZ} \tag{3}$$

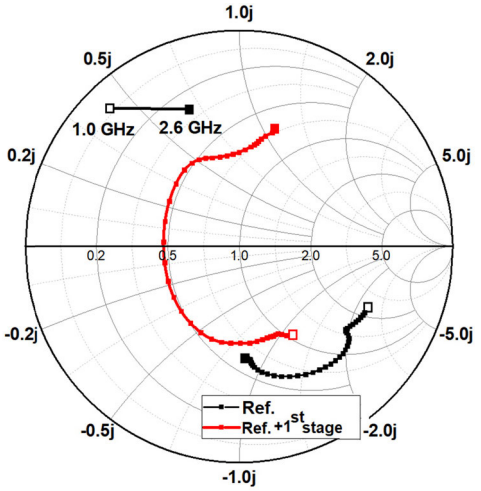

FIGURE 5. Input impedance Z_{in1} after the 1st stage design at $P_{in} = 5$ dBm.

The total reflection coefficient at $l = 0$ by combining all the partial reflections with their appropriate phase shifts.

$$\Gamma(\theta) = \frac{1}{2}\int_0^L e^{-j2\beta l}\frac{d(ln(Z/Z_0))dl}{dl} \tag{4}$$

The length of the tapered line is determined by minimizing the reflection coefficient at the input, $\Gamma(\theta)$. Fig. 5 shows the input impedance Z_{in1} after the 1st stage over 1.0 to 2.6 GHz at $P_{in} = 5$ dBm. As observed, the imaginary part of input impedance is odd symmetrical with $Z_{in1}(f_m)$ around 25 Ω achieved by the 1st stage of impedance matching. At f_l, f_m, and f_h, the diode input impedance after the 1st stage at $P_{in} = 5$ dBm can be observed as $Z_{in1}(f_l) = 50 - 52.9\text{j}\ \Omega$, $Z_{in1}(f_m) = 24.5\ \Omega$, and $Z_{in1}(f_h) = 35 + 52.8\text{j}\ \Omega$. It can be observed that the reactance part of $Z_{in1}(f_l)$, and $Z_{in1}(f_h)$ are approximately conjugate.

$$X_{in1}(f_l) \approx -X_{in1}(f_h) \tag{5}$$

B. DESIGN OF THE 2nd STAGE

A short circuit shunt stub with the characteristic impedance Z_s and θ_s is added in the 2nd stage to cancel out the imaginary part of $Z_{in1}(f_l)$ and $Z_{in1}(f_h)$, making the real part nearly constant. The input admittance of short circuit shunt stub can be represented as

$$Y_s(f) = \frac{1}{jZ_s tan\theta_s(f)} \tag{6}$$

Proper width and length of shunt stub can be employed to make the imaginary part at f_l and f_h close to zero.

$$Imag(Y_{in1}(f_l)) = -(Imag(Y_{in1}(f_h))) = -jB \tag{7}$$

Therefore,

$$Y_s(f_l) = \frac{1}{jZ_s tan\theta_s(f)} = jB \tag{8}$$

$$Y_s(f_h) = \frac{1}{jZ_s tank\theta_s(f)} = -jB \tag{9}$$

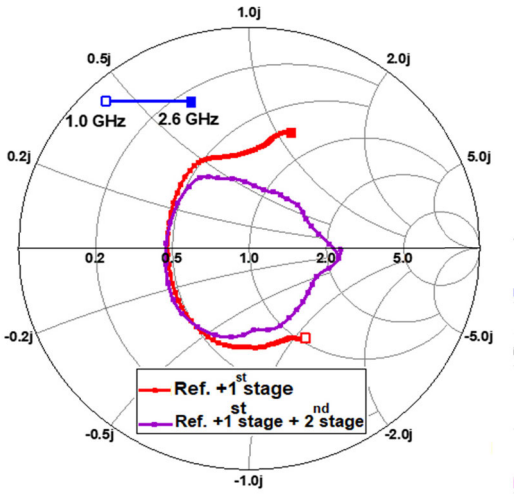

FIGURE 6. Input impedance Z_{in2} after the 2nd stage design at $P_{in} = 5$ dBm.

By combining (8) and (9), the short circuit shunt stub dimensions can be derived as

$$\theta_s = \frac{\pi}{(1+k)} \tag{10}$$

$$Z_s = \frac{1}{B\tan(K\theta_s)} \tag{11}$$

Thus, the characteristic impedance Z_s and electrical length θ_s of the short circuit shunt stub can be estimated. In this design, a length of 25 mm and a width of 0.8 mm are utilized after careful ADS simulation. Fig. 6 shows the input impedance Z_{in2} after the 2nd stage over 1.0 to 2.6 GHz at $P_{in} = 5$ dBm. It clearly reveals the circular impedance curve obtained after 2nd stage impedance matching. Moreover, the reactance part of $Z_{in2}(f_l)$ and $Z_{in2}(f_h)$ approaches zero as intended.

$$X_{in2}(f_l) \approx -X_{in2}(f_h) \approx 0 \tag{12}$$

C. DESIGN OF THE 3rd STAGE

A broad stopband DC-pass filter is required at the output of the rectifier to choke the RF signals within a wide frequency range. In conventional rectenna design, a DC pass filter is employed to acquire a ripple free DC signal by suppressing the fundamental and harmonic frequencies from the rectified output. Even though a large value of capacitor (typically higher than 100 pF) can be utilized with *RL* for realizing the output low-pass filter, the equivalent series resistance (ESR) of a large capacitor results in power losses, reduced efficiency, and instability of power supplies and regulators circuits. Thus, parallel connection of small capacitors is utilized to reduce the effective ESR in addition to reducing the ripple voltage and allows the circuit to handle higher currents with less losses [18]. In [19], open stubs are utilized to substitute shunt-to-ground capacitor to produce additional transmission zero in each transmission path to improve the required stopband level. Therefore, a combination of open stubs and a small shunt capacitor are introduced for enhancing the stop band and to realize a ripple free DC voltage in this design. Additionally, the open stubs are also helpful to improve the impedance matching by fine tuning of the stub dimensions.

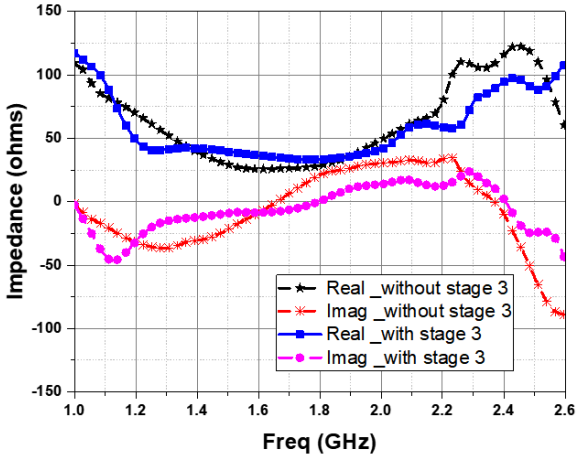

FIGURE 7. Real and imaginary parts of input impedance Z_{in3} with and without the 3rd stage design.

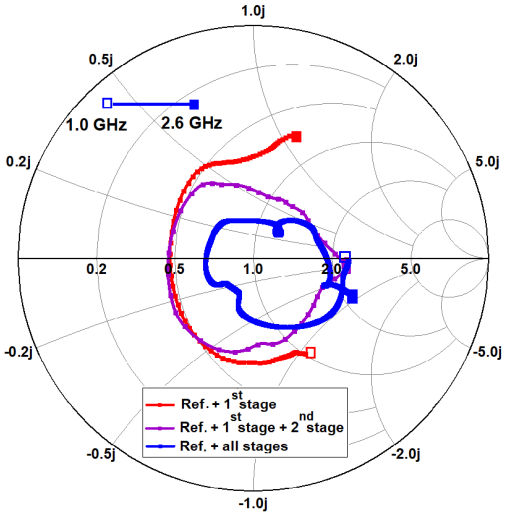

FIGURE 8. Input impedance Z_{in3} after the 3rd stage design at $P_{in} = 5$ dBm.

In the 2nd stage, a constant reflection coefficient circle is achieved with a VSWR value of around 2. For high RF-DC efficiency performance, it is necessary to shrink the impedance curve close to 50 Ω. As the DC-pass capacitor C2 is having a low value of 22 pF, a pair of open circuit shunt stubs are utilized to perform the fine-tuning of rectifier impedance and to achieve high output DC power. Fig. 7 shows the real and imaginary parts of the rectifier impedance in with and without adding stage 3. The imaginary part of impedance crosses 0 Ω three times as expected (at f_l, f_h and f_m). It can be observed that the open stubs help to make the real part close to 50 Ω and the imaginary part more constant about 0 Ω in the desired band. Fig. 8 shows the input impedance Z_{in3} after the 3rd stage over 1.0 to 2.6 GHz at $P_{in} = 5$ dBm.

Following the three-stage process, a broadband rectifier is designed. Layout level simulations are performed

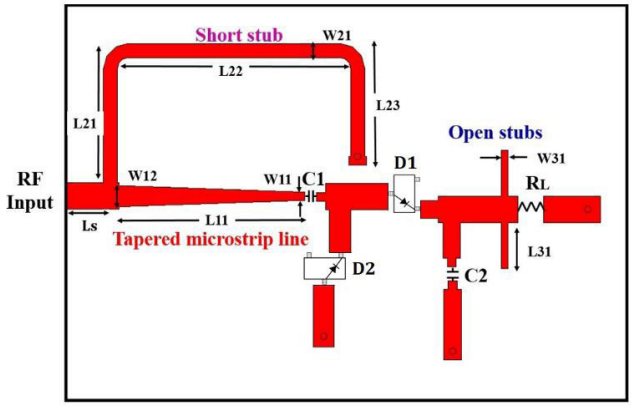

FIGURE 9. Layout of the proposed broadband rectifier.

TABLE 1. Parameters of the proposed rectifier.

Parameter	Value (mm)	Parameter	Value (mm)
W11	0.5	L11	10
W12	1.2	L21	7
W21	0.8	L22	12.5
W31	0.4	L23	5.5
L31	2.6	Ls	3

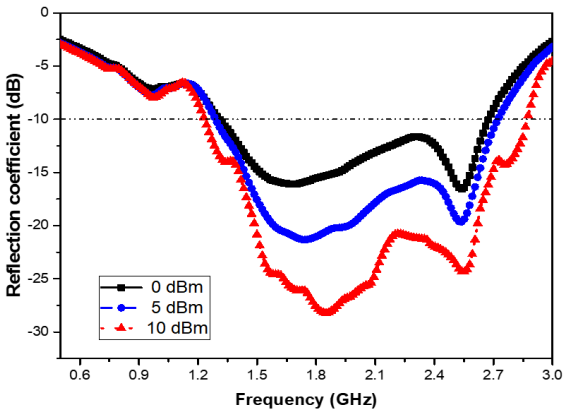

FIGURE 10. Simulated reflection coefficients of broadband rectifier at three input power levels.

using electromagnetic (EM) simulator Momentum in ADS. Fig. 9 shows the layout of the proposed rectifier and the parameters are summarized in Table 1. The simulated reflection coefficients at three input power levels are shown in Fig. 10. It can be observed that at 10 dBm input power, the simulated return loss is better than 10 dB over a 1640 MHz bandwidth from 1.23 to 2.87 GHz. The reflection coefficient is better than -10 dB for a wide bandwidth at the desired input power levels. At high input powers, the impedance matching performance is comparably better than that of low input power levels.

III. BROADBAND RECTIFIER PERFORMANCE

The proposed broadband rectifier is fabricated for experimental validation on a Rogers 4350B material of 1.52 mm

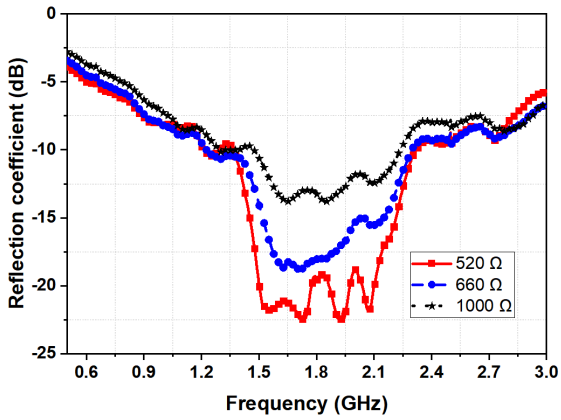

FIGURE 11. Reflection coefficients of the broadband rectifier at different load resistors.

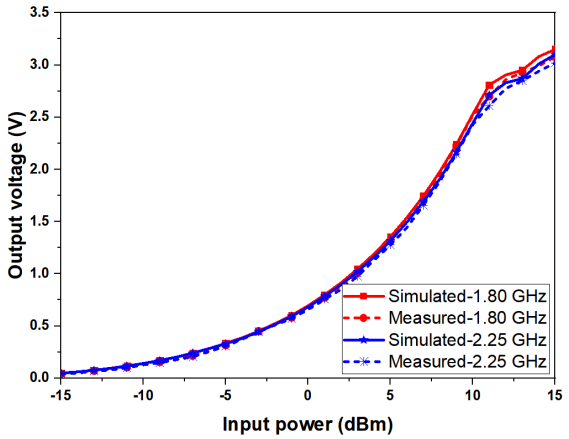

FIGURE 12. Output voltage versus input power.

thickness with a relative permittivity of 3.48. Initially, the reflection coefficient of the rectifier was evaluated using a VNA. In Fig. 11, the measured reflection coefficient at 0 dBm input power with different load values are shown. At 520 Ω, the measured 1.3 GHz bandwidth ranges from 1.2 to 2.5 GHz which corresponds to a fractional frequency bandwidth of 70%. Even though, the upper limit crosses −10 dB at 2.5 GHz, reflection coefficient is around −9 dB till 2.75 GHz. For higher load values, the impedance bandwidth is decreased.

The power conversion efficiency of the fabricated rectifier is evaluated using the measurement setup shown in Fig. 13. A Keithley 2920 RF signal generator with an output power up to 13 dBm was utilized to generate the RF signal at 1 to 3 GHz. A 40 dB gain GaN power amplifier was employed to amplify the signal for the testing of broadband rectifier. To protect the signal generator from any power surge and reflections, a 3-dB attenuator was connected between the signal generator and power amplifier. For analyzing and estimating the signal power from the power amplifier, a Keithley signal analyzer together with a 20 dB attenuator is utilized. A digital multimeter is used to measure the output voltage across the R_L resistor. The measurement setup is

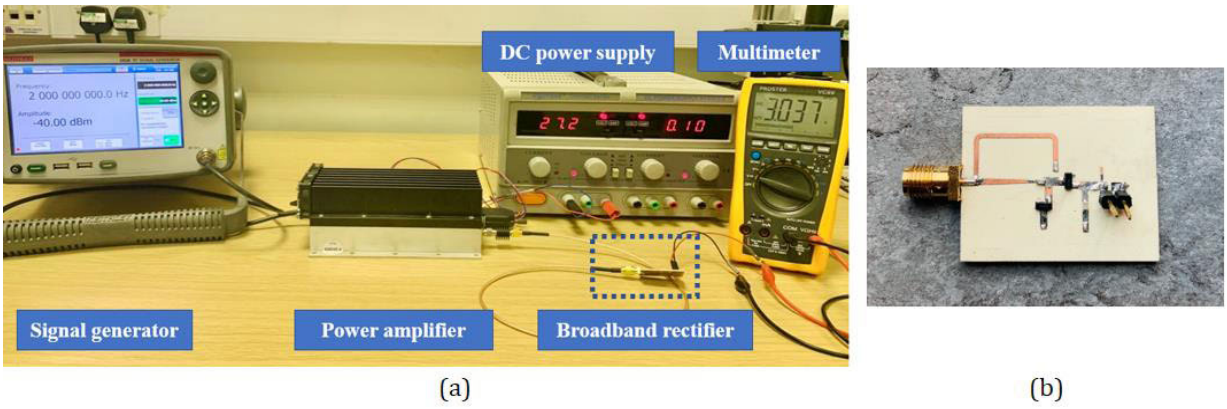

FIGURE 13. (a) Measurement setup of broadband rectifier (b) Fabricated rectifier.

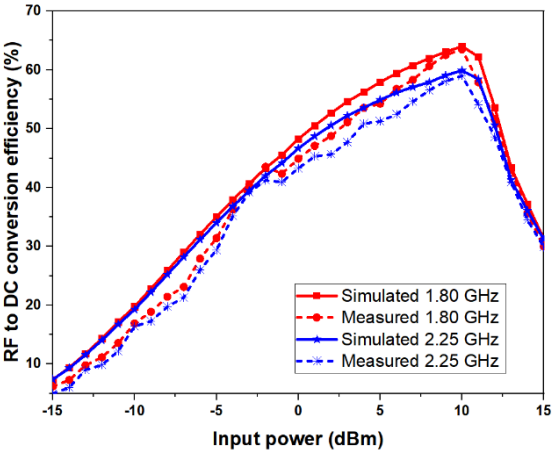

FIGURE 14. RF-DC conversion efficiency versus input power.

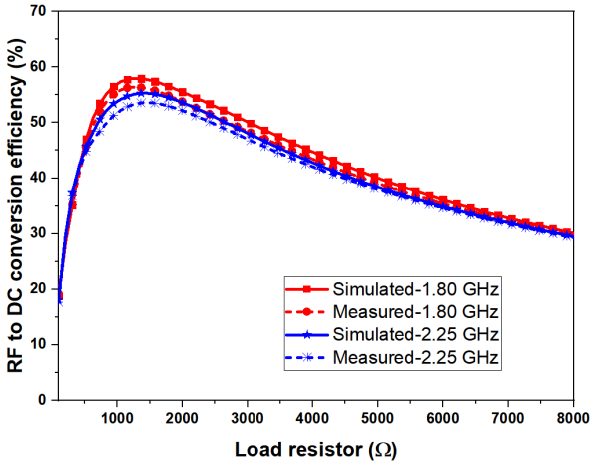

FIGURE 15. RF-DC conversion efficiency versus load resistor at an input power of 5 dBm.

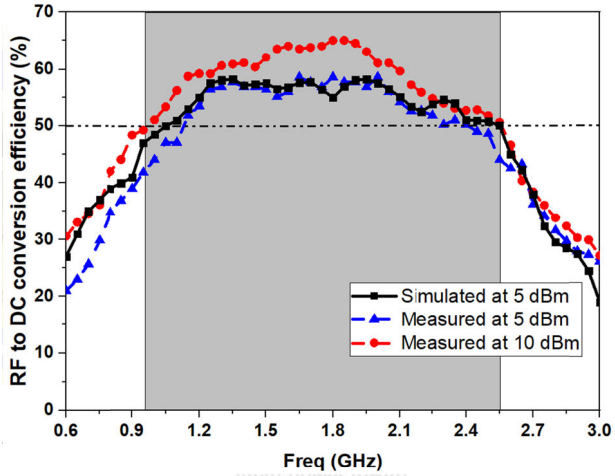

FIGURE 16. RF-DC conversion efficiency versus frequency at an input power of 5 dBm and 10 dBm.

appropriately calibrated considering all device losses to provide the most reliable results. Initially, output voltage is measured at 1.8 and 2.25 GHz by varying the input power from −15 to 15 dBm as shown in Fig. 12. It can be observed that maximum output voltage of 3.1 V is measured at 1.8 GHz. Simulated and measured values are in close agreement. The RF-to-DC conversion efficiency (η) of a microwave rectifier is calculated as the ratio of the rectified DC output power to the incident RF power, it can be expressed as

$$\eta = V_{out}^2 \Big/ R_L P_{in} \times 100\% \tag{13}$$

where P_{in} is the input power and V_{out} is the DC output voltage across the load resistor R_L of the microwave rectifier. Fig. 14 shows the simulated and measured conversion efficiencies of the proposed microwave rectifier at 1.8 and 2.25 GHz as a function of input power. Maximum efficiency of 65% is achieved at 1.8 GHz with 10 dBm input power. Fig. 15 depicts that the proposed rectifier has a relatively stable efficiency over a wide circuit load range from 300 to 8000 Ω. This shows that the proposed rectifier could be integrated with different load devices.

For analyzing the broadband performance of the rectifier, the RF-to-DC conversion efficiency is measured at an input power level of 5 dBm and 10 dBm as shown in Fig. 16 by varying the frequencies from 0.6 to 3 GHz. It can be observed that a peak efficiency of 58% is obtained at 1.8 GHz by 5 dBm input power. The conversion efficiency is higher than 50 % for

TABLE 2. Comparison of the proposed rectifier with related rectifiers.

Ref. (year)	Description	Efficiency in operating bandwidth at input power			Area (λ^2)
		FBW (GHz)	η (%)	Input power (dBm)	
[20] (2019)	Dual-stub matching network	2.2-2.7 (20.4%)	>50	5	N.A.
[21] (2019)	Multi-stage matching, and a DC-pass filter	1.75-3.2 (58.5%)	>50	10	0.29 ×0.31
[22] (2018)	Two-Stage Matching Network	1.5-2.3 (42.1%)	>50	5.5	N.A.
[23] (2018)	Non-uniform transmission line matching	0.45-0.86 (67%)	>50	10	0.22 ×0.31
[24] (2020)	Microstrip line matching of shunt rectifier	2-3.3 (45%)	>50	4	0.16 ×0.27
This work	**3-stage matching technique**	**1.12-2.43 (74%)** **0.97-2.55 (90 %)**	**>50** **>50**	**5** **10**	**0.14 ×0.21**

*λ is the free-space wavelength at center frequency of the operating band.

a fractional bandwidth (FBW) of 74% from 1.12 to 2.43 GHz at 5 dBm input power. At 10 dBm, the conversion efficiency is higher than 50 % from 0.97 to 2.55 GHz (FBW = 90%).

In order to evaluate the performance of the proposed rectifier, it is compared with other similar broadband rectifiers in Table 2. The important parameters are the operational bandwidth, efficiency, input power, and size. It can be concluded that our transmission line-based impedance matching design achieves high conversion efficiency over a wide frequency band. More specifically, a fractional bandwidth (FBW) of 74% is achieved at 5 dBm and 90% at 10 dBm input power which is the highest among all the designs under comparison. Furthermore, our design has the smallest overall dimension 24 × 36 mm^2 (electrical size is $0.14\lambda \times 0.21\lambda$). Therefore, the proposed rectifier is very much suitable for energy harvesting applications due to its small footprint and high energy conversion efficiency performance over a wide bandwidth at low input power.

IV. CONCLUSION

A compact broadband rectifier for microwave energy harvesting has been proposed. This approach utilized a novel three-stage transmission lines-based impedance matching technique to achieve a broadband rectifier with excellent RF-to-DC conversion efficiency. A circular impedance curve has been realized by utilizing a tapered microstrip line, short circuit shunt stub and open stubs. The fabricated broadband rectifier achieved a conversion efficiency of more than 50% at a 5 dBm input power level over a wide bandwidth of 1.12-2.43 GHz (FBW = 74%). In addition, the rectifier has more than 50% efficiency from 0.97-2.55 GHz (FBW = 90%) at an input power of 10 dBm, which is the highest bandwidth reported under this condition to the best of our knowledge. The proposed transmission lines-based impedance matching design has superior performance in terms of its wide bandwidth and compactness making it suitable for realizing broadband rectifier for WEH and WPT applications.

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SUMIN DAVID JOSEPH received the B.Tech. degree (Hons.) in electronics and communication from the Cochin University of Science and Technology, India, in 2012, and the M.Tech. degree (Hons.) in communication systems from the Visvesvaraya National Institute of Technology, India, in 2015. He is currently pursuing the dual Ph.D. degree in electrical engineering with the University of Liverpool, U.K., and National Tsing Hua University, Taiwan.

He was a Lab Engineer under CoE with the Visvesvaraya National Institute of Technology, where he was involved in projects of national importance. He serves as a technical reviewer for leading academic journals and conferences. His research interests include self-biased circulators, mm-wave antenna arrays, rectifying antennas, rectifiers, wireless power transfer, and energy harvesting.

YI HUANG (Senior Member, IEEE) received the B.Sc. degree in physics from Wuhan University, China, in 1984, the M.Sc. (Eng.) degree in microwave engineering from NRIET, Nanjing, China, in 1987, and the D.Phil. degree in communications from the University of Oxford, U.K., in 1994.

He worked as a Research Fellow at British Telecom Labs, in 1994, and then, he joined the Department of Electrical Engineering and Electronics, University of Liverpool, U.K., as a Faculty, in 1995, where he is currently a Full Professor of Wireless Engineering, the Head of High Frequency Engineering Group, and the Deputy Head of Department. He has published over 350 refereed papers in leading international journals and conference proceedings, and authored three books, including a bestseller *Antennas: From Theory to Practice* (Wiley, 2008, 2021). He has received many patents, research grants from research councils, government agencies, charity, EU, and industry. His experience includes three years spent with NRIET, as a Radar Engineer, and various periods with the Universities of Birmingham, Oxford, and Essex at U.K., as a member of Research Staff. He has been conducting research in the areas of wireless communications, applied electromagnetics, radar and antennas, since 1987. More recently, he is focused on mobile antennas, wireless energy harvesting, and power transfer.

Dr. Huang is currently a Fellow of IET and Senior Fellow of HEA. He was a recipient of over ten awards, such as the BAE Systems Chairman's Award 2017 and best paper awards. He has served for a number of national and international technical committees and has been an editor, an associate editor or a guest editor of five international journals. In addition, he has been a keynote/invited speaker and organizer of many conferences and workshops, such as IEEE iWAT2010, LAPC2012, and EuCAP2018. He is currently the Editor-in-Chief of *Wireless Engineering and Technology*, an Associate Editor of IEEE Antennas and Wireless Propagation Letters, U.K., and Ireland Representative to European Association of Antenna and Propagation (EurAAP).

SHAWN S. H. HSU (Member, IEEE) received the B.S. degree in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1992, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Michigan, Ann Arbor, MI, USA, in 1997 and 2003, respectively.

He is currently a Professor with the Department of Electrical Engineering, Institute of Electronics Engineering, National Tsing Hua University. He is involved in the design, fabrication, and the modeling of high-frequency transistors and interconnects. His research interests include the design of monolithic microwave integrated circuits and RF integrated circuits using Si/III–V-based technologies, heterogeneous integration using system-in-package, and three-dimensional integrated circuit technology for high-speed wireless/optical communications and power electronics applications.