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Investigation of Electrical Behaviors Observed in Vertical GaN Nanowire Transistors Using Extended Landauer-Büttiker Formula

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ABSTRACT In this report, we study nonlinear electrical behaviors found in vertical-architecture transistors based on wrap-around-gated gallium nitride (GaN) nanowires (NWs) by extending a one-dimensional case of the Landauer-Büttiker formula. Here, the GaN NWs are considered ''almost'' one-dimensional ideal wires connecting the drain and source terminals, with the gate terminal serving to control the flowing current. Unlike previous models, which require several parameters and complex calculations, our proposed model only needs three parameters and simple calculations to match the experimental data. With this model, we confirm that the maximum current before saturation is a consequence of quasi-ballistic drain current. Thus, electron mobility has no effect in this device. Using a simple formulation, we discuss gating hysteresis in the device that is mediated by the selected oxide layer interface. We show that the memory effect of the device is attributed to time-delay current. The shorter gate length increases the transmission coefficient. As a result, the model can be employed to predict the next-generation NW transistor performance.

INDEX TERMS Conductance, density of states, GaN nanowire transistor, nonlinear drain current, time-delay current, transmission coefficient.

I. INTRODUCTION

Gallium nitride (GaN)-based transistors are promising candidates for the next-generation power-conversion devices, which offer a low on-resistance (R_{on}), fast switching rate, high frequency, and highly efficient power conversion because of their wide band gap and high electron mobility [1]–[4]. Commonly, the devices are realized with a single nanowire (NW) structure, where they are transferred from the original substrate onto some foreign carrier substrates and are subsequently processed by electron-beam lithography in a planar architecture. AlGaN/GaN-based high electron mobility transistors (HEMTs) are an excellent candidate for highly efficient switched power supplies. However, the heterojunction structure of HEMTs will typically produce stress and strain that can induce spontaneous polarization. Introducing a high-quality B-doped GaN cap layer with low surface-related defects under the gate has been proven to be efficient in dealing with the polarization effect [5]–[8].

Furthermore, Yu *et al.* recently fabricated vertical-architecture structures from GaN nanowires (NWs) with wrap-around gates for optimum electrostatic control, made by top-down etching [9]. They used a-plane GaN NWs for the channel and an etched nanowire architecture to eliminate stress and strain. Thus, the polarization effect was negligible in their device. A seven-nanowire transistor exhibits an enhancement mode operation with a threshold voltage of 1.2V, an on/off current ratio as high as 10^8, and a subthreshold slope as low as 68 mV/dec. In addition, the device can reach a drain current and transconductance of up to 314 mA/mm and 125 mS/mm, respectively [9], [10].

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Several device design and processing optimizations were conducted (e.g., introduction of the p-type channel, insertion of mesa mechanical support, and change of gate oxide from SiO_2 to Al_2O_3 thin films), allowing higher threshold voltages, enhanced joining technique of the device with characterization instruments, and reduction of gate hysteresis to nearly zero level under different current sweep directions, respectively [4], [11], [12]. Moreover, they have demonstrated current upscaling capability of the devices by realizing and measuring transistors with different numbers of integrated GaN nanowires on a single 2-inch wafer.

A recent hydrodynamic study analyzing the performance of vertical GaN NW transistors with a non-overlapping gate structure based on the work in Yu *et al*. [9] has been reported by Witzigmann *et al*. [13]. In that study, the energy flux was only applied to electrons, while a drift-diffusion system was applied to holes to account for velocity overshoot effects, especially in the drift region of the transistor. The study found that electrons in motion do not follow the equilibrium of the Fermi–Dirac distribution and showed that the curve for drain current against drain-source voltage (i.e., I_d–V_{ds}) is nonlinear in the low-voltage regime. However, Witzigmann *et al*. did not find a maximum current in the high-voltage regime, as observed in the experiment [9].

Moreover, a common model used to study GaN-based metal-oxide-semiconductor field effect transistors (MOSFETs) performance is gradual channel approximation (GCA) [14]–[16], although it still cannot explain the nonlinear behavior of the I_d–V_{ds} curve. Meanwhile, the Mott–Gurney law is less appropriate for solving the device issues [9]. This is because these laws are limited to high-voltage operations [17], [18]. Nanostructures based on these laws can have non-constant mobility [19], [20]; hence, the laws cannot be applied to the completion of their functions.

In nanoscale devices, it is not possible to apply the drift-diffusion-based simulation approach to explain related physical phenomena, because the mean free path of the carrier charge is comparable to the channel length of the device. For nanoscale devices, Natori's ballistic models are often used instead [21]. However, there is a marked difference between the current-voltage characteristics of a purely ballistic model and experimental data. The tunneling current model might provide an accurate description of the experimental data from several studies [22]–[25], though it requires complex mathematics to calculate the NW current behavior. Until now, a simple model explaining the phenomenon of the nonlinear current behavior in GaN NW transistors has not been available. Such a model is urgently required to gain new physical insights into GaN NW transistors and to further optimize their design and fabrication.

In this article, we describe our model of the drain current nonlinear behavior in a vertical GaN NW transistor. The model was developed by extending the ''ideal wire'' of Landauer-Büttiker's work with an almost one-dimensional case, where the resulting current is directly proportional to the density of states (DOS) and the quasi-Fermi level, implying that the conductance is also directly proportional to the DOS [26]. To check the accuracy of the model, the theoretical results were compared to the experimental data in Yu *et al*. [9] and Fatahillah *et al.* [11] using three fitting parameters. By using a simple formulation, we also discuss gating hysteresis in the device, which is mediated by the selected oxide layer interface. Thus, the model can predict the existing physical phenomena in the device and is suitable for determining the characteristics of the transistor prior to further device fabrication.

II. METHODS

A. GaN NANOWIRE TRANSISTOR

We study the nonlinear behavior of drain current from two different types of vertical GaN nanowire transistors fabricated by Yu *et al*. [9] and Fatahilah *et al*. [11]. The striking difference between those two devices is their gate dielectric materials. The former FET employed silicon dioxide (SiO_2) thin layer, while the latter counterpart used aluminum oxide (Al_2O_3) thin film, and has an added Mg acceptor in the channel and a shorter gate length. By optimizing gate dielectric material, gate hysteresis can be reduced during voltage sweep resulting in almost-zero threshold voltage shift (ΔV_{th}). To ease the discussion from the results obtained in this study, from this point forward, the devices fabricated by Yu *et al*. [9] and Fatahilah *et al*. [11] are assigned as GaN-FET_{SiO2} and GaN-FET_{Al2O3}, respectively. Moreover, those two vertical GaN NW FETs embedded different doped materials for their channels (i.e., unintentionally doped i-GaN and p-GaN, respectively), in which their original layer stacks were grown by metalorganic vapour-phase epitaxy (MOVPE) [9], [11].

The vertical GaN NW transistors were processed using a top-down approach. As a building block, the GaN NW arrays were prepared by combining UV photolithography, inductively coupled plasma reactive ion etching (ICP-RIE), and potassium hydroxide (KOH)-based wet chemical [see Fig. 1(a)]. This approach is more beneficial compared to the direct selective area growth (SAG) that is normally used in bottom-up approach, as the composition and doping concentration of the layer stacks can be well-defined by standard planar growth process [27], [28]. Besides, it has been known that bottom-up epitaxy of nanowire structures with complicated layer compositions (i.e., including n-GaN, p-GaN, and InGaN structures) suffers from the unreliable doping control and inhomogeneous material deposition along the wire sidewalls in c-axis direction [29]. Thus, as a result, the subsequent 3D processing of the grown nanostructures often face several difficulties and imperfections resulting in downgrading of the device performance. For instance, although the lithography has been involved during the SAG, the bottom-up GaN nanorods were grown irregularly with different heights and diameters [29]. Moreover, the growth process is very sensitive towards slight modifications of chamber temperature and patterning mask. Meanwhile, for top-down processing, the process is more reliable, in which the same hybrid etching

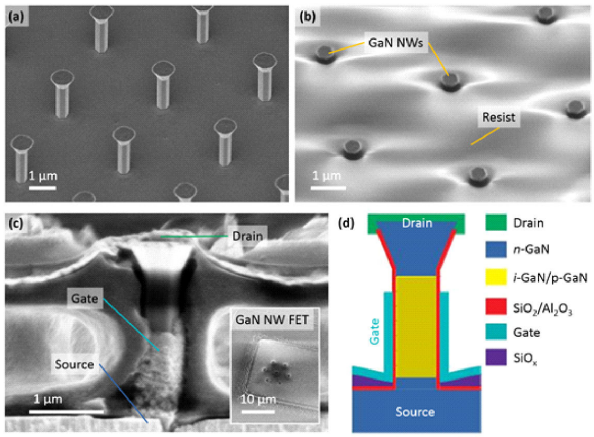

FIGURE 1. (a) Top-down GaN nanowire (NW) arrays fabricated by photolithography and hybrid etching techniques. (b) Resist filling process for creating mechanical support of the top drain contact. Cross-sectional (c) SEM image and (d) 2-D sketch of a single GaN NW field-effect transistor (FET). The inset shows the bird-view of an FET comprising seven GaN NWs. Here, either i-GaN or p-GaN can be opted as a conduction path or channel for two different transistor devices (i.e., GaN-FET$_{SiO2}$ and GaN-FET$_{Al2O3}$), where the SiO_2 and Al_2O_3 thin films deposited using atomic layer deposition (ALD) method were used as their gate dielectric materials, respectively. [9], [11].

recipe can be implemented directly onto different GaN nanostructures (e.g., vertical wires and fins) without changing the etch parameters.

After the GaN NWs have been prepared, a 20-nm-thick SiO_2 as a dielectric layer was deposited on their a-plane sidewalls at 300°C by plasma-enhanced atomic layer deposition (PEALD), using triethoxysilane and oxygen plasma as the silicon and oxygen precursors, respectively. However, it should be noted that to minimize gate hysteresis during forward and backward sweeps, ∼25 nm thick Al_2O_3 could be opted instead of SiO_2 as gate dielectric layer [11]. Then, a 200-nm-thick SiO_x as a passivation layer between highly doped source layer and gate metal was deposited by e-beam evaporation. Afterwards, the Cr layer with a thickness of 300 nm was coated by e-beam evaporation as a wrap-around gate. During the fabrication of the GaN NW FETs, several filling processes using photoresist were carried out, in which the resist was sufficiently stable to be used as a mechanical support of the top metal contact [see Fig. 1(b)]. Finally, in order to form a drain contact, a stack of Ti/Cr/Au (20/50/300 nm) layers was deposited on top of the nanowires [9]. To ensure the contact creation, the top part of the GaN NWs needed to be freely exposed. This metallization process was simultaneously performed to create the contact pads for other electrodes (i.e., gate and source). The cross-sectional scanning electron microscopy (SEM) image and schematic of a GaN nanowire transistor are depicted in Fig. 1(c) and (d), respectively. Details of the device fabrication can be found in [9], [11].

B. THEORETICAL MODEL

To create the model, we considered GaN NWs as one-dimensional wires with two reservoirs at each end, in which the source and drain are considered as a reservoir, and the gate length is the same as the channel length. The current inside the wire could then be represented by a simple formula based on Landauer-Büttiker's work [26], [30]

$$I_{chan} = G_0 T_e \frac{\Delta\mu}{q}, \tag{1}$$

where $G_0 T_e$ represents the conductance, q is the elementary charge, and $\Delta\mu = \mu_1 - \mu_2$. Here, μ_1 is the quasi-Fermi level of the left-end reservoir that emits charge-carrier flow to the right, and μ_2 is the quasi-Fermi level for the reverse direction. The term G_0 in (1) is the conductance quantum, with $G_0 = 2qv\left(\partial n/\partial E\right)$. The term v is the Fermi velocity, while $\partial n/\partial E$ is the density of state (DOS). For one-dimensional wires, the conductance quantum is constant and can be replaced with $G_0 = 2q^2/\hbar$, which means $\partial n/\partial E = 1/\pi\hbar v$. The complete derivative of conductance can be found in Ryndyk *et al.*'s work [31], but it is important to note here that conductance is proportional with DOS.

In the case of GaN-FET$_{SiO2}$ and GaN-FET$_{Al2O3}$, there are two conditions that must be considered in involving Landauer-Büttiker's formula. First, as Yu *et al.* [9] and Fatahilah *et al.* [11] showed, the slope of the I_d–V_{ds} curve varies depending on the gate-source voltage $\left(V_{gs}\right)$, indicating that G_0 is not constant. This means that the GaN NW model for GaN-FET$_{SiO2}$ and GaN-FET$_{Al2O3}$ cannot be considered as a "pure" one-dimensional case. Thus, G_0 represents the condition of electron motion inside the channel. We then carried out the investigation and found that the G_0 followed the DOS pattern of a three-dimensional bulk material. This means that the DOS followed $\partial n/\partial E \propto \sqrt{q\left(V_{gs} - V_{th}\right)}$. Therefore, the GaN-FET$_{SiO2}$ was approached as "almost" one-dimensional, and G_0 was modeled as

$$G_0 = \xi\sqrt{q(V_{gs} - V_{th})}, \tag{2.1}$$

where ξ is a fitting parameter for GaN-FET$_{SiO2}$ with a unit of $\mathrm{mAV}^{-3/2}$. However, for GaN-FET$_{Al2O3}$, which has a shorter gate length, G_0 follows the following formula:

$$G_0 = \zeta\left(q\left(V_{gs} - V_{th}\right)\right)^2, \tag{2.2}$$

which has characteristics of three-dimensional linear dispersion DOS. Here, ζ is a fitting parameter for GaN-FET$_{Al2O3}$ with a unit of $\mu\mathrm{AV}^{-3}$. This parameter determines the magnitude of G_0 for every gate voltage. V_{gs} refers to gate–source voltage, and V_{th} represents threshold voltage. Second, the non-overlapped gate structure of GaN-FET$_{SiO2}$ results in a drain-channel-source junction. We argue that this structure has a similar effect to a diode where the junction creates built-in potential. The difference with a GaN-FET$_{SiO2}$ is that its potential is controlled by gate-source potential. Consequently, $\Delta\mu$ is no longer equal to qV_{ds}, as explained by Landauer-Büttiker, but is formulated as

$$\Delta\mu = q(V_{ds} - V_{bi}). \tag{3}$$

Here, V_{ds} is the drain-source voltage and V_{bi} is the built-in potential as a function of gate-source voltage.

In (1), T_e represents transmission coefficient. In this study, we show that transmission coefficient for GaN-FET$_{SiO2}$ has a similar form to the Fermi–Dirac distribution, as shown below, where, the values of p and λ depend on the device character [see (A.9) of the Appendix]

$$T_e = \frac{1}{1 + \exp(\lambda\beta\Delta\mu + p)}. \tag{4}$$

In general, p will be composed of the surface potential function of the device that causes a potential energy barrier for electrons in the channel. Even so, where the gate length is not too short in a GaN-FET$_{SiO2}$ device, the electron interaction with the surface potential becomes important and numerically close to the gradual channel approximation (GCA) model. We found for GaN-FET$_{SiO2}$, $\lambda = R/L$ and p can be numerically modeled as [see (A.8) of the Appendix A]:

$$p = -ln(2\lambda\beta q(V_{gs} - V_{th}) - 1), \tag{5}$$

where R and L are the radii and the gate length of GaN NWs, respectively, and $\beta = 1/kT$ with T and k are the absolute temperature and Boltzmann constant, respectively. However, where the I_d–V_{ds} term before saturation follows the parabolic function, then $\lambda \ll 1$ and (1) becomes similar to the GCA model. Thus, GCA is a special case of our model (see Appendix A). Meanwhile, in devices where the short channel is available, such as GaN-FET$_{Al2O3}$, the barrier energy for electrons in the channel will decrease, and numerically p can be assumed constant with respect to the variation of gate-source voltage in the model.

On the other hand, the consequence of (3) also impacts (1), producing a shifted ohmic condition in the I_d–V_{ds} characteristic, causing nonlinear behavior in currents. Equation (1) is, in fact, the current due to channel conductance, which can be confirmed with $(\partial I_{chan}/\partial V_{ds}) = 0$. Meanwhile, in MOSFETs, the current should approach saturation as V_{ds} approaches infinity. Thus, in the present work, the total current with nonlinear behavior has the following formulation

$$I_d = I_{chan} + I_{sat}, \tag{6}$$

where I_{sat} is saturation current. In the cases of GaN-FET$_{SiO2}$ and GaN-FET$_{Al2O3}$, due to the scattering effect, the I_{sat} can be described as follows [see (B.4) of the Appendix B]:

$$I_{sat} = \Gamma I_{max}, \tag{7}$$

where Γ is the fitting parameter for transmission coefficient as the device reaches saturation due to the scattering effect [see (B.4) of the Appendix B]. Therefore, the MOSFET device is quasi-ballistic while $\Gamma < 1$ and ballistic for $\Gamma = 1$. Here, I_{max} is the maximum current that occurs when $(\partial I_d/\partial V_{ds}) = 0$, which gives

$$V_{dsmax} = V_{bi} + \frac{1}{\lambda\beta q}(1 + W(z)). \tag{8}$$

Here, $W(z)$ is the Lambert W function, in which $z = (2\beta q(V_{gs} - V_{th}) - 1)/e$, and e is the Euler constant. V_{dsmax} is V_{ds} at which the current reaches maximum. In general, for the quasi-ballistic case, I_{max} has the following formula after substituting V_{dsmax} into (6):

$$I_{max} = \frac{1}{1 - \Gamma}\frac{G_0}{\lambda\beta q}W(z). \tag{9}$$

The next component of (8) that needs to be determined is the V_{bi} potential. After investigating the data in GaN-FET$_{SiO2}$, V_{bi} for GaN-FET$_{SiO2}$ can be modeled as

$$V_{bi} = \frac{H}{q\beta}W\left(\frac{ze + 1}{2e}\right). \tag{10.1}$$

Here, H is a fitting parameter that represents the donor concentration inside the device. However, in the case of GaN-FET$_{Al2O3}$ where $\lambda \ll 1$, V_{bi} can be approximated to:

$$V_{bi} \approx \frac{\lambda H}{e}(V_{gs} - V_{th}) + V_{bi0}. \tag{10.2}$$

where V_{bi0} is the built-in potential due to the pn junction in GaN-FET$_{Al2O3}$. We need V_{bi0} in (10.2) to determine the true built-in potential for the case of a short gate length.

III. RESULTS AND DISCUSSION

To examine the model, we used the experimental data in Yu *et al*. [9], which used a threshold voltage of 1.2 V. The length and diameter of the transistor were 1.6 μm and 500 nm, respectively, while the device temperature was 300 K. To determine the parameters of Γ, H, and ξ, we first collected I_d–V_{ds} characteristic data, ranging from 2 V to 4.5 V in 0.5 V increments for V_{gs}. We used a nonlinear least-squares Marquardt–Levenberg algorithm [32], [33] to fit G_0, V_{bi}, and I_{sat} parameters with the (6) model for every constant V_{gs}; this process also provided an opportunity for us to obtain I_{max}. Fig. 2 shows the fitting result of the I_d–V_{ds} characteristic of GaN-FET$_{SiO2,}$ in which the calculated currents fit well with the measured ones. These results confirm that the I_d current is determined by G_0, V_{bi}, and I_{sat}, as modeled in (6) and also reveal that the currents are not influenced by electron mobility.

As mentioned previously, the consequences of V_{bi} in (3) will cause Ohm's law to shift from the origin. It is confirmed in Fig. 2 that the drain current does not increase at the low V_{ds} regime. Here, the current is equal to 0 for this regime due to the barrier resulting from V_{bi}. This certainly weakens the model in the regime, as seen in the figure for $V_{gs} =$ 4.5V, where the experimental results show 0.25 mA for drain current when V_{ds} is at 2 V, while this model gives exactly 0 mA. Nevertheless, for other V_{gs} outside the regime, our model gives the best fit with experimental data for V_{ds} of above 2 V. From the values of G_0, V_{bi}, and I_{sat} obtained from this process, the maximum current could be determined easily from the figure based on the condition $\partial I_{chan}/\partial V_{ds} = 0$. We then extracted the I_{sat} and I_{max} information in Fig. 3.

We used (7) to determine Γ, and from Fig. 3, we found $\Gamma =$ 0.934911. Since Γ is less than 1, the carriers experience a scattering mechanism due to defects in GaN-FET$_{SiO2}$ caused by unintentional doping. Therefore, the electrical behavior in the GaN-FET$_{SiO2}$ device can be considered as quasi-ballistic

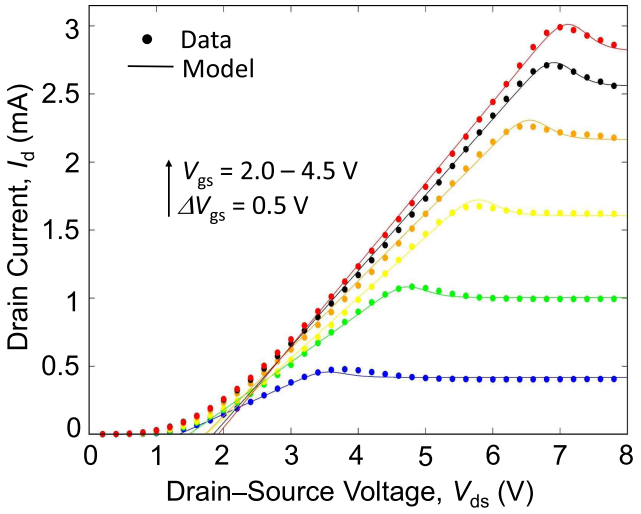

FIGURE 2. The I_d – V_{ds} characteristics of GaN-FET$_{SiO2}$ based on Yu *et al.* [9]. The solid circles represent experimental data, while the solid lines demonstrate the model developed in this study and how it fits with the measured data.

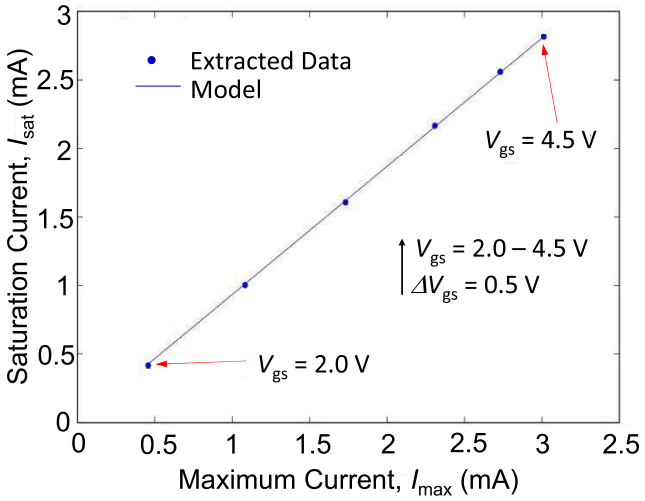

FIGURE 3. The maximum current with respect to saturation current for each V_{gs}. The slope of this plot is $\Gamma = 0.934911$.

drain current [34]. By using when $\Gamma = l_{eff}/(l_{eff}+L)$, in which L is channel length and l_{eff} is the carrier mean free path [see (B.3) of the Appendix B], the mean free path for backscattering for this device is almost 15 times larger than L. This information is in line with our model, where the I_d current is not affected by electron mobility. There have been several ballistic models [35]–[37], including an improved physics-based virtual-source (VS) model, to describe transport in quasi-ballistic drain current [34]. Still, those models require many parameters to fit with the experimental data compared to the present model. Thus, our model can greatly simplify the analysis without sacrificing the accuracy.

Next, from the V_{bi} obtained previously, we used (10.1) to determine the H parameter (see Fig. 4). From the fitting process, we obtained $H = 168.796$. Since (10.1) represents built-in potential, this equation has a similar effect to the potential resulting from the diode junction. Thus, the H

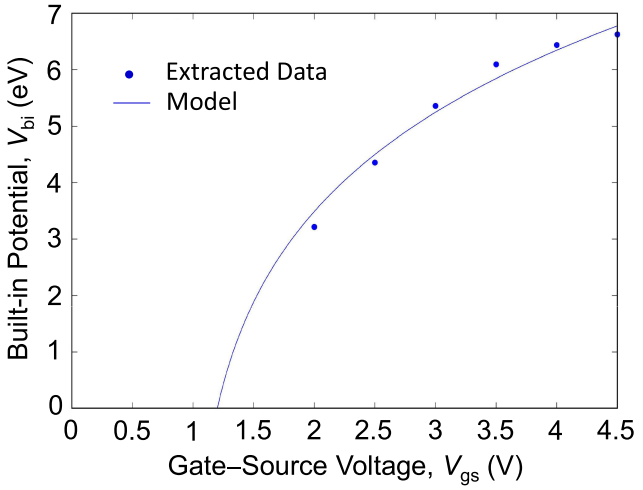

FIGURE 4. The model and extracted experimental data for built-in potential (V_{bi}). The fitting result gives $H = 168.796$.

parameter has the same meaning as $ln\left(N_d N_a/n_i^2\right)$, which is represented in the built-in potential of the diode junction, where N_d and N_a are the total density of donor and acceptor, respectively, and n_i is the intrinsic concentration [21]. However, as noted by Yu *et al.*, much larger current density should be attributed mainly to the high carrier density in the accumulated channel due to unintentional doping, in which case determining $ln\left(N_d N_a/n_i^2\right)$ will not yield the best result [9]. Thus, we prefer to use H as a parameter for V_{bi} rather than $ln\left(N_d N_a/n_i^2\right)$, as presented in (10.1). The high value of H resulting from the fitting process can also be understood as a result of unintentional doping. The difference between the built-in potentials of (10.1) and the diode junction is that the built-in potential of (10.1) is influenced by V_{gs}, based on the results in Fig. 4. One explanation for this relationship is that the gate leakage current causes V_{bi} to be unstable for each V_{gs}. This is confirmed by Yu *et al.*'s statement that their device had an interface trap density of 1.3×10^{11} cm^{-2}eV^{-1} [9]. Although their device had smaller leaks for the SiO_2/GaN interface configuration than other experiments [38], the leakage was still sufficient to let V_{gs} affect V_{bi}. Thus, V_{bi} can yield a different result if the gate oxide interface layer of GaN-FET$_{SiO2}$ is replaced with another material. This is in line with Yu *et al.*'s statement that gate oxide charge trapping could be the source of hysteresis [9]. This statement, however, requires experimental proof for GaN NW transistors covered by another oxide layer material.

We then determined the ξ parameter using the G_0 obtained from Fig. 2 for every V_{gs} and fitting these using (2.1). The results are shown in Fig. 5. From the fitting process, we found $\xi\sqrt{q} = 0.322466\text{mAV}^{-3/2}$. The figure confirmed that the G_0 for the GaN-FET$_{SiO2}$ device is not completely a one-dimensional case due to G_0 not being constant for every V_{gs}. However, the three-dimensional architecture still affects the drain current character, as shown in (2.1). The non-constant G_0 obtained in this model indicates that the gate leakage current generated in GaN-FET$_{SiO2}$ causes

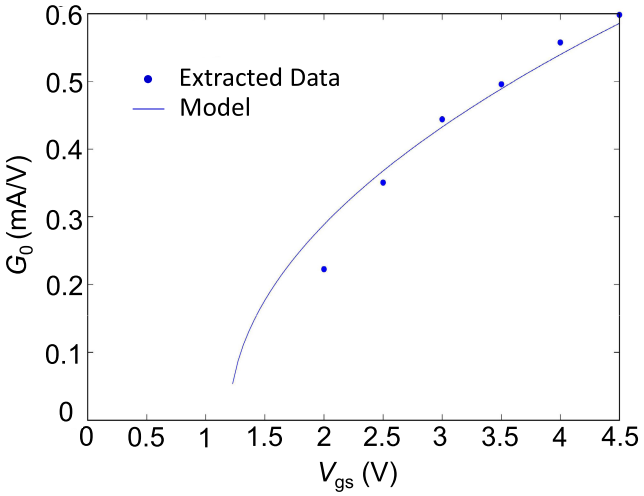

FIGURE 5. The G_0 for every V_{gs} compared to (2.1). The fitting result produces $\zeta\sqrt{q} = 0.322466\ \text{mAV}^{-3/2}$.

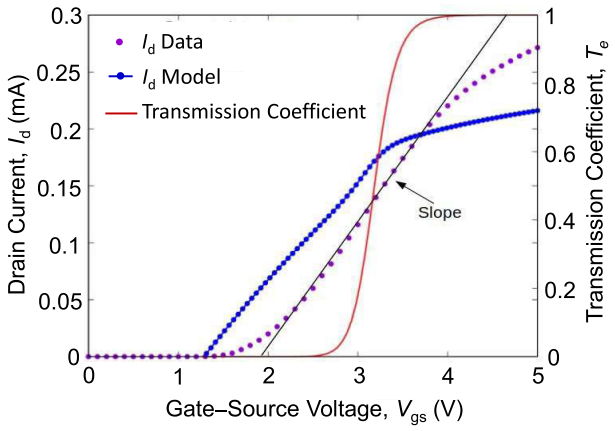

FIGURE 6. The $I_d - V_{gs}$ characteristics with $V_d = 6$ V. The solid circles show the experimental data.

the electrons to no longer flow in a one-dimensional pattern in GaN NWs. Thus, this result confirms our approach for nonlinear behavior current in GaN-FET$_{SiO2}$ as "almost" one-dimensional.

Next, to support our model, we used the Γ, H, and ξ parameters to test the I_d–V_{gs} characteristic with the experimental data for $V_{ds} = 6$V [9]. Fig. 6 shows the result. In general, the I_d–V_{gs} characteristic shown by our model has a similar pattern to experimental data, except for the accuracy level. Fig. 6 reveals the predicted values of I_d increase more rapidly as V_{gs} increases above 1.2 V compared to the experimental data. However, these results are not surprising because (2.1), (5), (9), and (10.1) are highly dependent on V_{th}. Meanwhile, from the Fig. 6, we noticed that V_{th} is around 1.8 V based on the slope of I_d–V_{gs}, which explains why the model shows an earlier increase in current. Moreover, there is also the transmission coefficient dependence of the gate-source voltage. It reveals that when $0.5 < T_e < 1$, gating hysteresis occurs, which was also observed in Yu *et al.*'s experiment [9]. This means that the gating hysteresis is influenced by the transmission coefficient, which is controlled by the gate-source voltage. By analyzing the transmission coefficient, our study offers an easy way to predict the gating hysteresis of the device.

There is yet another physical phenomenon that can happen in the GaN-FET$_{SiO2}$ device. As Yu *et al.* pointed out, the recorded nonlinear currents indicate a carrier charge trap filling mechanism [9]. There have been many discussions related to this mechanism [39]–[42], but we want to point out that if there is a trap-filling mechanism, it will require a time delay for electrons to flow in GaN NWs. Uniquely, a Lambert W function can be derived from the time-delay case, where the solution has an exponential function with respect to time [43]. This means that (8) is also a time-delay case due to the Lambert W function within it. To prove this case, we assumed that the total charge of the trapped electrons at any given time had the function $Q_d(t) \propto \exp\left(\lambda\beta q\left(V_{dsmax} - V_{bi}\right)t/\tau\right)$, where τ is a time delay. By multiplying $Q_d(t)$ with (8), the drain current under V_{gs} control can be written as

$$\frac{\tau}{2\lambda\beta q(V_{gs} - V_{th}) - 1} I_d(t) = Q_d(t) + \frac{1}{2\lambda\beta q(V_{gs} - V_{th}) - 1} Q_d(t - \tau), \quad (11)$$

where $I_d = dQ_d/dt$. From (11), we know that the drain current propagation is not only caused by the $Q_d(t)$ but also comes from the $Q_d(t - \tau)$ delay charge, which causes the I_d current to be severely time-dependent, implying that the I_d current is a case of delayed time. On the other hand, Yu *et al.* revealed that the GaN-FET$_{SiO2}$ device has a memory effect similar to the Blanchard *et al.* experiment [44], in which the I_d current evolves with time as V_{gs} cycles repeatedly. From the Blanchard *et al.* experiment, the I_d current drifts significantly during the first few cycles, then stabilizes during later cycles. Between them, the I_d current decreases exponentially. Thus, the memory effect is caused by a time-delay current. However, further study is required to confirm this result.

Using this model, we also studied the characteristics of the second GaN NW transistor (GaN-FET$_{Al2O3}$) from the work of Fatahilah *et al.* [11]. In comparison to GaN-FET$_{SiO2}$, GaN-FET$_{Al2O3}$ has an added Mg acceptor in the channel, a shorter gate length, and the drain current follows a parabolic function with respect to the drain-source voltage. Therefore, λ is small and p is relatively constant. To determine both values, we use (6) and vary λ to obtain the p-value from the experimental I_d–V_{ds} data given by Fatahillah *et al.* [11]. Thus, we take I_d–V_{ds} data at V_{gs} equal to 7 V as the reference for λ and p for other V_{gs} in order to find I_{sat} in the fitting process. The optimum values for λ and p-value are reached when the difference between saturation current data and I_{sat} for each V_{gs} has the lowest deviation. We obtain $\lambda = 0.0354$ and $e^p = 216.553$ for GaN-FET$_{Al2O3}$, as shown in Fig. 7. If $\lambda < 0.0354$ then the deviation will be larger, meanwhile if $\lambda > 0.0354$ then fitting processes become divergent (not shown in the figure). The fitting results with those values closest to the experiment are depicted in Fig. 8. This figure shows that

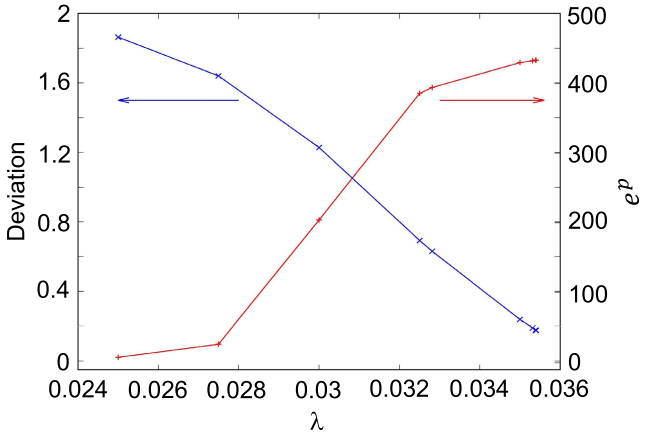

FIGURE 7. Determination of λ for GaN-FET$_{Al2O3}$. From this figure, $\lambda = 0.0354$ is the lower deviation and $e^p = 216.553$.

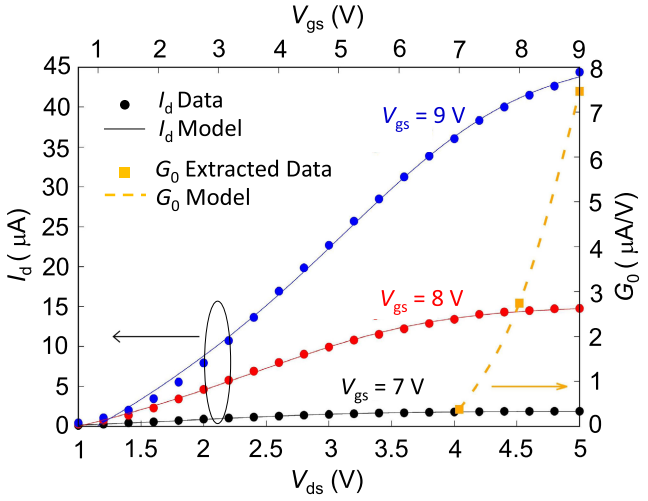

FIGURE 8. Fitting result of I_d and G_0 with $\lambda = 0.0354$ and $e^p = 216.553$ in comparison to experiment by Fatahilah *et al.* [11].

GaN-FET$_{Al2O3}$ has relatively constant p with respect to the variation of V_{gs} while the gate has a short length.

Next, using the same procedure for GaN-FET$_{SiO2}$ to obtain the fitting parameters, we then extract G_0 and V_{bi} for each V_{gs} based on the I_d–V_{ds} data of 9 NWs as shown in Fig. 8. We use (2.2) to acquire $q^2\zeta$ and (10.2) for $(\lambda H/e)$, and the fitting process for V_{bi0} parameters. Those parameters $q^2\zeta$, $(\lambda H/e)$, and V_{bi0} are 1.30697 μAC^{2}V^{-3}, 0.6194, and 6.0527 V, respectively. As shown in Fig. 8, there is no maximum current, which means $\Gamma = 1$ for a ballistic case and the mean free path becomes very large relative to the channel $(l_{eff} \gg L)$ for the GaN-FET$_{Al2O3}$ device based on our model. This is because the GaN-FET$_{Al2O3}$ device has a gate length 0.256 times shorter than GaN-FET$_{SiO2}$, which reduces the potential energy barrier for electrons in the channel and subsequently causes the scattering mechanism [45]–[47]. Therefore, from analyses of these devices, shortening the gate length of MOSFET based on the GaN NW can increase the mean free path so that the transmission coefficient enhances. This result also in lines with Esqueda's work, where the transmission coefficient increases as the channel length decreases,

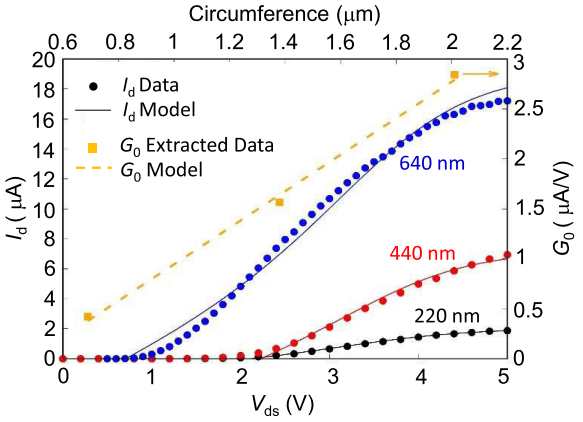

FIGURE 9. Fitting result of I_d and G_0 with respect to the diameter variation of single NW FET experiment data [11].

and the conductance is proportional to the DOS [48], [49]. Shortening the gate length also reduces the distance between the source and drain, meaning that the built-in potential due to the *pn*-junction of GaN-FET$_{Al2O3}$ significantly exists even if $(V_{gs} - V_{th})$ is zero in magnitude at $V_{bi0} = 6.0527$V, which is in contrast to that in GaN-FET$_{SiO2}$. Furthermore, there is an increased effect on V_{bi} due to a relatively small gate-source voltage based on the result of fitting to $(\lambda H/e)$.

In the ballistic case for GaN-FET$_{Al2O3}$ in our model, a scattering mechanism still occurs in the channel during electron propagation. Adding Mg alters the dominant scattering mechanism from electron-electron collision, such as with GaN-FET$_{SiO2}$ (Fig. 5), into electron-phonon, but only to a small extent based on the fitting result of $q^2\zeta$. This can be confirmed from the parabolic trendline in Fig. 8, which is characteristic of a three-dimensional linear dispersion DOS. This scattering mechanism occurs due to the high optical phonon of GaN [50] and the usage of Al_2O_3 as the gate dielectric. The use of this dielectric results in near-zero gate hysteresis, however the interface effect between this dielectric with GaN NW triggers phonon scattering [51].

Furthermore, we discuss the effect of diameter in 1 NW FET for $V_{gs} = 9$V from the work of Fatahilah *et al.* [11]. They found that the maximum current differs in NW and diameter variation, but the normalized current has a relatively constant density. Thus, e^p and λ do not vary with different NW and diameter. In addition, for the same V_{gs}, V_{bi} is relatively constant for those different parameters. The numerical approximation using this assumption and device processing imperfection causes the difference between this model prediction and the experiment. Hence, we take $V_{bi} = 7.53926$V after using the extracted data of $(\lambda H/e)$ and V_{bi0} also (10.2) at $V_{gs} = 9$V. The values of e^p, λ, and V_{bi} are then used to describe the effect of diameter, as shown in Fig. 9. Our model is less accurate for a circumference of 2.01 μm (or diameter of 640 nm) owing to the assumption. Because of the deposition shading and the hexagonal wire shape of NW, the gate metal length varies along the perimeter, as noted by Fatahilah *et al.*, which is another reason for this inaccuracy. Our model reveals that G_0 increases linearly with

the diameter of NW. Therefore, the Ohmic shift is reduced as a consequence.

IV. CONCLUSION

We have investigated nonlinear current–voltage characteristics in vertical-architecture GaN NW transistors by developing the Landauer-Büttiker formula, extending the ideal wire of Landauer-Büttiker's work to be "almost" one-dimensional for GaN NWs. Thus, the DOS played an important role in determining the current between drain and source. The non-overlapped gate structure has the effect of the built-in potential in the drain-channel-source junction, which can be controlled by the gate-source voltage. Our model needs only three parameters (i.e., Γ, H, and ξ) to fit the experimental data in terms of understanding the related physical phenomena. The modelling results revealed that, due to built-in potential dependent on gate-source voltages, the current can exhibit different characteristics for different oxide layer materials. Changing the gate dielectric into Al_2O_3 will trigger the electron-phonon scattering mechanism. Our model suggests that the success of the GaN NW transistor depends on the selected oxide layer material. The maximum current is a result of the transistor being quasi-ballistic drain current, which means that the drain current is not affected by the electron mobility of the GaN material. Meanwhile, reducing the gate length for GaN NWs in transistors will increase the transmission coefficient inside the channel. The memory effect of the device is attributed to a time-delay current. The model is thus very suitable for rapidly analyzing NW transistors prior to their device fabrication.

APPENDIX A: DERIVATION OF T_e

We started from the general definition of the Buttiker–Landauer formula for conductance as follows [26], [52]:

$$G = G_0 \int_{\varepsilon}^{\infty} \left(\frac{-df(E)}{dE} \right) I(E) dE, \tag{A.1}$$

where the last term on the right-hand side (RHS) is a total transmission coefficient, T_e, which is given by

$$T_e = \int_{\varepsilon}^{\infty} \left(\frac{-df(E)}{dE} \right) I(E) dE. \tag{A.2}$$

Meanwhile, $I(E)$ is the transmission coefficient of each electron flowing in a GaN NW. We take the approach that there is a case of perfect transmission for each electron so that $I(E) = 1$. Here, $f(E)$ is the Fermi–Dirac distribution function, which is written as

$$f(E) = \frac{1}{1 + \exp(\lambda\beta E + p)}. \tag{A.3}$$

The appearance of the λ and p parameters in (A.3) is in anticipation of our $I(E) = 1$ approach. By substituting (A.3) into (A.2), the transmission coefficient, T_e, is obtained

$$T_e = \frac{1}{1 + \exp(\lambda\beta\varepsilon + p)}, \tag{A.4}$$

where ε is the Eigen energy. By substituting (A.4) into (1), the formula for I_{chan} can be written as

$$I_{chan} = \frac{G_0}{q} \frac{\Delta\mu}{1 + \exp(\lambda\beta\varepsilon + p)}. \tag{A.5}$$

In the case where there is no shift in Ohm's law ($V_{bi} = 0$) and given the condition of small drain bias, (A.5) must describe the linear region of current for the above-threshold equation of the general model of gradual channel approximation (GCA) as follows [14]:

$$I_{chan} = \frac{\mu_m (2\pi R)}{L} C_{ox} (V_{gs} - V_{th}) V_d - \frac{1}{2} \frac{\mu_m (2\pi R)}{L} C_{ox} V_d^2, \tag{A.6}$$

where μ_m is mobility and C_{ox} is oxide capacitance. To avoid complicated calculations for I_{chan}, the $\varepsilon \approx \Delta\mu$ and $\lambda\beta\Delta\mu \ll 1$ approaches are used in (A.5). Then, using Taylor's expansion for $e^{-x} \approx (1+x)^{-1} \approx 1 - x$, it is found that

$$I_{chan} \approx \frac{G_0}{1 + e^p} V_d - \frac{1}{2} \frac{G_0 q \lambda\beta e^p}{2(1 + e^p)^2} V_d^2 \tag{A.7}$$

By using simple mathematical operations (A.6) and (A.7), it is obtained that

$$p = ln(2\lambda\beta q(V_{gs} - V_{th}) - 1) \tag{A.8}$$

Finally, by applying $\varepsilon \approx \Delta\mu$ to (A.4), the transmission coefficient is written as

$$T_e = \frac{1}{1 + exp(\lambda\beta\Delta\mu + p)} \tag{A.9}$$

APPENDIX B: DERIVATION OF Γ

The assumption $I(E) = 1$ is only true for the numerical approach, where the flow of each electron is assumed to be ballistic in a GaN NW. Although we use λ and p parameters to compensate, $I(E) = 1$ does not hold completely true under physical observation, where a small number of electrons still experience a backscattering event. Thus, we add backscatter compensates to the high drain bias (saturation) regime with the simple formula [53]–[55]:

$$I_{sat} = B_R I_{BL}, \tag{B.1}$$

where $B_R = (1 - r) / (1 + r)$ is the ballistic ratio, r is the backscattering coefficient, and I_{BL} represents the ballistic current. The model for ballistic current is usually comprised of oxide capacitance, thermal velocity, inversion charge, and injection velocity. However, due to the $I(E) = 1$ approach used in this study, the I_{BL} is the maximum current I_{max} in the saturation regime, $I_{BL} = I_{max}$. As emphasized by Lundstrom, the critical distance l and the mean-free-path l_{eff} determine the backscattering coefficient [55]. The critical distance is defined as the region where the backscattering event happens. In the case of GaN NW, according to Lundstrom, this event occurs throughout the entire channel, thus we set $l = L$ and the backscattering coefficient has the following form:

$$r = L / (l_{eff} + L). \tag{B.2}$$

Meanwhile, the transmission coefficient has the following formula [34], [56]:

$$\Gamma = l_{eff} \big/ \left(l_{eff} + L\right). \tag{B.3}$$

By using (B.2) and (B.3), the ballistic ratio can be written as $B_R = \Gamma \big/ (2 - \Gamma)$. In this case only a small number of electrons suffer backscattering so that $r \ll \Gamma$, however the ballistic ratio can be approached with transmission coefficient $B_R \approx \Gamma$ [46]. Thus, we can rewrite (B.1) for this model as follows:

$$I_{sat} = \Gamma I_{max}. \tag{B.4}$$

The mean free path reduction due to scattering mechanism can be determined using the Γ parameter from the fitting process.

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