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Systematic Design Methodology of Broadband Doherty Amplifier Using Unified Matching/Combining Networks With an Application to GaN MMIC Design

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ABSTRACT This paper presents a new design methodology for broadband Doherty architecture using the three-port input and output networks technique. The proposed topology was developed to overcome the Doherty power amplifier (DPA) bandwidth limitations. The output three-port network performs the impedance matching from any load impedance to the optimum loads for both main and peaking transistors and also combines the power delivered from the two devices at any power ratio. On the other hand, the input-splitting network is proposed for matching the input impedances of the two transistors to the source impedance. The freedom in choosing the power division ratio of the input network enables us to achieve a tradeoff between efficiency and linearity. Also, it provides a way to accomplish the phase compensation using an arbitrary phase difference between the two branches of the Doherty power amplifier and thus, helps obviate the need of the highly bandwidth limiting offset lines found in the Doherty design. A two-stage broadband Doherty power amplifier is implemented using 0.25-um GaN HEMT MMIC process to validate the proposed topology. The fabricated DPA was measured under both continuous wave (CW) and modulated signal at different operating frequencies. Across 3.3–3.7 GHz, the implemented DPA delivers a maximum output power exceeding 42 dBm, power added efficiency (PAE) over 52 % at the peak power and over 38 % in the back-off state over the operating 400 MHz bandwidth. The fully integrated circuit has a chip-size of 4.4 mm × 3.5 mm.

INDEX TERMS Three-Port network, Doherty, Gallium Nitride, multiple-input multiple-output (MIMO), microwave monolithic integrated circuit (MMIC), peak-to-average power ratio (PAPR).

I. INTRODUCTION

Recently, the evolution of the wireless communication systems from the fourth generation (4G) to the fifth generation (5G) networks has accelerated significantly; opening the door to many opportunities for scientific research. The 5G networks are destined to become a core of the future commercial communication and infrastructure applications. In 5G wireless networks, the massive multiple-input multiple-output (MIMO) systems play a significant role because they achieve higher data rates than the single-input, single-output (SISO) systems. This improvement in data rate will require more complex modulation schemes and also larger instantaneous signal bandwidths (more than 200 MHz) [1]. These

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challenges will drive demand for small, efficient, and cost-effective power amplifiers (PAs) that can be integrated with 64- or even 128-way MIMO active antennas. One such solution is to use integrated technologies such as the complementary metal oxide semiconductor (CMOS) and monolithic microwave integrated circuit (MMIC) which offer high reliability, excellent repeatability, high yield, as well as low cost. Also, the complexity of the modulation schemes used in 5G networks will require efficient power amplifiers and must remain highly efficient at output power back-off (OPBO) [2].

Several strategies can achieve efficiency enhancement at the output power back-off region, such as bias modulation, out-phasing technique [3], and envelope tracking [4]. Among these topologies, Doherty power amplifier (DPA) is one of the most well established methods used in commercial base stations for its ability to achieve high peak-to-average power ratio (PAPR) [5]–[12]. In Doherty PA, there is an interaction that results in a load modulations between two devices: the main and peaking devices. These devices are allowed to interact via impedance modulation, while the impedances presented to both devices are varied dynamically as a function of the envelope magnitude. The main device is biased to operate in Class-B or AB, while the peak device is biased deeper in Class-C. The main device conducts at a low power level up to a preselected average power level, while the peak device conducts when the power surpasses the preselected power level which often fixed at 6-dB OPBO. The impedance modulation in DPA is enacted using $\lambda/4$ transformers as in [9]–[12].

Many different techniques were studied previously to improve the performance of the DPA by broadening the operating bandwidth and extending the efficiency range. In [10], [13], the efficiency performance was improved over a wide power range by using a digitally controlled input power scheme which minimizes the power waste into the peaking branch at the back-off power levels. The bandwidth limitation was mitigated in the Doherty region by using different optimized characteristic impedances for $\lambda/4$ transformers at the output combiners as in [14]–[17]. In [18] and [19] a modified power combining network with an L-C tank and compensating reactance C-R was used respectively to maintain the back-off impedance seen by the main transistor over a frequency band to obtain a higher bandwidth, while [20] reported an optimal complex load range instead of multiple R_{opt} to extend the efficiency range. The frequency response of the output-combining network of the Doherty amplifier with arbitrary back-off level configuration was reported in [21]–[23]. Furthermore, post-matching networks were employed in [24]–[28] to achieve improved bandwidth and efficiency. In [29], an GaN MMIC Doherty PA was designed using a reversed uneven power splitting network to improve the linearity performance, and it included two-section $\lambda/4$ transformer to get uniform frequency response, while in [30], a modified impedance inverter network was used to increase the bandwidth. Since the main obstacles in obtaining a DPA with wideband performance is the use of output impedance inverters and offset lines, a transformer-less load-modulation network was reported in [31], which resulted in wideband DPA. A single RF-input modified MMIC Doherty amplifier with reconfigurable efficiency was proposed in [32] showing the effect of the input network and the bias voltages on the amplifier frequency response. In [33], [34], the Doherty amplifier was designed with a second harmonic control circuit at the main branch to get high efficiency and a modified input phase compensation network for broadband operation.

In the literature, the majority of the studies rely on discrete GaN devices to design high power Doherty PAs and only a few of them use MMIC technology. Despite the abundance of challenges and difficulties in designing a high power MMIC Doherty amplifier, it deserves a great deal of research attention as it can help fulfill the requirement of small-cell base stations. Furthermore, it can be used as a building block for an active MIMO transmitter. An alternative Doherty design topology was reported in [35] which examined the performance of the three-port matching and combining networks. In [35] the three-port networks were realized based on discrete components at a single frequency. Inspired by [35], an adopted analysis and a stream out design methodology of the three-port input and output networks were developed and adopted throughout this paper to enhance the bandwidth of the Doherty amplifier design and reduce its size to make it appropriate for MMIC implementation. Also, for the first time, the implementation of the three-port matching and combining networks topology was realized based on MMIC technology to fulfill the integration requirements.

In this paper, we present a compact GaN MMIC two-stage DPA design based on a new and comprehensive design methodology suitable for MMIC design. This methodology was employed to optimize the DPA behavior not only for performance such efficiency, back-off range and frequency bandwidths but also to optimize MMIC design constraints such as circuit's sizes, the process variability and limitations. The three-port technique has been used to synthesize the DPA matching and splitting input/output networks. A detailed procedure of the broadband Doherty design is given in the paper. Consideration is given to the degree of freedom for implementation of the networks, which provides high flexibility to the design of input/output networks with minimal sensitivity to the process variation, and broadband frequency response. Also, we sought a compact size that would be suitable for integration with MIMO active antennas. This paper is organized as follows: Section II presents the DPA design methodology. Section III provides the amplifier architecture and the three-port networks design and synthesis concepts. A brief description of the technology platform and the details of the prototype implementation of the MMIC DPA is mentioned in Section IV. Afterward, in Section V the measurement setup and the experimental results will be discussed and analyzed compared to state-of-the-art results. Finally, Section VI elaborates upon the conclusion.

II. GENERIC DESIGN METHODOLOGY

In the conventional DPA shown in Fig.1, the matching networks of the main and auxiliary amplifiers are usually designed separately from the input-splitting and output-combining networks.

To start the design, the designer needs to: fix the ratio $\alpha = Z_{PK}/Z_{BO}$ which is equal to 0.5 in most cases as shown in Fig.1, with the impedance seen by the main amplifier at peak power, $Z_{PK} = 50\Omega$ and the impedance seen by the main amplifier at 6-dB back-off power level, $Z_{BO} = 100\Omega$. The characteristic impedance of $\lambda/4$ transformer equals $Z_{\lambda/4} = \alpha Z_{PK}$. Also, the designer needs to fix the value of the power dividing factor of the input-splitting network, which commonly equals 3 dB. To equalize the phase between the main and auxiliary branch of the Doherty amplifier, a 90-degree delay line cascaded to an in-phase splitter or else a quadrature hybrid is used as in Fig.1. The second $\lambda/4$ transformer has no impact on the load-modulation, and it is inserted between the combining junction and the output of the Doherty amplifier to be used only for impedance matching purpose to transform $Z_{Pk}/2$ to Z_{PK}.

In contrast with the above approach, the proposed design methodology unifies and merges the concurrent design of the input matching networks of main and auxiliary amplifiers with the input-splitting network. Also, The output matching networks of the main and auxiliary amplifiers are merged with the output-combining network without using an additional impedance transformer for impedance matching at the output network. Furthermore, by selecting the two appropriate transistors for the main and auxiliary amplifiers and knowing through simulations or source-pull/load-pull characterization their respective complex gain, optimum source and load matching impedances and their respective peak power capabilities when they are entirely driven. One can define: First, the voltage ratio α of the output matching-combining network needed to equalize the magnitude and phase of the two signals outputted by the two amplifiers at the combining junction. Second, the complex voltage splitting ratio γ of the input matching-combining network is needed to properly drive both main and auxiliary amplifiers to equalize the gain's magnitude and phase in both branches of the Doherty amplifier.

The optimum source and load matching impedances for both amplifiers and the output impedance of the auxiliary amplifier have to be known through simulations or source-pull/load-pull characterization at an arbitrary back-off power level, (not necessarily 6 dB) where only the main amplifier is active and the auxiliary amplifier biased in Class-C is in the turn-off mode. The values of α, γ and the source and load optimum impedances for the main and auxiliary amplifiers at the back-off level and the full drive level will be sufficient to determine the S-parameters of the input and output three-port networks needed to design the Doherty amplifier as shown in Fig.2. This approach is generic and can be used for the symmetrical or non-systematical design of Doherty amplifier design. Furthermore, the approach can be applied

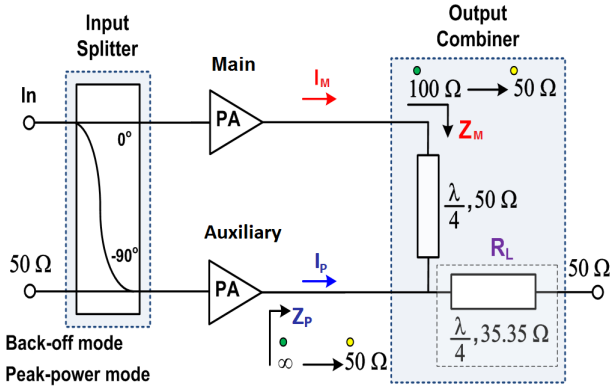

FIGURE 1. Conventional Doherty amplifier architecture.

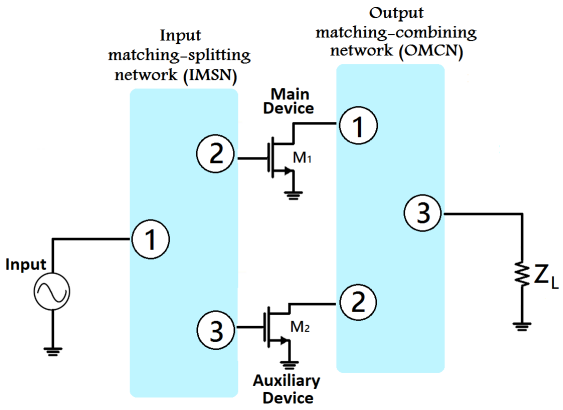

FIGURE 2. The Doherty amplifier topology.

over a broader frequency band since no transformer or offset lines are required. It is also anticipated that it will lead to a smaller form-factor and substantial gain in the surface area and cost when MMIC technology is selected for fabrication.

III. DOHERTY PA TOPOLOGY

The block diagram structure of the proposed MMIC Doherty amplifier is shown in Fig. 3. The amplifier configuration is composed of two-stage. The first one is the driver stage, which consists of a single transistor biased at Class-AB. For the second power stage, it is like the Doherty amplifier operation, as the main transistor operates at the Class-AB biasing conditions while the auxiliary transistor is biased at Class-C. The two transistors can deliver different output powers to achieve the desired back-off performance. The first step to design three-port Doherty PA is to obtain the parameters of the output matching-combining network (OMCN). The function of the OMCN is to combine the output powers from both main and auxiliary transistors and to match the impedances of the two devices at peak power and back-off power to the required loaded impedances by the load modulation scheme taking place in the Doherty amplifier. The input matching-splitting network (IMSN) affects the Doherty back-off performance based on the splitting ratio selected and serves to

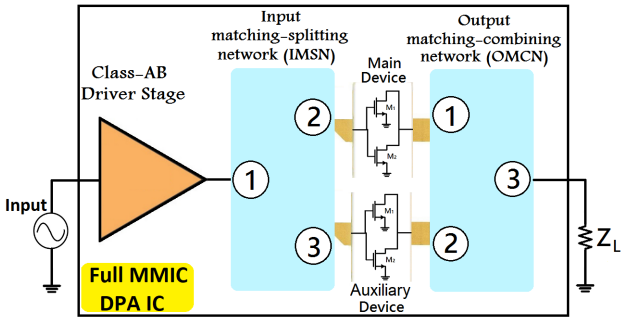

FIGURE 3. Proposed two-stage GaN MMIC Doherty power amplifier with input/output networks.

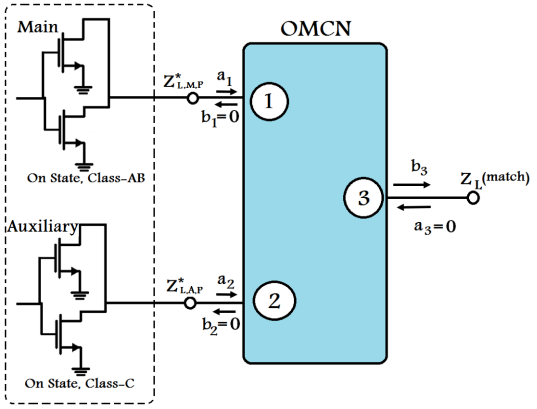

FIGURE 4. Output matching-combining network with three-port reference impedances (@ peak power).

equalize the phase and gain between the two branches of the Doherty amplifier in addition to the input matching of the transistors. Inspired by the design criteria reported in [35], generalized design procedure was developed below in order to realize a broadband performance for the Doherty amplifier design.

A. OUTPUT MATCHING-COMBINING NETWORK (OMCN)

The first step in designing a three-port Doherty PA is to get the parameters of the OMCN. This nonsymmetrical OMCN is employed as a non-isolated power combiner network that combines the output powers from both main and auxiliary transistors. Moreover, it is used to match the reference load impedance to the optimum impedance of the two transistors at output peak power, and also keep the optimal response at output power back-off (OPBO). The reference impedances are defined as shown in Fig. 4. The complex conjugate of the optimum impedance at the maximum output power of the main transistor $Z^*_{L,M,P}$ is the impedance for Port 1, while the complex conjugate of the optimum impedance at the maximum output power of the auxiliary transistor $Z^*_{L,A,P}$ is the reference impedance for Port 2. The reference impedance for Port 3 is $Z_L = 50\ \Omega$. The output-combining network assumed to be a lossless and reciprocal network and, combines the output powers from the two transistors with an arbitrary ratio. We define the output power ratio (α) between the powers of the auxiliary and the main amplifiers as a function of the frequency by:

$$\alpha(f) = \frac{S_{32}a_2(f)}{S_{31}a_1(f)} \tag{1}$$

where S_{ij} are the S-parameters of the three-port network in 50 Ω characteristic impedance. In case of indicating the phase of the S_{ij}-parameters to be (θ_{ij}), then based on [35], the general S-parameters matrix can be written as in (2), shown at the bottom of the page.

From the S-matrix, the three phases difference of the three-port network $\theta_{21}(f), \theta_{31}(f), \theta_{32}(f)$ are used mainly to optimize the performance of the DPA in term of efficiency over the frequency bandwidth. The choice $\theta_{21}(f)$ will impact the impedance seen by the main transistor at the back-off state and hence the efficiency in the back-off region. As well, the choice of $\theta_{31}(f)$ and $\theta_{32}(f)$ will impact the phase balance between the two branches and hence the efficiency at peak power. This will depend mainly on the output reflection coefficient of the auxiliary transistor and $\theta_{21}(f)$. Fig. 5 shows the OMCN configuration at the back-off state. At output power back-off, Port 3 is connected to its reference impedance 50 Ω, so the load reflection coefficient seen by the main transistor was calculated based on [35], [36], as shown in (3) at the bottom of the page.

$\Gamma_{t,A,BO}(f)$ is the output reflection of the auxiliary transistor in the back-off state at different frequencies. At back-off the auxiliary transistor is turned off, and the value of $\Gamma_{t,A,BO}(f)$ is calculated with the reference impedance of Port 2 ($Z^*_{L,A,P}$) as:

$$\Gamma_{t,A,BO}(f) = \frac{Z_{t,A,BO}(f) - Z^*_{L,A,P}(f)}{Z_{t,A,BO}(f) + Z_{L,A,P}(f)} \tag{4}$$

The steps to find the optimum $\Gamma_{L,M,BO}(f)$ at the desired back-off output power are as follows:

1- Perform load-pull simulation for the main device at the desired output power back-off level.

2- Obtain the dc power combustion and the delivered output power in the $\Gamma_{L,M,BO}(f)$ plane with $Z^*_{L,M,P}$ as the reference impedance.

3- Estimate the values of efficiency at the back-off level from the delivered power to the load and the dc power combustion.

4- Then plotting the efficiency contours to get the optimum load impedance for the main transistor at the back-off region.

The phase difference between Port 1 and Port 2 of the OMCN $\theta_{21}(f)$ is a function of the phase of $\Gamma_{L,M,BO}(f)$ and $\Gamma_{t,A,BO}(f)$ which should be known in advance from load-pull simulation or characterization. The value of $\alpha(f)$ models the peak power ratio between the auxiliary and the main transistors, and it is known as well once the transistors are selected and characterized. The selection of the value of $\theta_{21}(f)$ can be used to tune the actual impedance presented by the auxiliary branch to the main transistor to make it as close as possible to an open circuit. Furthermore, this phase controls the level

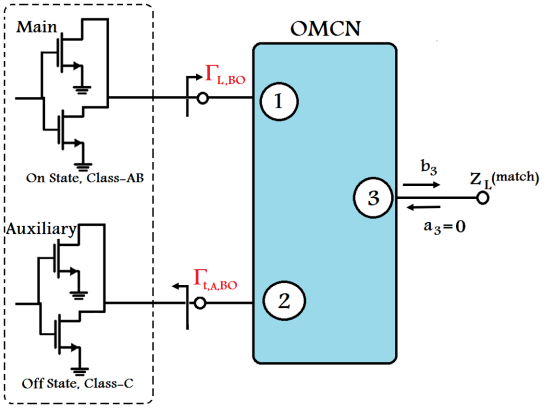

FIGURE 5. Three-port output matching-combining network (@ back-off).

of leakage of the signal from the main branch to the auxiliary branch at back-off mode, and hence it can be used to optimize the efficiency of the DPA in the back-off region.

The phase difference value $\theta_{31}(f) - \theta_{32}(f)$ is a function of the phases of $\Gamma_{L,M,BO}(f)$, $\Gamma_{t,A,BO}(f)$ and the value of $\alpha(f)$ which should be known in advance from simulation or characterization. The proper selection of $\theta_{31}(f) - \theta_{32}(f)$ will ensure that the signal from the auxiliary transistor and the signal from the main transistor, which are not necessarily identical, will be in-phase and hence maximize the efficiency at peak power. Based on the optimum $\Gamma_{L,M,BO}(f)$, $\Gamma_{t,A,BO}(f)$ and the value of $\alpha(f)$, we selected the appropriate values for $\theta_{21}(f)$ and $\theta_{31}(f) - \theta_{32}(f)$. Since only $\theta_{31}(f) - \theta_{32}(f)$ is relevant for the design approach, one can select an arbitrary but an adequate value for $\theta_{31}(f)$ taking into account the process constraints and then select $\theta_{32}(f)$. Consequently, the degree of freedom in selecting the value of $\theta_{31}(f)$ will lead to a realizable OMCN with much lower sensitivity and wideband characteristics.

B. INPUT MATCHING-SPLITTING NETWORK (IMSN)

The three-port input matching-splitting network (IMSN) proposed here is a non-isolated, nonsymmetrical power splitter. It also matches the source impedance to the input impedance of the two transistors. The IMSN provides any arbitrary phase difference between the two transistors which means there is no need to offset lines in the Doherty amplifier design. A set of reference impedances was selected for the input three-port network as shown in Fig. 6 and using these reference impedances, we can obtain the S-parameters for the IMSN. The IMSN parameters are chosen based on the analysis of the main and auxiliary transistors input impedances to get an optimized broadband performance of the Doherty amplifier. The input-splitting network is assumed to be a lossless and a reciprocal network and, it splits the input powers into the two branches with an arbitrary complex ratio. At peak input power the input signal to the main transistor is different in amplitude and phase from the one applied to the input of the auxiliary transistor. At this power level, the main and auxiliary transistor's large-signal input impedances are equal to the impedances $Z_{in,M,P}(f)$ and $Z_{in,A,P}(f)$ at Ports 2 and 3 respectively. This means that the loads at Ports 2 and 3 have no reflection ($a_2 = a_3 = 0$) then according the network lossless condition; one can deduce that the IMSN S-parameters matrix can be driven as in [35], (5) shown at the bottom of the next page.

From (5), the phase parameters $\theta^*_{21}(f)$ and $\theta^*_{33}(f)$ can be used to adjust the performance of the IMSN at power back-off. The input impedances of the transistors are dependent on the input power. These impedances can be used to adjust the amplifier's performance at power back-off. Theorizing that the large-signal input impedances at peak power and power back-off are $Z_{in,M,P}(f)$ and $Z_{in,M,BO}(f)$, respectively. For the auxiliary transistor, the large-signal input impedances are $Z_{in,A,P}(f)$ and $Z_{in,A,BO}(f)$ at peak power and back-off state, respectively.

At peak power, the proposed IMSN function is to divide the power with an appropriate ratio to both branches of the Doherty such that both the auxiliary and main amplifiers will deliver the same in-phase current at the combining junction of the OMCN. At back-off mode, we will obtain the input reflection coefficient of the main transistor $\Gamma_{in,M,BO}(f)$ and, the input reflection coefficient of the auxiliary transistor $\Gamma_{in,M,BO}(f)$. These input reflection coefficients $\Gamma_{in,M,BO}(f)$ and $\Gamma_{in,A,BO}(f)$ are obtained either from load-pull /source-pull simulation or characterization of the main and the auxiliary transistors are:

$$\Gamma_{in,M,BO}(f) = \frac{a_2(f)}{b_2(f)} = \frac{Z_{in,M,BO}(f) - Z_{in,M,P}(f)}{Z_{in,M,BO}(f) + Z^*_{in,M,P}(f)} \quad (6)$$

$$\Gamma_{in,A,BO}(f) = \frac{a_3(f)}{b_3(f)} = \frac{Z_{in,A,BO}(f) - Z_{in,A,P}(f)}{Z_{in,A,BO}(f) + Z^*_{in,A,P}(f)} \quad (7)$$

$$S = \begin{bmatrix} -\dfrac{\alpha(f)e^{j(\theta_{21}(f)+\theta_{31}(f)-\theta_{32}(f))}}{1+\alpha(f)} & \dfrac{\sqrt{\alpha(f)}}{1+\alpha(f)}e^{j\theta_{21}(f)} & \dfrac{e^{j\theta_{31}(f)}}{\sqrt{1+\alpha(f)}} \\ \dfrac{\sqrt{\alpha(f)}}{1+\alpha(f)}e^{j\theta_{21}(f)} & -\dfrac{e^{j(\theta_{21}(f)-\theta_{31}(f)+\theta_{32}(f))}}{1+\alpha(f)} & \sqrt{\dfrac{\alpha(f)}{1+\alpha(f)}}e^{j\theta_{32}(f)} \\ \dfrac{e^{j\theta_{31}(f)}}{\sqrt{1+\alpha(f)}} & \sqrt{\dfrac{\alpha(f)}{1+\alpha(f)}}e^{j\theta_{32}(f)} & 0 \end{bmatrix} \quad (2)$$

$$\Gamma_{L,M,BO}(f) = -\frac{\alpha(f)e^{j(\theta_{21}(f)+\theta_{31}(f)-\theta_{32}(f))}}{1+\alpha(f)+|\Gamma_{t,A,BO}(f)|e^{j(\theta_{t,A,BO}(f)+\theta_{21}(f)+\theta_{32}(f)-\theta_{31}(f))}} \quad (3)$$

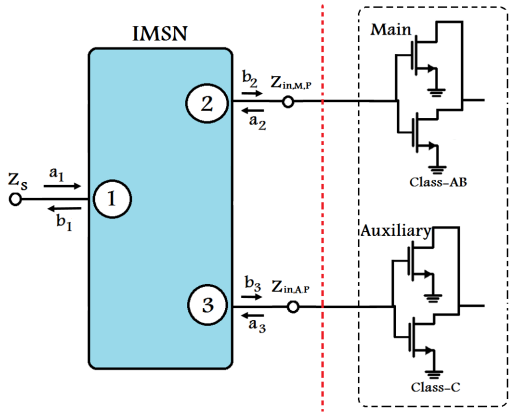

FIGURE 6. Input matching-splitting network with three-port reference impedances.

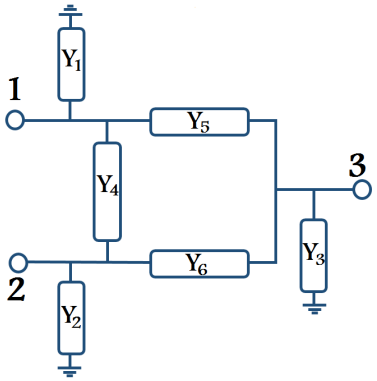

FIGURE 7. Three-port realization network based on circuit elements.

The ratio of powers delivered to the two transistors at power back-off state can be derived as:

$$|\frac{b_2(f)}{b_3(f)}|^2_{back-off} = \frac{1}{\gamma^2(f)}|\frac{1-\Gamma_{in,A,BO}(f)e^{j\theta^*_{33}(f)}}{e^{j\theta_0(f)}-\Gamma_{in,M,BO}(f)e^{j(\theta^*_{33}(f)-\theta_0(f))}}|^2 \tag{8}$$

where $\theta_0(f)$ is the phase difference between the main and the auxiliary input signals, and $\gamma(f)$ indicate the ratio between the power feeding the auxiliary and main amplifiers at peak power.

From (8), one can conclude that the value of the phase difference between the main and auxiliary input signals $\theta_0(f)$ is used to balance the over-all phases between the auxiliary and main branches of the DPA at peak power. Also, the power dividing ratio at back-off state is a function of $\theta^*_{33}(f)$, $\Gamma_{in,M,BO}(f)$ and $\Gamma_{in,A,BO}(f)$. Since all the parameters are preferably fixed or known from characterization or simulation expect the value of $\theta^*_{33}(f)$, this can later be used to set the splitting power factor of the IMCN at power back-off. The selection of $\theta^*_{33}(f)$ will impact the broadband performance and the Doherty amplifier behavior at the back-off state. Afterward, using the values of $\theta_0(f)$ and $\theta^*_{33}(f)$, we can obtain the S-matrix parameters. In (5), the non-constrained variable $\theta^*_{21}(f)$ can be selected such that the IMCN design satisfies the constraints of the MMIC fabrication process, the frequency response and yield performance.

C. THE REALIZATION OF THE THREE-PORT NETWORK

The parameters of the three-port networks that were driven based on the analysis in Sections III-A and III-B for the OMCN and the IMSN can be realized using six-element circuit structure reported in [35]. It is a simple implementation for these parameters using circuit elements. This structure is suitable for MMIC design to get a compact layout for the final amplifier. The three-port network is shown in Fig. 7. This network may be adopted and developed to be with more elements to get a broader frequency response but will affect the circuit size and the insertion loss.

Based on the obtained networks, we can select the most reliable network considering the foundry process limitations, yield requirements, and broadband performance. The new generalized design methodology is described in details by the flowchart reported in Table 1 and is based on the theory presented in Section III.

IV. MMIC BROADBAND DOHERTY PA USING THREE-PORT MATCHING AND COMBINING NETWORKS

The GaN MMIC DPA was designed using WIN-Semiconductors Foundry GaN HEMT process. This technology is based on a 250 nm gate length process on GaN/SiC substrates. In this paper, the Doherty amplifier was designed based on two power bars, which consisted of two GaN HEMT cells to achieve a high power density and enhance the power performance compared to the single device. This improvement is due to the higher output resistance (R_{ds}) and lower gate-to-drain capacitance (C_{gd}). As well, using the power bar can enhance the performance of the breakdown voltage because of sharing the original electric field. Moreover, as per the load-pull power simulation, the RF maximum output power increases from 12 Watts to 16.8 Watts at 3.5 GHz operating frequency for eight-finger

$$S = \begin{bmatrix} 0 & \frac{1}{\sqrt{1+\gamma^2(f)}}e^{j\theta^*_{21}(f)} & \frac{\gamma(f)}{\sqrt{1+\gamma^2(f)}}e^{j(\theta^*_{21}(f)+\theta_0(f))} \\ \frac{1}{\sqrt{1+\gamma^2(f)}}e^{j\theta^*_{21}(f)} & \frac{\gamma^2(f)}{1+\gamma^2(f)}e^{j(\theta^*_{33}(f)-2\theta_0(f))} & \frac{-\gamma(f)}{1+\gamma^2(f)}e^{j(\theta^*_{33}(f)-\theta_0(f))} \\ \frac{\gamma(f)}{\sqrt{1+\gamma^2(f)}}e^{j(\theta^*_{21}(f)+\theta_0(f))} & \frac{-\gamma(f)}{1+\gamma^2(f)}e^{j(\theta^*_{33}(f)-\theta_0(f))} & \frac{1}{1+\gamma^2(f)}e^{j\theta^*_{33}(f)} \end{bmatrix} \tag{5}$$

TABLE 1. Design flowchart of the generalized Doherty amplifier.

1- Specification of the Doherty Amplifier in terms of peak power, gain, efficiency, turn-on level of auxiliary amplifier, frequency bandwidth.
2- Selection of the transistors for the main and auxiliary amplifiers.
3- Load-pull/source pull characterization @ peak power at several frequency points within the bandwidth.
4- Knowledge of $Z_{L,M,P}$, $Z_{in,M,P}$, $Z_{L,A,P}$, $Z_{in,A,P}$,$P_{out,A,Peak}$, $P_{out,M,Peak}$, $G_{M,Peak}$ and $G_{A,Peak}$ for conjugate input matches over the frequency bandwidth.
5- Determine $\alpha(f) = \frac{P_{out,A,Peak}}{P_{out,M,Peak}}$.
6– Determine the ratio of complex gains for the main and peaking amplifiers $\gamma(f) = \frac{G_{M,Peak}}{G_{A,Peak}}$.
7- Load-pull/source-pull characterization @ Back-off power over the frequency bandwidth.
8- Knowledge of $Z_{in,M,BO}$, $Z_{in,A,BO}$, $Z_{L,M,BO}$ and $Z_{t,A,BO}$
9- Convert the three-port S-parameters to the Y-parameters matrix .
10- From the four sets of Y-parameters for the output matching-combining network, select the appropriate values that suit wideband design.
11- In the range of Y-parameters, which meet the foundry process limits, perform yield analysis taking into account the process variation.
12- Converting three-port networks Y-parameters to circuits elements (L, C and transmission lines (TL)).
13- Synthesize the two three-port networks and assess the Doherty amplifier performance.

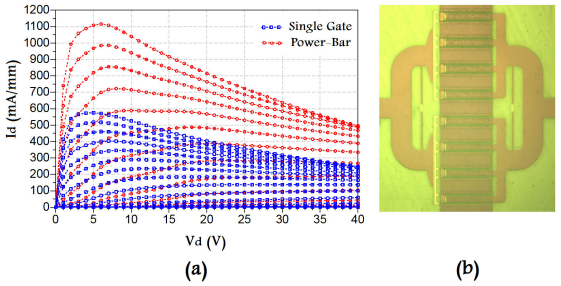

FIGURE 8. (a) Typical DC–IV of GaN single-gate and power bar devices, (b) Layout of the power bar.

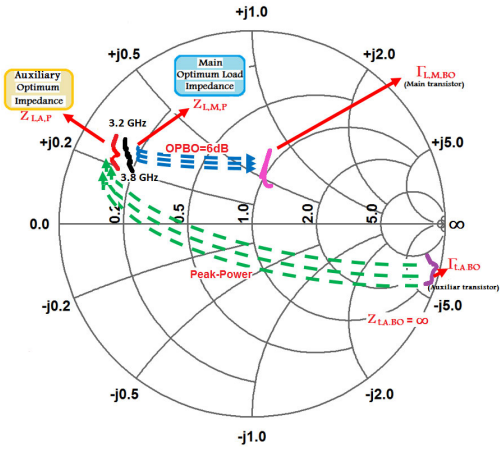

FIGURE 9. Load impedances seen by the main and auxiliary transistors at peak power and back-off states, and the load-modulation effects.

devices with 250 um gate width. Fig.8(a) shows DC–IV data for both single-gate (8-fingers and 250 um width) and power bars with 16-fingers and 250 um gate width. The gate bias range is from −4 to −1.5 V with 0.25 V step for both single-gate and the power bar. A microscopic image of the power bar HEMT device with 16-fingers is shown in Fig.8(b).

The Doherty power amplifier is designed based on the proposed amplifier topology to validate the analysis shown in Section III. The power bar device was used for both the main and auxiliary branches. The design center frequency is 3.5 GHz. The design procedure was repeated for different frequencies targeting a frequency band of 400 MHz bandwidth (3.3 – 3.7 GHz) to achieve the best input and output circuits parameters. The dc bias of the main transistor is set to a quiescent current of 300 mA and a drain voltage of 30 V (Class-AB operation), while the Class-C auxiliary transistor is biased at the drain voltage of 30 V and the gate voltage of −5.3 V.

A parallel R-C network is added to the input of the transistors to stabilize the amplifier and prevent any oscillations, then the optimum load impedance for each transistor was obtained using load-pull simulations. Fig. 9 shows that at the center operating frequency 3.5 GHz, the optimum load impedance at the maximum output power was $Z_{L,M,P} = 8.25 + \text{j}\ 12.6\ \Omega$ and $Z_{L,A,P} = 6.5 + \text{j}\ 12\ \Omega$ for the main and auxiliary transistors, respectively. The maximum output power was 41.7 dBm from the main device while, it was 40.85 dBm from the auxiliary transistor, and this means that $\alpha = 0.82$. At back-off the auxiliary transistor's small–signal output impedance was $Z_{t,A,BO} = 0.58 - \text{j}\ 22.26\ \Omega$. At 3.4 GHz, the main transistor optimum load impedance was $Z_{L,M,P} = 7.8 + \text{j}\ 12.9\ \Omega$ and for the auxiliary transistor $Z_{L,A,P} = 5.5 + \text{j}\ 12.5\ \Omega$ at maximum output power. The maximum output power was 41.8 dBm from the main device while, it was 41 dBm from the auxiliary transistor, and this means that $\alpha = 0.83$. At back-off the auxiliary transistor's small–signal output impedance was $Z_{t,A,BO} = 0.58 - \text{j}\ 24.413\ \Omega$. Moreover, at 3.6 GHz, $Z_{L,M,P} = 8.7 + \text{j}\ 12.1\ \Omega$ for the main transistor and $Z_{L,A,P} = 6 + \text{j}\ 11\ \Omega$ for the auxiliary transistor and at this frequency the maximum output power was 41.65 dBm from the main device but for the auxiliary transistor it was 40.7 dBm. According to these values, the power ratio coefficient $\alpha = 0.81$. The small–signal output impedance was $Z_{t,A,BO} = 0.58 - \text{j}\ 22.6\ \Omega$ for the auxiliary transistor at output power back-off. Based on these optimum load impedances at different frequencies, we obtained the load reflection coefficients seen by the auxiliary transistor $\Gamma_{t,A,BO}$. According to the characterization of the IMSN, the input power splitting ratio, $\gamma = 1.1$ was selected for the input network at 3.5 GHz,

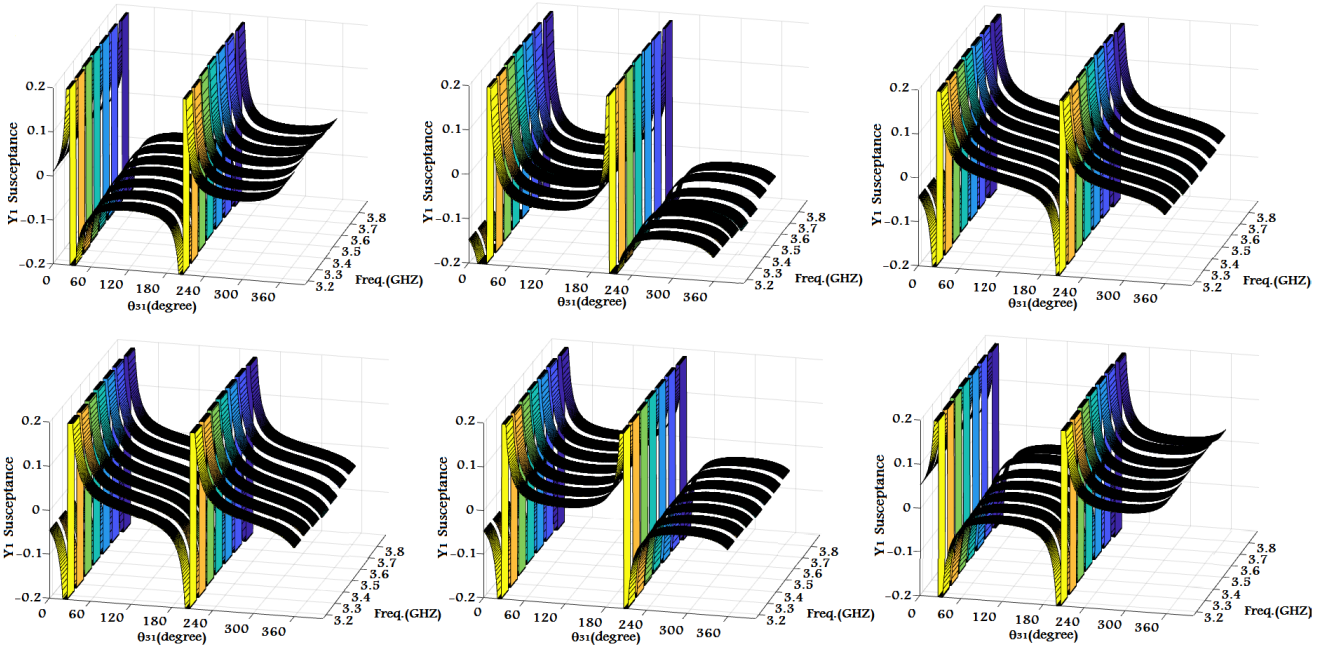

FIGURE 10. Possible output matching-combining network admittance values as a function of θ_{31} form pre-selected values of θ_{21} over the frequency range 3.2-3.8 GHz.

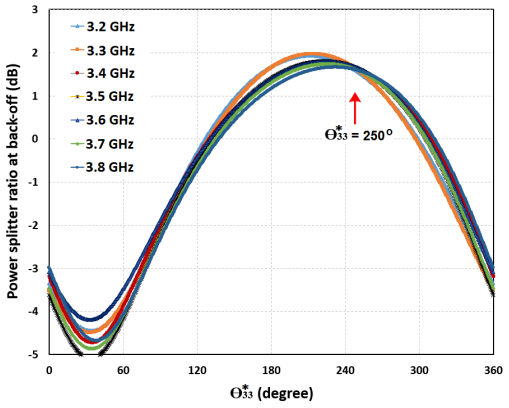

FIGURE 11. IMSN Input power ratio of the main transistor to the auxiliary transistor at back-off region versus θ^*_{33}.

TABLE 2. θ_{21} as a function of the frequency.

Frequency (GHz)	$\theta_{21}(f)$			
	1^{st} value	2^{nd} value	3^{rd} value	4^{th} value
3.3	151.35^o	-34.61^o	155.6^o	-27.63^o
3.35	154.76^o	-25.23^o	148.3^o	-31.7^o
3.4	156.33^o	-23.66^o	145.42^o	-29.58^o
3.45	173.22^o	-6.77^o	143.34^o	-36.65^o
3.5	189.55^o	9.55^o	139.3^o	-40.72^o
3.55	183^o	3^o	140.24^o	-39.75^o
3.6	177.9^o	-2.1^o	138^o	-42^o
3.65	182^o	1.88^o	135.4^o	-47.6^o
3.7	185.63^o	3.42^o	132.65^o	-49.8^o

$\gamma = 1.09$ at 3.4 GHz and $\gamma = 1.1$ at 3.6 GHz at output peak power.

The source and load reference impedances for the designed amplifier was 50 Ω, based on the reference impedances and by following the step procedures in Section III-A. The possible four values of the phase θ_{21} can be obtained for the OMCN at the targeting frequency range as mentioned in Table 2. By sweeping θ_{31}, we can get the available admittance values Y_1 to Y_6 at a given frequency. These procedures were repeated at frequencies 3.2, 3.3, 3.4, 3.5, 3.6, 3.7 and 3.8 GHz to get the best output parameters. By comparing the admittance parameters, we found that the shaded third and fourth phase's parameters in Table 2 gave us a symmetrical admittance values across the desired operating frequency band from 3.3 to 3.7 GHz. In this Doherty design, we select the third phase parameter from Table 2. For a selected value of θ_{21}, Fig. 10 displays the possible admittance values at these frequencies as function of θ_{31}, it is noted that for some values of θ_{31} the admittance parameters have the same values for certain range of frequencies. On the other hand, at other values of θ_{31} the admittance parameters show large differences within the design frequency band. This means that using the parameters from Fig. 10, one can select a value of θ_{31} that suits a wideband design.

In addition, a yield analysis was performed to obtain the convenient matching network with a low sensitivity to the process variation and of course, meeting the process limitations of the foundry. Based on this analysis, the output network parameters were chosen from Fig. 10 at the phase values of $\theta_{31} = 240°$. It can be noted that $\theta_{31} = 120°$ can be a good choice as well.

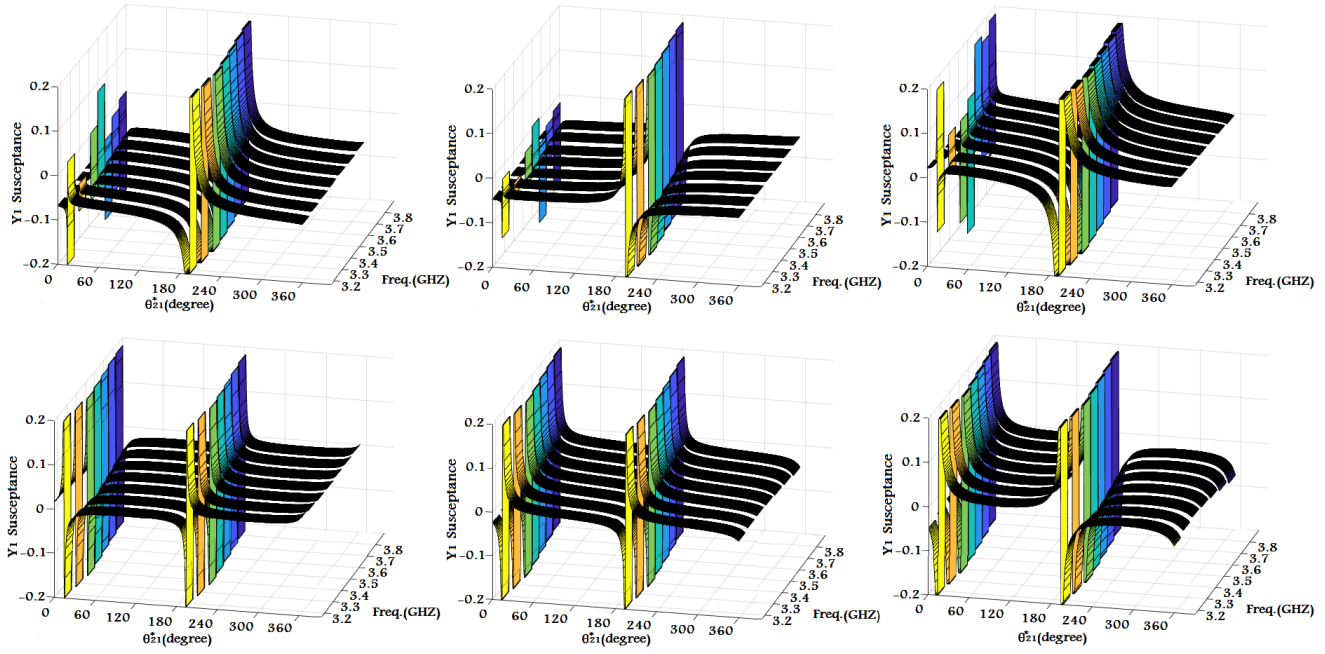

FIGURE 12. Input matching-splitting network admittance values from 3.2 - 3.8 GHz for ($\theta^*_{33} = 250^o$).

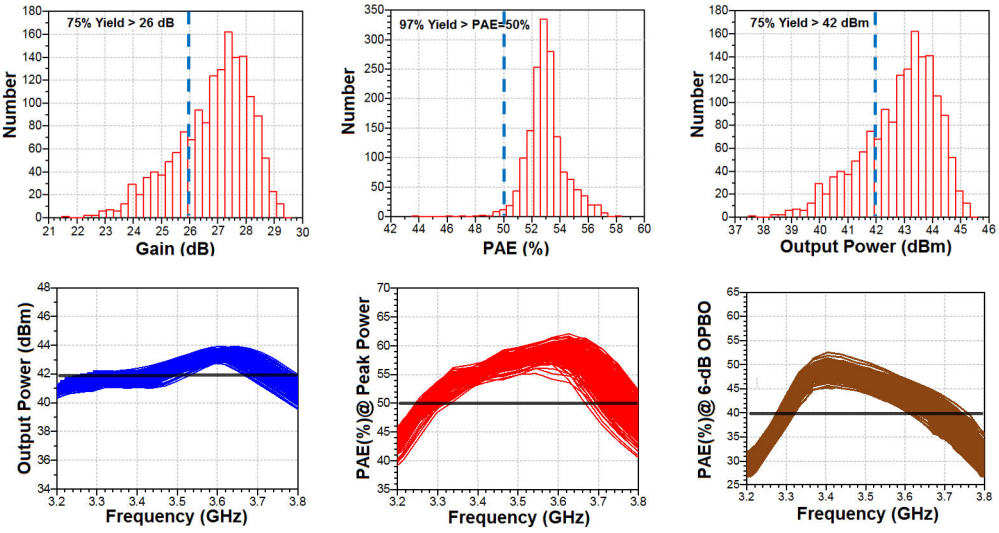

FIGURE 13. Variations, due to the yield process dispersion of gain, PAE and output power of the MMIC Doherty PA across the operating bandwidth.

By using the obtained OMCN and performing source–pull simulation, at the center frequency of 3.5 GHz, the main transistor's large-signal input impedance at the peak power was $Z_{in,M,P}$ = 2 - j 15.8 Ω, while at the power back-off, it was found to be $Z_{in,M,BO}$ = 1.9 - j 15.5 Ω. For the auxiliary transistor, the large-signal input impedances were found to be $Z_{in,A,P}$ = 2.24 - j 21.7 Ω and $Z_{in,A,BO} = 4 - j\,23.8$ Ω at the peak power and the power back-off, respectively. To design the IMSN, The complex input-splitting factor was found as $\gamma = 1.1$, and the required phase difference between the main and the auxiliary input signals was determined to be $\theta_0 = 60°$ degree based on the design methodology presented in Table 1. From load-pull/source-pull simulation we indicated the input reflection coefficients $\Gamma_{in,M,BO}(f)$ and $\Gamma_{in,A,BO}(f)$ of the main and the auxiliary transistors respectively. Then, to obtain the value of $\theta^*_{33}(f)$, the power splitting factor at the power back-off from 3.2 to 3.8 GHz is plotted in Fig. 11 using equation (8). The value of $\theta^*_{33} = 250°$ turns out to be an appropriate choice over the desired frequency band and also, it provides a higher gain of the Doherty amplifier at power back-off and minimizes the power dissipated

TABLE 3. Admittance values Y_1 to Y_6 for the OMCN and IMSN.

Y-Parameters	Pass-yield		Fail-yield	
	OMCN Susceptance (S) ($\theta_{21} = 139^o$ and $\theta_{31} = 240^o$)	IMSN Susceptance (S) ($\theta^*_{33} = 250^o$ and $\theta^*_{21} = 45^o$)	OMCN Susceptance (S) ($\theta_{21} = -40.7^o$ and $\theta_{31} = 80^o$)	IMSN Susceptance (S) ($\theta^*_{33} = 230^o$ and $\theta^*_{21} = 180^o$)
Y_1	-0.02	-0.054	-0.023	0.08
Y_2	-0.13	-0.058	-0.076	0.04
Y_3	0.02	0.015	-0.04	0.04
Y_4	0.04	-0.015	-0.03	0.025
Y_5	-0.035	0.018	0.025	0.028
Y_6	0.046	0.035	0.03	-0.01

TABLE 4. Yield analysis of output power and PAE across the frequency of operation.

Yield	1^{st} Solution			2^{nd} Solution		
	Max. Output power	PAE @ Peak power	PAE @ 6-dB OPBO	Max. Output power	PAE @ Peak power	PAE @ 6-dB OPBO
Peak-Peak variation	41-44 dBm	46-58 %	35-53 %	40-44 dBm	40-56 %	30-48 %
Yield process	75% Yield>42 dBm	97% Yield>50 %	90% Yield>40 %	70% Yield>42 dBm	50% Yield>50	50% Yield>40

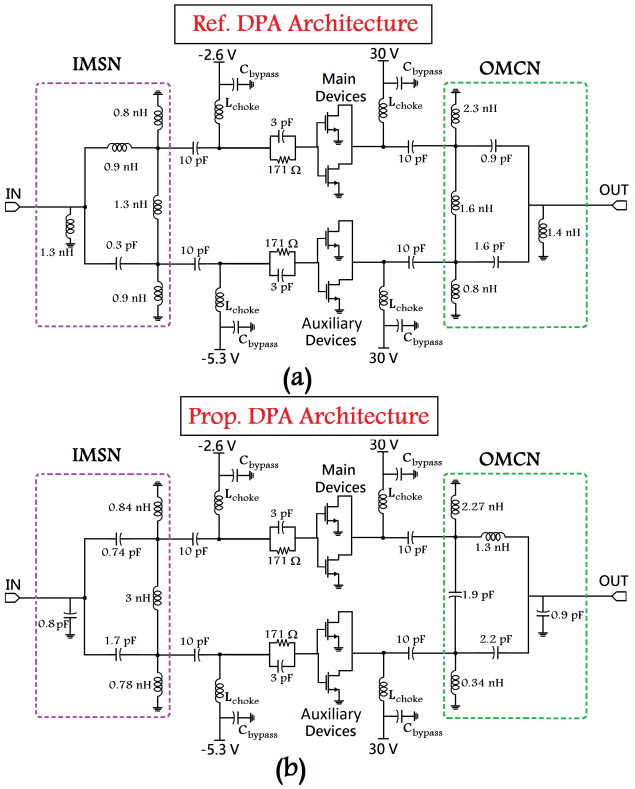

FIGURE 14. Doherty amplifier circuits (a) Reference DPA architecture, (b) Proposed DPA architecture.

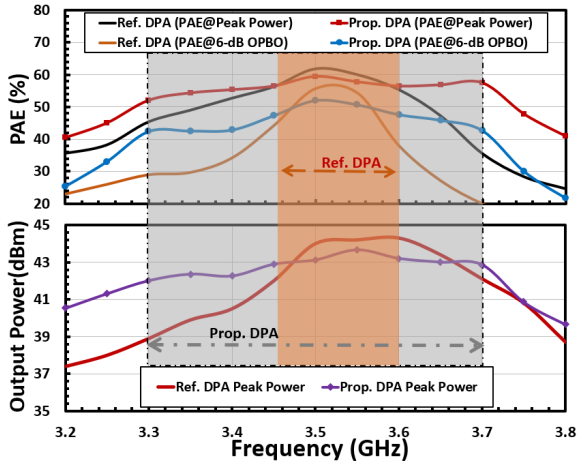

FIGURE 15. Simulation comparison between reference and proposed DPA architectures.

in the input resistance of the auxiliary amplifier, when it is off.

Using the selected θ^*_{33}, the values of the admittance Y_1 to Y_6 as a function of $\theta^*_{21}(f)$ are plotted for the target frequency band as shown in Fig. 12. To obtain an input-splitting network with reasonable element values, $\theta^*_{21} = 45^o$ was selected because the admittance values at different frequencies fall around the same value. This means that using these parameters at this selected phase will suit a broadband design at the input network of the DPA. As a result, the elements of the input and output networks were obtained based on the proposed design methodology, which optimizes the DPA performance such as efficiency, back-off range, and frequency response, and also deals with the MMIC design constrains like circuit's sizes and yield as shown in Table 3. The admittance values Y_1 to Y_6 for the OMCN and IMSN are reported (first solution) in Table 3. These values were obtained from Fig. 10 and Fig. 12 respectively. We transformed these values using combined distributed and lumped elements taking into account the derating's processes limits and to improve the yield dispersion. In Table 3, we also reported another possible three-port networks combination. The first one (shaded red) passed the yield analysis according to the foundry process limits and design requirements which were used in the DPA implementation, while the second solution (shaded blue) failed in the yield performance. The specific yield analysis variations are illustrated in Table 4. After modifying the designed circuit and adding the physi-

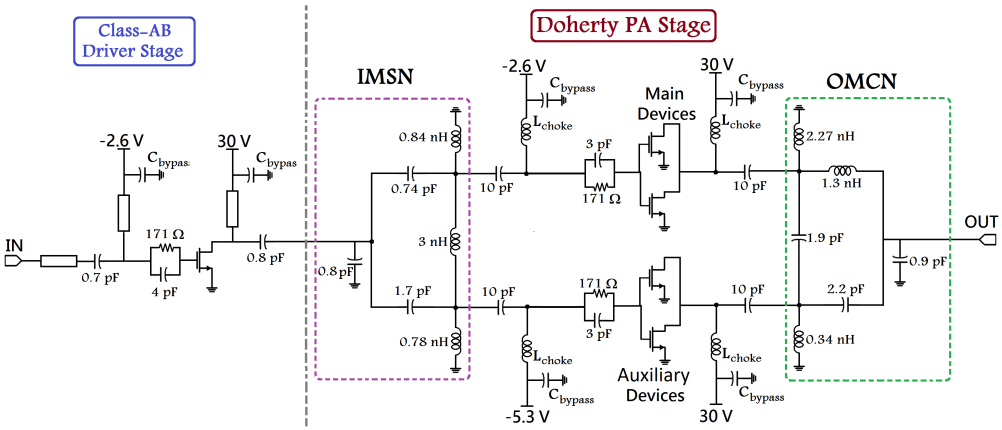

FIGURE 16. Complete schematic of the two-stage GaN MMIC three-port Doherty amplifier.

cal variable standard deviations and the yield requirements, a Monte Carlo analysis was performed on the full MMIC Doherty circuit. A performance histogram of gain, PAE and output power using 1600 trials was calculated at the operating frequency band as displayed in Fig. 13 to obtain the accurate deviation. The Monte Carlo analysis shows that the yield of gain greater than 26 dB is 75% while the yield of PAE greater than 50% at saturation power level is 97%.To verify the new design methodology, two DPAs based on the three-port network are designed using the reference topology as in [35] and the new analysis proposed in this paper. Fig. 14 shows the detailed circuit parameters of the designed two Doherty amplifiers. The simulated large-signal performance of the referenced and proposed DPAs were plotted from 3.2 to 3.8 GHz, as in Fig. 15. For the proposed DPA, wideband Doherty behavior can be observed from 3.3 to 3.7 GHz. The PAE is 42.5%–52% and 52%–59.4% for the 6 dB OPBO and saturation power level over this frequency band, respectively. For reference DPA, the operating bandwidth is narrow (3.45–3.6 GHz). However, the corresponding PAE is 38%–54% and 52%–60% for the 6 dB OPBO and saturation regions. Compared with the reference case, the proposed DPA can achieve broadband behavior with better large-signal performance. The full schematic of the proposed two-stage three-port network-based DPA is presented in Fig. 16.

V. FABRICATION AND EXPERIMENTAL CHARACTERIZATION

The two-stage MMIC Doherty amplifier was designed and fabricated using a 0.25 um GaN-HEMT process. The carrier amplifier operates under a Class-AB condition with a quiescent current of 300 mA, and the auxiliary amplifier is biased to the Class-C condition. Both amplifiers have a drain supply voltage of 30V. A microscopic photo of the fabricated DPA IC on a package is displayed in Fig. 17(a). In the design work, a compact layout was tailored, resulting in a chip-size of 4.4 mm × 3.5 mm. Fig. 17(b) shows a photograph of the implemented evaluation board. The DPA IC was mounted on

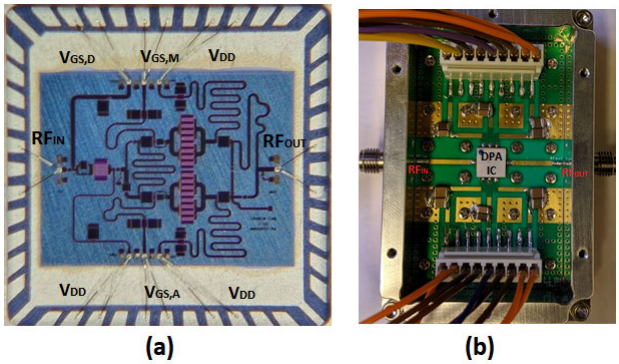

FIGURE 17. Microscope image of the fabricated GaN-HEMT DPA. (a) DPA IC on a QFN package. (b) Evaluation board.

a 7 mm × 7 mm QFN package. As shown in Fig. 17(b), a few bypass capacitors were added to the evaluation board.

A. MEASUREMENT WITH PULSED AND CW SIGNALS

The fabricated DPA has been experimentally characterized using pulsed-RF and CW signals. In the pulsed-RF setup, the gate quiescent voltage for the first stage and the main amplifier is varied from on state ($V_g = -2.6\ V$) to a large negative voltage ($V_g = -5\ V$) covering voltages at which a HEMT operates in a switch circuit. The pulse width is 5 μsec, and the pulse period is 200 μsec. The peak power of the pulsed-RF signal was estimated by sensing the average power of the pulse and then dividing it by the duty cycle of the pulse [37]. Fig. 18 illustrates the detailed components of the full setup used in the Doherty PA measurements, while the actual measurement bench is depicted in Fig. 19.

Six samples of the MMIC PA have been characterized, to determine the process performance uniformity, and thus verify the robustness of the design strategy. Fig. 20 shows the measured power added efficiency (PAE) and the gain of the fabricated DPA as a function of output power at different frequencies within the band. Drain efficiency of 51% – 59.2% and 38.6% – 51.5% is achieved at the peak output

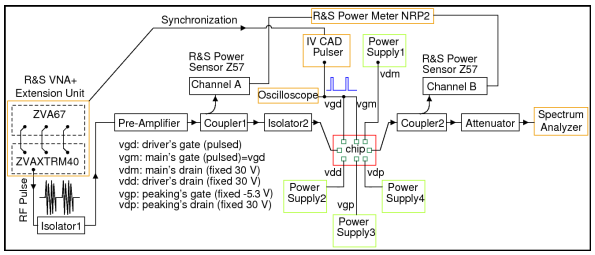

FIGURE 18. Block-diagram of the measurement setup.

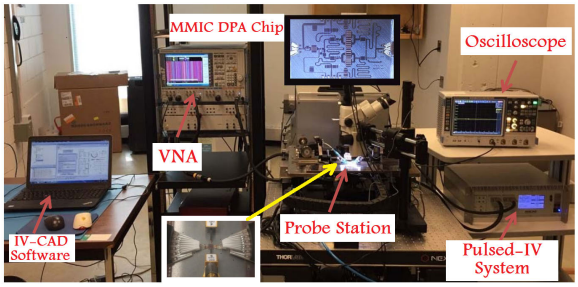

FIGURE 19. The actual measurement setup for amplifier characterization.

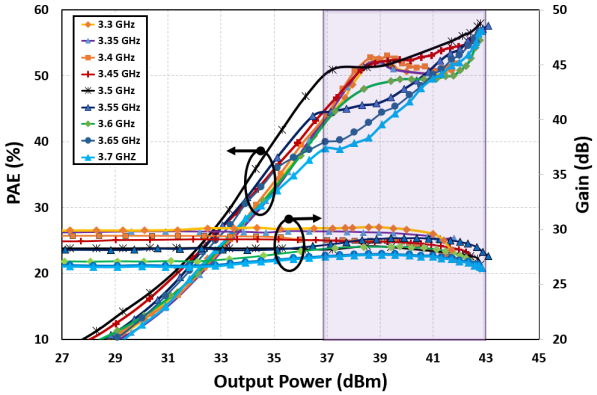

FIGURE 20. Measured gain and power added efficiency versus output power.

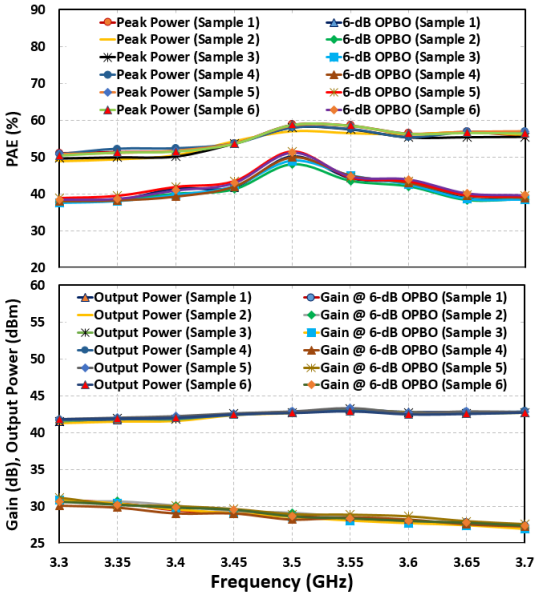

FIGURE 21. Measured power added efficiency, peak output power, and gain at OPBO versus frequency.

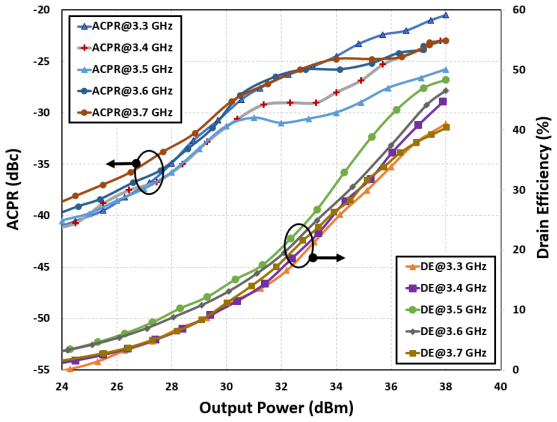

FIGURE 22. Measured ACPR and the drain efficiency of the modulated signal versus average output power.

power and at 6-dB output power back-off region, respectively. The measured maximum output power is more than 42 dBm.The above CW measurement results verify that the designed MMIC amplifier shows excellent performance at the frequency band from 3.3-3.7 GHz.

To better present, the outcome broadband performance of the proposed DPA, the measured PAE, peak output power and gain at 6-dB output power back-off for the six samples of the fabricated MMIC DPA are plotted versus frequency as depicted in Fig. 21. The plotted data shows that the PAE is in excess of 50.8% and 38% is obtained at peak output power and 6-dB OPBO, respectively, over the targeting frequency band. In addition, the saturated output power across the band is in order of 41.8 dBm with an associated gain in the range of 27.4 dB to 30.6 dB.

B. MEASUREMENT WITH MODULATED SIGNAL

To evaluate the performance of the fabricated MMIC DPA when driven by a modulated signal, a long-term evolution (LTE) signal having 7.5 dB of PAPR and 20 MHz of bandwidth was employed to test the DPA at 3.5 GHz. The power of the LTE signal was swept and the values of the average drain efficiency (DE) and adjacent channel power ratio (ACPR) for the designed DPA were obtained and plotted versus output power, as displayed in Fig. 22. The measured ACPR at an average output power of 36.5 dBm, changed from −27 dBc to −22.4 dBc. Meanwhile, the measured average drain efficiency of the amplifier was between 36.5% and 46.4% across the whole working frequency band. Digital predistortion (DPD) consisting of the lookup table and memory polynomial was performed to linearize the implemented DPA. Fig. 23 displays the output spectrum with, and without,

TABLE 5. Comparison with recently reported DPAs.

Ref.	Freq. (GHz)	Psat.(dBm)	Gain at 6-dB OPBO (dB)	PAE at peak power (%)	PAE at 6-dB OPBO (%)	Technology
[30] one-stage	6.8-8.5	35	6-14	32-53	30-43	GaN HEMT 0.25 um
[33] one-stage	2.1-2.7	41	12-14	-	-	GaN HEMT 0.25 um
[35] one-stage	0.95	41	15	58	54	GaN Cree
[38] one-stage	5.5-6.5	44	9	37-43	32-36	GaN HEMT 0.25 um
[39] one-stage	2.14	42	13.5	63	55	GaN HEMT 0.25 um
[40] one-stage	5.1-5.9	38.7	14.4-17.3	43.2-47.3	31.6-49.5	GaN HEMT 0.25 um
[41] two-stage	1.7	38.6	16	45.8	35	GaN HEMT 0.25 um
[42] two-stage	2.41	41.2	19	56.2	43.4	GaN HEMT 0.25 um
[43] two-stage	7	38	14	57	41	GaN HEMT 0.25 um
This Work (two-stage)	3.3-3.7	41.8-43.2	27.4-30.6	51-59	38-52	GaN HEMT 0.25 um

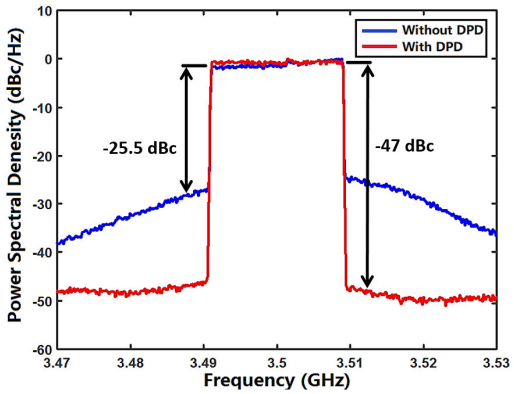

FIGURE 23. Measured normalized power spectral density of a 20 MHz LTE signal at 3.5 GHz with and without digital pre-distortion.

DPD linearization of the DPA under a 20 MHz signal at 3.5 GHz. It is clear from the results in Fig. 23 that the ACPR, after performing DPD, was improved to better than −47 dBc. These results confirm that the fabricated MMIC DPA achieves consistent power and efficiency performance, across the targeting frequency of operation, and relatively excellent performance compared with the other published studies, as listed in Table 5.

VI. CONCLUSION

A general broadband design methodology for Doherty architecture based on three-port input and output combining and matching networks is introduced in this paper. The approach introduces a detailed theoretical parameter for both input and output networks. For broadband operation, a new design methodology was used to alleviate the bandwidth limitations. For the first time, the three-port matching and combining networks were implemented using MMIC technology. The non-isolated output network performs as a power combiner and it matches the reference load impedance to the optimum impedance of the two transistors at output peak power. it also keep the optimal response at the back-off region. The input-splitting network is proposed for matching the input impedances of the two transistors to the source impedance. According to the measured results, the proposed DPA achieves the desired Doherty operation, resulting in a high PAE and high output power across the targeting operation band. The proposed Doherty PA delivers 42 dBm peak power with an associated gain of 27.4 dB. Over the design band of 400 MHz, it exhibits PAE of 52% - 60% at peak power and of 38% – 51% at – 6 dB back-off. When driven by 20-MHz LTE signal with 7.5-dB PAPR, the implemented DPA exhibits 36.5%–46.4% average drain efficiency.These results show superior performance compared to other reported MMIC Doherty PAs.

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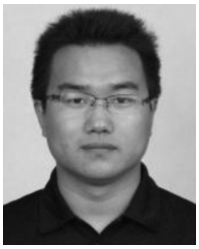

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