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Design and Implementation of Multilevel Inverters for Electric Vehicles

C. DHANAMJAYULU[1,2], (Member, IEEE), SANJEEVIKUMAR PADMANABAN[2], (Senior Member, IEEE), VIGNA K. RAMACHANDARAMURTHY[3], (Senior Member, IEEE), JENS BO HOLM-NIELSEN[2], (Senior Member, IEEE), AND FREDE BLAABJERG[4], (Fellow, IEEE)

[1]School of Electrical Engineering, Vellore Institute of Technology (VIT) University, Vellore 632014, India
[2]Center for Bioenergy and Green Engineering, Department of Energy Technology, Aalborg University, 6700 Esbjerg, Denmark
[3]Department of Electrical Power Engineering, College of Engineering, Institute of Power Engineering, Universiti Tenaga Nasional, Selangor 43000, Malaysia
[4]Center of Reliable Power Electronics (CORPE), Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark

Corresponding authors: C. Dhanamjayulu (dhanamjayulu.c@vit.ac.in) and Sanjeevikumar Padmanaban (san@et.aau.dk)

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ABSTRACT The efficient and compact design of multilevel inverters (MLI) motivates in various applications such as solar PV and electric vehicles (EV). This paper proposes a 53-Level multilevel inverter topology based on a switched capacitor (SC) approach. The number of levels of MLI is designed based on the cascade connection of the number of SC cells. The SC cells are cascaded for implementing 17 and 33 levels of the output voltage. The proposed structure is straightforward and easy to implement for the higher levels. As the number of active switches is less, the driver circuits are reduced. This reduces the device count, cost, and size of the MLI. The solar panels, along with a perturb and observe (P&O) algorithm, provide a stable DC voltage and is boosted over the DC link voltage using a single input and multi-output converter (SIMO). The proposed inverters are tested experimentally under dynamic load variations with sudden load disturbances. This represents an electric vehicle moving on various road conditions. A detailed comparison is made in terms of switches count, gate driver boards, sources count, the number of diodes and capacitor count, and component count factor. For the 17-level, 33-level, and 53-level MLI, simulation results are verified with experimental results, and total harmonic distortion (THD) is observed to be the same and is lower than 5% which is under IEEE standards. A hardware prototype is implemented in the laboratory and verified experimentally under dynamic load variations, whereas the simulations are done in MATLAB/Simulink.

INDEX TERMS Multilevel inverter, photovoltaic (PV) system, maximum power point tracking (MPPT), electric vehicles (EV), total harmonic distortion (THD).

I. INTRODUCTION

With the demand for an increase in the requirements of high-power quality in industrial applications and solar PV systems, the conventional inverters in meeting the desired conditions like a pure sine-wave output and less harmonic distortions is a challenging task. The multilevel inverters receive more attention in reaching the desired requirements and acts as an alternative in delivering a quality of power. It provides several advantages such as reduced device count, operates in low switching frequency, reduced dv/dt stress, less harmonic distortions, etc. [1]. The recent multilevel inverter topologies comprise a smaller number of components used in the circuit compared with the conventional inverters such as flying capacitor type (FC) [2], cascaded H-bridge type (CHB) [3], and the neutral point clamped type (NPC) [4]. The number of components in the circuit is directly proportional to the number of levels in MLI, which increases cost and complex structure [5]. In both the FC MLI and NPC MLI, the capacitor voltage balancing is a challenging task with which these are limited to five-level and unable to cascade. This lowers the output voltage to half of the input voltage, providing a high

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switching frequency with more losses [6]. A wide range of research is reducing the components of MLI, and several topologies are proposed based on the various levels which are having their challenges [7], [8].

In the recent past, various MLI topologies without association with the conventional three types of classification are reported in [9]–[13]. Significantly, the sub multilevel converter configurations are proposed in [15]. In [10], a basic level topology is reported, where multiple dc voltages are required. The coupled inductor-based topologies are documented in [9] and [11]. These architectures are simple but extending to higher levels is a challenging task. A novel MLI topologies based on switched-capacitor (SC) with boost techniques are presented in [12] and [13] where the output voltage levels are limited to 5, 7, and 13, respectively. The MLI topology proposed in [14] can be extended to higher levels. The utilization of several switches and devices increases the cost and size of the system.

Concerning the switched capacitor (SC) technique, a new MLI topology with a multilevel converter and a full bridge is represented in [16]. A five-level single phase inverter with a full bridge makes up two diodes, and a single switch is presented in [17] which provides five levels in its output, and its circuitry limits the extension of higher levels. The SC-based MLI topology reported in [18] makes up a front-end SC, and full-bridge backend, the control complexity, and more device count limit the application. As the carrier frequency provides the switching frequency, a high switching loss is irresistible for providing the high-frequency output [51]. A boost MLI with a partial charging technique of SC theoretically can able to extend the number of output voltage levels. The control complexity is high in implementing partial charging [12]. Hence, designing an SC-based MLI with high-frequency output, fewer harmonics, and high efficiency is a challenging task [19]. The high-frequency output applies for implementing circuits in electric vehicle (EV) since the weight and size of the system is less [20].

The photovoltaic power generation comprises solar PV panels, where the output of a solar panel is fed to DC link through a DC-DC converter. The voltage from a DC link is fed to the DC-AC inverter and to load [21]. The output of solar PV is not constant, and it changes according to the solar irradiation and temperature [22]. Therefore, for an efficient operation of PV panels even under various climatic changes, it is essential to extract maximum power from the PV module, admitted to being Maximum power point tracking (MPPT) [23]. Whenever the MPPT exists in a system, a DC-DC converter plays a significant role in handling maximum power as it works with the duty cycle change [24].

For a PV fed inverter, in producing a stable DC voltage, there is a need for a control technique. A standard PI controller realized in the standalone PV system to select a proper duty cycle of the DC-DC converter by comparing the converter output with reference [25]. It is not desirable to have control over the DC-DC converter with the MPPT technique, and hence various topologies are proposed to solve this issue for the standalone solar system. In the recent past, several advanced techniques like artificial intelligence (AI), practical swarm optimization (PSO), fuzzy and genetic algorithm (GA) to have an auto-control regarding the training data to regulate voltage [26]. The selection of the MPPT technique for a suitable application is an astonishing task where every method has its own merits and demerits. For example, hill climbing (HC), perturb, and observing (P&O) and are widely used MPPT methods because of their simple implementation. Under partial shading conditions, the conventional methods like fuzzy, P&O, INC algorithms cannot extract global MPP (GMPP) [27]. Many works of literature have been implemented MLI with DC link with MPPT, where the control of outputs can be done by the load [28] or under steady solar irradiance [29]. MPPT consistently changes the energy of the solar panel to operate at the maximum point of the power, which depends on temperature, load, and solar irradiance. Both solar irradiance and temperature change during day time for climatic conditions and depending on the season. So, it is vital to track all these parameters and get maximum power-point.

In this paper, a solar PV system is implemented using a 53-level multilevel inverter integrated with a single input, and multiple output DC-DC boost converter is presented. P&O powered MPPT technique is implemented in the proposed system to extract peak energy from the solar panels. DC voltage from the between the solar panels fed to the single input and multiple output boost converter where the voltage gets boosted to the desired level and provided to the 53-level inverter. The SC units are cascaded to achieve 17, 33 levels of output voltages. Performance of these MLIs based on many such parameters like device count, power losses, efficiency, THD is compared with various MLI topologies and represented. The implemented system is tested in MATLAB/Simulink, whereas it is tested experimentally with a hardware setup.

The organization of the paper is: Modeling of PV and single input and multiple output DC-DC boost converter is represented in section-II, the proposed 53-level MLI modeling with the SC units cascade combinations to get 17 and 33-level MLIs along with the power loss calculations are shown in section III. The simulation and experimental results are explained in section IV. Several comparisons with the same and distinct levels of MLI topologies are presented in section-V. Finally, conclusions are made in section VI.

II. MODELLING OF PV AND DC-DC BOOST CONVERTER

A. MODELLING OF SOLAR PV

The modeling of a solar cell is an important segment of analyzing a solar PV system. The overall proposed circuit comprises solar panels, a three-level DC-DC boost converter fed to 53-level MLI shown in Figure 1. The solar PV can be modeled with three categories such as an equivalent circuit with current-voltage (I-V) and power-voltage (P-V) characteristics, the effect of solar irradiance and temperature, and

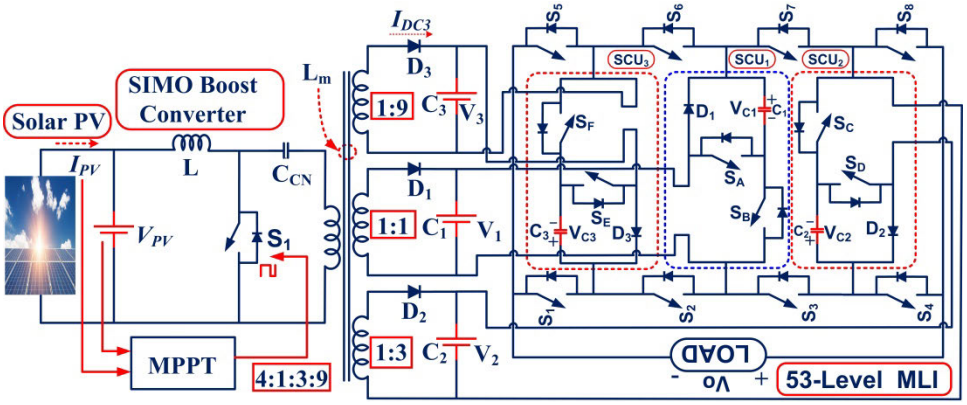

FIGURE 1. Overall structure of the proposed system.

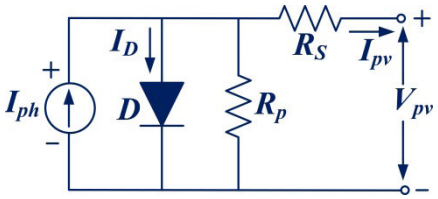

FIGURE 2. Equivalent circuit of solar cell.

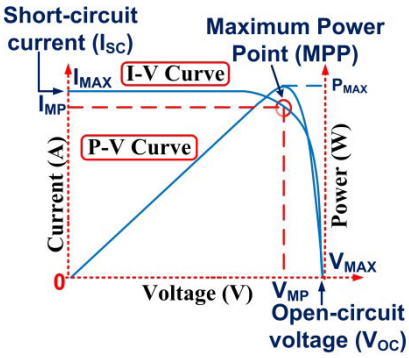

FIGURE 3. I-V Characteristics of solar cell.

the partial shading condition is taken into consideration. PV resembles two words photo and voltaic: photo represents the photonic energy and voltaic represents the electrical energy, which implies that the energy conversion from photonic energy into electrical energy [30]. The combination of a solar array is of various types of modules, where each module comprises solar cells. This comprises of p-n semiconductor diodes [31]. The designed solar PV has a behavior of changing its output with the variation of temperature and climatic conditions [32]. Therefore, the factors in modeling a solar PV are represented below:

1) SOLAR CELL: EQUIVALENT CIRCUIT AND I–V CHARACTERISTICS

The solar cell comprises internal resistance R_{SE} and R_{SH} connected to the diode in series and parallel combination, known to be an equivalent circuit shown in FIGURE 2.

V_{PV} and I_{PV} are the output voltage and current of a solar cell, respectively. These are got from the series and parallel connection of several PV modules shown in equation (1),

$$I_{PV} = \left\{ I_{Ph} - I_0 \left[exp\left(\frac{q(V_{PV} + R_{SE} I_{PV})}{N_{SE} AKT} \right) - 1 \right] - \frac{(V_{PV} + R_{SE} I_{PV})}{N_{SE} R_{SH}} \right\} \quad (1)$$

where N_{SE} and N_{SH} are the number of PV cells in series and parallel connection. R_{SE} is the series resistance, and R_H is the parallel resistance. A is the ideality factor of a semiconductor device. K is Boltzmann's constant ($1.3806503 \times 10^{-23}$ J/K), T is 'he temperature. I_p is the current produced and is depends on the irradiation and temperature shown in equation (2)

$$I_P = [I_{SK-STM} + K_i (T - T_{STM})] - \left(\frac{G}{G_{STM}} \right) \quad (2)$$

where I_{SK-STM} is a short-circuited current at standard testing cases (STM), Ki is the SCC coefficient, G (W/m^2) is the irradiance on the surface of the cell, GSTM ($1000W/m^2$) is the irradiance at STM, and the cell temperature is T_{STM} [33].

$$I_O = \left\{ \frac{I_{SK-STM} + K_i (T - T_{STM})}{exp\left[(V_{OK-STM} + K_{OV} (T - T_{SKC}) / AV_{Sth} \right]} \right\} \quad (3)$$

where V_{OK-STM} is an open-circuited voltage at the standard testing case, K_{OV} represents the open-circuit voltage coefficient, V_{Sth} is solar cell thermal voltage.

$$P_{PV} = V_{PV} \times N_{SH} \left(I_{Ph} - I_O exp\left(\frac{qV_{PV}}{N_{SE} AKT} \right) - \left(\frac{V_{PV}}{N_{SE}} \right) \right) \quad (4)$$

I-V/P-V curves represent the characteristics of a solar cell is shown in FIGURE 3 [4]. It is clear from the curve there is instability for the operating point of a PV; it varies continuously from null to open-circuit voltage. In this process, there is a single point that provides peak power for the design of solar PV at various irradiance. Here, the respective voltage and currents are V_{MPP}, I_{MPP} shown in Figure 3.

The values of current and voltage got from the solar PV depend on irradiance, temperature, number of series, and parallel connected strings. So, it is required to choose the solar panel wisely. In this paper, the 1Soltech 1STH-215-P panel is chosen from the list of given solar modules data in MATLAB with 2 series and parallel connected modules per string. The specifications of the selected solar panel are described in table 1 and the readings in the table are given for 1 parallel string and 1 series-connected module with a solar irradiance of 1000 W/m^2 and 250°C temperature.

2) IRRADIANCE AND TEMPERATURE EFFECT

The solar PV output continuously varies with variation in climatic changes [34]. As the solar irradiance confides on the incidence angle of sun rays, this effect forces the I-V/P-V characteristics to change. The output current I_{PV} varies with the variation of sunray incidence, making V_{PV} constant and V_{PV} also shifts its magnitude, making I_{PV} constant [34]. Three factors are influencing the variation in temperature of a solar PV: The heat dissipated on its own during the functioning of PV, for the infrared wavelength started, which is a worn on the cell and the gradual increase in the sunbeam intensity [26]. The V_{OC} and I_{SC} are measured based on the equations (5) and (6) at variable irradiance.

$$V_{OC} = V'_{OC} + a_2\left(T - T'\right) - (I_{SC} - I'_{SC})R_{SE} \quad (5)$$

$$I_{SC} = I'_{SC}\left(\frac{G}{G'}\right) + a_1\left(T - T'\right) \quad (6)$$

From the above equations, the temperature coefficients are a_1 and a_2 of the PV cell, respectively [35]. V'_{OC} and I'_{SC} are the reference parameters at solar intensity G' and temperature T'.

As the variations of climatic conditions are specific, it affects the output voltage and currents. At any point during the operation of solar PV, the maximum extraction of power can be done. This can be possible with an efficient MPPT technique that tracks the irradiation and temperature and provides a constant voltage at the output.

3) PARTIAL SHADING EFFECT

Apart from the temperature and irradiance conditions, a partial shading case is also a challenging task for the MPPT technique in achieving maximum power. This partial shade occurs with mists, consecutive structures, trees, etc. [36]. According to equation (2), the photocurrent I_{ph} gets reduced with low insolation. With series-connected PV modules, the current is the same in all cells. But in this case, the shaded cell goes to a breakdown, and instead of providing the energy, this acts as a load because of the weakening of photocurrent.

B. MPPT CONTROLLER

The operating of solar PV is to extract the maximum power from the PV module is an MPPT controller. During all the disturbances mentioned above, if the controller can able to operate efficiently in tracking and to provide peak power from the solar panels, the efficiency and life span of the solar PV gets increased. This can be achieved by sinking the solar source to the load for various climate conditions to produce maximum power. There are two ways to extracting the maximum power from a solar panel. They are Mechanical and electrical tracking. With mechanical tracking, the solar panels change their direction depends on the climatic variation patterns. This includes seasonal climate changes for several months. With electrical tracking, the I-V curve is forced to locate the point of maximum power in the operation of the PV array [37]. The MPPT controller is an internal part of the system which feeds the maximum power to load (batteries/motors).

TABLE 1. Specifications of the 215W PV system.

Maximum power	213.15W
The voltage at maximum power point (V_{MPP})	29V
Open circuit voltage (V_{oc})	36.3V
Current at maximum power point (I_{MPP})	7.35A
Short circuit current (I_{sc})	7.84A
Diode ideality factor	0.98117
Diode saturation current (I_O)	2.9259×10^{-10}A

For tracking maximum power during the operation of the PV module, a suitable algorithm is to be used. This can be seen in the P-V graph of a solar cell. There are many such methods to track the maximum power such as incremental conductance, perturb and observe, genetic algorithm, fractional open-circuit voltage, etc. In this paper, the perturb and observe algorithm it has many advantages. It is easy to implement using various controllers such as Arduino, microcontroller, etc. The maximum power point determination speed can be controlled by varying the perturbation value. The P&O algorithm is shown in Figure 4.

The algorithm for Perturb and Observe Technique is:

a) Ipv and Vpv values are gathered from PV module.
b) Ppv is calculated from Ipv and Vpv.
c) Voltage and power values are stored.
d) The values are recorded for the next consecutive $(k+1)^{th}$ instant and repeat step 'a'.
e) The values got at $(k+1)^{th}$ instant are subtracted from the values got at kth instant.
f) In the PV curve of a solar panel, on the right side, the slope is negative i.e., (dP/dV<0) whereas on the left side, the slope is positive (dP/dV>0). Therefore, the lesser duty cycle occurs on the right side of the curve and the high-duty occurs on the left side of the curve.
g) Based on the polarity of the slope after subtraction, the algorithm decides the change in the duty cycle.

The solar panel is designed with a power of 215W; the respective parameters and their specifications are shown in TABLE 1.

C. DC-DC BOOST CONVERTER

A single input multiple output DC-DC boost converter interfaced in between the solar panels and the proposed inverter is

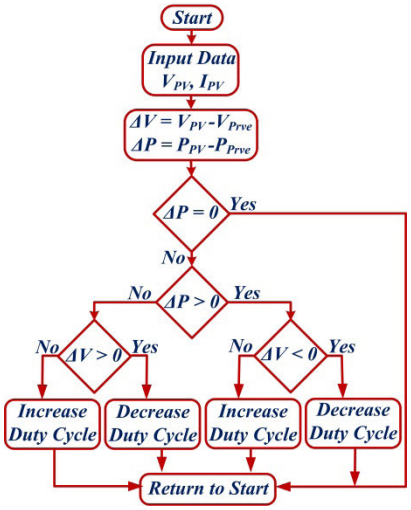

FIGURE 4. Flowchart of P&O algorithm.

shown in Figure 1 [38]. This converter provides three isolated dc sources in the ratio of 4:1:3:9. The converter feeds on a single solar PV to eliminate the unequal voltages along with the variations in the step size based on several climatic conditions.

The magnitude of the inductance can be calculated using the relation:

$$L = \left(\frac{mV_{dc}}{4af_sI_r}\right) \tag{7}$$

where V_{dc} is the input dc voltage, m is the modulation index, and fs is the switching frequency, Ir is the ripple current, a is the overloading factor which is usually 1.25.

The value of capacitance can be calculated using the relation:

$$C = \left(\frac{DI_{dc}}{V_{dc}rf_s \times 0.5}\right) \tag{8}$$

where I_{dc} is the dc current, fs is the switching frequency, r is the ripple voltage, V_{dc} is the input dc voltage, D is the duty cycle.

The duty cycle of the converter can be calculated using the following relation :

$$D = \left(\frac{V_O}{V_O + V_{dc}}\right) \tag{9}$$

The simulation and experimental results are shown in FIGURE 5 and FIGURE 6, respectively. The specifications of the boost converter are represented in Table II.

III. PROPOSED ASYMMETRICAL 53-LEVEL MLI

The proposed 53-level MLI is designed and implemented with a switched capacitor approach. SC is incorporated at the front end along with the H-bridge. It acts as an individual energy storage system for the proposed MLI. Hence it is essential to select the specific value of the capacitance, and the value depends on the operating frequency, load current

TABLE 2. Specifications of the boost converter.

Parameters	Value
Inductance L	4.8 mH
Capacitance C1	22 µF
Input DC voltage	29V
Output voltage	200V
Duty Cycle	0.87
Switching frequency	50kHz

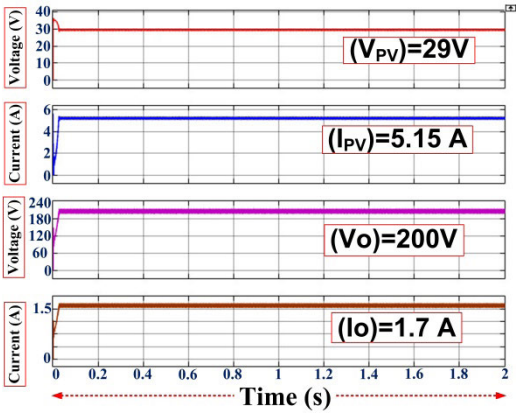

FIGURE 5. The solar PV and boost converter simulation waveforms.

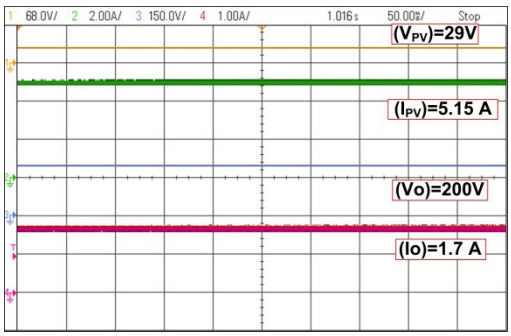

FIGURE 6. The solar PV and boost converter experimental waveforms.

requirement, and the upper limits of the additional ripple voltage. SC has the advantage of increasing the voltage level with its structural design. In general, a DC-DC converter is required to get a rated output fed to the inverter but irrespective of the converter rated output, in the proposed topology voltage gets boosted based on the SC design in its charging and discharging behavior. The addition of several SC units results in the production of the various number of levels of multilevel inverters. Here, the SC units are cascaded to form 17-, 33- and 53-level MLI. The respective MLIs are designed represented in the following subsections. A basic unit of SC is represented in FIGURE 7(a). The charging and discharging behavior of an SC are represented in FIGURE 7(b)& FIGURE 8(a). Under optimal, the capacitor C charged to V_1 when connected in parallel to conditions, the capacitor C charged to V_1 when connected in parallel to the source, and it gets discharged to the load with a series connection. As represented

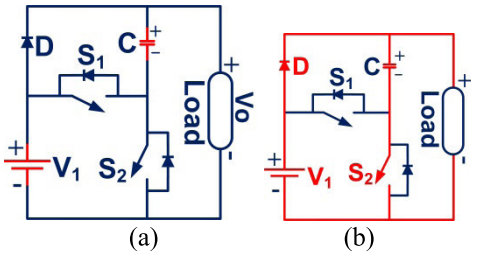

FIGURE 7. SCU (a) Basic SC unit: (b) Charging.

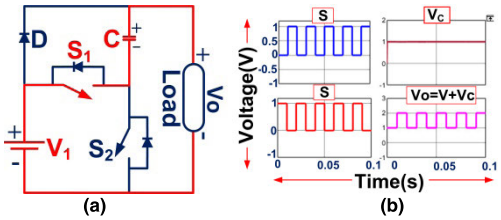

FIGURE 8. Capacitor in SC unit: (a) Discharging, (b) Simulation output.

in FIGURE 7(a) & FIGURE 8(a), under optimal conditions, during each half-cycle, the capacitor C is charged through S_2 switch during $V_0 = \pm Vc_1$.

The discharging of the capacitor C is started when the switch S_1 is in conduction at the front end of the proposed MLI topology. During the discharging period, the diode D and switch S_2 gets turned off. V_1 and V_{C1} supply energy to the load and the respective maximum load current is known where

$$V_0 = V_1 + V_{C1} \tag{10}$$

The discharging period can be used for obtaining the optimum value of SC for obtained ripple voltages. The simulation output waveform shown in FIGURE 8(b).

Let Q_C be the charge released by $C1$ during the period, then

$$Q_C = \int_{td1}^{td2} [I_0 sin\,(2\pi fst - \varphi)\,dt] \tag{11}$$

where $td1$, $td2$ is the period of discharging, $I0$ is maximum output current, fs is the fundamental frequency, and φ is the phase difference among the voltage and current. ΔVC is the ripple voltage and can be calculated using the angles computed using

$$\Delta VC = \frac{1}{2\pi fsC} \int_{\theta}^{\pi-\theta} I0 \sin(2\pi fst - \varphi) d\omega t \tag{12}$$

where θ is the angle where the capacitor discharges and $\pi\theta$ is the angle where the capacitor is discharging stops.

A. 17-LEVEL MLI

A 17-level MLI is designed with the two SC units connected in cascade with a smaller number of components is shown in FIGURE 9. The proposed MLI topology comprises 10 controlled switches with two asymmetric DC sources with the

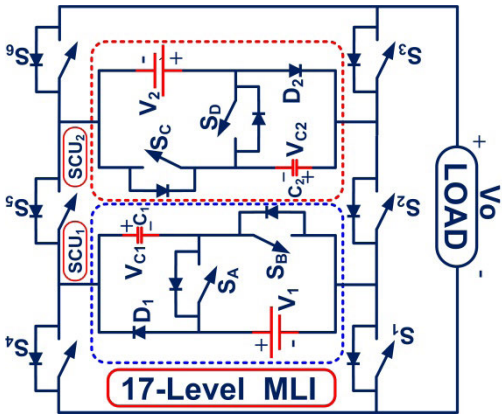

FIGURE 9. Developed structure of 17-level MLI.

absence of inductors. The two DC sources are of unequal voltage levels formed to be an asymmetrical configuration. Several power quality issues like total standing voltage (TSV), cost factor, and cost per unit with various values of the weight factor, THD, switch count, component count level, voltage stress is minimized with this MLI topology. This topology achieves less TSV and is compared with various topologies. The path of the load current through the switches, along with the states of the operation is represented in TABLE III. Few modes of operation, along with the switching pulses, is shown in FIGURE 10, and the expected output waveform is represented in FIGURE 11.

The developed 17-level MLI is operated in various modes of operation shown in TABLE III. In mode-1 operation of the circuit, the switches S_A, S_5, S_D, S_3, S_1 turn on forming a load current path, where V_1, V_{C1}, V_2, and V_{C2} sources act in the circuit and produce a voltage of 50V, 150V, 50V, 150V respectively to get a maximum voltage of 400V. The respective switching pulses, switching states, and current paths are represented in Table III. In mode-2 operation, the switches D_1, S_5, S_D, S_3, S_1 turn on where V_1, V_2, and V_{C2} sources act in the circuit and produce a voltage of 50V, 50V, and 150V respectively and get a voltage of $7V_{dc}$ which is equal to 350V. In mode-3 operation, the switches S_D, S_3, S_6, S_5 turn on forming a load current path where V_2, V_{C2} sources act in the circuit and produce a voltage of 50V and 150V respectively and get a voltage of $6V_{dc}$ equal to 300V. In mode-4 operation, the switches S_A, S_5, D_2, S_3, S_1 turn on with the voltages V_1, V_{C1}, and V_2 sources act in the circuit and produce a voltage of 50V, 150V, and 50V respectively and get a voltage of $5V_{dc}$ which is equal to 250V. In mode-5 operation, the switches D_1, S_5, D_2, S_3, S_1 turn on with the voltages V_1 and V_2 sources act in the circuit and produces a voltage of 50V and 150V respectively and get a voltage of $4V_{dc}$ equal to 200V. In mode-6 operation, the switches D_2, S_3, S_4, S_5, turn on with the voltage V_2 source act in the circuit and produce a voltage of 50V and get a voltage of $3V_{dc}$ which is equal to 150V. In mode-7 operation, the switches S_A, S_5, S_6, S_1, turn on with the voltages V_1 andV_{C1}

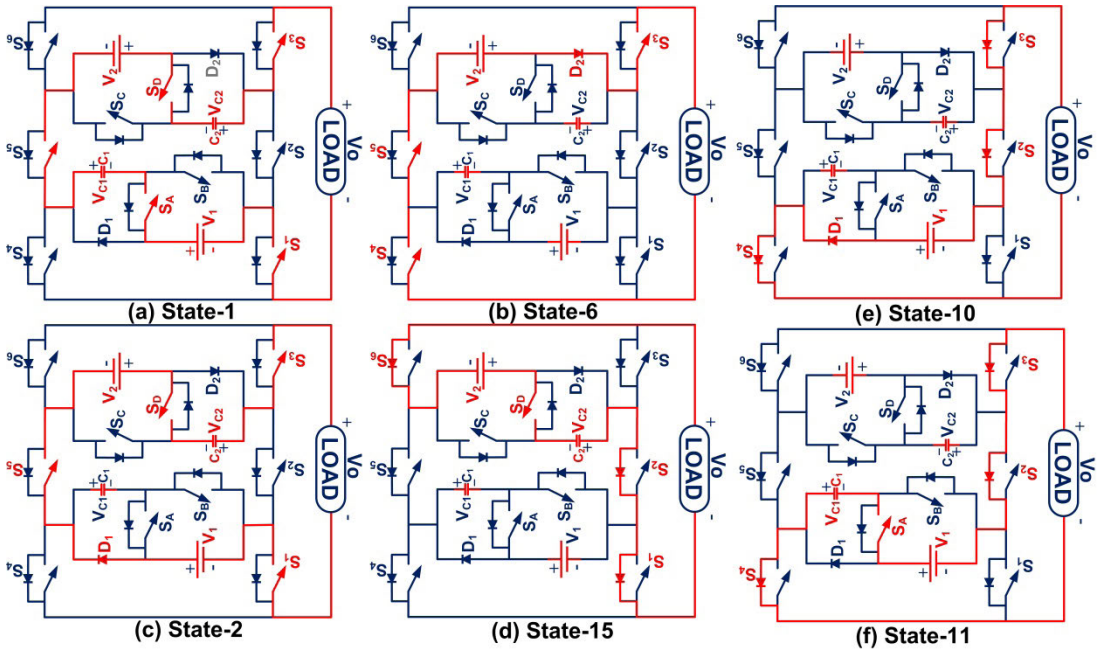

FIGURE 10. Modes of operation of the proposed 17-Level MLI topology.

sources act in the circuit and produces a voltage of 50V and 150V respectively and get a voltage of $2V_{dc}$ equal to 100V. In mode-8 operation, the switches D_1, S_5, S_6, S_1 turn on with the voltages V_1 source act in the circuit and produces a voltage of 50V respectively and get a voltage of V_{dc} which is equal to 50V. In mode-9 operation, the switches S_1, S_2, S_3, turn on with no voltages acts in the circuit and produces a voltage of 0V. Hence the positive cycle is created. The negative cycle is implemented with the negative modes of operation, along with the switching states shown in Table III. Therefore, the 17-level MLI output waveform is achieved with a simulation THD of 4.12% shown in FIGURE 14. The experimental THD is shown in Figure 21 is 4.12%, which is like that of simulation THD. The output waveform for output voltage and currents are shown in FIGURE 12, FIGURE 13, FIGURE 14, and FIGURE 15.

The experimental output voltage and output current are represented in FIGURE 16. The MLI is tested with R-load, and the obtained voltage and currents are 400V and 4A, respectively, and the result obtained is shown in FIGURE 17. For L-load, the experimental result is shown in FIGURE 18, where the voltage and currents are of 400V and 6.8A, respectively. For RL-load, the result is shown in FIGURE 19. For LR-load, the experimental result is shown in FIGURE 20. The complete experimental setup is shown in FIGURE 44. The experimental specifications used in implementing 17-level MLI are shown in Table VI.

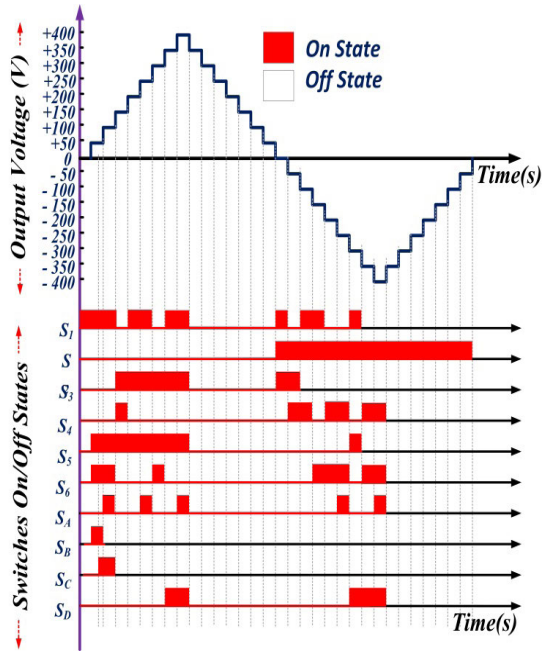

FIGURE 11. 17-Level expected output voltage waveform with switching pulses.

B. 33-LEVEL MLI

A 33-level MLI is designed with the combination of two 17-level MLI units connected with a smaller number of components is shown in FIGURE 22. The proposed MLI topology comprises 20 controlled switches with four asymmetric DC sources with the absence of inductors. The four DC sources are of unequal voltage levels formed to be an asymmetrical configuration. Several power quality issues like total standing voltage (TSV), cost factor, and cost per unit with various values of the weight factor, THD, switch count, component

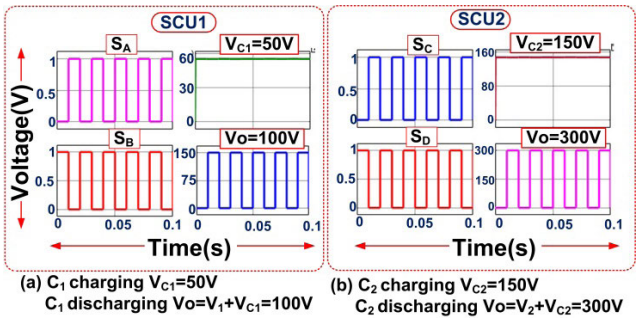

FIGURE 12. SCU Simulation output voltage waveforms of 17MLI.

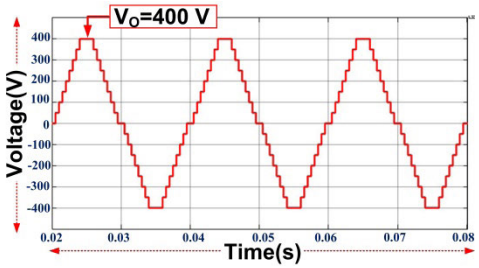

FIGURE 13. Simulation output voltage waveform of the 21-Level MLI.

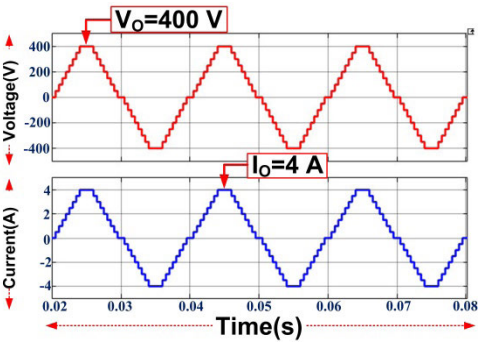

FIGURE 14. Simulation output voltage and current waveforms of the 17-Level MLI.

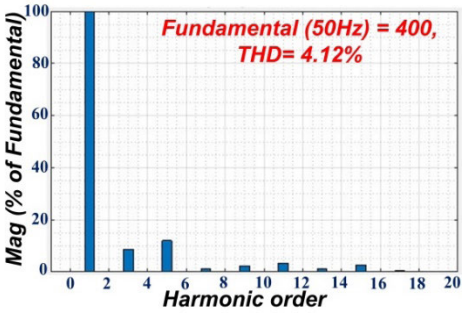

FIGURE 15. Simulation THD.

count level, voltage stress are minimized with this MLI topology. This topology achieves less TSV and is compared with various topologies. The path of the load current through the switches, along with the states of operation, are represented in

TABLE 3. Generation voltage levels according to Conduction of Switches of 17 MLI.

States	*Load current path*	*Output Voltage (V)*		
State-1	S_A, S_5, S_D, S_3, S_1	$8V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}$	+400
State-2	D_1, S_5, S_D, S_3, S_1	$7V_{dc}$	$V_1+V_2+V_{C2}$	+350
State-3	S_D, S_3, S_6, S_5	$6V_{dc}$	V_2+V_{C2}	+300
State-4	S_A, S_5, D_2, S_3, S_1	$5V_{dc}$	$V_1+V_{C1}+V_2$	+250
State-5	D_1, S_5, D_2, S_3, S_1	$4V_{dc}$	V_1+V_2	+200
State-6	D_2, S_3, S_4, S_5	$3V_{dc}$	V_2	+150
State-7	S_A, S_5, S_6, S_1	$2V_{dc}$	V_1+V_{C1}	+100
State-8	D_1, S_5, S_6, S_1	V_{dc}	V_1	+50
State-9	S_1, S_2, S_3	0	0	0
State-10	D_1, S_4, S_3, S_2	$-V_{dc}$	$-V_1$	-50
State-11	S_A, S_4, S_1, S_2	$-2V_{dc}$	$-(V_1+V_{C1})$	-100
State-12	D_2, S_2, S_1, S_6	$-3V_{dc}$	$-(V_2)$	-150
State-13	D_2, S_2, D_1, S_4, S_6	$-4V_{dc}$	$-(V_1+V_2)$	-200
State-14	D_2, S_2, S_A, S_4, S_6	$-5V_{dc}$	$-(V_1+V_{C1}+V_2)$	-250
State-15	S_D, S_2, S_1, S_5	$-6V_{dc}$	$-(V_2+V_{C2})$	-300
State-16	S_D, S_2, D_1, S_4, S_6	$-7V_{dc}$	$-(V_1+V_2+V_{C2})$	-350
State-17	S_D, S_2, S_A, S_4, S_6	$-8V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2})$	-400

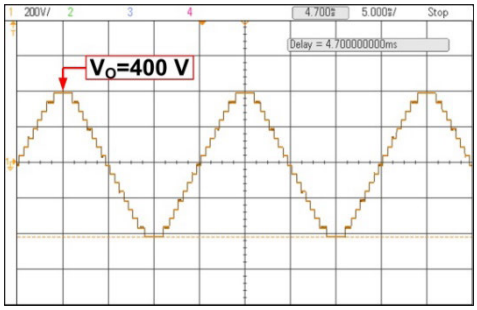

FIGURE 16. Experimental output waveform (Vo).

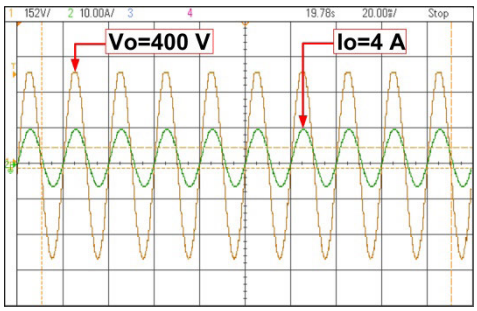

FIGURE 17. Experimental output waveform for R-load.

TABLE IV. Few modes of operation, along with the switching pulses, are shown in FIGURE 23.

The developed 33-level MLI is operated in various modes of operation shown in TABLE IV. In mode-1 operation of the circuit, the switches S_A, S_5, S_D, S_3, S_7, S_E, S_{11}, S_H, S_9, S_1 turn on forming a load current path, where V_1, V_{C1}, V_2, V_{C2}, V_3, V_{C3}, V_4, and V_{C4} sources act in the circuit and produce the voltages of 25V, 25V, 75V, 75V, 25V, 25V and75V respectively to get a maximum voltage of 400V. The respective switching pulses, switching states, and current paths are represented in Table IV. In mode-2 operation,

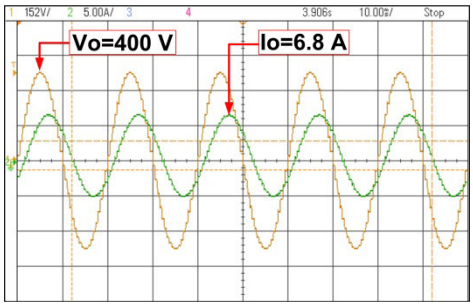

FIGURE 18. Experimental output waveform for L-load.

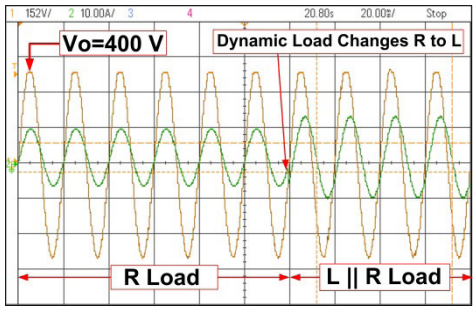

FIGURE 19. Experimental output waveform for R || L-load.

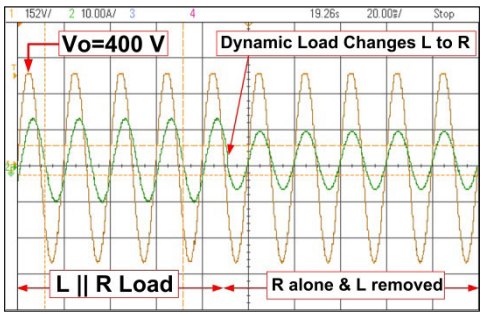

FIGURE 20. Experimental output waveform for L || R-load.

the switches D_1, S_5, S_D, S_3, S_7, S_E, S_{11}, S_H, S_9, S_1 turn on where V_1, V_2, V_{C2}, V_3, V_{C3}, V_4, and V_{C4} sources act in the circuit and produce the voltages of 25V, 75V, 75V, 25V, 25V and 75V respectively, and get a voltage of 15Vdc, which is equal to 375V. In mode-3 operation, the switches S_D, S_3, S_7, S_E, S_{11}, S_H, S_9, S_1, S_B, S_A, D_1, S_5 turn on forming a load current path where V_2, V_{C2}, V_3, V_{C3}, V_4, and V_{C4} sources act in the circuit and produce the voltages of 75V, 75V, 25V, 25V and 75V respectively and get a voltage of $14V_{dc}$ equal to 350V. In mode-4 operation, the switches S_D, S_3, S_7, D_3, S_{11}, S_H, S_9, S_1, S_B, S_A, D_1, S_5 turn on with the voltages V_2, V_{C2}, V_3, V_4, and V_{C4} sources acts in the circuit and produces a voltage of 75V, 75V, 25V, 75V and 75V respectively and get a voltage of $13V_{dc}$ which is equal to 325V. In mode-5 operation, the switches S_D, S_3, S_7, S_F, S_E, D_3, S_{11}, S_H, S_9, S_1, S_B, S_A, D_1, S_5 turn on with the voltages V_2, V_{C2}, V_4, and V_{C4} sources acts in the circuit and produces a voltage of 75V, 75V, 75V and 75V respectively and get a voltage of $12V_{dc}$ equal to 300V. In mode-6 operation, the switches S_A, S_5, S_D, S_3, S_7, S_F, S_E, D_3, S_{11}, D_4, S_9, S_1, turn on with the voltage V_1, V_{C1}, V_2, V_{C2}, and V_4 sources acts in the circuit and produce a voltage of 25V, 25V, 75V, 75V and 75V respectively and get a voltage of $11V_{dc}$ which is equal to 275V. In mode-7 operation, the switches D_1, S_5, S_D, S_3, S_7, S_F, S_E, D_3, S_{11}, S_4, S_9, S_1, turn on with the voltages V_1, V_2, V_{C2}, and V_4 sources acts in the circuit and produces a voltage of 25V, 75V, 75V and 75V respectively and get a voltage of $10V_{dc}$ which is equal to 250V. In mode-8 operation, the switches D_2, S_3, S_7, S_F, S_E, D_3, S_{11}, D_4, S_9, S_1, S_B, S_A, D_1, S_5 turn on with the voltages V_2, V_{C2}, and V_4 sources acts in the circuit and produces a voltage of 75V, 75V and 75V respectively and get a voltage of $9V_{dc}$ which is equal to 225V. In mode-9 operation, the switches S_A, S_5, S_D, S_3, S_7, S_8, S_9, S_1, turn on with the voltages V_1, V_{C1}, V_2, and V_{C2} acts in the circuit and produces a voltage of 25V, 25V, 75V, 75V respectively and get a voltage of $8V_{dc}$ equal to 200V. In mode-10 operation, the switches D_1, S_5, S_D, S_3, S_7, S_8, S_9, S_1, turn on with the voltages V_1, V_2, and V_{C2} acts in the circuit and produces a voltage of 25V, 75V and 75V respectively and get a voltage of $7V_{dc}$ which is equal to 175V. In mode-11 operation, the switches S_D, S_3, S_7, S_8, S_9, S_1, S_B, S_A, D_1, S_5, turn on with the voltages V_2 and V_{C2} acts in the circuit and produces a voltage of 75V and 75V respectively and get a voltage of $6V_{dc}$ equal to 150V. In mode-12 operation, the switches S_A, S_5, D_2, S_3, S_7, S_8, S_9, S_1 turn on with the voltages V_1, V_{C1} and V_2 acts in the circuit and produces a voltage of 25V, 25V and 75V respectively and get a voltage of $5V_{dc}$ which is equal to 125V. In mode-13 operation, the switches S_A, S_5, S_6, S_7, S_E, S_{11}, S_{12}, S_1 turn on with the voltages V_1, V_{C1}, V_3, and V_{C3} acts in the circuit and produces a voltage of 25V, 25V, 25V, and 25V respectively and get a voltage of $4V_{dc}$ which is equal to 100V. In mode-14 operation, the switches D_2, S_3, S_7, S_8, S_9, S_1, S_B, S_A, D_1, S_5 turn on with the voltages V_2 acts in the circuit and produces a voltage 75V and get a voltage of $3V_{dc}$ which is equal to 75V. In mode-15 operation, the switches S_A, S_5, S_6, S_7, S_8, S_9, S_1 turn on with the voltages V_1 and V_{C1} acts in the circuit and produces a voltage 25V and 25V respectively and get a voltage of $2V_{dc}$ equal to 50V. In mode-16 operation, the switches D_1, S_5, S_6, S_7, S_8, S_9, S_1 turn on with the voltages V_1 acts in the circuit and produces a voltage 25V and gets a voltage of V_{dc} which is equal to 25V. Hence the positive cycle is produced. The negative cycle is implemented with the negative modes of operation, along with the switching states shown in Table IV. Therefore, the 33-level MLI output waveform is achieved with a simulation THD of 2.54% shown in FIGURE 26. The experimental THD is shown in FIGURE 32 is 2.54%, which is like that of simulation THD. The output waveform for output voltage and currents are shown in FIGURE 24 and FIGURE 25. The MLI is tested with R-load, and the obtained voltage and currents are 400V and 4A, respectively, and the result obtained is shown in FIGURE 27 & FIGURE 28. For L-load, the experimental result is shown in FIGURE 29. Where

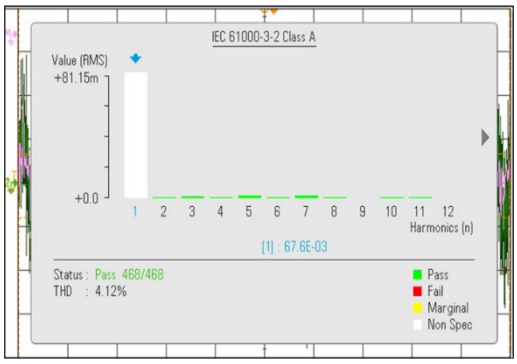

FIGURE 21. Experimental THD.

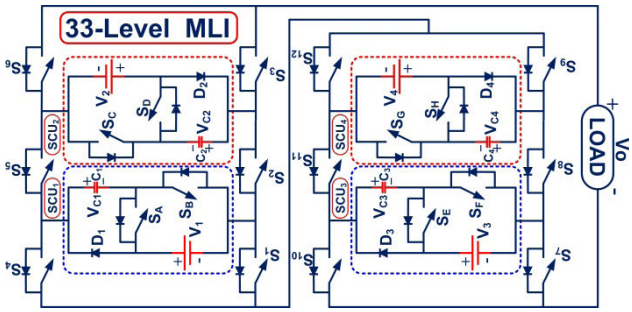

FIGURE 22. Developed structure of 33-level MLI.

the voltage and currents are 400V and 6.8A, respectively. For RL-load, the result is shown in FIGURE 30. For LR-load, the experimental result is shown in FIGURE 31. The complete experimental setup and specifications are shown in FIGURE 44 and Table V.

C. 53-LEVEL MLI

A 53-level MLI is designed with a combination of three SC units connected with a smaller number of components is shown in FIGURE 33. The proposed MLI topology comprises 14 controlled switches with three asymmetric DC sources with the absence of inductors. The three DC sources are of unequal voltage levels formed to be an asymmetrical configuration. Several power quality issues like total standing voltage (TSV), cost factor, and cost per unit with various values of the weight factor, THD, switch count, component count level, voltage stress is minimized with this MLI topology. This topology achieves less TSV and is compared with various topologies. The path of the load current through the switches along with the states of operation are represented in TABLE VI. Few modes of operation, along with the switching pulses are shown in FIGURE 34. The developed 53-level MLI is operated in various modes of operation shown in TABLE VI. In mode-1 operation of the circuit, the switches S_E, S_2, S_A, S_7, S_D, S_4, S_5 turns on forming a load current path, where V_1, V_{C1}, V_2, V_{C2}, V_3, and V_{C3} sources act in the circuit and produce the voltages of 15.4V, 15.4V, 46.2V, 46.2V, 138.6V, and 138.6V respectively to get a maximum voltage of 400.4V. The respective switching pulses, switching states and current paths are represented in Table V. In mode-2 operation of the circuit, the switches S_E, S_2, D_1, S_7, S_D, S_4, S_5 turn on forming a load current path, where V_1, V_2, V_{C2}, V_3, and V_{C3} sources act in the circuit and produce the voltages of 15.4V, 46.2V, 46.2V, 138.6V and 138.6V respectively to get a maximum voltage of 385V. In mode-3 operation of the circuit, the switches S_E, S_2, S_B, S_A, D_1, S_7, S_D, S_4, S_5 turn on forming a load current path, where V_2, V_{C2}, V_3, and V_{C3} sources act in the circuit and produce the voltages of 46.2V, 46.2V, 138.6V and 138.6V respectively to get a maximum voltage of 369.6V. In mode-4 operation of the circuit, the switches S_E, S_2, S_A, S_7, D_2, S_4, S_5 turn on forming a load current path, where V_1, V_{C1}, V_2, V_3, and V_{C3} sources act in the circuit and produce the voltages of 15.4V, 15.4V, 46.2V, 138.6V and 138.6V respectively to get a maximum voltage of 354.2V. In mode-5 operation of the circuit, the switches S_E, S_2, D_1, S_7, D_2, S_4, S_5 turn on forming a load current path, where V_1, V_2, V_3, and V_{C3} sources act in the circuit and produce the voltages of 15.4V, 46.2V, 138.6V and 138.6V respectively to get a maximum voltage of 338.8V. In mode-18 operation, the switches D_3, S_2, S_3, S_4, S_5 turn on where the V_3 source acts in the circuit and produces the voltages of 138.6V and gets a voltage of $9V_{dc}$ which is equal to 138.6V. In mode-28 operation, the switches D_1, S_6, S_5, S_4, S_3 turn on forming a load current path where the $-V_1$ source acts in the circuit and produces the voltage of -15.4V and gets a voltage of $-V_{dc}$ equal to -15.4V. In mode-53 operation, the switches S_D, S_3, S_A, S_6, S_E, S_1, S_8 turn on with the voltages V_1, V_{C1}, V_2, V_{C2}, V_3, and V_{C3} sources act in the circuit and produce a voltage of 15.4V, 15.4V, 46.2V, 46.2V, 138.6V, and 138.6V respectively and get a voltage of $26V_{dc}$ which is equal to 400.4V. Hence the positive cycle is produced. The negative cycle is implemented with the negative modes of operation, along with the switching states shown in Table VI. Therefore, the 53-level MLI output waveform is achieved with a simulation THD of 1.41% shown in FIGURE 37. The experimental THD is shown in FIGURE 43 is 1.41%, which is like that of simulation THD. The output waveform for output voltage and currents are shown in FIGURE 35 and FIGURE 36. The MLI is tested with R-load, and the obtained voltage and currents are 400V and 4A, respectively, and the result obtained is shown in FIGURE 38 & FIGURE 39. For L-load, the experimental result is shown in FIGURE 40. Where the voltage and currents are 400V, and 6.8A, respectively. For RL-load, the result is shown in FIGURE 41. For LR-load, the experimental result is shown in FIGURE 42. The complete experimental setup and specifications are shown in FIGURE 44 and Table V.

D. TOTAL STANDING VOLTAGE (TSV)

The total standing voltage (TSV) plays a significant role in the selection of switches in the circuit. It is the sum of all blocking voltages for the total number of semiconductor devices in the topology.

The voltage stresses on the bi-directional and unidirectional switches are given as $V_{Sbi} = V_i$ and $V_{Suni} = 2V_i$

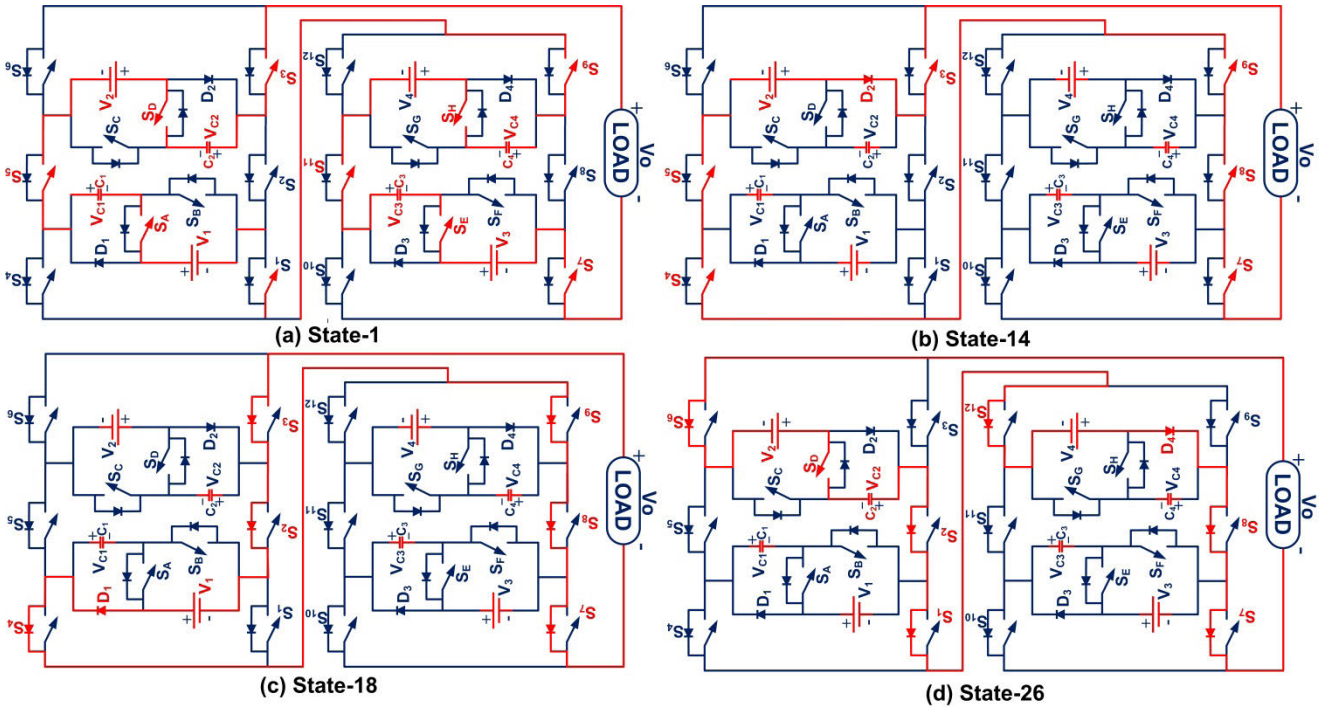

FIGURE 23. Modes of operation of the proposed 33-Level MLI topology.

TABLE 4. Generation voltage levels according to Conduction of Switches of 33 MLI.

States	*Load current path*	*Output Voltage (V)*		
State-1	S_A, S_5, S_D, S_3, S_7, S_E, S_{11}, S_H, S_9, S_1	$16V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}+V_3+V_{C3}+V_4+V_{C4}$	+400
State-2	D_1, S_5, S_D, S_3, S_7, S_E, S_{11}, S_H, S_9, S_1	$15V_{dc}$	$V_1+V_2+V_{C2}+V_3+V_{C3}+V_4+V_{C4}$	+375
State-3	S_D, S_3, S_7, S_E, S_{11}, S_H, S_9, S_1, S_B, S_A, D_1, S_5	$14V_{dc}$	$V_2+V_{C2}+V_3+V_{C3}+V_4+V_{C4}$	+350
State-4	S_D, S_3, S_7, D_3, S_{11}, S_H, S_9, S_1, S_B, S_A, D_1, S_5	$13V_{dc}$	$V_2+V_{C2}+V_3+V_4+V_{C4}$	+325
State-5	S_D, S_3, S_7, S_F, S_E, D_3, S_{11}, S_H, S_9, S_1, S_B, S_A, D_1, S_5	$12V_{dc}$	$V_2+V_{C2}+V_4+V_{C4}$	+300
State-6	S_A, S_5, S_D, S_3, S_7, S_F, S_E, D_3, S_{11}, D_4, S_9, S_1	$11V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}+V_4$	+275
State-7	D_1, S_5, S_D, S_3, S_7, S_F, S_E, D_3, S_{11}, S_4, S_9, S_1	$10V_{dc}$	$V_1+V_2+V_{C2}+V_4$	+250
State-8	D_2, S_3, S_7, S_F, S_E, D_3, S_{11}, D_4, S_9, S_1, S_B, S_A, D_1, S_5	$9V_{dc}$	$V_2+V_{C2}+V_4$	+225
State-9	S_A, S_5, S_D, S_3, S_7, S_8, S_9, S_1	$8V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}$	+200
State-10	D_1, S_5, S_D, S_3, S_7, S_8, S_9, S_1	$7V_{dc}$	$V_1+V_2+V_{C2}$	+175
State-11	S_D, S_3, S_7, S_8, S_9, S_1, S_B, S_A, D_1, S_5	$6V_{dc}$	V_2+V_{C2}	+150
State-12	S_A, S_5, D_2, S_3, S_7, S_8, S_9, S_1	$5V_{dc}$	$V_1+V_{C1}+V_2$	+125
State-13	S_A, S_5, S_6, S_7, S_E, S_{11}, S_{12}, S_1	$4V_{dc}$	$V_1+V_{C1}+V_3+V_{C3}$	+100
State-14	D_2, S_3, S_7, S_8, S_9, S_1, S_B, S_A, D_1, S_5	$3V_{dc}$	V_2	+75
State-15	S_A, S_5, S_6, S_7, S_8, S_9, S_1	$2V_{dc}$	V_1+V_{C1}	+50
State-16	D_1, S_5, S_6, S_7, S_8, S_9, S_1	V_{dc}	V_1	+25
State-17	S_1, S_2, S_3, S_7, S_8, S_9	0	0	0
State-18	D_1, S_4, S_9, S_8, S_7, S_3, S_2, S_1	$-V_{dc}$	$-V_1$	-25
State-19	S_A, S_4, S_9, S_8, S_7, S_3, S_2, S_1	$-2V_{dc}$	$-(V_1+V_{C1})$	-50
State-20	D_2, S_2, S_1, S_9, S_8, S_7, S_6	$-3V_{dc}$	$-V_2$	-75
State-21	S_A, S_4, S_9, S_8, S_E, S_{10}, S_3, S_2	$-4V_{dc}$	$-(V_1+V_{C1}+V_3+V_{C3})$	-100
State-22	D_2, S_2, S_A, S_4, S_9, S_8, S_7, S_6	$-5V_{dc}$	$-(V_1+V_{C1}+V_2)$	-125
State-23	S_D, S_2, S_1, S_9, S_8, S_7, S_6	$-6V_{dc}$	$-(V_2+V_{C2})$	150
State-24	S_D, S_2, D_1, S_4, S_9, S_8, S_7, S_6	$-7V_{dc}$	$-(V_1+V_2+V_{C2})$	-175
State-25	S_D, S_2, S_A, S_4, S_9, S_8, S_7, S_6	$-8V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2})$	-200
State-26	S_D, S_2, S_1, S_{12}, D_4, S_8, S_7, S_6	-9Vdc	$-(V_2+V_{C2}+V_4)$	-225
State-27	S_D, S_4, D_1, S_4, S_{12}, D_4, S_8, S_7, S_6	-10Vdc	$-(V_1+V_2+V_{C2}+V_4)$	-250
State-28	S_D, S_2, S_A, S_4, S_{12}, D_4, S_8, S_7, S_6	$11V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2}+V_4)$	-275
State-29	S_D, S_2, S_1, S_{12}, S_H, S_8, S_7, S_6	$12V_{dc}$	$-(V_2+V_{C2}+V_4+V_{C4})$	-300
State-30	S_D, S_2, S_1, S_{12}, S_H, S_8, D_3, S_{10}, S_6	$13V_{dc}$	$-(V_2+V_{C2}+V_3+V_4+V_{C4})$	-325
State-31	S_D, S_2, S_1, S_{12}, S_H, S_8, S_E, S_{10}, S_6	$14V_{dc}$	$-(V_2+V_{C2}+V_3+V_{C3}+V_4+V_{C4})$	-350
State-32	S_D, S_2, D_1, S_4, S_{12}, S_H, S_8, S_E, S_{10}, S_6	$15V_{dc}$	$-(V_1+V_2+V_{C2}+V_3+V_{C3}+V_4+V_{C4})$	-375
State-33	S_D, S_2, S_A, S_4, S_{12}, S_H, S_8, S_E, S_{10}, S_6	$16V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2}+V_3+V_{C3}+V_4+V_{C4})$	-400

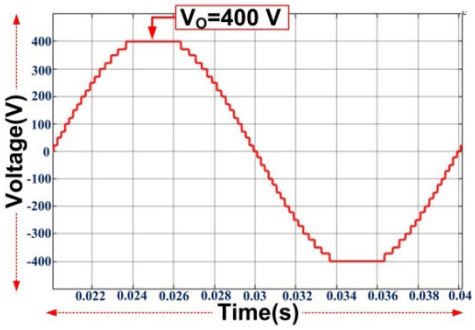

FIGURE 24. Simulation output voltage waveform of the 33-Level MLI.

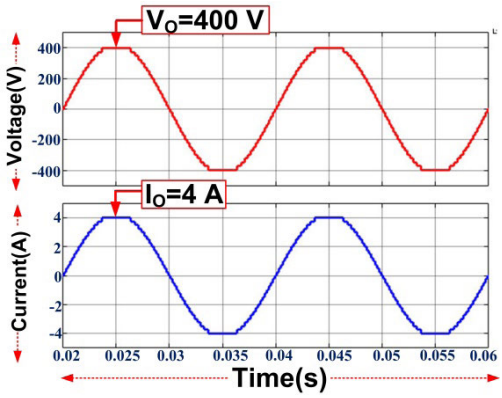

FIGURE 25. Simulation output voltage and current waveforms of the 33-Level MLI.

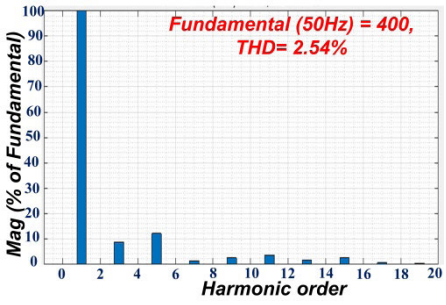

FIGURE 26. Simulation THD.

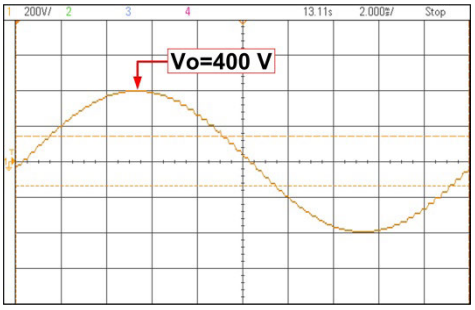

FIGURE 27. Experimental output waveform (Vo).

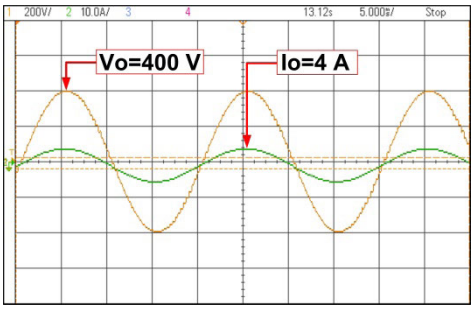

FIGURE 28. Experimental output waveform for R-load.

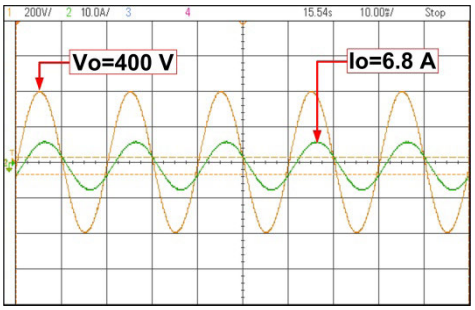

FIGURE 29. Experimental output waveform for L-load.

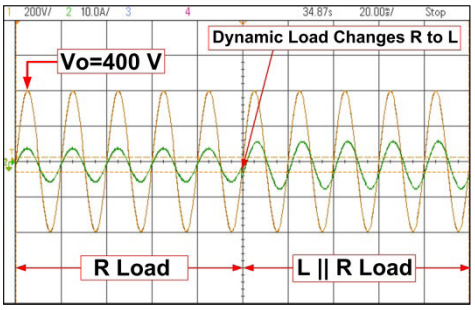

FIGURE 30. Experimental output waveform for R || L-load.

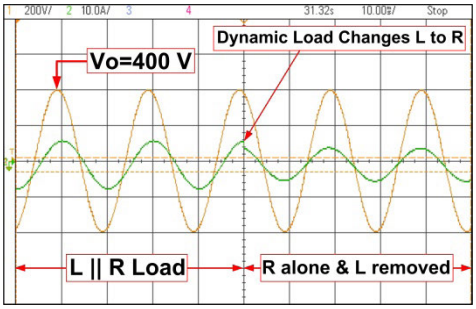

FIGURE 31. Experimental output waveform for L || R-load.

respectively, where i = 1, 2.....n, and n are complimentary switches count. The maximum output voltage (V_o) for the proposed topology is $V_{o,\,max} = 400V$. In the proposed MLI, the voltages are equal for complimentary switches, and all switches are unidirectional. Hence TSV is calculated using the following relation:

$$TSV = 2(V_{S1} + V_{S3} + \ldots\ldots\ldots\ldots V_{S(2n+1)}) \quad (13)$$

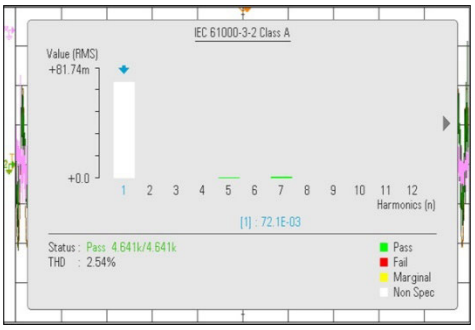

FIGURE 32. Experimental THD.

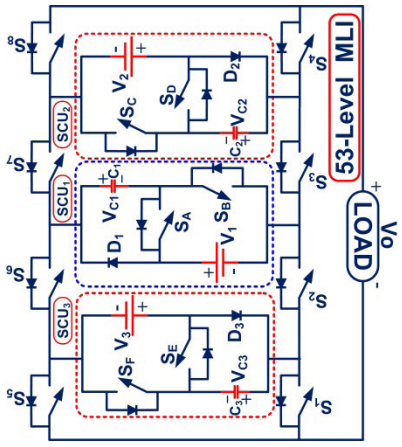

FIGURE 33. Proposed 53-Level MLI.

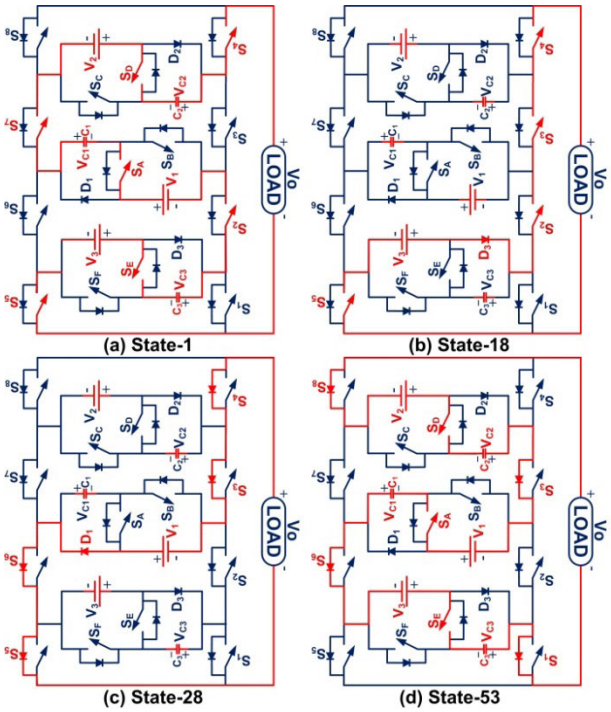

FIGURE 34. Modes of operation of the proposed 53-Level MLI topology.

For the developed 17-level MLI, TSV can be calculated based on the equation (7) and found to be $16V_{dc}$. Similarly, for the 33-level MLI and the proposed 53-level MLI, TSV is found to be $50V_{dc}$ and $30.8V_{dc}$, respectively.

TABLE 5. Specifications of 53-level MLI.

Output Voltage V_o	400V
Output current I_o	4A
dSPACE controller	RTI1104
Resistive load (Lamp)	100Ω
Inductive load	98Mh
IGBT	IGBT CM75DU-12, 600V, 75A
Motor load	Single-phase, 230V, 0.5HP

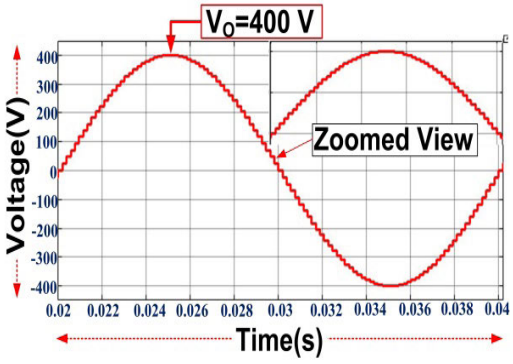

FIGURE 35. Simulation output voltage waveform of the 53-Level MLI.

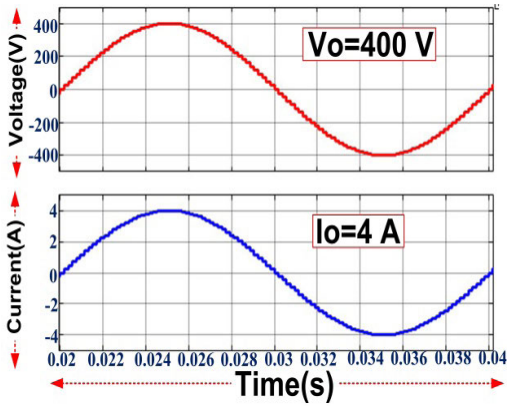

FIGURE 36. Simulation output voltage and current waveforms of the 53-Level MLI.

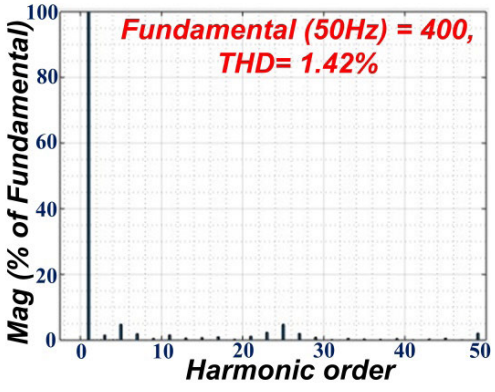

FIGURE 37. Simulation THD.

E. COST FUNCTION

The cost factor for the proposed 53-level MLI can be calculated using the parameters like several switch counts, source

TABLE 6. Generation voltage levels according to Conduction of Switches of 53 MLI.

States	Load current path	Output Voltage (V)		
State-1	S_E, S_2, S_A, S_7, S_D, S_4, S_5	$26V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}+V_3+V_{C3}$	400.4
State-2	S_E, S_2, D_1, S_7, S_D, S_4, S_5	$25V_{dc}$	$V_1+V_2+V_{C2}+V_3+V_{C3}$	385
State-3	S_E, S_2, S_B, S_A, D_1, S_7, S_D, S_4, S_5	$24V_{dc}$	$V_2+V_{C2}+V_3+V_{C3}$	369.6
State-4	S_E, S_2, S_A, S_7, D_2, S_4, S_5	$23V_{dc}$	$V_1+V_{C1}+V_2+V_3+V_{C3}$	354.2
State-5	S_E, S_2, D_1, S_7, D_2, S_4, S_5	$22V_{dc}$	$V_1+V_2+V_3+V_{C3}$	338.8
State-6	S_E, S_2, S_B, S_A, D_1, S_7, D_2, S_4, S_5	$21V_{dc}$	$V_2+V_3+V_{C3}$	323.4
State-7	S_E, S_2,S_A, S_7, S_8, S_5	$20V_{dc}$	$V_1+V_{C1}+V_3+V_{C3}$	308
State-8	S_E, S_2, D_1, S_7, S_8, S_5	$19V_{dc}$	$V_1+V_3+V_{C3}$	292.6
State-9	S_E, S_2, S_3, S_4, S_5	$18V_{dc}$	V_3+V_{C3}	277.2
State-10	D_3, S_2, S_A, S_7, S_D, S_4, S_5	$17V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}+V_3$	261.8
State-11	D_3, S_2, D_1, S_7, S_D, S_4, S_5	$16V_{dc}$	$V_1+V_2+V_{C2}+V_3$	246.4
State-12	D_3, S_2, S_B, S_A, D_1, S_7, S_D, S_4, S_5	$15V_{dc}$	$V_2+V_{C2}+V_3$	231
State-13	D_3, S_2, S_A, S_7, D_2, S_4, S_5	$14V_{dc}$	$V_1+V_{C1}+V_2+V_3$	215.6
State-14	D_3, S_2, D_1, S_7, D_2, S_4, S_5	$13V_{dc}$	$V_1+V_2+V_3$	200.2
State-15	D_3, S_2, S_B, S_A, D_1, S_7, D_2, S_4, S_5	$12V_{dc}$	V_2+V_3	184.8
State-16	D_3, S_2, S_A, S_7, S_8, S_5	$11V_{dc}$	$V_1+V_{C1}+V_3$	169.4
State-17	D_3, S_2, D_1, S_7, S_8, S_5	$10V_{dc}$	V_1+V_3	154
State-18	D_3, S_2, S_3, S_4, S_5	$9V_{dc}$	V_3	138.6
State-19	S_A, S_7, S_D, S_4, S_1, S_2	$8V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}$	123.2
State-20	D_1, S_7, S_D, S_4, S_1, S_2	$7V_{dc}$	$V_1+V_2+V_{C2}$	107.8
State-21	S_D, S_4, S_5, S_6, S_7	$6V_{dc}$	V_2+V_{C2}	92.4
State-22	S_A, S_7, D_2, S_4, S_1, S_2	$5V_{dc}$	$V_1+V_{C1}+V_2$	77
State-23	D_1, S_7, D_2, S_4, S_1, S_2	$4V_{dc}$	V_1+V_2	61.6
State-24	D_2, S_4, S_5, S_6, S_7	$3V_{dc}$	V_2	46.2
State-25	S_A, S_7, S_8, S_1, S_2	$2V_{dc}$	V_1+V_{C1}	30.8
State-26	D_1, S_7, S_8, S_1, S_2	V_{dc}	V_1	15.4
State-27	S_1, S_2, S_2, S_4	0	0	0
State-28	D_1, S_6, S_5, S_4, S_3	$-V_{dc}$	$-V_1$	-15.4
State-29	S_A, S_6, S_5, S_4, S_3	$-2V_{dc}$	$-(V_1+V_{C1})$	-30.8
State-30	D_2, S_3, S_2, S_1, S_8	$-3V_{dc}$	$-(V_2)$	-46.2
State-31	D_2, S_3, D_1, S_6, S_5, S_8	$-4V_{dc}$	$-(V_1+V_2)$	-61.6
State-32	D_2, S_3, S_A, S_6, S_5, S_8	$-5V_{dc}$	$-(V_1+V_{C1}+V_2)$	-77
State-33	S_D, S_4, S_5, S_6, S_7	$-6V_{dc}$	$-(V_2+V_{C2})$	-92.4
State-34	S_D, S_3, D_1, S_6, S_5, S_8	$-7V_{dc}$	$-(V_1+V_2+V_{C2})$	-107.8
State-35	S_D, S_3, S_A, S_6, S_5, S_8	$-8V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2})$	-123.2
State-36	S_3, S_1, S_8, S_7, S_6	-9Vdc	$-V_3$	-138.6
State-37	D_1, S_6, D_3, S_1, S_4, S_3	-10Vdc	$-(V_1+V_3)$	-154
State-38	S_A, S_6, D_3, S_1, S_4, S_3	$11V_{dc}$	$-(V_1+V_{C1}+V_3)$	-169.4
State-39	D_2, S_3, S_B, S_A, D_1, S_6, D_3, S_1, S_8	$12V_{dc}$	$-(V_2+V_3)$	-184.8
State-40	D_2, S_3, D_1, S_6, D_3, S_1, S_8	$13V_{dc}$	$-(V_1+V_2+V_3)$	-200.2
State-41	D_2, S_3, S_A, S_6, D_3, S_1, S_8	$14V_{dc}$	$-(V_1+V_{C1}+V_2+V_3)$	-215.6
State-42	S_D, S_3, S_B, S_A, D_1, S_6, D_3, S_1, S_8	$15V_{dc}$	$-(V_2+V_{C2}+V_3)$	-231
State-43	S_D, S_3, D_1, S_6, D_3, S_1, S_8	$16V_{dc}$	$-(V_1+V_2+V_{C2}+V_3)$	-246.4
State-44	S_D, S_3, S_A, S_6, D_3, S_1, S_8	$17V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2}+V_3)$	-261.8
State-45	S_E, S_1, S_8, S_7, S_6	$18V_{dc}$	$-(V_3+V_{C3})$	-277.2
State-46	D_1, S_6, S_E, S_1, S_4, S_3	$19V_{dc}$	$-(V_1+V_3+V_{C3})$	-292.6
State-47	S_A, S_6, S_E, S_1, S_4, S_3	$20V_{dc}$	$-(V_1+V_{C1}+V_3+V_{C3})$	-308
State-48	D_2, S_3, S_B, S_A, D_1, S_6, S_E, S_1, S_8	$21V_{dc}$	$-(V_2+V_3+V_{C3})$	-323.4
State-49	D_2, S_3, D_1, S_6, S_E, S_1, S_8	$22V_{dc}$	$-(V_1+V_2+V_3+V_{C3})$	-338.8
State-50	D_2, S_3, S_A, S_6, S_E, S_1, S_8	$23V_{dc}$	$-(V_1+V_{C1}+V_2+V_3+V_{C3})$	-354.2
State-51	S_D, S_3, S_B, S_A, D_1, S_6, S_E, S_1, S_8	$24V_{dc}$	$-(V_2+V_{C2}+V_3+V_{C3})$	-369.6
State-52	S_D, S_3, D_1, S_6, S_E, S_1, S_8	$25V_{dc}$	$-(V_1+V_2+V_{C2}+V_3+V_{C3})$	-385
State-53	S_D, S_3, S_A, S_6, S_E, S_1, S_8	$26V_{dc}$	$-(V_1+V_{C1}+V_2+V_{C2}+V_3+V_{C3})$	-400.4

count, total standing voltage, driver circuits count, and using the formula shown in equation (14) [37].

$$CF = (N_S + N_{dk} + N_d + N_c + \alpha TSV_{pu}) \times n \quad (14)$$

where CF is the cost factor, N_S is the number of switches, N_{dk} is the gate driver circuit count, N_d is the diodes count, N_c is the number of capacitors. TSV is the maximum standing voltage for the switches in conduction. TSV_{pu} is the total standing voltage per unit, which is given by

$$TSV(pu) = V_{TSV}/V_{omax} \quad (15)$$

where n is the DC sources count in the circuit. α is the weight coefficient which is multiplied with TSVpu. The inverter topology with the absence of diodes and capacitors can be neglected, and the cost function is calculated using the relation.

$$CF = (S + N_{dk} + \alpha TSV_{pu}) \times n \quad (16)$$

TABLE 7. Cost comparison of various multilevel inverters with proposed 17-Level MLI.

Components required		[39]	[40]	[41]	[42]	[43]	[44]	Proposed
Number of Switches (Ns)		16	14	10	20	10	20	10
Number of diodes (Nd)		16	20	10	20	12	20	12
Number of capacitors (Ncap)		4	4	0	0	0	0	2
DC sources (n)		4	8	4	8	2	8	2
Driver board circuits (Ndk)		14	14	10	20	10	20	10
Components count per level (Fccl)		3.17	3.52	2	4	2	4	1.53
Total Standing Voltage (TSV)		11	22	36	36	40	36	16
Total harmonic distortion (THD)		-	-	7.1	3.7	-	4.12	4.23
CF/N_{Lev}	α=0.5	3.5	4.17	4.94	5.05	5.18	4.97	2
	α=1.5	4.14	5.47	9.18	7.17	9.88	2.94	2.94

TABLE 8. Variance of various 33-Level MLI topologies.

Components required		NPC	FC	CHB	[45]	[46]	[47]	[48]	Proposed
Number of Switches (Ns)		64	64	20	18	21	79	20	20
Number of diodes (Nd)		32	0	20	18	32	0	20	4
Number of capacitors (Ncap)		32	0	16	6	16	15	0	4
DC sources (n)		32	32	5	1	1	1	8	4
Driver board circuits (Ndk)		64	64	20	18	21	79	20	20
Components count per level (Fccl)		6.78	4.84	2.12	1.84	2.75	5.27	2.06	1.57
Total Standing Voltage (TSV)		64	64	64	60	64	55	72	50
Total harmonic distortion (THD)		-	-	-	-	-	-	5.2	2.54
Cost Function/Levels (CF/L)	α=0.5	6.84	4.9	2.51	1.9	2.81	5.37	2.12	1.62
	α=1.5	6.96	5.0	2.63	2.0	2.93	5.45	2.26	1.71

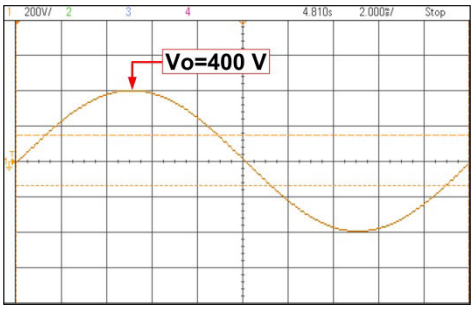

FIGURE 38. Experimental output waveform (Vo).

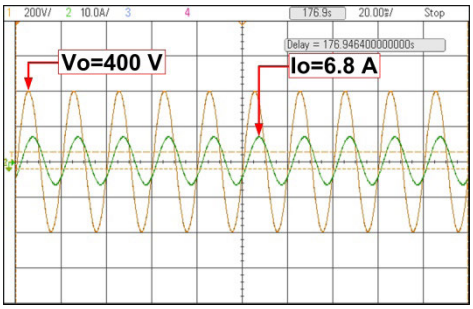

FIGURE 40. Experimental output waveform for L-load.

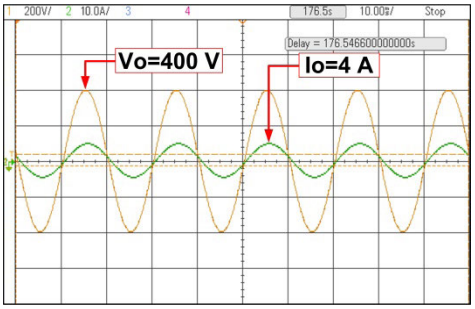

FIGURE 39. Experimental output waveform for R-load.

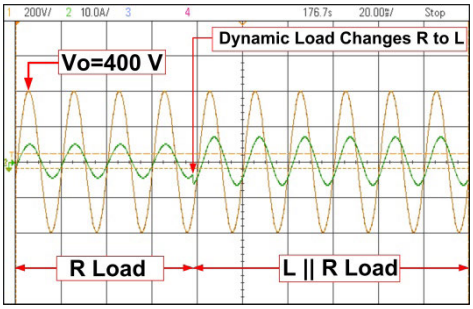

FIGURE 41. Experimental output waveform for R || L-load.

The value of α is to be considered in such a way that one value is greater than one, and the other is less than one. In this paper, the value of α is realized as 0.5 (<1), and the other value is 1.5 (>1) for the evaluation of the cost function. The cost-effectiveness of any MLI is calculated with level count (CF/L). This value is to be calculated for both values of α shown in TABLE VI. The cost function for the various developed MLIs is calculated based on the equation (14). For the developed 17-level MLI, 33-level MLI, and the proposed 53-level MLI, the cost function per level count is found to be 2.94, 1.62, and 0.65, respectively. The component count level factor represents the total number of semiconductor devices

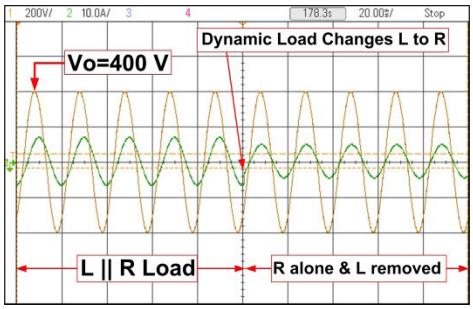

FIGURE 42. Experimental output waveform for L || R-load.

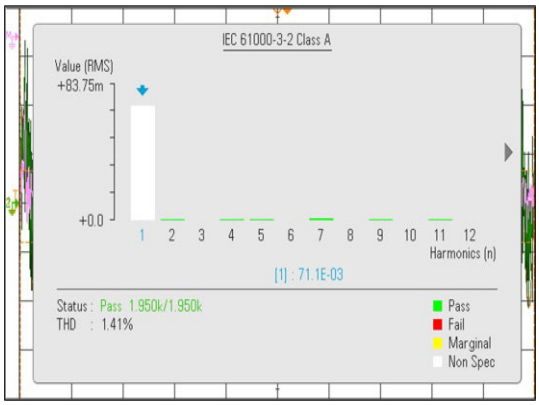

FIGURE 43. Experimental THD.

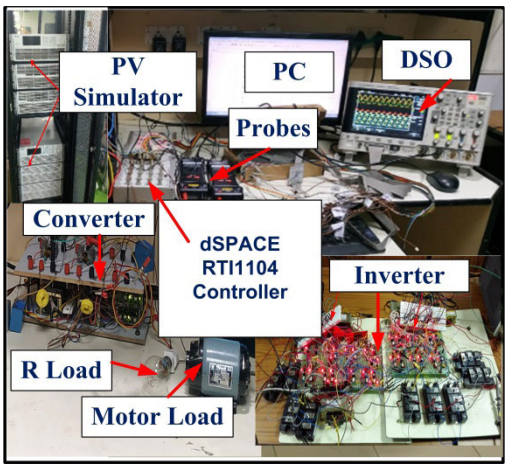

FIGURE 44. Experimental setup.

used in a circuit. The lesser the value, the fewer components are used, which provides fewer losses and more efficiency. The component count per level factor F_{ccl} is calculated using the following relation:

$$F_{ccl} = \frac{N_s + N_d + N_c + N_{dk} + n}{N_{Lev}} \tag{17}$$

The component count level factor for the developed 17-level MLI, 33-level MLI, and the proposed 53-level MLI is found to be 1.53, 1.57, and 0.69, respectively.

TABLE 9. Cost comparison of various multilevel inverters with proposed 53-Level MLI.

Components required		NPC	FC	CHB	[49]	[50]	Proposed
Number of levels N_L		53	53	53	49	42	53
Number of Switches (Ns)		104	104	32	12	12	14
Number of diodes (Nd)		52	0	0	0	0	3
Number of capacitors (Ncap)		52	52	8	4	3	3
DC sources (n)		52	52	8	2	3	3
Driver board circuits (Ndk)		104	104	32	12	12	14
Components count per level (Fccl)		6.86	5.88	1.5	0.61	0.66	0.69
Total Standing Voltage (TSV)		104	104	104	34	32	30
Total harmonic distortion (THD)		-	-	-	0.7	1.5	1.41
Cost Function/Levels (CF/L)	α=0.5	6.9	5.92	1.54	0.62	0.73	0.7
	α=1.5	6.98	6.0	1.62	0.65	0.76	0.73

F. POWER LOSS AND EFFICIENCY

The total losses are divided into conduction and switching losses related to switches. The conduction losses for the switches can be calculated using equation (18).

$$P_{Cls} = \left[V_S + R_S i^{\beta}(t)\right] i(t) \tag{18}$$

where V_S is the voltage drop of the IGBT switch, and V_d is the voltage drop of diodes. R_S is the equivalent resistance of the switch, R_d is the diodes equivalent-resistance. The generaliseded relation for finding conduction power losses (P_{cl}) considering the N_{IGBT} switches and N_d diodes at t instant of time is given in equation (12).

$$P_{Cl} = \frac{1}{2\pi}\int_0^{2\pi}\left[N_{IGBT}(t)\, P_{cl,IGBT}(t)\, dt\right] \tag{19}$$

The switching losses can be calculated from the equation (13)

$$P_{Sl} = f\sum_{K=1}^{N_{switch}}\left[\sum_{j=1}^{N_{on,k}} En_{on,kj} + \sum_{j=1}^{N_{off,k}} En_{off,kj}\right] \tag{20}$$

where Eon and Eoff are the energy used by the switches.

The total power losses ($P_{total\ loss}$) is calculated:

$$P_{total\ loss} = P_{cl} + P_{sl} \tag{21}$$

The efficiency (η) is calculated using the following relation:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{22}$$

where P_{out} and P_{in} are the output and input powers.

The output power can be estimated:

$$P_{out} = V_{rms} * I_{rms} \tag{23}$$

IV. COMPARISON STUDIES

The comparison can be done for the developed 17-level, 33-level, and proposed 53-level MLIs based on the various parameters listed below. In the designed 17-level MLI topology, it is noticed that it is cost-effective as compared with the different recent topologies for both values of α. The proposed MLI is compared with various current topologies considering essential parameters like the number of switches,

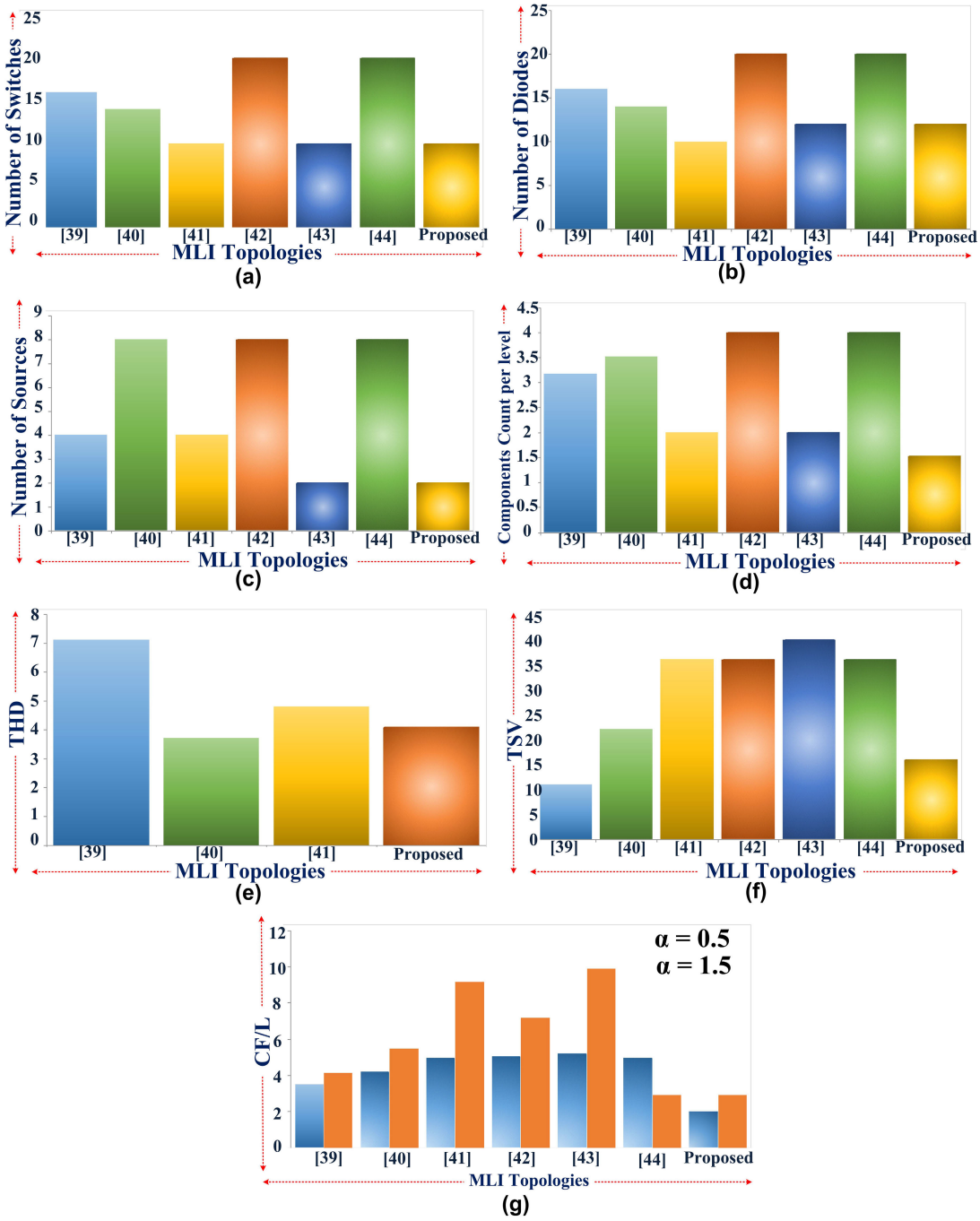

FIGURE 45. Comparison of various 17-Level MLI topologies (a) Switches count (b) Diodes count (c) DC sources count (d) Components count per level (e) THD (f) TSV (g) Cost function/Level count.

DC source count, gate driver circuits, Capacitor count, total standing voltage, component count per level in Table VII and graphically represented in FIGURE 45. FIGURE 45 (f) represents the comparison of full standing voltage and is less than the other topologies. FIGURE 45 (g) shows the comparison of the cost function for various topologies and found cost-effective. Also, the 33-level MLI is compared with the same parameters discussed above and represented in Table VIII and graphically represented in Figure 46. Figure 46 (i) Shows the comparison of the cost function for various topologies and found cost-effective. The proposed 53-level MLI is compared with multiple topologies are of different levels, and it is noticed that this topology is cost-effective as compared with the various recent topologies for both values of α. The proposed MLI is compared with multiple current topologies considering essential parameters like the number of switches,

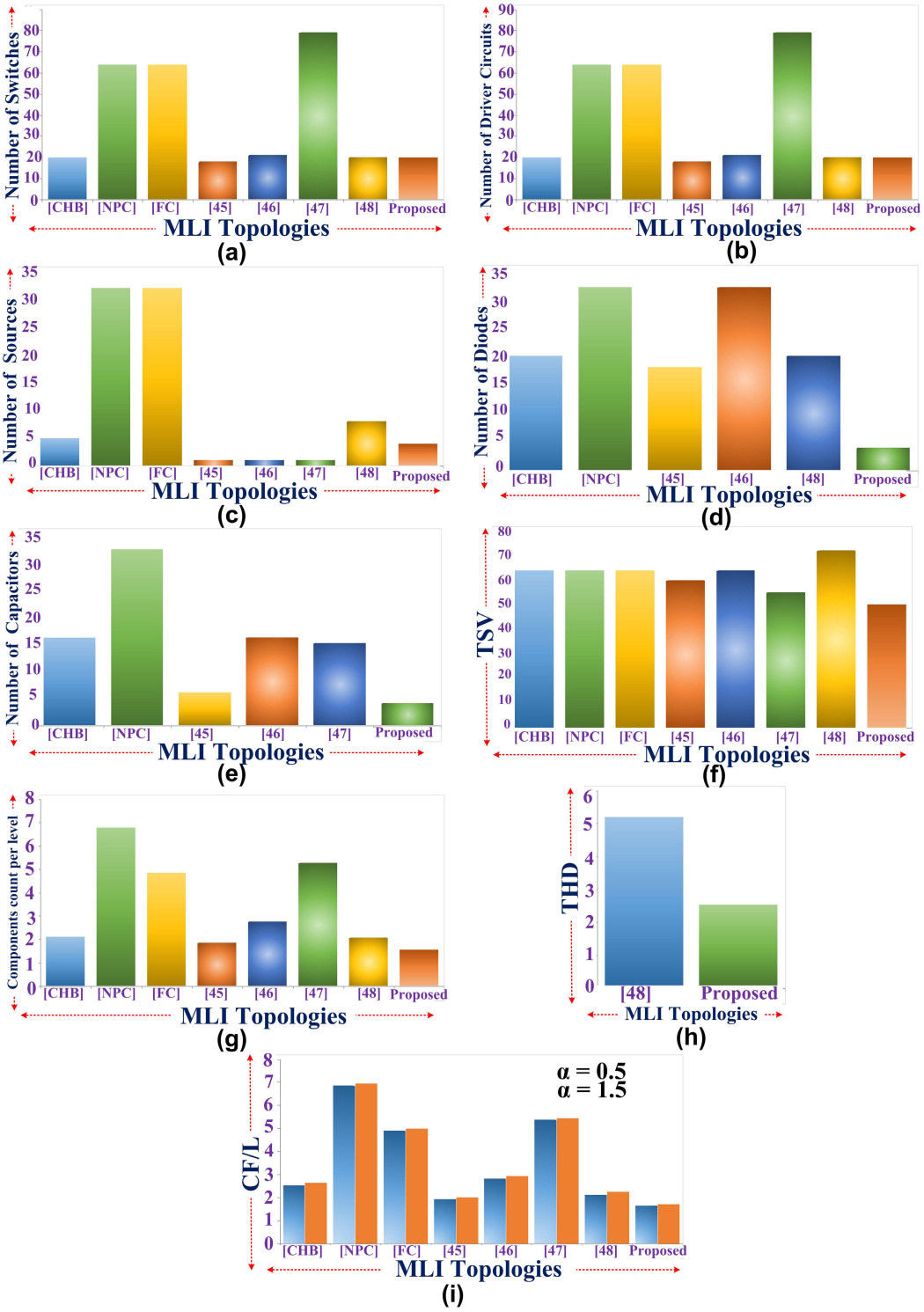

FIGURE 46. Comparison of various 33-Level MLI topologies. Switches count (b) Gate driver circuits count (c) DC sources count (d) Diodes count (e) Capacitors count (f) TSV (g) Components count per level (h) THD (i) Cost function/Level count.

DC source count, gate driver circuits, Capacitor count, and total standing voltage in TABLE IX and graphically represented in FIGURE 47, FIGURE 47 (d) represents the comparison of full standing voltage and is less than the other topologies. FIGURE 47 (i) shows the comparison of the cost function for various topologies and found cost-effective. The proposed MLI got better results in all parameters of comparison.

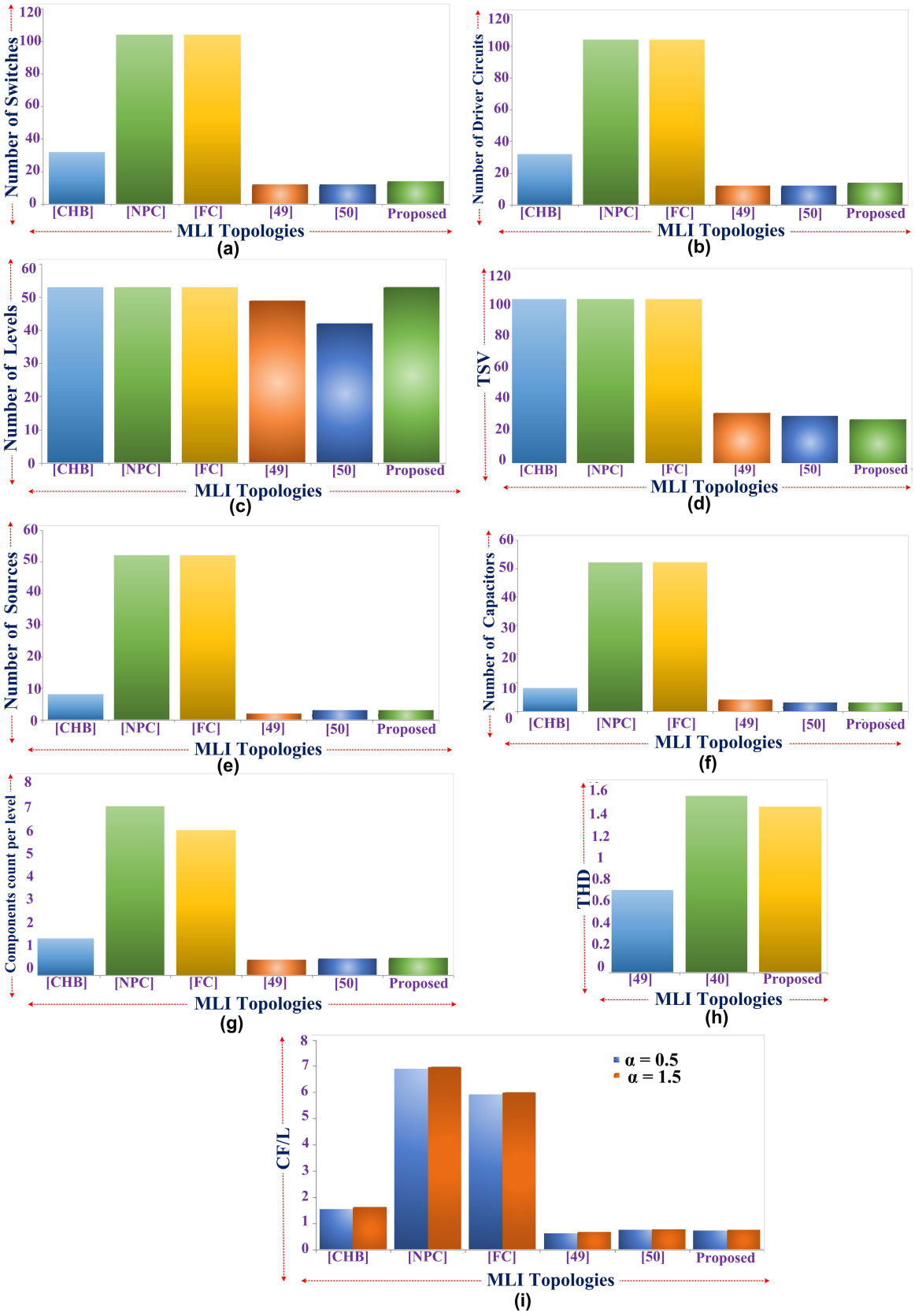

FIGURE 47. Comparison of various topologies of MLI with different levels with proposed 53-Level MLI Switches count (b) Gate driver circuits count (c) Number of levels (d) TSV (e) DC sources count (f) Capacitors count (g) Components count per level (h) THD (i) Cost function/Level count.

V. CONCLUSION

The proposed switched-capacitor based 53-level MLI topology for electric vehicle applications is designed and implemented for the solar PV energy system with lesser semiconductor devices to reduce the cost and size of the inverter, improving efficiency and reliability. P&O algorithm based MPPT technique is used, the stable output is achieved under all circumstances. The proposed MLI is implemented with various combinations of SC connections. A basic two units are cascaded and obtained a 17-level MLI configuration. The cascade connection of two 17-level MLIs results in the formation of a 33-level MLI, and the proposed 53-level MLI is achieved by cascading three SC units. All the MLIs are designed and compared with various topologies based on several parameters like devices count, TSV, THD, and cost function per level count. The comparative analysis shows that the proposed MLI is more efficient with fewer power losses. It is noticed that both simulation and experimental THD are 1.41%. TSV_{pu} is 1.15; efficiency is 94.21%, CF/L values for both values of α are 0.7 and 0.73, which clearly shows the cost is significantly less compared with various topologies. The proposed MLI is tested under multiple dynamic load variations. This topology is most suited for renewable energy applications.

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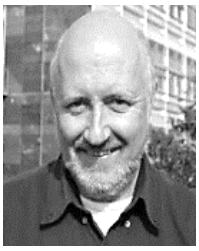
C. DHANAMJAYULU (Member, IEEE) received the B.Tech. degree in electronics and communication engineering from JNTU University, Hyderabad, India, the M.Tech. degree in control and instrumentation systems from the Indian Institute of Technology Madras, Chennai, India, and the Ph.D. degree in power electronics from the Vellore Institute of Technology, Vellore, India. He is currently a Postdoctoral Researcher with the Department of Energy Technology, Aalborg University, Esbjerg, Denmark. He is currently a Faculty Member and a member of the Control and Automation Department, School of Electrical Engineering, Vellore Institute of Technology. He is also a Senior Assistant Professor with the School of Electrical Engineering, Vellore Institute of Technology. Since 2010, he has been a Senior Assistant Professor with the Vellore Institute of Technology. He was invited as a Visiting Researcher with the Department of Energy Technology, Aalborg University, Esbjerg, Denmark, funded by the Danida Mobility Grant, Ministry of Foreign Affairs of Denmark on Denmark's International Development Cooperation. His research interests include multilevel inverters, power converters, active power filters, power quality, grid-connected systems, smart grid, electric vehicle, electric spring, and tuning of memory elements and controller parameters using soft-switching techniques for power converters, average modeling, steady-state modeling, and small-signal modeling stability analysis of the converters and inverters.

SANJEEVIKUMAR PADMANABAN (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Bologna, Bologna, Italy, in 2012. He was an Associate Professor with VIT University, from 2012 to 2013. In 2013, he joined the National Institute of Technology, India, as a Faculty Member. In 2014, he was invited as a Visiting Researcher with the Department of Electrical Engineering, Qatar University, Doha, Qatar, funded by the Qatar National Research Foundation (Government of Qatar). He continued his research activities with the Dublin Institute of Technology, Dublin, Ireland, in 2014. Further, he served an Associate Professor with the Department of Electrical and Electronics Engineering, University of Johannesburg, Johannesburg, South Africa, from 2016 to 2018. Since 2018, he has been a Faculty Member with the Department of Energy Technology, Aalborg University, Esbjerg, Denmark. He has authored more than 300 scientific papers. He was a recipient of the Best Paper cum Most Excellence Research Paper Award from IET-SEISCON'13, IET-CEAT'16, IEEE-EECSI'19, IEEE-CENCON'19, and five best paper awards from ETAEERE'16 sponsored Lecture Notes in Electrical Engineering, Springer book. He is a Fellow of the Institution of Engineers, India, the Institution of Electronics and Telecommunication Engineers, India, and the Institution of Engineering and Technology, U.K. He is an Editor/Associate Editor/Editorial Board for refereed journals, in particular the IEEE Systems Journal, IEEE Transaction on Industry Applications, IEEE Access, *IET Power Electronics*, *IET Electronics Letters,* and Wiley-*International Transactions on Electrical Energy Systems,* Subject Editorial Board Member – *Energy Sources – Energies Journal*, MDPI, and the Subject Editor for the *IET Renewable Power Generation*, *IET Generation, Transmission and Distribution*, and *FACTS* journal (Canada).

VIGNA K. RAMACHANDARAMURTHY (Senior Member, IEEE) received the bachelor's degree in electrical and electronics engineering from the Institute of Science and Technology, University of Manchester (UMIST), U.K., in 1998, under the Malaysian Government scholarship, and the Ph.D. degree in electrical engineering from the Institute of Science and Technology, The University of Manchester, U.K., in 2001. He is currently a Professor with the Institute of Power Engineering, Universiti Tenaga Nasional, Malaysia. He is also a Chartered Engineer registered with the Engineering Council of U.K., and a Professional Engineer registered with the Board of Engineers, Malaysia. He is also the Principal Consultant for Malaysia's most prominent electrical utility, Tenaga Nasional Berhad, and has completed over 250 projects in renewable energy. He has also developed several technical guidelines for distributed generation, Malaysia. He is also in the editorial board/associate editor of *IET Smart Grid, IET RPG*, the *IEEE Smart Grid*, and IEEE Access. His areas of interests include power systems related studies, renewable energy, energy storage; power quality, electric vehicle, and rural electrification. He joined the Malaysian electrical utility, Tenaga Nasional Berhad, in 2002, as an Electrical Engineer. In 2005, he moved to Universiti Tenaga Nasional (UNITEN) and presently a Professor with the Institute of Power Engineering. He has received many awards for research and leadership. In 2008, he received the 'Institution of Engineering and Technology (IET) Mike Sargeant Award' in London. The award is given to a young professional who is judged to have made significant achievements in career over several years globally. In 2009, he received the prestigious Institution of Engineers Malaysia (IEM) Young Engineers Award. He was also a recipient of the Best Researcher Award for few consecutive years in College of Engineering and UNITEN. He has also won several gold medals at International Invention Competition. His achievement has led to him being appointed as the Chief Judge at the National Schools Robotics Competition and at the World Young Inventors Exhibition with ITEX, a leading invention exhibition in Asia.



JENS BO HOLM-NIELSEN (Senior Member, IEEE) was born in 1954. He received the Ph.D. degree. He is currently the Head of the Research Group of Bioenergy and Green Engineering, Department of Energy Technology, Aalborg University, Denmark. He has 30 years of experience in biomass feedstock production, biorefinery concepts, and biogas production. He is a Board member of Research and Development, committees of the cross-governmental body of biogas developments from 1993–2009, Denmark. He is a Secretary and/or chair of NGO biogas and bio-energy organizations. He is a Chair and presenter of Sustainable and 100 per cent Renewables and SDG-17 goals. He has experience of a variety of EU projects, organizer of international conferences, workshops and training programs in EU, USA, Canada, China, Brazil, India, Iran, Russia, Ukraine, among others. His researches include managing research, development and demonstration programs in integrated agriculture, environment, and energy systems. He fulfilled the biomass and bio-energy Research and Development projects. His principle focuses on biofuels, biogas and biomass resources. EDU and Supervising M.Sc. and PhD students in these research fields. His training programs are International courses, training programs, and supervision for PhD students and academic staff, governmental bodies and experts in bio-energy systems. His full biography at www.aau.dk—profile search Jens Bo Holm-Nielsen.

FREDE BLAABJERG (Fellow, IEEE) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He received the Ph.D. degree in electrical engineering from Aalborg University, in 1995.

He became an Assistant Professor, in 1992, an Associate Professor, in 1996, and a Full Professor of power electronics and drives, in 1998. Since 2017, he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania, and Tallinn Technical University (TTU), Estonia. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal articles in the fields of power electronics and its applications. He is the coauthor of four monographs and editor of ten books in power electronics and its applications.

Dr. Blaabjerg has received 32 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019, and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE Transactions on Power Electronics, from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society, from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. From 2019 to 2020, he serves as a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences. He is nominated in 2014–2019 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world. In 2020, he received the prestigious IEEE Edison award for his extraordinary contribution to the next generation of reliable power electronics technologies with industry. In 2017, he became Honoris Causa at University Politehnica Timisoara (UPT), Romania.