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High Performance Flexible Structure Three-Level DC-DC Converter: A Candidate DC Interface for Microgrids With Distributed Energy Resources

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ABSTRACT High-performance DC interfaces play a pivotal role in microgrids with distributed energy resources (DERs), which would significantly improve the utilization of DERs and the flexibility of the prosumers. For a candidate DC interface converter, how to maintain the performance over a wide operation range becomes the biggest challenge. This paper proposes a flexible structure soft-switching three-level (TL) dc-dc converter, which adds four high-speed MOSFETs and one low-speed electronic relay to achieve overall optimum performance over a wide range. Under high output or low input voltage conditions, the relay and the extra MOSFETs on the primary side are ON permanently. The proposed converter is a zero-voltage switching (ZVS) converter, which guarantees ZVS for all primary switches even under 0 load currents. Under low output or high input voltage conditions, the relay and the extra MOSFETs in the secondary side are OFF permanently. The proposed converter is a zero-voltage and zero-current switching (ZVZCS) converter, and two added MOSFETs provide ZVZCS operation not only for the main primary switches but also themselves over a wide range. Other advantages of the presented converter include reduced filter size, no primary side circulating currents, and reduced current stress of the clamping capacitor. Besides, the switching loss caused by the added power devices is low because of the full range of soft-switching operation and low on-state resistance of these devices. This paper discusses the circuit configuration, operation principle, soft switching characteristics, technical comparison, and experimental results from a 1-kW prototype prove the rightness of the presented converter.

INDEX TERMS TL dc-dc converters, DC interface, distributed energy resources, microgrids, soft switching.

I. INTRODUCTION

Recently, high-level integration of distributed renewable energy resources (DERs) into the grids becomes an irreversible trend [1]–[4], which is a promising solution to environmental pollution and an alternative to burning fossil fuels for electric power generation [5]. In a microgrid with DERs, high-performance DC interfaces are necessary to improve the utilization of DERs and the flexibility of the prosumers [6]–[10]. To achieve minimized power transfer loss and high-power capacity, the DC voltage of these power systems should be increased as high as possible [11], [12]. Consequently, dc-dc converters sustain high DC link voltage with optimum operation features become urgent topics in power electronics society [13].

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For an ideal high voltage dc-dc converter, the preferred features are list as follows: compact primary circuit; the reduced current stress of the clamping components; high efficiency over a wide range; the reduced size of passive components, such as the input and output filters; even voltage and current stress distribution among the main switches and capacitors [10]–[13]. To date, several promising solutions for high voltage dc-dc conversion improve the performance of the DC interface in the applications of DERs [9]. Among them, the three-level (TL) dc-dc converter is an attractive choice because of some outstanding merits, e.g., the one-half voltage stress on the primary switches, compact clamping circuits, and soft-switching operation over a wide load range [11]–[14]. The hot issues in this topic include new topology for different applications, solutions to wide soft-switching load range, the reduced volume of passive components, new modulation strategies for better

performance [11]–[26]. Soft-switching cascaded TL combined dc-dc converter in [11] improves the reliability of high power and high input industrial applications because of the simple clamping circuit and good soft-switching characteristics. Reference [12] proposed a secondary modulation TL dc-dc converter, which merits the compact primary structure, wide soft-switching load range, and the reduced filter's size. Reference [13] addressed the common problems about some typical TL dc-dc converters and highlighted the virtues and drawbacks of these TL dc-dc converters. With interleaving control strategy, a new input-parallel output parallel TL dc-dc converter achieves minimizing and balancing capacitor ripple currents, which may improve the expected lifetime of the DC link capacitors [14]. Other new interleaved PWM methods in [15], [16] balance the voltage or current distributions in TL dc-dc converters. Reference [17] reported a high-efficiency TL dc-dc converter with reduced circulating current and rectifier voltage stress. Hybrid resonant zero-current-switching (ZCS) TL dc-dc converter in [18] is well suitable for applications in DERs at medium voltage level. In [19], the active cutting-off switches are moving out of the main power transfer loop, which ensures zero-voltage zero-current switching (ZVZCS) over a wide load range and reduced conduction loss. A new full-bridge TL dc-dc converter in [20] adopts a variable circuit structure, which can change the topology structure according to the operation condition. Furthermore, this converter can adjust the current stress of the primary circuit over a wide load range, which active stables the junction temperature of the main switches [21]. And then, lots of good researches are published [22]–[26], which makes the TL dc-dc converter more applicable.

However, improvements are still required. In [12], the secondary modulated capacitor clamped TL dc-dc converter adopts four primary switches that are utilized to generate TL secondary rectified waveforms, and this converter is a candidate circuit for the DC interface to microgrids with DERs. But, some inherent drawbacks limit the operating range of this converter. When the phase angle among the primary switches and the secondary switches is 180 degrees, the converter in [12] operates in the primary modulation mode. And then, several severe problems would arise, such as high circulating currents of the primary side, high current stress of the flying capacitor, the uneven current distribution of the primary components, and worse ZVS condition. Consequently, a new topology based on [12] with optimum performance over a wide range is an attractive challenge.

This paper proposes a flexible structure soft-switching TL dc-dc converter, which merits all features of the converter in [12]. Furthermore, the proposed converter overcomes the abovementioned drawbacks in [12], which is more suitable for the DC interface to microgrids with DERs. In the following parts, section II discusses the circuit configuration and operational principle, and section III addresses some technical issues. In part IV, experimental results from a 1-kW prototype evaluate the proposed converter, and some brief conclusions are in the last paragraph.

II. CIRCUIT AND OPERATION PRINCIPLE

Fig.1 shows the circuit configuration. On the primary side, S_1 to S_4 are the main primary switches, which are series-connected with one-half voltage stresses of the input voltage. C_{in1} and C_{in2} are the input capacitors. C_{fly} ensures balanced voltage distributions among S_1 to S_4. L_a is a resonant inductor parallel-connected with the primary coil of the transformer, which assists ZVS operation for S_1 and S_4 in the secondary side modulation mode. S_{p1} and S_{p2} are two added MOSFETs, which realize the ZVZCS operation for the main switches in the primary side modulation mode. As the source ports of S_{p1} and S_{p2} directly connect with that of S_2 or S_3, S_{p1} and S_{p2} need no added isolated driver power sources. In the secondary side modulation mode, these MOSFETs are ON permanently. R_1 is a low-speed relay, which determines the status of L_a. In this paper, R_1 consists of two anti-series connected MOSFETs. On the secondary side, D_{o1} to D_{o6} are rectifier diodes. S_{s1} and S_{s2} are secondary switches, which generate TL voltage waveforms before the LC filter. There are four secondary coils of the main transformer, and the turn ratios of the transformer are $k_T = {}_p/N_{s1} = N_p/N_{s2}$. L_o and C_o are the components of the output filter.

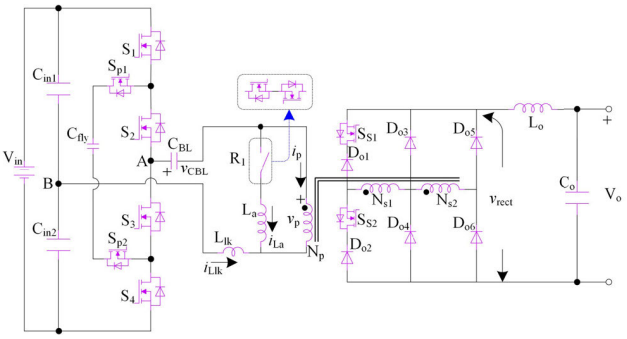

FIGURE 1. Flexible structure TL dc-dc converter.

Fig.2, Fig.3 and Table 1 show the switching schemes and core waveforms of the proposed converter. When S_{p1}, S_{p2}, and R_1 are ON permanently, the proposed converter is in the secondary side modulation mode. S_1 and S_2 are ON and OFF at the same time, while S_3 and S_4 are ON and OFF simultaneous. The phase angle between S_1 and S_3 is π. The phase angle between S_1 and S_{s1} vary V_o from V_{in}/k_T to $V_{in}/2k_T$. When S_{s1}, S_{s2}, and R_1 are OFF permanently, the proposed converter is in the primary side modulation mode. S_1 to S_4 switch in asymmetrical PWM (APWM) mode, and S_{p1} and S_{p2} switch as the scheme in Table 1. The simultaneous conducting time of S_1 and S_2 varies V_o from $V_{in}/2k_T$ to 0. In the primary modulation mode, S_{p1} and S_{p2} can obtain zero-voltage and zero-current switching (ZVZCS) over the entire load range, while in the secondary side modulation mode, S_{s1} and S_{s2} can achieve zero-current switching (ZCS) irrelevant to the load current. R_1 switches with very slow rate. Consequently,

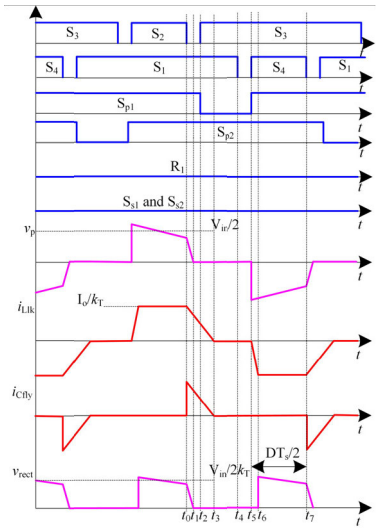

FIGURE 2. Core waveforms in the primary side modulation.

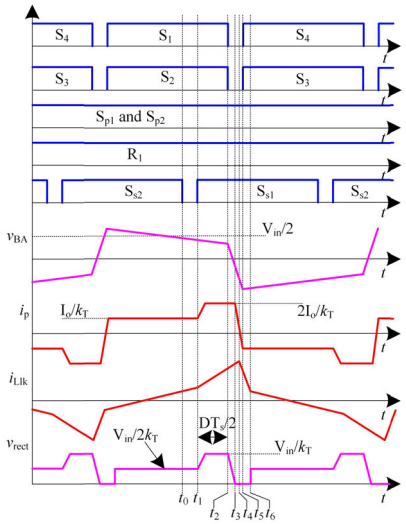

FIGURE 3. Core waveforms in the secondary side modulation.

TABLE 1. Switching schemes of the proposed converter.

Mode	Primary side modulation	Secondary side modulation
S_1 to S_4	APWM	Complementary
R_1	OFF	ON
S_{p1}	ON: at rising edge of S_4 OFF: at rising edge of S_3	ON
S_{p2}	ON: at rising edge of S_1 OFF: at rising edge of S_2	ON
S_{s1} and S_{s2}	OFF	Phase shift with S_1 to S_4

the added switching loss is small. Furthermore, the added conduction loss caused by S_{p1}, S_{p2}, S_{s1}, S_{s2}, and R_1 is also small because of low on-resistance.

In the analysis, the proposed converter operates under the following assumptions. All the components in the topology are ideal. The voltage ripple on C_{fly}, C_{in1} and C_{in2} is low. C_{BL} is designed with a specific value to assist the ZVZCS operation of the primary switches in the primary side modulation mode, and V_{CBL} is the max voltage of C_{BL}. I_o represents the output filter and load.

A. PRIMARY SIDE MODULATION

Fig. 2 shows the core waveforms of the primary side modulation mode, and the first seven sub-stages are in Fig.4. As depicted in Fig.2 and Table 1, R_1, S_{s1}, and S_{s2} are OFF.

Stage 1 [Fig.4 (a), before t_0]: The converter keeps in the stable state, and V_{in} powers the load. S_1, S_2, S_{p1}, and S_{p2} are on. D_{o3} and D_{o6} are on. i_{Llk} flows through S_1, S_2, the primary coil of the transformer, C_{in1}, C_{in2} and V_{in}. i_{Cfly} is zero, the current of S_{p1} and S_{p2} is zero. $v_{AB} = V_{in} - v_{Cin2}$, $v_{rect} = (V_{in} - v_{Cin2} - v_{CBL})/k_T$, $i_{Llk} = I_o/k_T$. i_{Llk} charges C_{BL} with the rate in (1).

$$\frac{dv_{CBL}}{dt} = \frac{I_o}{k_T C_{BL}} \tag{1}$$

Stage 2 [Fig.4 (b), t_0-t_1]: At t_0, S_2 is OFF, and the turn-off switching loss of S_2 is low because of the flat changing rate of v_{C2}. v_{CBL} keeps increasing and reaches its final value V_{CBL} at the end of this stage. i_{Llk} charges C_2 and discharges C_3 through C_{fly}. This stage continues until $v_{S2} = V_{in}/2$ and $v_{S3} = 0$.

Stage 3 [Fig.4 (c), $t_1 - t_2$]: At t_1, D_3 is conducted. The primary circuit is in the free-wheeling mode, and there is no power delivery from the input source to the secondary side. D_{o3} to D_{o6} are ON. S_3 should be gated on after t_1 to realize ZVS, and as shown in Fig.2, S_3 turns ON at t_2. The minus voltage between C_{BL} and C_{fly} is fully applied to L_{lk} to reset i_{Llk}, and this voltage is V_{CBL}. i_{Llk} is

$$i_{Llk}(t) = \frac{I_o}{k_T} - \frac{V_{CBL}}{L_{lk}}(t - t_1) \tag{2}$$

Stage 4 [Fig.4 (d), t_2-t_3]: At t_2, S_3 is switched on with zero voltage because D_3 conducts. S_{p1} turns off with zero-voltage because the anti-parallel diode of S_{p1} conducts naturally. i_{Llk} keeps decreasing. After i_{Llk} is zero, this stage is over, and the time is

$$T_{31} = \frac{I_o L_{lk}}{k_T V_{CBL}} \tag{3}$$

Stage 5 [Fig.4 (e), $t_3 - t_5$]: At t_3, i_{Llk} is zero. i_{Llk} cannot conduct in the reverse direction because of the one-way conductivity of the anti-parallel diode of S_{p1}. After t_3, i_{Llk} keeps zero, and S_1 can switch OFF with ZCS. According to Fig.2, S_1 turns OFF with ZCS at t_4, and Fig.4 (f) depicts the equivalent circuit. The voltage of C_{BL} keeps constant. The voltage on S_{p1} is V_{CBL}.

Stage 6 [Fig.4 (g), $t_5 - t_6$]: At t_5, S_4 and S_{p1} are on. S_3 achieves quasi ZCS because of the flat rate of i_{Llk}, and S_{p1} switches with ZCS because i_{Cfly} is 0. S_4 was on at t_2. i_{Llk} increases with a constant slope. The primary circuit keeps in the free-wheeling mode till i_{Llk} is I_o/k_T.

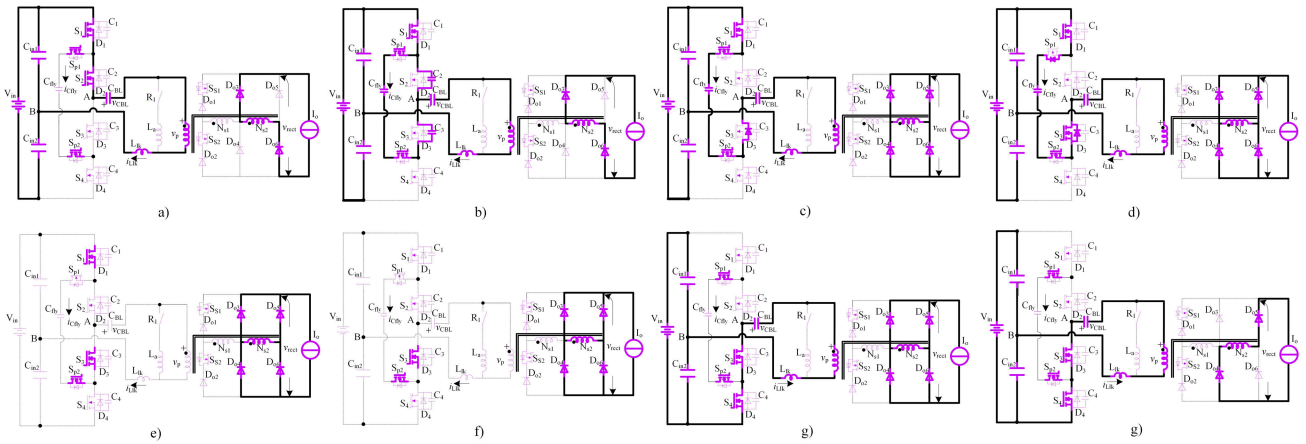

FIGURE 4. Power stages in the primary side modulation: a) stage 1; b) stage 2; c) stage 3; d) stage 4; e) stage 5; f) stage 6; g) stage 7; h) stage 8.

After t_6, i_{Llk} reaches to $-I_o/k_T$; the free-wheeling mode is over. The energy stored in C_{BL} powers the load. $v_{rect} = v_{Cin2}/k_T$; $i_{Llk} = -I_o/k_T$. As shown in Fig.4(h), the circuit is in the second half period after stage 6. A detailed analysis of the stages in the second half period is not provided in this paper for the sake of simplicity.

B. SECONDARY SIDE MODULATION

In the secondary side modulation mode, S_{p1}, S_{p2}, and R_1 are ON permanently, S_1 and S_2 switch ON and OFF at the same time, while S_3 and S_4 turn ON and OFF simultaneously. S_1 and S_4 gate ON and OFF with a constant phase angle π. The phase angle of S_{s1} and S_{s2} determines V_o. The core waveforms of the proposed converter in this mode are in Fig.3, which has a similar operation principle compared to that of [11]. Fig.5 shows the seven stages in the first half switching cycle, and detailed information of the operation principle can be referenced in [12].

III. TECHNICAL ANALYSIS

A. OUTPUT CHARACTERISTICS

1) PRIMARY SIDE MODULATION MODE

The ideal expression of V_o is

$$V_o = D\frac{V_{in}}{2k_T} \tag{4}$$

where V_{in} is the input voltage, k_T is the turn ratio of the transformer and D is the duty ratio. However, the real value of V_o is lower than that of (4) because of L_{lk}. In Fig.2, $[t_0, t_7]$ represents the interval of one-half switching period, and $[t_5, t_7]$ is the interval of the high voltage level defined as $DT_s/2$. During the interval of $[t_5, t_6]$, v_{rect} keeps zero because i_{Llk} is not identical to $-I_o/k_T$, which is the duty ratio loss. i_{Llk} is

$$i_{Llk} = -\frac{V_{in} + 2V_{CBL}}{2L_{lk}}\Delta t \tag{5}$$

At $t_5 i_{Llk} = 0$, and at t_6 $i_{Llk} = -I_o/k_T$. The time of $[t_5, t_6]$ is

$$\Delta t_{65} = \frac{2I_o L_{lk}}{(V_{in} + 2V_{CBL})k_T} \tag{6}$$

The duty ratio loss is

$$\Delta D = \frac{2\Delta t_{65}}{T_s} = \frac{2I_o L_{lk}}{T_s(V_{in} + 2V_{CBL})k_T} \tag{7}$$

V_o is

$$V_o = (D - \frac{2I_o L_{lk}}{T_s\,(V_{in} + 2V_{CBL})\,k_T})\frac{V_{in}}{2k_T} \tag{8}$$

2) SECONDARY SIDE MODULATION MODE

The ideal expression of V_o is

$$V_o = (1 + D)\frac{V_{in}}{k_T} \tag{9}$$

where V_{in} is the input voltage, k_T is the turn ratio of the transformer and D is the duty ratio. Just as the primary side modulation mode, V_o is low than that of (9) because v_{rect} is zero during the interval of $[t_5, t_6]$ in Fig.3. In this interval, i_{Llk} is

$$i_{Llk} = \frac{2I_o}{k_T} - \frac{V_{in} + 2V_{CBL}}{2L_{lk}}\Delta t \tag{10}$$

At t_5 $i_{Llk} = 2\ I_o/k_T$, and at t_6 $i_{Llk} = -I_o/k_T$. The time of $[t_5, t_6]$ is

$$\Delta t_{65} = \frac{6I_o L_{lk}}{(V_{in} + 2V_{CBL})k_T} \tag{11}$$

The duty ratio loss is

$$\Delta D = \frac{2\Delta t_{65}}{T_s} = \frac{12I_o L_{lk}}{T_s(V_{in} + 2V_{CBL})k_T} \tag{12}$$

V_o is

$$V_o = (D - \frac{12I_o L_{lk}}{T_s\,(V_{in} + 2V_{CBL})\,k_T})\frac{V_{in}}{2k_T} \tag{13}$$

B. SOFT SWITCHING IN THE PRIMARY SIDE MODULATION MODE

1) TRUN-ON INSTANTS OF S_1 AND S_3

S_1 and S_3 can obtain zero-voltage turn-on over a wide load range because the output inductance provides enough energy

FIGURE 5. Power stages in the secondary side modulation: a) stage 1; b) stage 2; c) stage 3; d) stage 4; e) stage 5; f) stage 6; g) stage 7.

to discharge or charge the output capacitors of the primary switches. For example, the turn-on instant of S_3 is in Fig.4 (b), and the ZVS condition of S_3 is [18]

$$I_{o,\min} = 2k_T V_{in}\sqrt{\frac{C_2 + C_3}{(L_{lk} + k_T^2 L_o)}} \tag{14}$$

2) TRUN-OFF INSTANTS OF S_1 AND S_3

In Fig.2, i_{Llk} drops to zero after S_2 or S_4 switches OFF for the time of T_{31} in (3). And then, S_1 or S_3 can turn OFF with ZCS. For instance, the turn-off instant of S_3 is in Fig.4(e), and the ZCS condition of S_1 is [18]

$$C_{BL} \le \frac{(T_s - 2T_{reset})T_{reset}}{2L_{lk}} \tag{15}$$

As suggested in (15), a small C_{BL} would generate a high primary reset voltage, which is better for the zero-current turn-off. However, it would induce high voltage stress on the rectifier diodes. Thus, there must be a trade-off between the ZCS load range and the voltage rating of the secondary rectifier diode.

3) TRUN-ON INSTANTS OF S_2 AND S_4

At the turn-on instant, S_2 and S_4 can achieve quasi ZCS because of L_{lk}. As the rising slope of i_{Llk} determines the turn-on power loss of S_2 and S_4, high L_{lk} or smaller driver resistance of S_2 and S_4 is preferred.

4) TRUN-OFF INSTANTS OF S_2 AND S_4

When S_2 or S_4 turns off, v_{S2} or v_{S4} increases slowly because the voltage across the output capacitors cannot change sharply. S_2 and S_4 achieve quasi zero-voltage turn-off, and high output capacitance can significantly reduce the turn-off power loss. Besides, high output capacitance does not affect the turn-on process of S_2 and S_4. Hence, S_2 and S_4 can optimize turn-on and turn-off power loss at the same time.

5) SOFT SWITCHING OF S_{P1} AND S_{P2}

As shown in Fig. 2, S_{p1} and S_{p2} generate no switching power loss. For example, when S_{p1} is OFF, its anti-parallel diode would conduct naturally. Hence, S_{p1} achieve ZVS. When S_{p1} is ON, it obtains ZCS because there is no current flowing through this device.

C. SOFT SWITCHING IN THE SECONDARY SIDE MODULATION MODE

1) TRUN-ON INSTANTS OF S_1 TO S_4

In the secondary side modulation mode, L_a helps the ZVS of S_1 to S_4. As S_1 to S_4 switches in the complementary mode, i_{La} is not in phase with i_p and increases the value of the input voltage. Hence, L_a provides more resonate energy to assist S_1 to S_4 achieving ZVS over the full load range. The ZVS condition is [12]

$$L_m \le \frac{T_s}{2}\sqrt{\frac{L_{lk}}{C_{os}}} \tag{16}$$

2) TRUN-OFF INSTANTS OF S_1 TO S_4

At turn-off instants, v_{S1} to v_{S4} rise slowly because of C_1 to C_4. Therefore, the turn-off power loss S_1 to S_4 is small.

3) SOFT SWITCHING OF S_{S1} TO S_{S2}

As shown in Fig.3, S_{s1} and S_{s2} can obtain ZCS over the full load range. For example, when S_{S1} is OFF, it turns off with ZCS because there is no current flowing through this device.

D. OUTPUT INDUCTANCE

The output inductance of the proposed converter is identical to that of [12], which is much small than that of conventional TL dc-dc converter because of the TL secondary rectified voltage waveform. According to [12], the output inductance of the presented converter is about one-third of that of conventional TL dc-dc converters. Therefore, the expected volume of the output filter in the proposed converter is small.

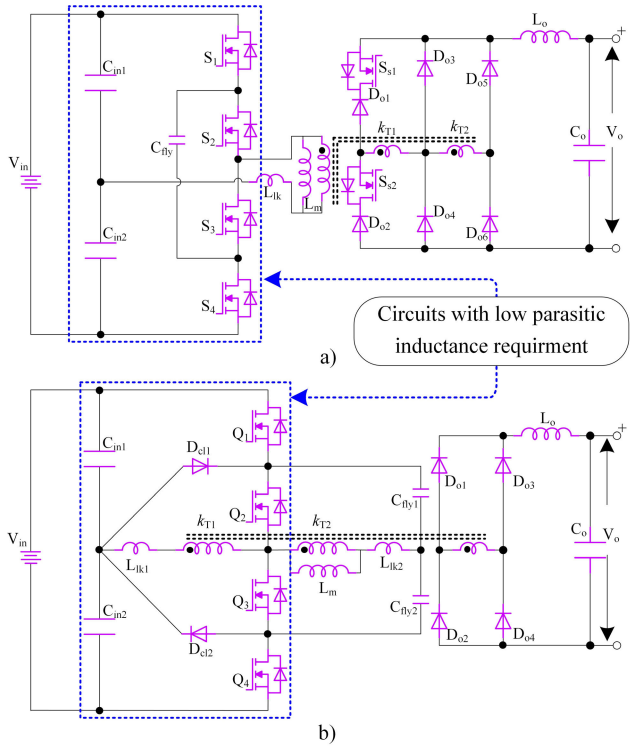

FIGURE 6. Circuit for comparison: 1) converter in [12]; 2) converter in [28].

IV. COMPARISON

In this part, a comparative study evaluates the proposed converter. The circuits for comparison are in Fig.6. Both the converters in Fig.6 are HB TL converter with variable turn ratios, which are also suitable for the applications that operate in a wide range of conditions.

A. SPECIFICATION FOR COMPARISON

The comparison is under the following assumptions: the input voltage is varied from 400V to 800V; the rated output voltage is 220V, and the rated output power is 1 kW; the switching frequency is 50-kHz.

B. COMPARISON INDICES

Normalized comparison indices in this paper help to provide a clear and valid performance quantification of the converters and Table 2 gives the reference values used in the comparison. In comparison, the reference values of the output parameters are the rated values. The input voltage is one-half of the rated input voltage, and the input current is I_o/k_T.

TABLE 2. Reference values used in the comparison.

Items	Value
Output voltage V_o	220V
Output current I_o	4.55A
Input voltage V_{in}	600V
Turn ratio k_T	1.36
Input current I_{in}	3.35A

1) RELATIVE VA VALUE OF THE PRIMARY SIDE

Relative primary side voltage stress is

$$\delta_{\mathrm{VA\_}pk} = \frac{\sum VA_{\mathrm{MAX\_}pk}}{V_{\mathrm{in}} I_{\mathrm{in}}} \tag{17}$$

where $\delta_{\mathrm{VA\_}pk}$ is comparison index, and $v_{\mathrm{MAX\_}pk}$ is the maximum VA of the kth primary component.

2) RELATIVE VA VALUE OF THE SECONDARY SIDE

Relative primary side average current is

$$\delta_{\mathrm{VA\_}pk} = \frac{\sum VA_{\mathrm{MAX\_}sk}}{V_{\mathrm{o}} I_{\mathrm{o}}} \tag{18}$$

where $\delta_{\mathrm{VA\_pk}}$ is comparison index, and $VA_{\mathrm{MAX\_sk}}$ is the maximum VA of the kth secondary component.

3) RELATIVE VOLTAGE STRESS

Relative voltage stress is

$$\delta_{\mathrm{V\_}k} = \frac{v_{\mathrm{MAX\_}k}}{V_{\mathrm{in}}} \tag{19}$$

where $\delta_{\mathrm{V\_}k}$ is comparison index, and $v_{\mathrm{MAX\_}k}$ is the maximum voltage stress of the kth component.

4) RELATIVE AVERAGE CURRENT STRESS

Relative average current stress is

$$\delta_{\mathrm{AI\_}k} = \frac{i_{\mathrm{MAX\_}k}}{I_{\mathrm{in}}} \tag{20}$$

where $\delta_{\mathrm{AI\_}k}$ is comparison index, and $i_{\mathrm{MAX\_}k}$ is the maximum average current of the kth component.

5) RELATIVE RMS CURRENT STRESS

Relative average current stress is

$$\delta_{\mathrm{IRMS\_}k} = \frac{i_{\mathrm{RMS\_}k}}{I_{\mathrm{in}}} \tag{21}$$

where $\delta_{I\mathrm{RMS\_}k}$ is comparison index, and $i_{\mathrm{RMS\_}k}$ is the maximum RMS current of the kth component.

6) RELATIVE CAPACITANCE

Relative capacitance is

$$\delta_{\mathrm{C\_}k} = \frac{C_k}{C_{\mathrm{iden}}} \tag{22}$$

where δ_{C_k} is comparison index, and C_k is the capacitance of the kth capacitor.

7) RELATIVE SOFT SWITCHING LOAD RANGE

Relative soft switching load range is

$$\delta_{\mathrm{LoadR\_}k} = \frac{1 - I_{\mathrm{min\_}k}}{I_o} \tag{23}$$

where $\delta_{\mathrm{LoadR\_}k}$ is comparison index, and $I_{\mathrm{min\_}k}$ is the minimum load of the kth component to achieve soft switching.

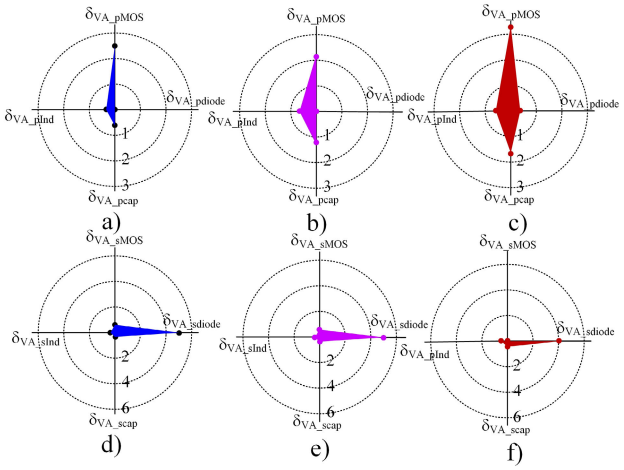

FIGURE 7. VA rating comparison: a) primary components, proposed; b) primary components, Fig.6 (a); c) primary components, Fig.6 (b); d) secondary components, proposed; e) secondary components, Fig.6 (a); f) secondary components, Fig.6 (b).

C. TOTAL VA RATING OF THE MAIN COMPONENTS

Fig.7 gives comparisons of the total VA rating. As shown in Fig.7 (a), δ_{VA_pMOS} of the proposed converter is a bit higher than that of Fig.6(b) because of four added MOSFETs. However, as the current rating of S_{p1}, S_{p2}, and R_1 is much small than the input rated current, the increments of the total VA rating are small. The converter in Fig. 6(c) has four primary MOSFETs, however as depicted in Fig.7 (c), the total VA rating of these devices is highest because S_2 and S_3 suffer high current stress.

All three converters have a resonate inductor, and the VA rating of L_a in the proposed converter is the lowest due to less current rating. As depicted in Fig.7 (a) to (d), the proposed converter has the minimum VA rating of the primary capacitor. As the high-value capacitors take high volume and shorten the overall life cycle, the proposed converter has strong competitiveness in power density and reliability. As mentioned in [26], a high current flow through clamping diodes of the converter in Fig. 6(b) during free-wheeling stages. And it is recommended to integrate the clamping diodes and the main switches into one power module by the producer to ensure safe operation. Although producers of power devices have provided some integrated diode clamped TL power modules, the voltage and current ratings, selected range, cost, and performance of these modules are still dissatisfied compared to widely used two-level HB power modules. Therefore, the proposed converter and the converter in Fig.6 (a) allow customers to achieve high input dc-dc power conversion by using cheap and high-performance two-level power modules without a reduction in reliability.

D. PRIMARY CAPACITORS

Fig.8 provides a detailed capacitor comparison, and the data of the proposed converter is calculated according to (19) to (22). The proposed converter features a reduced current rating of the primary capacitors. As proved in Fig.5, no current flows through C_{fly} in the secondary side modulation mode. And in Fig.4, the current of C_{fly} is lower because i_{Llk} drops to zero during the free-wheeling stages. Hence, the required current rating of C_{fly} in the proposed converter is smaller. The voltage rating of the flying capacitor in the proposed converter and the converters in Fig.6 (a) is identical, and the value is $0.5V_{in}$. The voltage rating of the two flying capacitors in Fig.6 (b) is 0.25 V_{in}. According to Fig.8, C_{fly} in the proposed converter has the smallest VA rating.

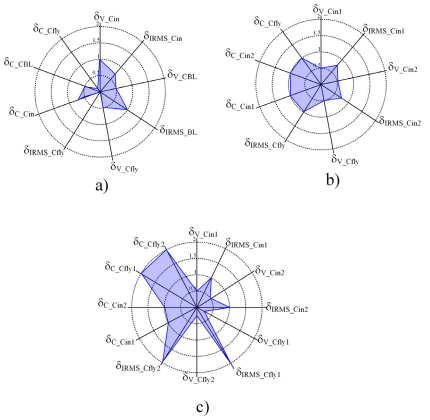

FIGURE 8. Comparison of the primary flying capacitor: a) proposed; b) Fig.6 (a); c) Fig.6 (b).

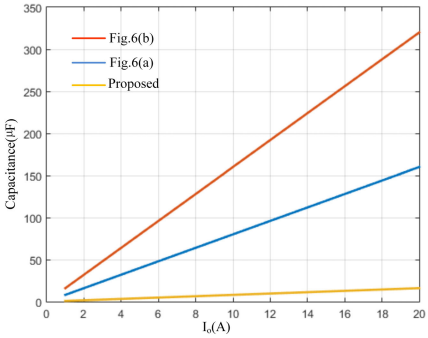

FIGURE 9. Comparison of the capacitance: a) proposed; b) Fig.6 (a); c) Fig.6 (b).

For safe operation, C_{fly} should have a small voltage ripple. The voltage ripple on the flying capacitor is

$$\Delta v_{Cfly} = \int_0^{T_s/2} i_{Cfly} dt \tag{24}$$

Fig.9 depicts the capacitance comparison of the flying capacitors in the three converters versus output current and the switching frequency. In the process of comparison, the voltage ripple on C_{fly} is 5V. I_o varies from 1 to 20A, and f_s is 50 kHz.

As shown in Fig.9, when the output current is 20A, the required capacitance of the flying capacitor in Fig.6 (a) is about 160μF with 50kHz switching frequency, while the

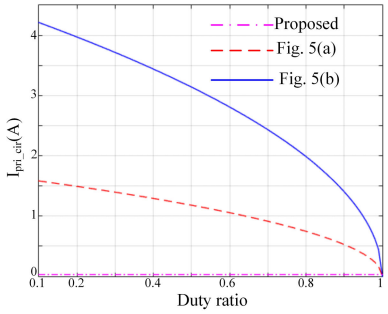

FIGURE 10. Primary circulating current vs. duty ratio.

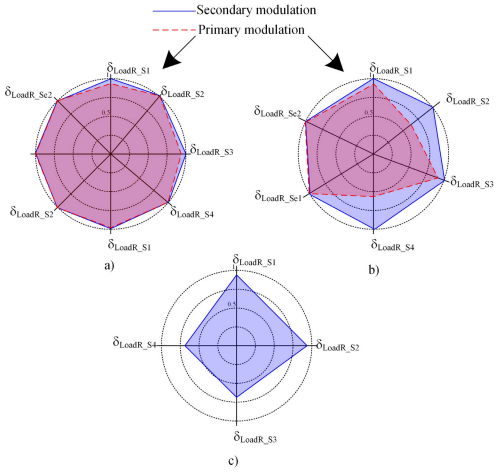

FIGURE 11. Soft-switching load range of the primary switches: a) proposed; b) Fig.6 (a); c) Fig.6 (b).

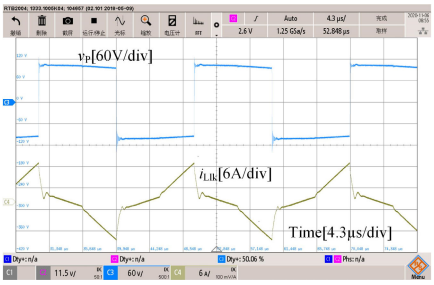

FIGURE 12. v_p and i_{Llk} in the secondary side modulation mode.

capacitance of the flying capacitors in Fig.6 (b) is about 350μF under the same condition. But, in the proposed converter, a film capacitor with smaller capacitance is enough, e.g., 10μF, due to no current flows through this capacitor in the both operation modes. Hence, the flying capacitor in the proposed converter has the smallest capacitance. The smallest capacitance of C_{fly} in the proposed converter mean the lowest volume of the flying capacitor. Furthermore, the smaller current stress of the flying capacitor means a longer operating lifetime, which is better for high-voltage dc-dc applications due to its pivotal role in maintaining the off-state voltage of the primary switches.

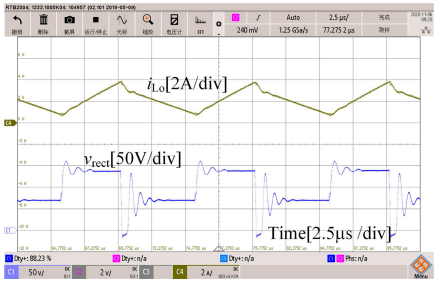

FIGURE 13. v_{rect} and i_{Lo} in the secondary side modulation mode.

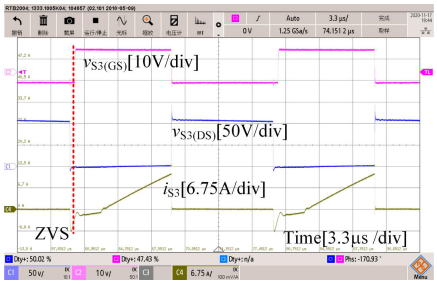

FIGURE 14. ZVS of S_3 in the secondary side modulation mode.

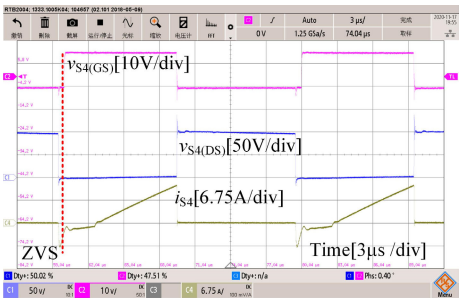

FIGURE 15. ZVS of S_4 in the secondary side modulation mode.

E. PRIMARY CIRCULATING CURRENT

The primary circulating current of the proposed converter is zero in the secondary side modulation modes. When the proposed converter is in the primary side modulation mode, the primary circulating current is also small because the primary current decreases to zero within a limited time. For the converter in Fig.6 (a), high primary circulating appears in the primary side modulation mode, and the converter in Fig.6 (b) suffer the largest primary circulation current with small duty ratio among the three converters.

F. SOFT SWITCHING LOAD RANGE

Fig.11 gives the load range comparison of the soft-switching operation. The soft switching load range of the proposed converter is calculated according to (14) and (15), and corresponding soft switching load ranges of the converters in Fig.6 are predicted by references [12] and [28]. In Fig.11(a), the switches in the proposed converter obtain soft-switching over nearly the entire load range, and the

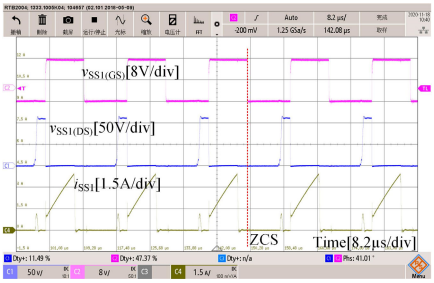

FIGURE 16. ZCS of S_{S1} in the secondary side modulation mode.

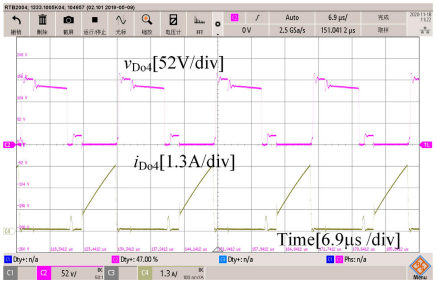

FIGURE 17. v_{DO4} and i_{Do4} in the secondary side modulation mode.

expected efficiency is high. As suggested in Fig.11 (b), the converter in Fig.6 (a) has a wide soft-switching load range in the secondary side modulation mode. And, when the converter in Fig.6(a) operates in the primary side modulation mode, some switches face more obstacles to achieve ZVS. Hence, the efficiency of the converter in Fig.6(a) will be low in the primary side modulation mode. As shown in Fig.6 (c), the converter in Fig.6(b) has the narrowest soft-switching load range because some switches cannot achieve enough energy to charge or discharge their output capacitance. It is emphasized that the duty ratio loss of the proposed converter and the converter in Fig.6 (a) is small than that of Fig.6 (b), which can optimize the power loss furtherly.

V. EXPERIMENTAL RESULTS

This paper designs a 1-kW laboratory prototype to prove the proposed converter, and Table 3 depicts the main parameters. Figs.12 to 17 are the waveforms in the secondary side modulation mode, and Figs.18 to 22 are the waveforms in the primary side modulation mode. Figs.23 and 25 give the results of the efficiency. Fig.26 shows the photo of the proposed converter.

In Fig.12, v_p is a square wave with a 100% duty ratio, and the top and bottom levels are not constant due to C_{BL} is charging or discharging during the power transfer procedure. i_{Llk} is identical to i_p plus i_{La}, as i_{La} is not in phase with i_p, a high value of i_{La} would not cause much-added conduction loss. As illustrated in Fig.13, the waveform before the LC filter is a TL type, which means a small volume of the output inductors. A small output inductor is used in the prototype to minimize the recovery energy of the rectifier diodes, and the ripple of i_{Lo} is a little high. Fig. 14 proves the ZVS of S_3. When the $v_{S3(GS)}$ reaches the threshold voltage, i_{S3} is negative, and $v_{S3(DS)}$ is zero. Therefore, S_3 can achieve ZVS. Fig.15 gives the waveforms of S_4, and S_4 can also obtain ZVS. Fig.16 shows the ZCS operation of the secondary switches. Fig.17 provides the waveform of D_{o4}.

TABLE 3. Parameters of the prototype.

Item	Value
Input voltage (V)	200-500
Output voltage(V)	220
Rated power(kW)	1
Switching frequency (kHz)	50
Turn ratios	1:1.2:1.2
L_a (μH)	10
L_o (μH)	100
C_{fly}(μF)	22
Transformer	Ferrite(PC40)/EE42
S_1 to S_4	TSK80R240S1
S_{p1} and S_{p2}	IRFB4137PBF
S_{S1} and S_{S2}	STF18N65M5
D_{o1} to D_{o6}	SCS220AE2

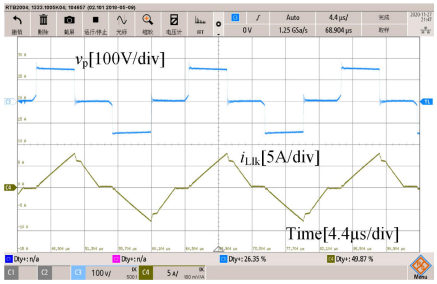

FIGURE 18. v_p and i_{Llk} in the primary side modulation mode.

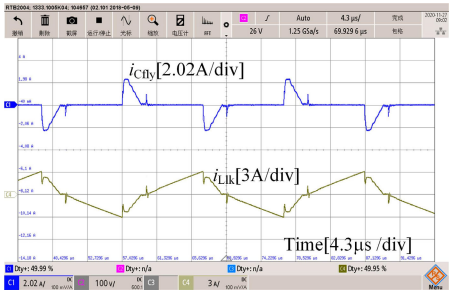

FIGURE 19. i_{Cfly} and i_{Llk} in the primary side modulation mode.

In Fig. 18, v_p is a square wave with a variable duty ratio, and the top and bottom levels are not constant values because v_{CBL} varies with time. i_{Llk} is identical to i_p, and i_{Llk} decreases to zero due to L_{lk} sustain negative voltage during the freewheeling stages. Fig.19 gives i_{Cfly} and i_{Llk}, and i_{Cfly} is zero at power transfer stages, which means low current stress. The current flowing in C_{fly} would reduce furtherly with small C_{BL}. In Fig.20, S_4 can achieve ZCS OFF and ZVS ON operation. As the soft-switching conditions of ON instants decouple from OFF instants, S_4 can both reduce switching ON and OFF power loss at the same time. In Fig.21,

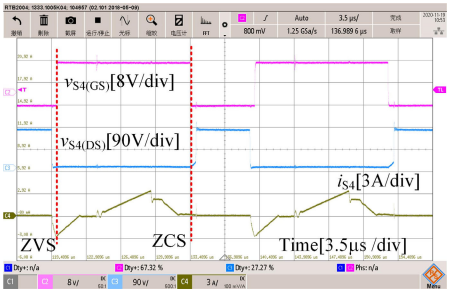

FIGURE 20. ZVZCS of S_4 in the primary side modulation mode.

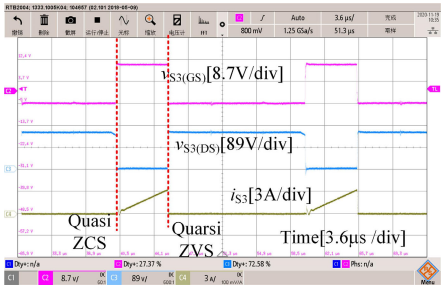

FIGURE 21. ZVZCS of S_3 in the primary side modulation mode.

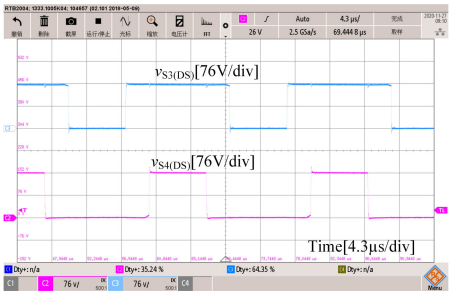

FIGURE 22. $v_{S4(DS)}$ and $v_{S3(DS)}$ in the primary side modulation mode.

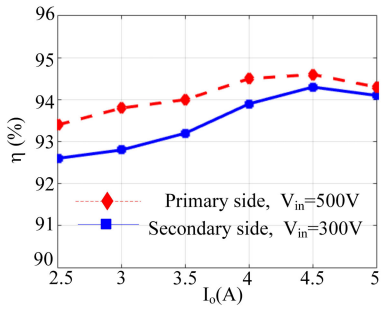

FIGURE 23. Efficiency results of the proposed converter.

S_3 turns ON with quasi ZCS and switches OFF with quasi ZVS. Also, S_3 obtains optimum power loss at ON and OFF instants without cross-influence on each other. Fig.22 proves the voltage stress of S_3 and S_4 is even.

Fig.23 shows the efficiency results of the proposed converter under different operation modes. As the turn ratio of the proposed converter is changing under different operation modes, both operation modes have no narrow duty

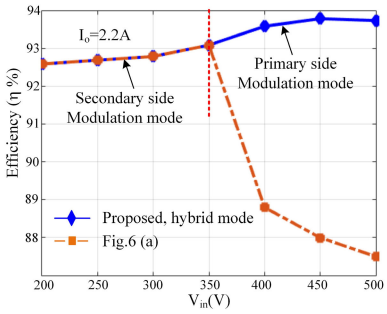

FIGURE 24. Efficiency comparison.

FIGURE 25. Hard copy of the efficiency result.

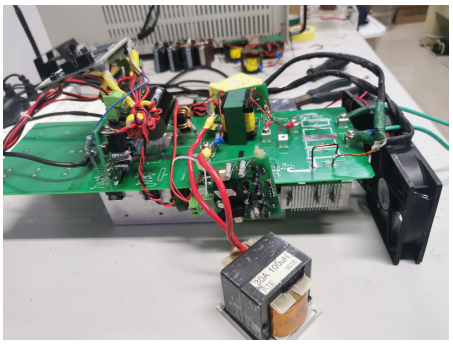

FIGURE 26. Photo of prototype.

ratio condition. Thus, the efficiency maintains high value over a wide input voltage and output load range. In Fig.24, the efficiency of the proposed converter in hybrid operation mode compares with that of Fig.6 (a), and the proposed converter achieves high efficiency under high input voltage conditions.

VI. CONCLUSION

This paper proposes a flexible structure soft witching TL dc-dc converter, and a 1-kW prototype verifies the theoretical analysis. The proposed converter has some clear benefits. The structure of the primary circuit is compact. The current of the clamping capacitor is low over the full operating range. The primary switches share even current distribution over a wide load range. As power devices have a wide soft-switching load range, the total switching power loss is low, and the conduction loss is also low because of no primary side circulating current. Besides, the added switching and conduction loss caused by the auxiliary switches is small. Hence, the efficiency over the full load range is high. At last,

the minimized size of the filters means a high-power density. In brief, the proposed converter is a promising solution to the DC interface converter for the microgrids with DERs.

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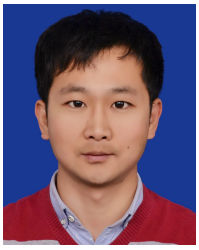

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