Hardware-in-the-Loop Implementation of Projectile Target Search Algorithm for Selective Harmonic Elimination in a 3-Phase Multilevel Converter

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ABSTRACT Multilevel converters (MLCs) are extensively used in medium- and high-power applications. Currently, MLCs are also used in grid integration of renewable sources of energy. In this paper a three-phase 11-level MLC topology is investigated which requires a smaller number of active switches compared to similar existing topologies for the same number of levels. In order to eliminate lower order harmonics, selective harmonic elimination (SHE) pulse width modulation technique is used. A projectile target search (PTS) algorithm is used to solve nonlinear SHE equations to determine the optimum values of switching angles to eliminate 5th, 7th, 11th and 13th harmonics from the converter output voltage. The PTS algorithm finds the best value of switching angles for different modulation indices (M) and these values are used in simulating the converter for eliminating lower order harmonics. Total harmonic distortion (THD) analysis is conducted for PTS optimization techniques at different modulation index. Simulation results are verified by hardware-in-the-loop test of the proposed three-phase converter using a Typhoon HIL-402 emulator.

INDEX TERMS Projectile-target search algorithm, multilevel converters, selective harmonic elimination, switching angle.

I. INTRODUCTION

Multilevel converters (MLCs) were introduced over 40 years ago and now have become the preferred choice for grid-connected and off-grid solar photovoltaic systems. MLCs are superior in performance compared with two-level converters in terms of higher efficiency, less %THD and the capability of the MLC to withstand high voltage. The design of MLCs mainly depends on the requirement of the DC supplies, the number of switches needed, voltage levels to be achieved, and the required output power quality [1]–[3].

MLCs are broadly divided into four categories. A neutral point clamped (NPC) MLC, was introduced in 1981 [4], the flying capacitor (FC) MLC, was introduced in the early

1990s [5], the cascaded H-bridge (CHB) MLC, was first proposed in 1975 [6] and the modular multilevel converter (MMC), was introduced in 2003 [7]. Currently MMCs are commonly used in high voltage direct current transmission and for large industrial applications. The NPC MLC requires clamping diodes for generating voltage levels at the output. For generating a higher number of levels at the output, more switches and clamping diodes are required which leads to voltage unbalance and more switching and conduction losses, which restrict its use to limited applications. The FC MLC has gained popularity in recent times for commercial and industrial applications. It is easier to implement than the NPC MLC but the requirement for a large number of capacitors makes it a difficult choice for complex circuitries. The CHB MLC has higher reliability than the other types of MLCs, so is often preferred. Various other types of MLC are proposed

by researchers in recent time for certain specific applications with a reduced switch count and improved efficiency [8]–[11].

Pulse width modulation (PWM) techniques provides the switching pulses to the converter. It can be classified as per switching frequency of the converter. Low switching frequency PWM, also known as a fundamental switching scheme, include SHE [12]–[15] and nearest level control (NLC) [3]. The second type of PWM techniques are multicarrier-based PWM schemes, which include level-shifted PWM and phase-shifted PWM in which the switching frequency is very high compared with the fundamental switching frequency scheme. Consequently, the switching losses are greater, and overall efficiency is lower [16], [17].

The key issue with SHE technique is the solution of nonlinear equations for finding the optimum switching angle to remove certain lower-order harmonics from the output waveform [18]–[20]. For solving these non-linear SHE equations, a number of nature-inspired optimization techniques have been used in the literature: the genetic algorithm (GA) [21], [22], particle swarm optimisation (PSO) [14], [22], [23], bee colony optimization [24] and bat [25] algorithm. In [26] GA algorithm is applied to a 7-level inverter which shows the %THD obtained with GA is 24.52% compared with 53.08% by using the conventional Newton-Raphson (NR) method. In [21] comparison between the NR technique and PSO technique is done. It showed that the computational time is approximately 2 seconds and corresponding THD is 6% for PSO, while for the NR method the computational time is 18 seconds and the corresponding THD is 7.5%. In [22] GA and PSO techniques were applied for solving SHE equations. The results show that GA yields better performance in %THD minimization and takes less computational time than PSO. The conventional techniques for solving nonlinear SHE equations take longer time and it also produces higher %THD.

The projectile target search (PTS) algorithm [27] is one of the nature-inspired optimization technique which is used in this paper for the first time for solving non-linear SHE equations. The advantage of the PTS algorithm over conventional and the other above-mentioned nature-inspired optimization techniques is the convergence speed; the disadvantage is that it requires proper selection of a larger number of variables.

The aim of designing a new converter topology is to reduce the number of switches, gate driver circuit and the number of DC sources. Improving the power quality by reducing %THD is also one of the motivations for designing new converter topology, which can be achieved by eliminating certain lower-order harmonics from the converter output. In [14], 12 power electronic switches are required to produce an 11-level output. In [15] the same number of levels are produced with 8 switches. In this paper a three-phase 11-level power electronic converter is presented for industrial use in which the three phase drives are mostly used for various applications. One phase of the converter consists of 7 IGBT switches and 3 DC sources. The SHE technique is
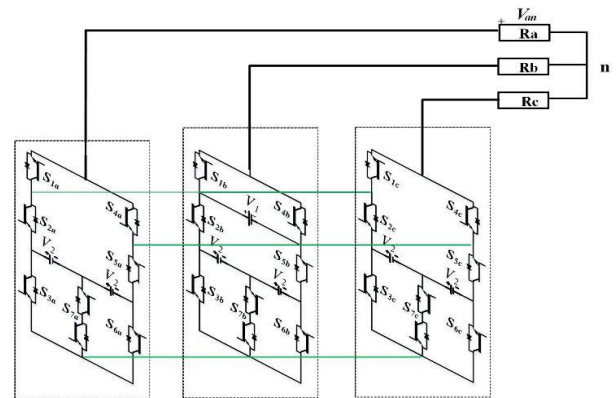

FIGURE 1. Circuit diagram of 3-phase 11-level converter.

used to determine optimal switching angles for the converter switching operation. In this case 5 switching angles can be controlled where one value of switching angle is to control the fundamental component and remaining four controllable switching angles are used to eliminate 5th, 7th, 11th and 13th order harmonics which, in turn, reduces the overall THD of the output waveform. The PTS algorithm is used to solve non-linear SHE equations to find the optimum solution for switching angles. The novelty of the presented work is as follows:

(1) This work is done for a 3-phase system where the overall %THD reduces in line voltage.
(2) The PTS algorithm is used to solve SHE equations which converges for a larger range of modulation index, which provides a large control range.
(3) Comparative analysis of BAT algorithm based SHE and PTS algorithm based SHE technique has been done.

This paper is structured as follows. Analysis of three phase 11-level converter topology is given in Section II. Section III discusses SHE technique. Section IV describes the PTS algorithm for SHE application. Results are presented in Section V. Section VI discusses the managerial implications and finally conclusions are presented in Section VII.

II. THREE PHASE 11-LEVEL CONVERTER

The circuit of a three-phase 11-level MLC topology consists of seven insulated gate bipolar transistors (IGBT), and three DC sources in one phase leg—see Fig. 1. Table 1 shows the switching states of the converter in one complete cycle for one phase. Fig. 2 shows the conduction diagram of the converter for voltage levels produced in the positive half cycle of the output voltage.

A. MODES OF OPERATION

The switching states of switches ($S_1 to S_7$) are shown in Table 1, during the positive and negative conduction period of the converter. For the sake of simplicity, the switching states for positive levels are shown in Fig. 2.

Mode 1: S_1, S_2, and S_3 conduct during mode 1. The output voltage is zero as shown in Fig. 2(a).

TABLE 1. Switching Table.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	V_{out}
1	1	0	0	0	0	1	V_2
1	1	0	0	0	1	0	$2V_2$
1	0	1	0	1	0	0	$V_1 - 2V_2$
1	0	0	0	1	0	1	$V_1 - V_2$
1	0	0	0	1	1	0	V_1
1	1	1	0	0	0	0	0
0	0	0	1	1	0	1	$-V_2$
0	0	1	1	1	0	0	$-2V_2$
0	1	0	1	0	1	0	$-V_1 + 2V_2$
0	1	0	1	0	0	1	$-V_1 + V_2$
0	1	1	1	0	0	0	$-V_1$

FIGURE 3. Voltage stress distribution among the switches during all 11 levels.

FIGURE 4. Voltage stress distribution for each switch in terms of V_{dc} during zero level of output voltage.
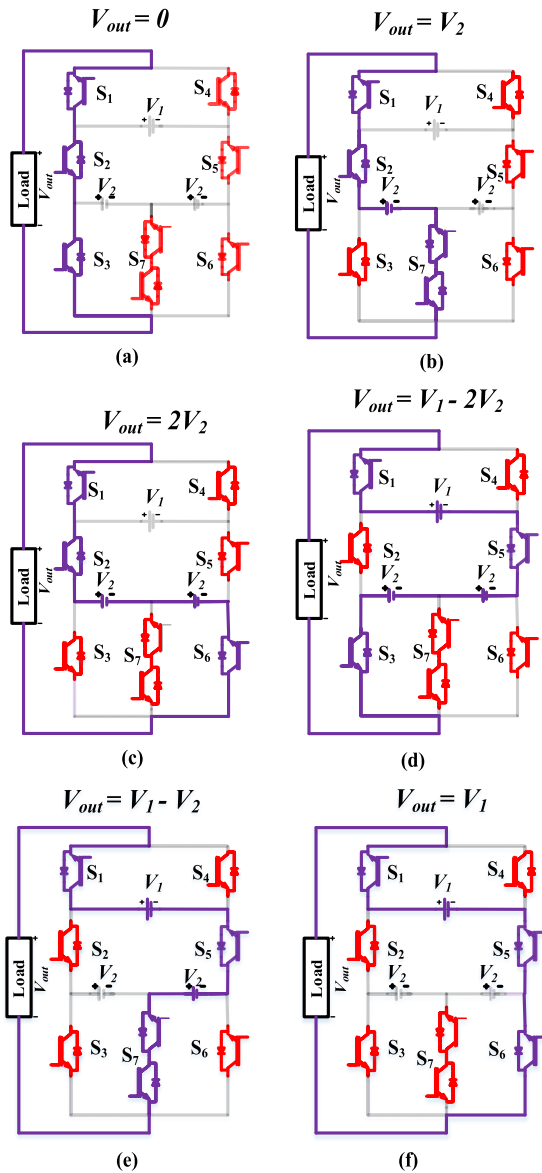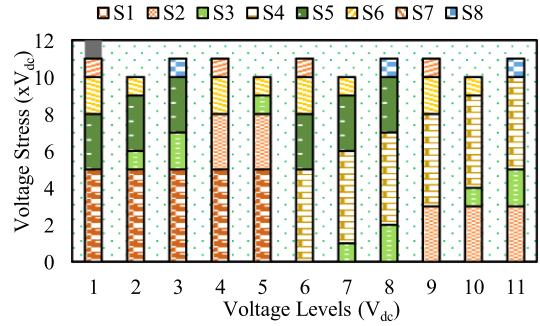

FIGURE 2. Different mode of operation for level generation in the positive half cycle of the output voltage.

Mode 4: S_1, S_3 and S_5 are in conducting state as shown in Fig. 2(d). In mode 4, the output voltage is $V_1 - 2V_2$.

Mode 5: S_1, S_5 and S_7 are in conducting state as shown in Fig. 2(e). The output voltage is $V_1 - V_2$.

Mode 6: S_1, S_5 and S_6 are turned on as shown in Fig. 2(f). In mode 6, the output voltage is V_1.

The working of the circuit for the remaining modes of operation can be explained in the same manner as discussed above.

B. COMPARISON WITH OTHER EXISTING TOPOLOGIES

This comparison is done on single phase basis and it is based on the number of switches (N_{switch}), the number of diodes (N_{diode}), the total number of switches used in the circuit, and the number of levels produced at the output. For total standing voltage (TSV) calculation voltage stress across each switch in one complete cycle and in one particular level (zero-level) is shown in Fig. 3 and Fig. 4 respectively. In [16] the total number of switches used is 11 and the voltage levels produced are 9 at the output. In [17], [18] the total number of switches used are 8 and the voltage levels produced are 7 and 11 respectively. In [27] the converter produces 7 level of output voltage with 11 switches. The converter used in this paper requires only seven switches for producing an 11-level output. From the Table 2 it can be seen for the same number of DC sources, the converter used in this paper requires fewer switches. Table 3 shows a comparison of converters producing an 11-level output based on the number of switches (N_{switch}), the number of driver circuits (N_{driver}) used, and the

Mode 2: S_1, S_2 and S_7 are in the conducting state as shown in Fig. 2(b). The output voltage is V_2.

Mode 3: S_1, S_2, and S_6 are in the conducting state as shown in Fig. 2(c). In this mode output voltage is $2V_2$.

TABLE 2. Comparison of different MLC topologies with three DC sources.

Topology Reference	N_{switch}	N_{Diode}	Total Switch	No. of levels
[16]	7	4	11	9
[17]	8	0	8	7
[18]	8	0	8	11
[32]	7	4	11	7
Proposed	7	0	7	11

TABLE 3. Comparison of 11-level converter topology.

Topology Reference	N_{switch}	N_{driver}	No of DC source	TSV
[14]	12	9	2	35
[15]	8	7	3	22
Proposed	7	7	3	22

total standing voltage (TSV). In [14] twelve switches are used which has TSV of $35V_{dc}$. In [15], 8 switches are used with a TSV of $22V_{dc}$ and converter used in this paper requires only 7 switches with same TSV.

III. SELECTIVE HARMONIC ELIMATION

The SHE technique is used to calculate switching angles for power electronic converter. The converter presented in this paper produces an 11-level output voltage and hence there are 5 degrees of freedom for eliminating lower-order harmonics. Among these controllable switching angles, one is used to control the fundamental component of the voltage waveform and the remaining four can be assigned to eliminate 5th, 7th, 11th and 13th order harmonics as per the following equations [28]:

$$\cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 + \cos\alpha_4 + \cos\alpha_5 = M \quad (1)$$

$$\cos 5\alpha_1 + \cos 5\alpha_2 + \cos 5\alpha_3 + \cos 5\alpha_4 + \cos 5\alpha_5 = F_1 \quad (2)$$

$$\cos 7\alpha_1 + \cos 7\alpha_2 + \cos 7\alpha_3 + \cos 7\alpha_4 + \cos 7\alpha_5 = F_2 \quad (3)$$

$$\cos 11\alpha_1 + \cos 11\alpha_2 + \cos 11\alpha_3 + \cos 11\alpha_4 + \cos 11\alpha_5 = F_3 \quad (4)$$

$$\cos 13\alpha_1 + \cos 13\alpha_2 + \cos 13\alpha_3 + \cos 13\alpha_4 + \cos 13\alpha_5 = F_4 \quad (5)$$

where M is the modulation index which can be calculated as follows:

$$M = \frac{\pi * V_d}{4NV_{dc}} \quad (6)$$

where, V_d is the desired fundamental voltage and N is the number of control variables.

Conventional techniques and some of the above-mentioned nature-inspired optimization techniques have been used to solve these SHE equations, but it takes more computational time to converge for the full range of M (from 0 to 1). In this paper we have chosen the PTS optimization technique to solve the SHE equations for different values of M.
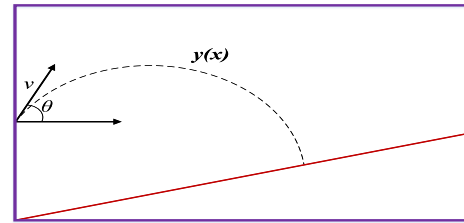

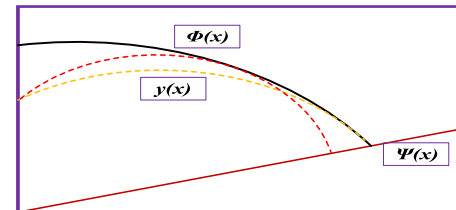**FIGURE 5.** The projectile motion path.

FIGURE 6. The enveloping parabolic path.

IV. PROJECTILE TARGET SEARCH ALGORITHM BASED SHE

The PTS algorithm is a metaheuristic optimization technique based on the kinematics of projectile motion [27]. The algorithm uses the projectile trajectory envelope to find the target in the search space. The control parameters provide the possibility for acceleration in the convergence and new better projectile for the search process. The PTS algorithm is used in this paper to solve the SHE equations.

A. PROJECTILE MODEL

The projectile is launched as shown in Figure 5 with a velocity of *v*. The projectile path function (y) as a function of distance in horizontal direction is given as:

$$y(x) = x\tan(\theta)\frac{gx^2}{2v^2}\sec^2(\theta) \quad (7)$$

where the value of g is $9.81 m/s^2$.

The shape and size of the projectile varies as per the launch angle as shown in Figure 6. The envelope of projectile trajectory (φ), with all projectile path for finding the target is defined as impact function (ψ). The equation of the projectile trajectory envelope can be given as:

$$\varphi(x) = \frac{v^2}{2g} - \frac{g}{2v^2}x^2 \quad (8)$$

For a continuous impact function the surface of ψ and the path of φ intersect at a unique point at $\psi(\mathrm{x}) = \varphi(\mathrm{x})$. The main objective of the PTS algorithm is to ensure that the projectile reaches the target precisely by minimizing the difference between ψ and φ.

B. PROJECTILE MODEL

The PTS algorithm is defined by some initial parameters: population size (N), maximum number of iterations (I_{max}), the number of variables (D), and the lower and upper bound X_{min} and X_{max} respectively. The lower bound and upper

bound variables can be expressed as,

$$x_{\min j} = [x_{\min 1}, x_{\min 2}, \ldots \ldots x_{\min D}];$$
$$x_{\max j} = [x_{\max 1}, x_{\max 2}, \ldots \ldots x_{\max D}] \quad (9)$$

The initial candidate solution is randomly generated within [0, 1] to each boundary as follows:

$$x_{i,j}^{(I=1)} = x_{\min j} + rand_j(x_{\max j} - x_{\min j})$$
$$i = 1, 2, \ldots \ldots N. \quad j = 1, 2, \ldots \ldots D \quad (10)$$

where by perturbing the randomly selected particles the target population is created as follows:

$$t_{k,j}^{(I)} = x_{a1,j}^I + 0.5(x_{a2,j}^I - x_{a3,j}^I),$$
$$k = 1, 2, \ldots \ldots N; \quad j = 1, 2 \ldots \ldots D \quad (11)$$

where, a_1, a_2 and a_3 are randomly chosen between $[1 \ldots \ldots N]$ and t_k represents the target population.

The fitness values of the projectile and target are evaluated by the following equations:

$$f_i^I = f(x_{i,j}^I)$$
$$f_k^I = f(t_{k,j}^I) \quad (12)$$

Now the fitness values of each $x_{i,j}^I$ and $t_{k,j}^I$ are compared. The best projectile and its best value are selected as per the following equation:

$$x_{bestj}^I = x_{i,j}^I \quad if \ \min(f(x_{i,j}^I)) \le \min(f(t_{k,j}^I))$$
$$x_{bestj}^I = t_{k,j}^I \quad otherwise \quad (13)$$

The new target population is created here as $(t_{k,j}^{I+1})$ and the best projectile for next iteration is:

$$x_{bestj}^{I+1} = x_{i,j}^{I+1} \quad if \ \min(f(x_{i,j}^{I+1})) \le \min(f(t_{k,j}^{I+1}))$$
$$x_{bestj}^{I+1} = t_{k,j}^{I+1} \quad otherwise$$
$$f_{best}^{I+1} = f(x_{bestj}^{I+1}) \quad (14)$$

The process is repeated until the projectile reaches its desired accuracy level or the number of iterations has reached *Imax* value and the corresponding result satisfies the projectile landing onto the target. The implementation process of the PTS algorithm for solving the SHE equations is presented as follows:

First select the value of M at which the SHE equations are to be solved. After selecting the value of M, the PTS parameters are chosen as follows: the number of objective function variables (D) is chosen as 5 and the search agent size (NP) is 1000. Initialize the position and population of the particle.

Now initialize the switching angles within constraint 0 to 180° and solve the SHE equations for finding the best switching angle values.

V. RESULTS
Simulation analysis of a 3-phase 11-level converter is carried out using MATLAB/Simulink. The simulation parameters are shown in Table 4. The SHE technique is used to generate switching pulse for the converter. The values of α_1, α_2, α_3, α_4

TABLE 4. Simulation parameters.

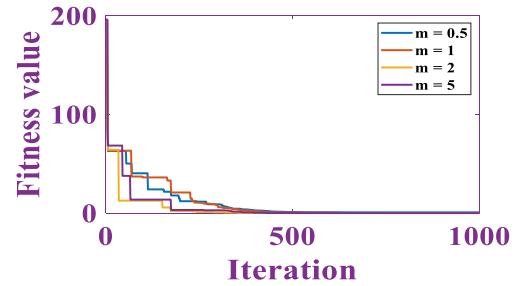| Type of switch used	IGBT (1200V, 75A)
Number of DC source	Two (600V and 120V)
PWM technique used	Selective Harmonic elimination
Modulation Index (M)	0.9
Load impedance (Z)	50Ω+100mH

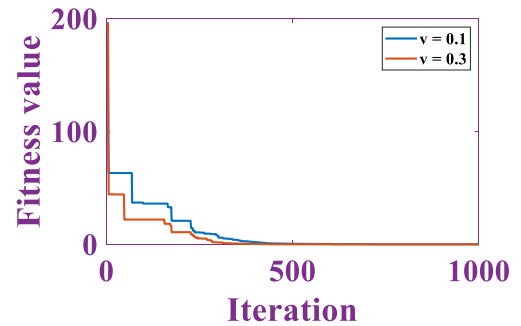**FIGURE 7.** Fitness value at different slop (m).

FIGURE 8. Fitness value at different slop velocity.

and α_5 are calculated by using the PTS algorithm for different modulation indices. The fitness value of the PTS algorithm is simulated for different values of slop as shown in Fig. 7 It converges very quickly for the third case (m = 2). The fitness value is checked for two velocities as shown in Fig. 8. For the higher value of velocity the algorithm converges quickly. From the results shown in Fig. 7 and Fig. 8 it is evident that a suitable value of parameters needs to be selected for faster convergence of the algorithm. The switching angles are calculated by using the PTS algorithm at different modulation indices which are shown in Fig. 9.

A. PROJECTILE TARGET SEARCH ALGORITHM BASED SHE RESULTS
In this subsection the results related to the PTS algorithm are presented. Fig. 10 and Fig. 11 shows the 3-phase voltage and current waveform at modulation index (M) equal to 0.9 at RL (50ohm + 100mH) load. The load current lags the output voltage by the load power factor angle. Fig. 12 shows the single phase voltage and current waveform for RL load. Fig. 13 shows the THD profile of the phase voltage at M = 0.9. Table 5 shows the optimum values of switching angle and corresponding %THD at different values of M.

B. COMPARISON OF PTS WITH OTHER ALGORITHM BASED SHE
The other algorithms can also be used to solve the non-linear SHE equations [25], [27], [28]. Table 6 shows the results
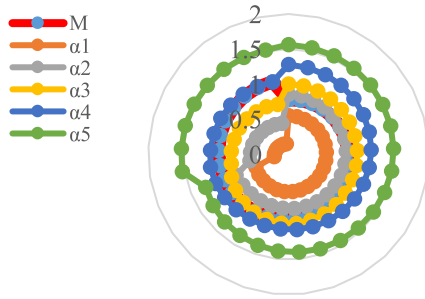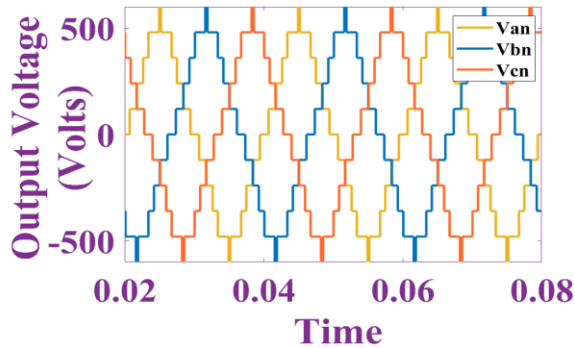
FIGURE 9. Plot of switching angle at different M.

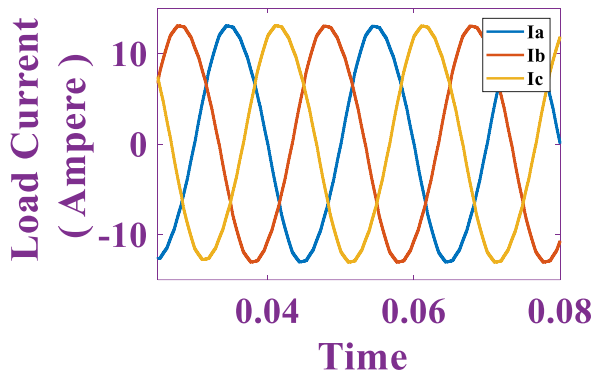**FIGURE 10.** Output voltage waveform for RL load at M = 0.8.

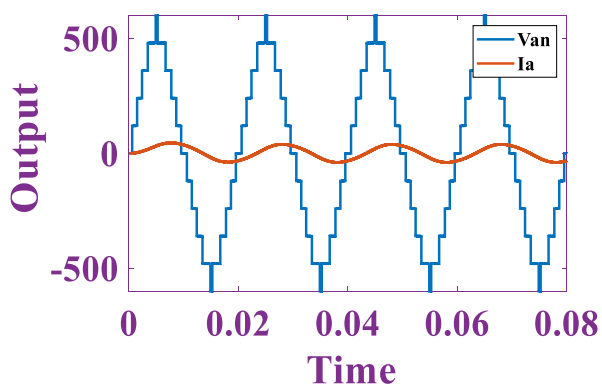**FIGURE 11.** Load current for RL load at M = 0.8.

FIGURE 12. Phase voltage and current at M = 0.9.

obtained by using bat algorithm. Table 7 shows the comparative results of PTS and BAT algorithm. The PTS algorithm
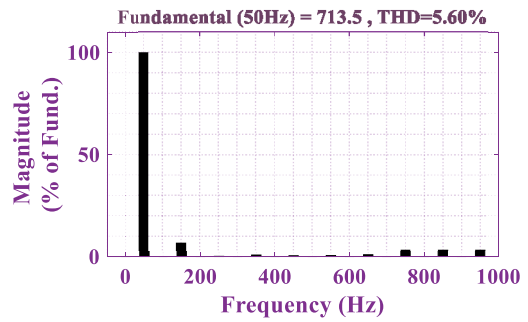

FIGURE 13. THD profile of output voltage (Line Voltage).

TABLE 5. %THD and switching angle at different M with PTS algorithm.

M	α_1	α_2	α_3	α_4	α_5	%THD
0.7	0.55	0.85	0.97	1.19	1.4	7.63
0.8	0.53	0.82	0.99	1.2	1.48	6.82
0.9	0.62	0.78	0.97	1.15	1.39	5.6
1.0	0.59	0.65	0.86	1.09	1.31	6.3
1.06	0.17	0.48	0.76	1.07	1.52	5.9

TABLE 6. %THD and switching angle at different M with BAT algorithm.

M	α_1	α_2	α_3	α_4	α_5	%THD
0.7	0.65	0.91	1.16	1.46	1.55	10.26
0.8	0.22	0.53	0.85	1.54	1.63	8.96
0.9	0.15	0.4	0.69	1.21	1.56	8.45
1.0	0.12	0.25	0.45	0.68	1.12	7.23
1.06	0.1	0.21	0.39	0.57	0.83	7.83

TABLE 7. Comparison of PTS and bat algorithms.

M	%THD (PTS algorithm)	%THD (BAT algorithm)
0.7	7.63	10.26
0.8	6.82	8.96
0.9	5.6	8.45
1.0	6.3	7.23
1.06	5.9	7.83

TABLE 8. Comparison of the SHE and NLC algorithms.

Method	V_{m1} (Volts)	V_{m5} (Volts)	V_{m7} (Volts)	V_{m1} (Volts)	V_{m13} (Volts)	%THD
SHE	713	0.04	0.03	0.05	0.08	5.6
NLC	697	4.68	4.09	3.58	2.95	7.14

provides the best values of switching angle for a larger range of M.

C. COMPARISON WITH OTHER EXISTING TOPOLOGIES
NLC is another fundamental switching frequency-based PWM technique which is used in DC-AC converter for providing switching pulses to the converter switches. The NLC technique is also used for this converter to perform comparative analysis of the results obtained through SHE. The comparative results are shown in Table 8. In case of the NLC algorithm, all lower-order harmonics are present in the output voltage but, in case of SHE, the selected lower-order, harmonics are absent. The overall %THD is less for SHE.
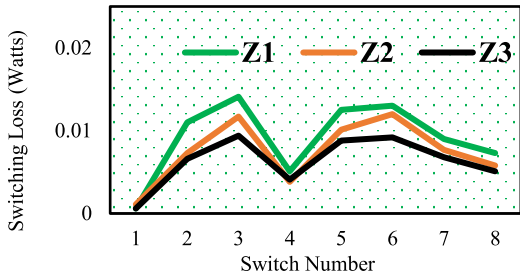
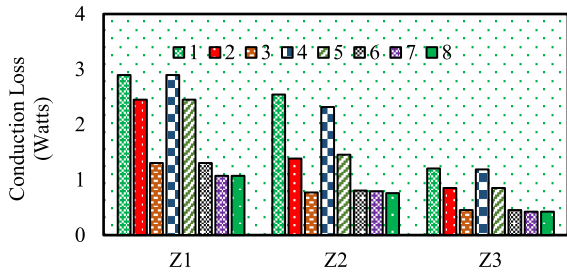**FIGURE 14.** Switching loss across each switch at different load.

FIGURE 15. Conduction loss through each switch in one cycle.
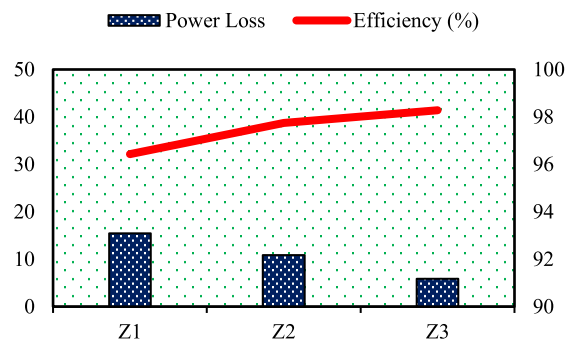

FIGURE 16. Power loss and efficiency of the converter at three different load.

D. POWER LOSS ANALYSIS

Power loss analysis of the converter has been conducted by using the PLECS software. Losses in the semiconductor device under operating condition are mainly switching loss and conduction loss. These losses are calculated by the practical data provided by the manufacturer in the data sheet. To determine switching and conduction loss, the 600V, 30A Infineon IGBT (IGA30N60H3) is used for power loss analysis for three different loading conditions. Fig. 14 shows the switching loss across each switch for all three loading conditions. Fig. 15 shows the conduction loss for each switch at loading of Z1, Z2 and Z3. Switching loss and conduction loss are both greater in the case of a purely resistive load. Fig. 16 shows the overall power loss and efficiency of the proposed converter at all three loading conditions, where $Z_1 = 50\Omega$, $Z_2 = 50\Omega + 100mH$ and $Z_3 = 100\Omega + 100mH$.

E. HARDWARE IN THE LOOP RESULTS

The simulated results are validated by performing hardware-in-loop testing of the proposed converter by using Typhoon HIL-402. The modelling of the converter is done using
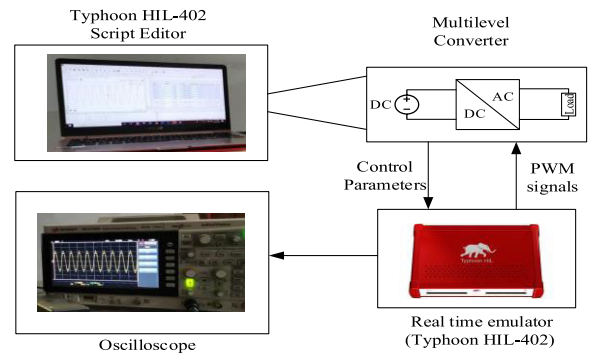

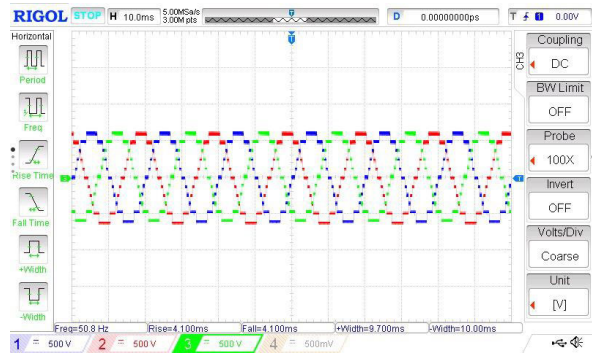**FIGURE 17.** Hardware-in-the-loop (HIL-402) setup.

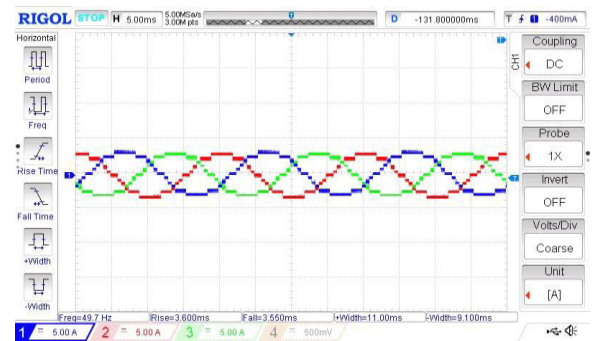**FIGURE 18.** Three phase voltage at M = 0.9.

FIGURE 19. Three phase load current at R load.

Typhoon script editer and HIL-402 acts as controller [31]. The complete setup of HIL is shown in Fig. 17. Fig. 18 shows 3 phase voltage waveform. Fig. 19 and Fig. 20 show three phase load current waveform for R and RL load respectively. For the R load, the current follows the same pattern as the voltage and, for the RL load, the current lags behind the output voltage by the load power factor angle. Fig. 21 shows the current waveform for varying load conditions.

VI. MANAGERIAL IMPLICATION

One of the most important parameters that needs to be minimized in any type of DC-AC converter is % THD, so as to improve the overall power quality of the system. In a conventional DC-AC converter all lower-order (odd) harmonics are present in the output voltage. These harmonics can be eliminated by using filters which are large and bulky.
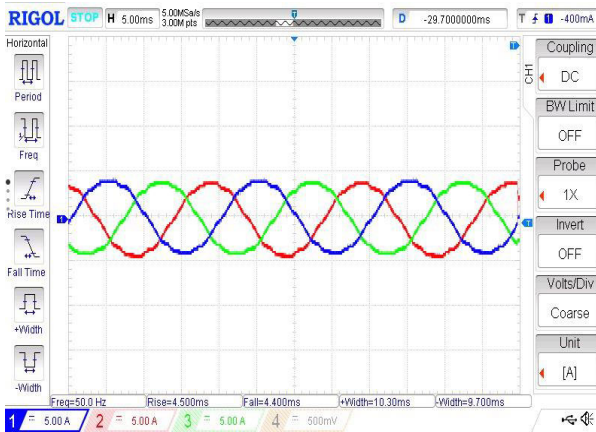
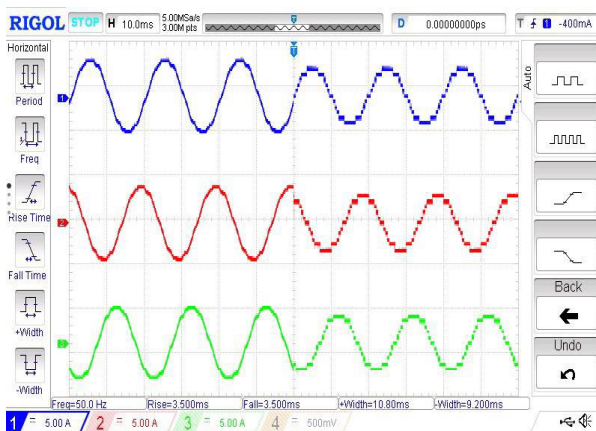**FIGURE 20.** Three phase current at RL load.

FIGURE 21. Load current variation from RL to R load after 3 cycle.

With the recent advancement of multilevel converters it is straightforward to filter out the harmonics from the output voltage by using small filters, because the harmonics present in the output are of higher order. Conventional multilevel converters requires a large number of switches for producing multilevel output voltage, which is more costly and less efficient. In recent times researchers seek to achieve a greater number of levels with a requirement for fewer switches. In this paper the converter under study has fewer switches than other existing multilevel converter topologies. As a result of having fewer switches, switching loss and conduction loss are reduced which in turn increases the overall efficiency of the converter. SHE technique is used to eliminate selected lower-order harmonics from the output voltage to reduce the % THD of the converter.

SHE equations are nonlinear equations which needs to be solved to find optimum values of switching angles which eliminate the lower-order harmonics from the output voltage. This can be achieved by various means which are available in literature. The PTS algorithm is used in this paper for solving nonlinear SHE equations as it provides better solutions of switching angles as compared with other techniques available in literature. It also provides solutions for a larger range of M.

VII. CONCLUSION

The PTS algorithm is a nature-inspired optimization technique that is used to calculate the optimum values of switching angles required to eliminate lower-order harmonics from the output voltage produced by the 11-level converter. In this paper we have eliminated 5th, 7th, 11th and 13th order harmonics from the output voltage waveform. For a three phase system, third harmonics and its multiples will be eliminated in the line voltage. Another nature inspired optimization technique, the bat algorithm, is also used for finding optimum solution for switching angles. Comparison shows that the PTS algorithm performs better in terms of convergence for a greater range of M. The NLC-based PWM technique was used for comparative analysis with the SHE algorithm. NLC has lower-order harmonics present in the output and therefore the %THD is higher than the SHE algorithm. The proposed converter produces 11 levels of output in the phase voltage with a lower requirement for switches and driver circuits. The proposed converter is extended for a three phase system.

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REFERENCES

[1] M. D. Siddique, B. Alamri, F. A. Salem, M. Orabi, S. Mekhilef, N. M. Shah, N. Sandeep, J. S. Mohamed Ali, A. Iqbal, M. Ahmed, S. S. M. Ghoneim, and M. M. Al-Harthi, "A single DC source nine-level switched-capacitor boost inverter topology with reduced switch count," *IEEE Access*, vol. 8, pp. 5840–5851, 2020.

[2] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 24498–24510, 2019.

[3] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, "A new multilevel inverter topology with reduce switch count," *IEEE Access*, vol. 7, pp. 58584–58594, 2019.

[4] A. Perra, "PWM inverter technology," *IEEE Aerosp. Electron. Syst. Mag.*, vol. 7, no. 4, pp. 20–22, Apr. 1992.

[5] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. 23rd Annu. IEEE Power Electron. Specialists Conf.*, 1992, pp. 397–403.

[6] I. R. H. Baker and L. H. Bannister, "Electric power converter," U.S. Patent 3 867 643 A, 1975.

[7] M. C. Teich, K. Matsuo, and B. E. A. Saleh, "Time and frequency response of the conventional avalanche photodiode," *IEEE Trans. Electron Devices*, vol. 33, no. 10, pp. 1511–1517, Oct. 1986.

[8] H. Shu, S. Lei, and X. Tian, "A new topology of modular multilevel converter with voltage self-balancing ability," *IEEE Access*, vol. 7, pp. 184786–184796, 2019.

[9] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, M. Tayyab, and M. K. Ansari, "Low switching frequency based asymmetrical multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 86374–86383, 2019.

[10] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi, "An envelope type (E-Type) module: Asymmetric multilevel inverters with reduced components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7148–7156, Nov. 2016.

[11] S. P. Gautam, S. Gupta, and L. K. Sahu, "Reduction in number of devices for symmetrical and asymmetrical multilevel inverters," *IET Power Electron.*, vol. 9, no. 4, pp. 698–709, Mar. 2016.

[12] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A review of multilevel selective harmonic elimination PWM: Formulations, solving algorithms, implementation and applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4091–4106, Aug. 2015.

[13] M. H. Etesami, D. M. Vilathgamuwa, N. Ghasemi, and D. P. Jovanovic, "Enhanced Metaheuristic methods for selective harmonic elimination technique," *IEEE Trans. Ind. Informat.*, vol. 14, no. 12, pp. 5210–5220, Dec. 2018.

[14] M. T. Hagh, H. Taghizadeh, and K. Razi, "Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2259–2267, Oct. 2009.

[15] J. Kumar, B. Das, and P. Agarwal, "Selective harmonic elimination technique for a multilevel inverter," in *Proc. 15th Natl. Power Syst. Conf.*, Dec. 2008, pp. 608–613.

[16] G. S. Konstantinou and V. G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques," in *Proc. 4th IEEE Conf. Ind. Electron. Appl.*, May 2009, pp. 3399–3404.

[17] M. Jayabalan, B. Jeevarathinam, and T. Sandirasegarane, "Reduced switch count pulse width modulated multilevel inverter," *IET Power Electron.*, vol. 10, pp. 10–17, doi: 10.1049/iet-pel.2015.0720.

[18] H. Lou, J. Lu, C. Mao, L. Wang, and D. Wang, "Fundamental modulation strategy with selective harmonic elimination for multilevel inverters," *IET Power Electron.*, vol. 7, no. 8, pp. 2173–2181, Aug. 2014.

[19] W. Hu, C. Ruan, H. Nian, and D. Sun, "Zero-sequence current suppression strategy with common mode voltage control for open-end winding PMSM drives with common DC bus," *IEEE Trans. Ind. Electron.*, early access, Apr. 21, 2020, doi: 10.1109/TIE.2020.2988221.

[20] J. Liu, B. Zhao, W. Zhou, G. Lyu, Z. Chen, C. Xu, Z. Yu, and R. Zeng, "Precise measurement methodology of nH-level gate electrode inductance based on Calculation-error-free algorithm for unity-gain turn-off devices," *IEEE Trans. Ind. Electron.*, early access, Jul. 10, 2020, doi: 10.1109/TIE.2020.3007089.

[21] M. A. Dahidah and V. G. Agelidis, "A hybrid genetic algorithm for selective harmonic elimination control of a multilevel inverter with non-equal DC sources," in *Proc. Int. Conf. Power Electron. Drives Syst.*, 2005, vol. 2, pp. 1205–1210.

[22] S. Debnath and R. N. Ray, "Harmonic elimination in multilevel inverter using GA and PSO: A comparison," in *Proc. IEEE Students' Conf. Electr., Electron. Comput. Sci.*, Mar. 2012, pp. 1–5.

[23] H. Taghizadeh and M. Tarafdar Hagh, "Harmonic elimination of cascade multilevel inverters with nonequal DC sources using particle swarm optimization," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3678–3684, Nov. 2010.

[24] A. Kavousi, B. Vahidi, R. Salehi, M. K. Bakhshizadeh, N. Farokhnia, and S. H. Fathi, "Application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1689–1696, Apr. 2012.

[25] S. Srinivasan, S. Muthubalaji, G. Devadasu, and R. Anand, "Bat algorithm based selective harmonic elimination PWM for an eleven level inverter," *Int. J. Recent Technol. Eng.*, vol. 8, nos. 2–8, pp. 1164–1169, 2019.

[26] Krismadinata, N. A. Rahim, H. W. Ping, and J. Selvaraj, "Elimination of harmonics in photovoltaic seven-level inverter with Newton-raphson optimization," *Procedia Environ. Sci.*, vol. 17, pp. 519–528, 2013.

[27] A. Hiendro, "Projectile-target search algorithm: A stochastic metaheuristic optimization technique," *Int. J. Electr. Comput. Eng.*, vol. 9, no. 5, pp. 3772–3778, 2019.

[28] C. Buccella, M. G. Cimoroni, and C. Cecati, "General formula for SHE problem solution," *Energies*, vol. 13, no. 14, p. 3740, Jul. 2020.

[29] H. Zhao, S. Wang, and A. Moeini, "Critical parameter design for a cascaded H-Bridge with selective harmonic Elimination/Compensation based on harmonic envelope analysis for single-phase systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2914–2925, Apr. 2019.

[30] Q. Sun, R. Han, H. Zhang, J. Zhou, and J. M. Guerrero, "A multiagent-based consensus algorithm for distributed coordinated control of distributed generators in the energy Internet," *IEEE Trans. Smart Grid*, vol. 6, no. 6, pp. 3006–3019, Nov. 2015.

[31] W. Rui, S. Qiuye, Z. Pinjia, G. Yonghao, Q. Dehao, and W. Peng, "Reduced-order transfer function model of the droop-controlled inverter via jordan continued-fraction expansion," *IEEE Trans. Energy Convers.*, vol. 35, no. 3, pp. 1585–1595, Sep. 2020.

[32] M. D. Siddique, S. Mekhilef, N. M. Shah, M. A. Momon, and A. Mustafa, "SHEPWM based new hybrid multilevel inverter topology with reduced switch count," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, Sep. 2019, pp. 1–9.

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