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A Thermal Failure Model for MOSFETs Under Repetitive Electromagnetic Pulses

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ABSTRACT A thermal failure model for MOSFETs under repetitive electromagnetic pulses is investigated in this paper. The analytic equation to analyze the relationship between the temperature rise and pulse parameters is given by a theoretical derivation. The electro-thermal process of a 180 nm MOSFET is simulated as an example. It shows that the model agrees well with the technology computer aided design (TCAD) results. Some discussions on the influence of the dissipation performance and on the electro-thermal coupled effect are given. Both the theoretical model and the TCAD results indicate that most of the failures occur in 1 or 2 cycles. Further increase in the pulse number does not change the failure probability. Influence of heat dissipation performance of the substrate is discussed. This work is useful for further failure analysis, and is also helpful in protection design for the MOSFET device and circuit under HPMs and other repetitive electromagnetic pulses.

INDEX TERMS High power microwave, electro-thermal, metal-oxide-semiconductor field-effect transistor, thermal effects.

I. INTRODUCTION

Semiconductor devices, such as the metal-oxide-semiconductor field-effect transistor (MOSFET), play key roles in modern electronic systems. However, they are susceptible to external electromagnetic interferences (EMI) [1]–[3]. External electromagnetic pulses generated by the high power microwave (HPM) source or other equipments can couple into an electronic system [4] through the slot, the RF receiver, or the cable [5]–[11]. In the work of electromagnetic compatibility (EMC) design and EMI shielding, it is important to locate the vulnerable devices in the equipment/circuit where the electromagnetic stress is weak, as well as to study the breakdown position and the failure mechanism of the device. Understanding these problems will help to provide better EMC design and better anti-EMI shielding. Besides the traditional electromagnetic shielding cavity, some other techniques, such as signal filter, fast response voltage suppression, etc., are used to harden the device and circuit against external EMIs [12], [13]. However, with the increase of interference sources, the semiconductor devices and circuits are still vulnerable to the EMI. The external electromagnetic power results in a serious damage on the semiconductor device. In most cases, the failure caused by the HPM or other interferences ensues from the thermal effect. The energy of the external electromagnetic pulses can couple into an electronic system, and result in an excessive voltage or current which inject into a semiconductor device in the circuit [14]–[17]. Heat caused by the excessive voltage or current will increase the temperature of the devices. If the heat generation ratio exceeds the cooling capacity of the device, thermal failure may happen. Therefore, special attentions have been paid to the thermal failure model. In 1960s, Wunsch and Bell reported the widely used Wunsch-Bell model [18] which was derived from a theoretical analysis. Other thermal models are further developed [19]–[21]. These models solve the thermal diffusion partial differential equations (PDEs) while the heat source inside a semiconductor device is supposed as an ideal infinite plane [18], a sphere immersed in an infinite medium [19], a long cylinder [20], or a cubic [21]. Though useful works have been done on the thermal failure of the bipolar junction transistor [22]–[24], the high electron mobility transistor [25] and the PIN diode [26], [27], efficient model that can accurately analyze the thermal failure process of the MOSFET is still lacking. The intricacy of the geometrical structures of MOSFETs

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is one reason. Another reason is that the carrier mobility of MOSFETs is complicated. In MOSFETs, the carriers in the insulator-semiconductor interface are limited due to the surface-related scattering. The surface roughness scattering and the acoustic phonon scattering make the response of carriers quite different from that of other silicon devices. This mechanism induces the complicacy in the electro-thermal effect in MOSFETs. Meanwhile, the failure is affected by the parameters of the pulse signal, such as pulse width, duty time of the pulse, number of pulses injected into the device. These reasons make it hard to give a general model to investigate the failure of MOSFETs.

Therefore, understanding the thermal failure of MOSFETs is challenging and pressing. Deriving an analytic equation for expressing the relationship between the temperature and pulse parameters is important in the HPM failure analysis and the circuit protection design. In this paper, a general equation is theoretically derived to predict the thermal failure process by covering these difficulties.

This paper is organized as follows. In Section II, a thermal failure model for analyzing the electro-thermal coupled process in MOSFETs under repetitive pulses is theoretically derived. In Section III, the semiconductor model and device parameters for the technology computer aided design (TCAD) simulation of a 180nm channel MOSFET are introduced. In Section IV, some TCAD simulation results are shown and compared with the theoretical model. The influence of the dissipation performance and the electro-thermal coupled effect are discussed briefly in Section V. In Section VI, a conclusion is summarized.

II. ELECTRO-THERMAL COUPLED FAILURE MODEL FOR THE MOSFET DEVICE

A. HEAT GENERATION MECHANISM INSIDE A MOSFET

The drift and diffusion model [28] (DDM) is widely used to describe the behavior of carriers in semiconductor devices [29]–[32]. When the quantum effect of carrier is not significant, the model can accurately describe the response and electro-thermal process of the device.

The carrier continuity PDEs including the temperature effect in the DDM can be expressed as

$$\frac{\partial n_n}{\partial t} = \nabla \cdot (\mu_n n_n \vec{E} + \mu_n \frac{k_b T}{q} \nabla n_n + \mu_n \frac{k_b n_n}{q} \nabla T) - (U - G) \tag{1}$$

$$\frac{\partial n_p}{\partial t} = -\nabla \cdot (\mu_p n_p \vec{E} - \mu_p \frac{k_b T}{q} \nabla n_p - \mu_p \frac{k_b n_p}{q} \nabla T) - (U - G). \tag{2}$$

where μ_n is the mobility of the N-type carrier and μ_p is the mobility of the P-type carrier. n_n is the N-type carrier concentration and n_p is the P-type carrier concentration. $\vec{E}$ is the electric field. t is the time. T is the temperature. k_b is the Boltzmann constant. q is the unit charge. U is the recombination rate of carriers. G is the ionization rate. For silicon devices, N-type carriers are electrons and P-type carriers are holes.

Both the Joule effect and the carrier ionization-recombination effect can generate the excess heat inside the semiconductor devices. The thermal generation process can be expressed as

$$\rho c_p \frac{\partial T}{\partial t} = k \nabla T + \vec{J} \cdot \vec{E} + (E_g + 3k_b T) \cdot (U - G). \tag{3}$$

where $\vec{J} \cdot \vec{E}$ is the Joule heat term. $(E_g + 3k_b T)(U - G)$ is the carrier ionization-recombination term. $\vec{J}$ is the current in a unit volume, defined as

$$\vec{J} = (\mu_n n_n + \mu_p n_p)\vec{E}. \tag{4}$$

In the carrier ionization-recombination term, the gas molecule approximation is applied, and $3k_b T$ denotes the average kinetic energy.

For the silicon material, when the temperature varies from the room temperature (300 K) to the melting point (1688 K), the intrinsic carrier concentration varies from about 1×10^{10} cm^{-3} to 3×10^{19} cm^{-3} [39]. so the change of the intrinsic carrier concentration is about 3×10^{19} cm^{-3} ($n_i \approx 3 \times 10^{19}$ cm^{-3}). In a unit volume, the influence of this term on the temperature rise can be expressed as

$$\Delta T = \frac{\Delta n_i (E_g + 3k_b T)}{\rho c_p}, \tag{5}$$

where c_p is the specific heat. ρ is the density. For silicon, $c_p = 0.6951$ J/g/K, $\rho = 2.32$ g/cm^3. By putting these parameters into (5), $T = 4.6$ K. Meanwhile, the temperature rise caused by the external electromagnetic energy is 1388 K. It is evident that the Joule effect is the primary heat generation mechanism in this problem. In the following, we neglect the carrier ionization-recombination term and focus on the Joule effect term.

The magnetic field effect is ignored in this paper for the following reasons:

i. The force generated by magnetic field is much smaller than that of electric field, so its influence on carrier motion can be ignored.

ii. The direction of the action of magnetic field force is perpendicular to the direction of motion, so there is no energy conversion and no heat is generated by the magnetic field force.

Although magnetic field is a very important factor in the EMC analysis of large equipments, for the electronic devices focused in this paper, the magnetic field effect is very small and can be ignored.

B. THERMAL MODEL OF A MOSFET

Unlike the PN junction devices, for the MOSFET, an insulator layer exists between the drain electrode and the source electrode. In the off state, there is nearly no current between the drain electrode and the source electrode. When a working voltage is applied to the gate electrode, the carriers are attracted by the electric field and form a laminal conductive channel connecting the drain electrode and the source electrode, as illustrated in Fig. 1. Current is concentrated in this laminal area. As mentioned above, the Joule effect is

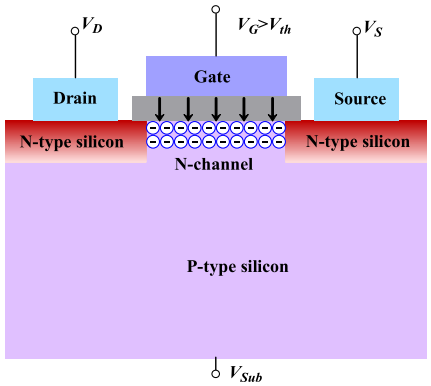

FIGURE 1. The N-channel consisting of electrons in an on-state MOSFET.

the primary heat generation mechanism, so the heat source locates in this laminal area.

The thermal PDE can be expressed as

$$c_p \rho \frac{\partial T}{\partial t} - K_{\mathrm{Si}} T = p_{ab}. \tag{6}$$

where p_{ab} is the power absorbed by the MOSFET in a unit volume. K_{Si} is thermal conductivity of Silicon. T is the temperature rise. In the steady state, the time derivative of temperature $\frac{\partial T}{\partial t}$ is 0, then (6) can be expressed as

$$-K_{\mathrm{Si}} T = p_{ab}. \tag{7}$$

The integral of (7) in the heat source zone is

$$\iiint_{source} -K_{\mathrm{Si}} T dV = P_{ab}. \tag{8}$$

In order to build a concise analysis model, two main hypotheses are introduced:

i. The boundary on which the channel contacts the SiO_2 is set to be adiabatic. Comparing to the conductivity of silicon, the thermal conductivity of SiO_2 is much lower, it is only 0.9% as that of silicon. It's a reasonable assumption to set this side of the boundary to be adiabatic.

ii. The heat generation region is set to be an infinitely thin layer. Both the results of physical analysis and numerical calculation show that the heat generation zone is confined to a thin layer in the channel. The thickness (less than 0.1 nm) is negligible compared with the scale of the channel (180 nm).

As shown in Fig. 2, the bottom boundary of the heat source is connected to the oxide insulator (SiO_2) and the top boundary is connected to the silicon substrate. While the thermal conductivity of SiO_2 is only 0.9% as that of silicon, most of the heat energy transfers from the top boundary. Then the bottom boundary is set to be adiabatic. (8) can be expressed as

$$K_{\mathrm{Si}} \frac{\partial T}{\partial y} LW = -P_{th}. \tag{9}$$

where L is the length of the heat source. W is the vertical width of the MOSFET.

The length L can be obtained by using these parameters in (9). The temperature distribution of this thermal model source is shown in the Appendix.

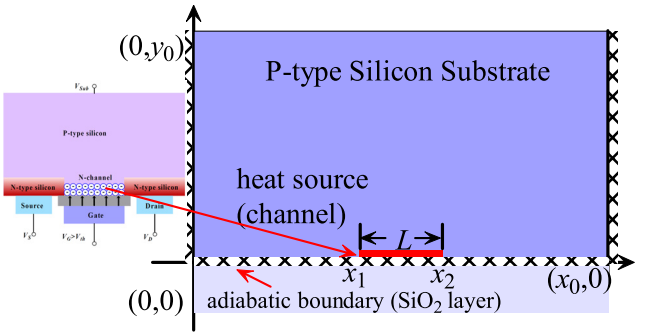

FIGURE 2. Model of the heat source.

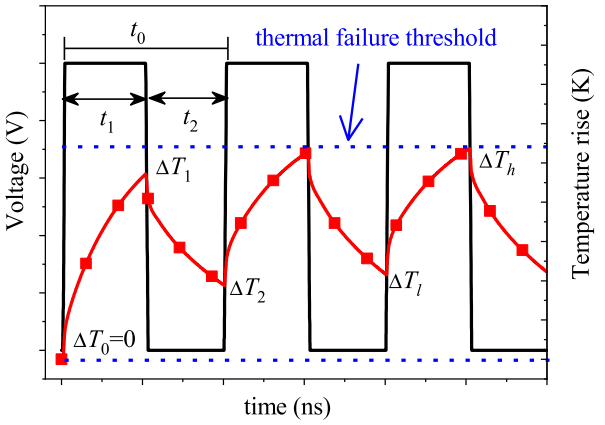

FIGURE 3. Temperature rise of the MOSFET under repetitive electromagnetic pulses. Thermal steady state is reached after a few durations.

C. TEMPERATURE RISE IN A MOSFET

The equation describing the temperature rise inside the device can be expressed as

$$\frac{\Delta T}{R_{th}} + C_{th} \frac{d(\Delta T)}{dt} = P_{ab}, \quad (where\ \Delta T = T - T_0), \tag{10}$$

where C_{th} is the thermal capacity. R_{th} is the thermal resistance. P_{th} is the total heat generation rate. T_0 is the initial temperature and is set to be 300 K. P_{ab} is the power absorbed by the MOSFET from the injected power P.

The solution of this non-homogeneous ordinary differential equation is [38]

$$\Delta T = C_0 e^{-\frac{t}{R_{th}C_{th}}} + R_{th} P_{ab}, \tag{11}$$

where C_0 is a constant determined by the initial condition.

As illustrated in Fig. 3, in a pulse duration t, during the duty course t_1, T increases from T_{2i} to $T_{2i+1} (i = 0, 1, 2 \cdots)$, and falls down from T_{2i+1} to $T_{2(i+1)}$ during t_2. In the first cycle, when $i = 0$, (11) can be expressed as

$$\Delta T_1 = (\Delta T_0 - R_{th} P_{th}) e^{-\frac{t_1}{R_{th}C_{th}}} + R_{th} P_{ab}, \tag{12}$$

$$\Delta T_2 = \Delta T_1 e^{-\frac{t_2}{R_{th}C_{th}}}, \tag{13}$$

the general expressions can be expressed as

$$\Delta T_{2i+1} = (\Delta T_{2i} - R_{th} P_{th}) e^{-\frac{t_1}{R_{th}C_{th}}} + R_{th} P_{ab}, \quad i = 0, 1, 2 \cdots, \tag{14}$$

$$\Delta T_{2(i+1)} = \Delta T_{2i+1} e^{-\frac{t_2}{R_{th}C_{th}}}, \quad i = 0, 1, 2 \cdots, \tag{15}$$

For the small scale (180 nm) of the MOSFET, the balance between heating and cooling can be reached in a short time (less than 1 μs). When the balance state is reached, the temperature rise oscillates between ΔT_h and ΔT_l. In a pulse cycle, ΔT increases from ΔT_l to ΔT_h during the duty time t_1, and falls down from ΔT_h to ΔT_l during t_2. Then (11) can be written as

$$\Delta T_h = (\Delta T_l - R_{th}P_{th})e^{-\frac{t_1}{R_{th}C_{th}}} + R_{th}P_{ab}, \tag{16}$$

$$\Delta T_l = \Delta T_h e^{-\frac{t_2}{R_{th}C_{th}}}, \tag{17}$$

The upper limit of the temperature rise can be derived as

$$\Delta T_h = \frac{1 - e^{-\frac{t_1}{R_{th}C_{th}}}}{1 - e^{-\frac{t_0}{R_{th}C_{th}}}} R_{th}P_{ab}, \tag{18}$$

When the pulse voltage V is injected to the gate electrode, the absorbed power can be obtained by

$$P_{ab} = \int_{V_{channel}} \vec{J}(\vec{r}) \cdot \vec{E}(\vec{r}) dv = I_{DS} \int_{l_{drain}}^{l_{source}} E_l dl = I_{DS} V_{DS}. \tag{19}$$

where I_{DS} is the current in a MOSFET [39]

$$I_{DS} = (\frac{W}{L})\mu_n C_{ox}(V_G - V_{TH} - \frac{V_{DS}}{2})V_{DS}. \tag{20}$$

III. STRUCTURAL PARAMETERS AND MOBILITY MODEL OF THE MOSFET

A. STRUCTURAL AND DOPING PARAMETERS OF THE DEVICE

Numerical simulations are used to study the thermal effect of semiconductor devices [29]. Commercial software and self-developed programs base on DDM are used to solve the PDEs of devices [30], [32]. Here, numerical simulations are taken to verify the failure model by a TCAD simulator GSRES (the General Simulator of Radiation Effect of Semiconductor) [40], which is developed by our team to study the electromagnetic radiation effect on electronic devices and circuits. The PDEs are solved by the finite volume method in this code. The GSRES has been used for more than 10 years in colleges and research institutes, and the device model library of GSRES has been proofread by comparing the simulated results to the results of Medici and Sentaurus TCAD.

The device parameters of a typical N-type channel MOSFET are set according to the 180 nm manufacturing process as shown in Fig. 4. The MOSFET is uniform in the vertical direction and the vertical width W is 1 μm. Four electrodes of the MOSFET are connected with external signals. The gate electrode consists of polycrystalline silicon. The electrodes of drain, source, and substrate consist of aluminum. The thickness of the insulator layer between the gate electrode and the substrate is 0.005 μm. This insulator layer consists of oxide (SiO_2). The spacers consist of Nitride (Si_3N_4). The length of the conduct channel is 0.18 μm.

The substrate of this MOSFET consists of a bulk silicon with a P-type doping concentration varying from 1.0×10^{18} cm^{-3} in the channel to 5.0×10^{16} cm^{-3} in the substrate. Two N-type silicon zones are under the electrodes of drain and source respectively. N-type impurities 1.0×10^{20} $cm^{-3}$are doped into these zones. The doping profile in the N-type silicon zone and the substrate along the cutline is illustrated in Fig. 5. Thermal boundaries of the three metal electrodes are set to be the thermal flux boundaries. The thermal conductance coefficient h is 1000 $W{\cdot}cm^{-2}{\cdot}K^{-1}$. Other boundaries are adiabatic.

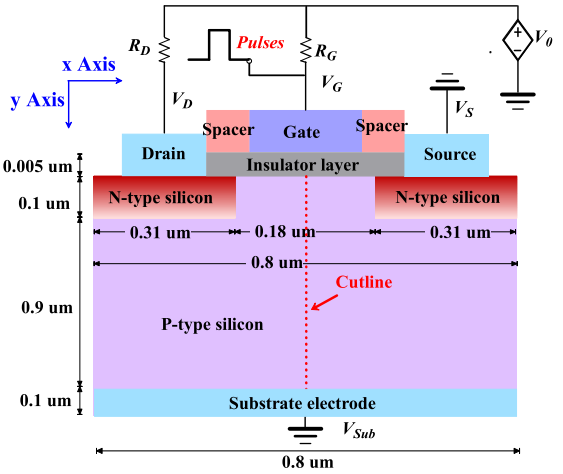

FIGURE 4. Schematic of a 180 nm N-type channel MOSFET in the TCAD simulation.

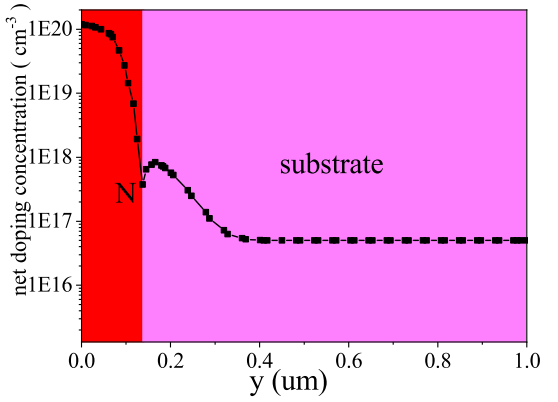

FIGURE 5. Doping profile in the N-type silicon and the substrate along the cutline in Fig. 4.

The working voltage is applied to the drain electrode. The source electrode and the substrate electrode are set to be grounded. The repetitive electromagnetic pulses are injected into the gate electrode.

B. MOBILITY MODEL FOR MOSFETS UNDER HIGH ELECTRIC FIELD

Because of the surface roughness scattering and the acoustic phonon scattering, the mobility model for PN junction device is not suitable for MOSFETs. The Lombardi mobility model [34], [35] is used in the simulation. This mobility model can be described as a sum of three terms [34], [35]

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}}, \tag{21}$$

where μ_b is the carrier mobility in bulk silicon. μ_{ac} is the carrier mobility corresponding to acoustic phonons scattering

TABLE 1. Parameters of Mobility of Silicon.

Parameters	n-type (electron)	p-type (hole)
$\mu_{min}(cm^2(V\cdot s)^{-1})$	55.24	49.70
$\mu_{max}(cm^2(V\cdot s)^{-1})$	1429.23	479.37
α	-2.2	-2.2
β	-3.8	-3.7
γ	0.8	0.8
v_{s0}(cm/s)	2.4×10^7	2.4×10^7
$n_{d\text{-}total}$	the total doping concentration	
n_{ref} (cm^{-3})	1.072×10^{17}	1.606×10^{17}

in the inversion. μ_{sr} is the carrier mobility corresponding to the surface roughness scattering. The bulk mobility can be expressed as [34], [35]

$$\mu_b = \mu_0 \exp(-\frac{P_c}{N_{tot}}) + \frac{\mu_{\max} - \mu_0}{1 + (N_{tot}/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s/N_{tot})^{\beta}}, \quad (22)$$

$$\mu_{\max} = \mu_2(\frac{T}{300K})^{\xi}. \quad (23)$$

The acoustic phonon limited mobility component can be expressed as [34], [35]

$$\mu_{ac} = \frac{B}{E_{\perp}} + \frac{CN_{total}^{\lambda}}{T\sqrt[3]{E_{\perp}}}, \quad (24)$$

where $E_{\perp}$ is the transverse component of the electric field.

The surface roughness limited mobility can be expressed as [34], [35]

$$\mu_{sr} = \frac{D}{E_{\perp}^{\gamma}}. \quad (25)$$

The Caughey-Thomas expression is used for the velocity saturation in high-field as [34], [35]

$$\mu = \frac{\mu_0}{[1 + \left(\frac{\mu_0 E_{//}}{v_s}\right)^b]^{1/b}}, \quad (26)$$

where [34], [35]

$$v_s(T) = \frac{v_{s0}}{1 + \gamma \exp(\frac{T}{600K})}, \quad (27)$$

here $E_{//}$ is the electric field parallel to the current flow. For silicon, the parameters are listed in TABLE 1.

The thermal conductivity of silicon is temperature dependent. In the simulation it is fitted as

$$K_{Si}(T) = \frac{1}{(a + b * T + c * T^2)}, \quad (28)$$

where a, b, and c are empirical parameters. Here they are set as follows: $a = 3.0\times10^{-2}$cm$\times$K$\times$S/J,$b = 1.56\times10^{-3}$cm$\times$S/J, and $c = 1.65\times10^{-6}$cm$\cdot$S/J/K. The fitted values agree well with the measured results [33]. Thermal parameters for the MOSFET are listed in TABLE 2.

C. FAILURE MECHANISM OF MOSFETs

For MOSFETs and other silicon devices, there are two failure mechanisms which will make the device to the deviant state or even breakdown:

i. The intrinsic carrier excitement in a MOSFET can cause the device breakdown before the silicon material burnout

TABLE 2. Thermal Parameters of Components of MOSFET.

Parameters	Parameter name	Value
ρ(Si)	Density of Si	2.32 g/cm^3
c_p (Si)	Specific heat of Si	0.6951 J/g/K
K_{Si}(300K)	Thermal conductivity of Si at 300K	1.547 W/cm/K
$\rho(SiO_2)$	Density of SiO_2	2.2 g/cm^3
c_p (SiO_2)	Specific heat of SiO_2	0.966 J/g/K
K_{SiO2}	Thermal conductivity of SiO_2	1.40×10^{-2} W/cm/K
ρ(Al)	Density of Al	2.7 g/cm^3
c_p (Al)	Specific heat of Al	0.897 J/g/K
K_{Al}	Thermal conductivity Al	2.27 W/cm/K
ρ(Ni)	Density of Nitride (Si_3N_4)	3.44 g/cm^3
c_p (Ni)	Specific heat of Nitride(Si_3N_4)	0.170 J/g/K
K_{Ni}	Thermal conductivity Nitride(Si_3N_4)	1.85 W/cm/K

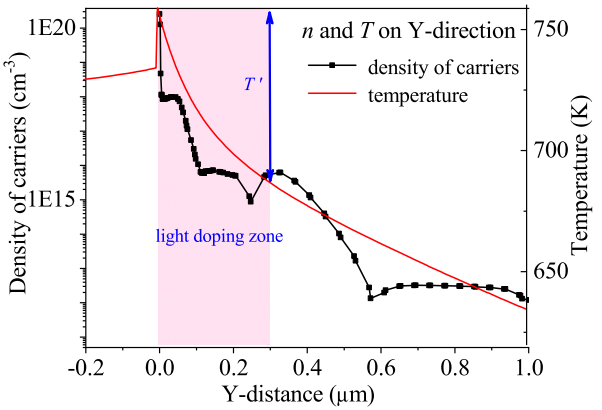

FIGURE 6. Distributions of T and n inside the MOSFET along the y axis direction (normal to the channel).

at the melting point (1688 K). The failure threshold of this mechanism can be dominated by an experimental equation as follows [41]:

$$n_i(T) = 3.88\times10^{16}\times T^{3/2}\times\exp(-\frac{7000K}{T})\cdot cm^{-3}. \quad (29)$$

The two heavy doping zones at the concentration of 1.0×10^{20} cm^{-3} are under the source electrode and the drain electrode, respectively. The light doping zone is in substrate and the doping concentration varies from 1.0×10^{18} cm^{-3} to 5.0×10^{16} cm^{-3}. So in the light doping zone, the failure temperature is 727 K at 5.0×10^{16} cm^{-3}. Meanwhile, the highest temperature of the MOSFET is in the channel. As illustrated in Fig. 6, T' is the difference between the temperatures in the channel and the temperature in the light doping zone (5.0×10^{16} cm^{-3}). The general failure threshold of this mechanism is 727K $+T'$.

ii. Although the melting point of silicon is hard to reach, that of aluminum 933 K [33] is much lower. However, when the temperature in the substrate reaches the failure temperature at 727 K, the temperature of aluminum electrodes is still lower than the melting point.

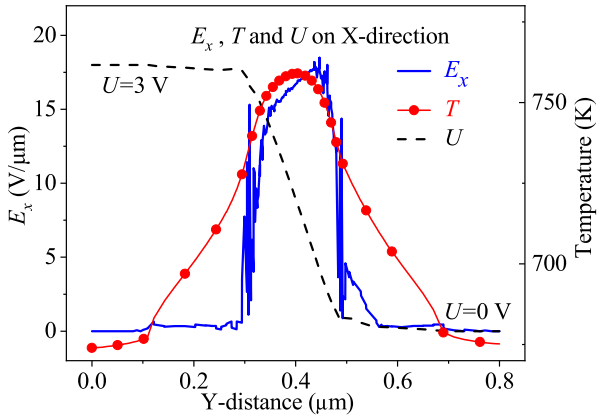

FIGURE 7. Distributions of E_x, T and U inside the MOSFET.

By synthesizing the analyses above, it is clear that the primary failure mechanism of the MOSFET is the intrinsic carrier thermal excitement. Consequently, $T_{max} = 727\text{K} + T'$ is a dependable and convenient failure threshold of this device, where T_{max} is the highest temperature inside the MOSFET.

If randomness factors are ignored and all devices are assumed to be uniform, the failure of the MOSFET can be considered as a binomial (failure or success) process. The failure probability function $F(T)$ can be defined as:

$$F(T) = \begin{cases} 0, & T < T_{\max} \\ 1, & T \geq T_{\max} \end{cases} \tag{30}$$

IV. SIMULATION AND RESULTS

A. COMPARISON OF RESULTS BETWEEN THE TCAD SIMULATION AND THE THEORETICAL MODEL

In this part, the TCAD simulation results of the MOSFET under the injected pulse is compared to the results from the theoretical model.

Fig. 6 shows the distributions of T and n in the y axis direction from the TCAD simulation, where n is the total carrier concentration. The directions of x axis and y axis are defined in Fig. 4. Carriers are localized in a lamina in the channel. Since the channel consists with carriers, the current is localized in this lamina, too. The thickness of the channel is 0.01 μm. T' is about 80 K as shown in Fig. 6. It means when light doping zone reaches the failure temperature at 727 K, the highest temperate T_{max} of the MOSFET is 727 K+80 K = 807 K in the channel.

Fig. 7 shows the distributions of electric field parallel to the channel E_x,, temperature T in the x axis direction and electric potential U from the TCAD simulation. It is clear that the current and the heat are both concentrated in the lamina. The TCAD results match to the theoretical analysis.

The length of the laminal heat source can be derived from (9), the mean value of $\partial T/\partial y$ is 0.87 K/nm. The thermal conductivity K_{si} is set to be 0.465 W/cm/K at 755 K. Putting these parameters into (9) obtains $L = 160.2$ nm.

The temperature distribution of the TCAD simulation and that of a theoretical analysis of the thermal model are compared in Fig. 8. Figs. 8 (a) and (b) are derived from the TCAD

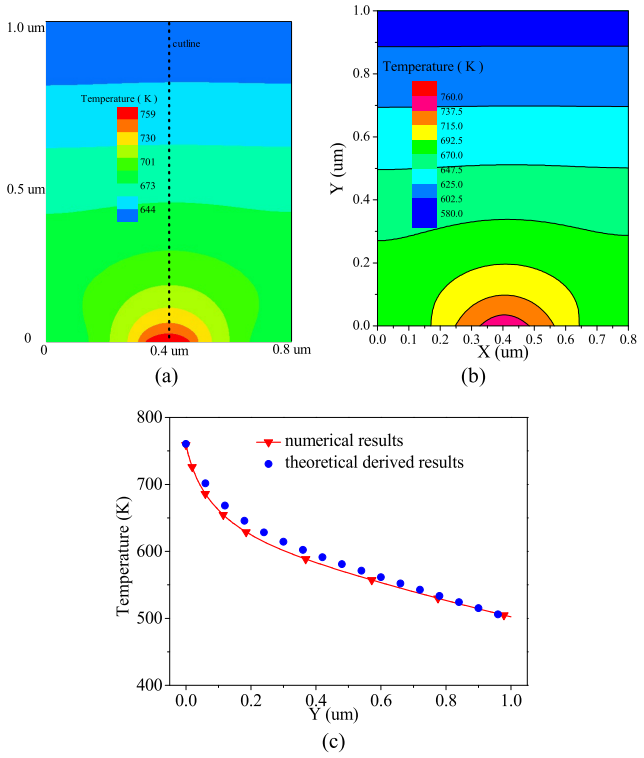

FIGURE 8. Temperature distribution in the MOSFET. (a) Results from the TCAD simulation. (b) Results from the theoretical model. (c) Comparison between the results from the TCAD simulation and the theoretical model.

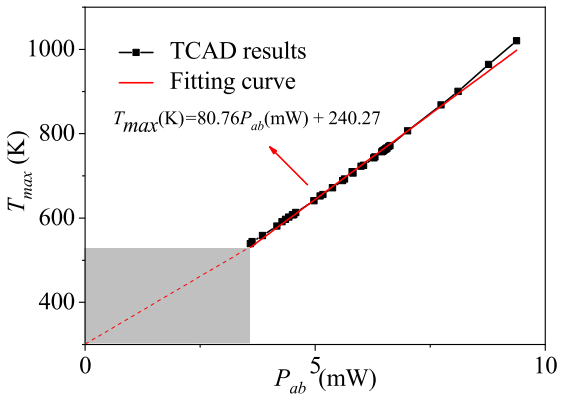

FIGURE 9. TCAD results agree well with the theoretical thermal resistance equation from (30).

simulation and the theoretical analysis of the thermal model respectively, the maximums and the tendencies of the temperature distribution agree well. The small difference come from the two main hypotheses of the model as mentioned in Sec. II B.

Because thermal conductivity of silicon is temperature dependent, it is hard even impossible to calculate the thermal resistance of the MOSFET directly. However, it can be derived from (11) by the limit of $t \to \infty$ as

$$\Delta T = R_{th} P_{ab}, \quad t \to \infty, \tag{31}$$

The results are illustrated in Fig. 9, the equation can be expressed as

$$T_{max} == 80.76 P_{ab}(\text{mW}) + 240.27\text{K}. \tag{32}$$

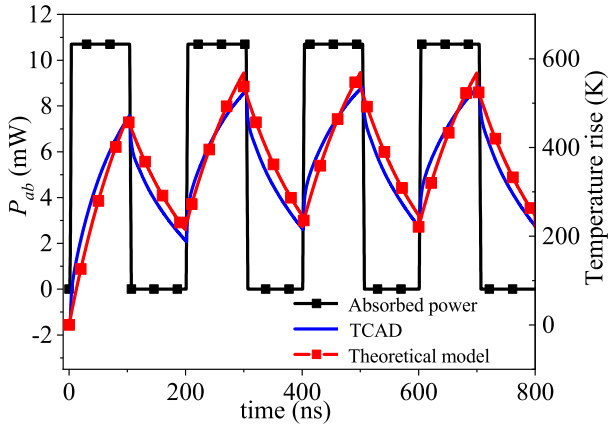

FIGURE 10. Comparison of the maximum temperature from the TCAD simulation and the theoretical model. The MOSFET is under a 200 ns and 100 ns duty course duration pulse. (t_0 = 200 ns, t_1 = 100 ns).

The thermal resistance R_{th} of the MOSFET is 80.76 K/mW. The intercept term is 240.27 K here because the thermal conductivity is temperature dependent. The data used in the fitting is from 540 K to 1020 K, so this equation is suitable and reliably in this temperature range. As discussed above, most of the failures happen in this temperature range. This equation is linear, so only two sets of data are needed to fit this analytic expression. The costs of experiment and numerical simulation can be remarkably reduced.

In the theoretical expression, thermal capacity of the MOSFET is needed. The thermal capacity C_{th} can be calculated directly as

$$C_{th} = C_{Si} + C_{Al} + C_{Ni}. \tag{33}$$

The value of C_{th} can be calculated by the structural parameters illustrated in Fig. 4. and the thermal parameters shown in TABLE 2. The volume of the silicon part is $1.0 \times 1.0 \times 0.8 = 0.8\text{um}^3$, then C_{si} is 1.29×10^{-12}J/K. In the same way, C_{Al} is 0.29×10^{-12}J/K, C_{Ni} is 0.069×10^{-12}J/K. Then the total thermal capacity C_{th} of the MOSFET is 1.649×10^{-12}J/K.

C_{th} can also be derived from the theoretical model. By fitting the TCAD results, the value of C_{th} is 1.595×10^{-12}J/K. The values from two different ways agree well. The temperature curves calculated by the TCAD simulation and the theoretical model agree well too, as shown in Fig. 10.

B. INFLUENCE OF PULSE PARAMETERS

Because of the small scale of the MOSFET, thermal balance state is reached in a short time. The upper limit of the temperature is reached in 1 or 2 cycles as shown in Fig. 11. Nearly no temperature rise occurs after the first two pulses. The temperature rise versus the repetitive number of pulses is illustrated. It is evident that the failure of the MOSFET happens in 1 or 2 cycles. If the temperature cannot reach the failure point in 1 or 2 cycles, no failure will happen even after a very long time.

Fig. 12 shows the temperature versus time under pulses with different duty courses. The pulse width is 400 ns. A longer duty course results in a higher temperature. For the long width (t_0 = 400 ns), heat accumulation reaches to a balance state, and nearly no temperature rise occurs after the first pulse cycle.

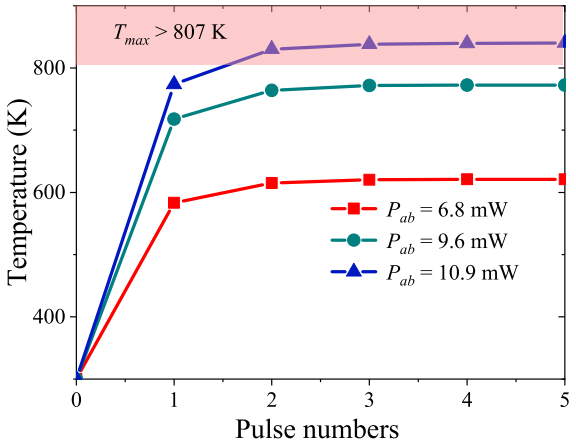

FIGURE 11. Influence of the repetitive number of pulses. Upper limit of the temperature is reached in 1 or 2 cycles. (t0 = 200 ns, t1 = 100 ns).

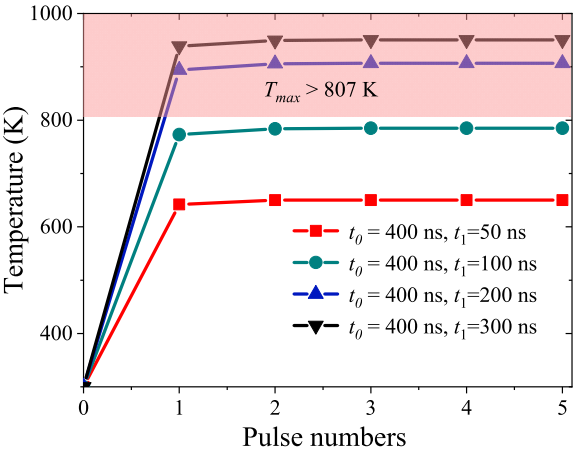

FIGURE 12. Influence of the duty course. t_0 = 400 ns. The duty cycle time t_1 are 50 ns, 100ns, 200ns, 300ns, respectively. P_{ab} = 10.9 mW.

Influence of the pulse width is illustrated in Fig. 13. The duty cycle time t_1 is set to be 100 ns. The pulse width t_0 are 50 ns, 100ns, 200ns, 300ns, respectively. A longer pulse width results in a lower temperature. For the long width (t_0 = 400 ns), heat accumulation reaches to a balance state, and nearly no temperature rise occurs after the first pulse cycle.

V. DISCUSSIONS

A. DISCUSSION ON THE HEAT DISSIPATION PERFORMANCE OF THE SUBSTRATE

As mentioned in Section II, most of the heat transfers through the substrate. Cooling the MOSFET become more efficient by increasing the heat dissipation performance. Higher heat dissipation performance of the substrate can result in a higher survivability of the MOSFET against external electromagnetic pulses. Fig. 14 shows the temperature rise versus the thermal conductance coefficient of the substrate h. Under a same injection pulse, no failure occurs when h is greater than 2000 $\text{W}\cdot\text{cm}^{-2}\cdot\text{K}^{-1}$. If the manufacturing process of the substrate interface is improved, or material with a higher thermal

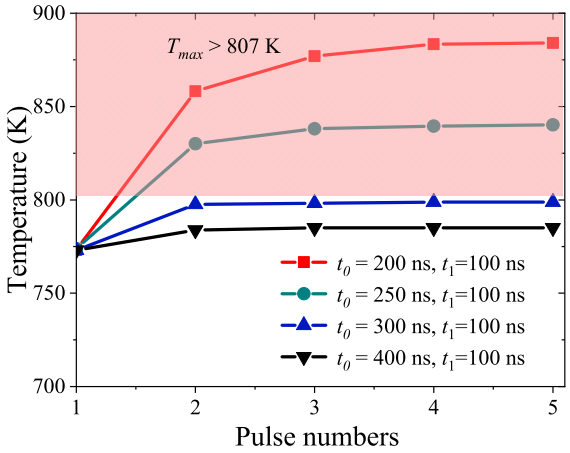

FIGURE 13. Influence of the pulse width. $t_1 = 100$ ns. The pulse width t_0 are 50 ns, 100ns, 200ns, 300ns, respectively. $P_{ab} = 10.9$ mW.

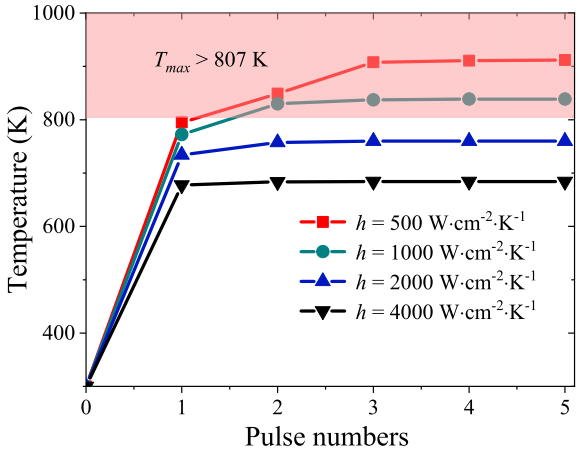

FIGURE 14. Influence of the heat dissipation performance of the substrate. $t_0 = 200$ ns, $t_1 = 100$ ns. $P_{ab} = 10.9$ mW.

conductance is used (for example, graphene and nanomaterials can significantly improve the heat dissipation performance of the devices [42], [43]), the device will be much more robust even immune against electromagnetic pulses. This is an encourage new for the EMC and EMI harden of electronic systems.

B. DISCUSSION ON THE ELECTRO-THERMAL COUPLED EFFECT OF MOSFETS

The thermal effect and the electric response in a semiconductor device under electromagnetic pulses are coupled. This means that the electrical properties of the material changes as the temperature rises. When the temperature rises, the carrier mobility in the MOSFET varies subsequently. A suitable mobility model must be selected to describe this coupled relationship. Fig. 15 shows the influence of mobility model. The simulation result by using the constant mobility, the result by using the Analytic Mobility Model which is widely used for PN junction device [36], and the result by using the Lombardi model are illustrated in Fig. 15. For the MOSFET, carrier mobility changes evidently when the temperature rises. This mechanism limits the current inside the MOSFET which

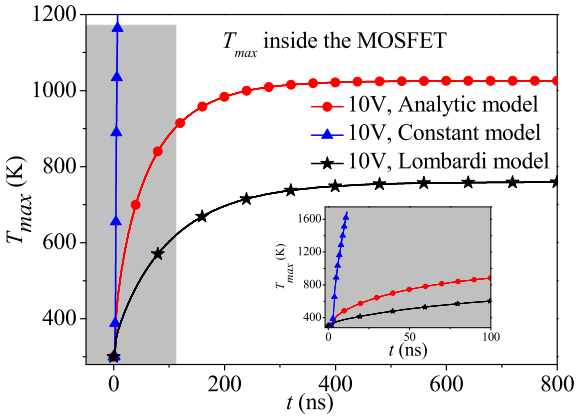

FIGURE 15. Maximum temperature in the MOSFET calculated by different mobility models. The injected voltage attached to the gate electrode is 10 V, and $V_{DS} = 3.0$ V.

determines the heat generation rate. Also, in the channel, the carrier mobility in the insulator-semiconductor interface is limited due to the surface-related scattering. Because of this scattering effect, the temperature dependency of a MOSFET is quite different from that of a PN junction device. Appropriate semiconductor model should be adopted in the simulation of MOSFETs.

VI. SUMMARY AND CONCLUSION

A thermal failure model for MOSFETs under repetitive electromagnetic pulses is studied in this paper. The analytic equation to analyze the relationship between the temperature rise and pulse parameters is given by a theoretical derivation. The electro-thermal process of a 180 nm MOSFET is numerically simulated as an example. It shows that the theoretical model agrees well with the TCAD results. Some discussions on the influence of the dissipation performance and on the electro-thermal coupled effect are given. Both the theoretical model and the TCAD simulation results indicate that most of the failures occur in 1 or 2 cycles. Further increase in the pulse number does not change the failure probability. Heat dissipation performance of the substrate is a key factor to upgrade the survivability of the device under injected pulses. This work is useful for further failure analysis, and is also helpful in the protection design for the MOSFET device and circuit under HPMs and other repetitive electromagnetic pulses.

APPENDIX

The PDEs to describe the temperature distribution of a laminal heat source can be expressed as

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} = 0 \tag{A-1}$$

$$\frac{\partial T}{\partial x} = 0, \quad x = 0 \text{ and } x = x_0 \tag{A-2}$$

$$-K_{\mathrm{Si}} \frac{\partial T}{\partial y} = hT, \quad y = y_0 \tag{A-3}$$

$$T = f(x), \quad y = 0,\ x_1 \le x \le x_2 \tag{A-4}$$

where $f(x)$ is the boundary condition of y $=$ 0. h is the thermal conductance coefficient of the thermal flux boundary.

According to the boundary conditions, the general solution of (A-1) can be expressed as

$$T(x,y) = C_0 + C_1 y + \sum_{n=1}^{\infty} \cos\frac{n\pi x}{x_0}\left[A_n \exp(\frac{n\pi y}{x_0}) + B_n \exp(-\frac{n\pi y}{x_0})\right] \quad \text{(A-5)}$$

where C_0 and C_1 are constants derived from the boundary condition, and can be expressed as

$$C_0 = \frac{1}{x_0}\int_0^{x_0} f(x)dx \quad \text{(A-6)}$$

$$C_1 = -\frac{h}{(K_{\mathrm{Si}} + hy_0)x_0}\int_0^{x_0} f(x)dx \quad \text{(A-7)}$$

The Fourier's series coefficients can be calculated as

$$A_n = \frac{K_{\mathrm{Si}}n\pi - hx_0}{K_{\mathrm{Si}}n\pi - hx_0 + \exp(\frac{2n\pi y_0}{x_0})(hx_0 + K_{\mathrm{Si}}n\pi)}F_n \quad \text{(A-8)}$$

$$B_n = \frac{\exp(\frac{2n\pi y_0}{x_0})(hx_0 + K_{\mathrm{Si}}n\pi)}{K_{\mathrm{Si}}n\pi - hx_0 + \exp(\frac{2n\pi y_0}{x_0})(hx_0 + K_{\mathrm{Si}}n\pi)}F_n \quad \text{(A-9)}$$

where F_n is an integral of cosine functions,

$$F_n = \frac{2}{x_0}\int_0^{x_0} f(x)\cos(\frac{n\pi x}{x_0})dx \quad \text{(A-10)}$$

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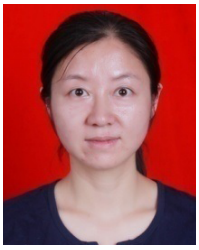

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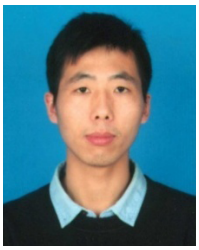

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