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A High Slew-Rate Enhancement Class-AB Operational Transconductance Amplifier (OTA) for Switched-Capacitor (SC) Applications

JAEDO KIM, (Graduate Student Member, IEEE), SEOKJAE SONG, (Graduate Student Member, IEEE), AND JEONGJIN ROH, (Senior Member, IEEE)
Department of Electrical Engineering, Hanyang University, Ansan 15588, South Korea

Corresponding author: Jeongjin Roh (jroh@hanyang.ac.kr)

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ABSTRACT This article presents a class-AB operational transconductance amplifier (OTA) with a high slew rate. The proposed class-AB OTA is applied with a slew-rate enhancement technique using an extremely low quiescent current. The additional current-reference common-mode feedback loop resolves the susceptibility to process, voltage, and temperature fluctuations resulting from slew-rate enhancement transistors. The proposed class-AB OTA is most widely used in block design, including, a switched-capacitor circuit, analog-to-digital converter, digital-to-analog converter, low-dropout regulator, and switched-capacitor DC-DC converters. In this study, performance was validated by applying the proposed class-AB OTA to a switched-capacitor delta-sigma modulator which requires high performance and high precision. The circuit was designed and simulated using a 0.18-μm complementary metal-oxide semiconductor process.

INDEX TERMS Operational transconductance amplifier, slew-rate, class-AB, delta-sigma modulator, feedforward architecture, switched-capacitor.

I. INTRODUCTION

Operational transconductance amplifiers (OTAs) are one of the most widely used blocks in analog circuit design [1]–[6]. The OTA is an essential structural component of a switched-inductor power converter, analog-to-digital converter, digital-to-analog converter (DAC), switched-capacitor circuit, low-dropout (LDO) regulator, analog output buffer, and liquid crystal display driver [5], [7]. For the circuit to operate successfully, the OTA must satisfy a large bandwidth, high gain, high slew rate, and low quiescent current. In particular, the power-to-performance ratio is one of the most important features of low-power OTAs for mobile applications [2]. As the OTA settling time is an important criterion for application, a number of theoretical analyses and modifications of the circuit structure have been performed to improve the transient responses of the OTA. However, circuit modification leads to greater parasitic effects and power consumption [5].

During the operation of switched-capacitor circuits, the transient response of the OTA circuit can be divided into deadtime, slewing, and settling, as shown in Fig. 1 [9]. The deadtime and settling periods are determined by a small-signal speed, and the unity-gain bandwidth (UGBW) of the OTA, in which the slewing operation varies accordingly. The settling time needed for the OTA output to lie within the desired error band is defined as the sum of the times required for each period. The slew-rate and UGBW of the OTA are proportional to the bias currents I_B and $\sqrt{I_B}$, respectively [10]. Increasing the bias current fosters the slewing operation of the OTA but increases power consumption, reduces DC gain, and decreases accuracy. The slew rate is defined as the ratio of the maximum output current to the load capacitance. Therefore, for a given load capacitance, one way to improve the slew rate is to increase the amount of bias current. However, this

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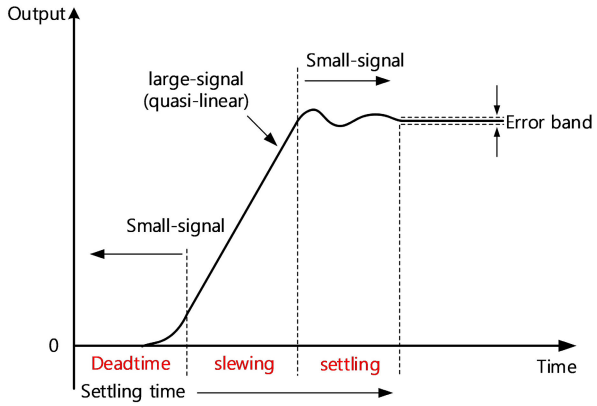


FIGURE 1. Transient response of the OTA under the unity-gain configuration.

approach results in the increased power consumption of the OTA. One solution to this problem is to adopt a class-AB OTA with an adaptive bias circuit, which temporarily increases the output current when needed, resulting in a low, well-controlled quiescent current [2].

Figure 2 shows the schematic of the conventional class-AB OTA [12]. In this article, an adaptive bias method and an additional current-reference common-mode feedback (CMFB) loop are used for the proposed class-AB OTA. The OTA is applied to a switched-capacitor delta-sigma modulator (SC-DSM) to verify the high slew rate and fast settling performance of the proposed OTA. Several factors produce harmonics in the digital output fast Fourier transform (FFT) spectrum of the SC-DSM [11]. Among these, the OTA performance of the first integrator applied to the SC-DSM has the greatest effect. If the OTA of the first integrator has a low slew rate, harmonic distortions occur in the output spectrum of the SC-DSM. Therefore, the proposed class-AB OTA is applied to the first integrator of an SC-DSM to improve performance. The rest of this article is organized as follows. Section II describes the design of the proposed class-AB OTA circuit and the implementation of the SC-DSM using OTA. Section III presents the experimental results of the proposed class-AB OTA applied to the SC-DSM chip. Section IV presents the conclusions of this study.

II. CIRCUIT DESIGN AND IMPLEMENTATION

A. CLASS-AB OTA WITH A HIGH SLEW-RATE ENHANCEMENT

The OTA is the most important block in the SC-DSM. In particular, the OTA of the first integrator plays the most important role in modulator performance [12], [13]. Therefore, the design of the SC-DSM requires a high-performance and power-efficient OTA structure. In this article, a new class-AB OTA is designed to improve the slew-rate performance. Equations (1)-(3) require an increase in R_{OUT} to achieve a high DC gain. To increase R_{OUT}, it is necessary to reduce the current in the output stage and to use a cascode topology. The proposed class-AB OTA implements the two methods mentioned above. In the conventional class-AB OTA, reducing the output current proportionally decreases g_m, so that the overall DC gain does not change. Additionally, reducing the output current directly contradicts the demand for a high slew rate. The solution is to add a control circuit to reduce the quiescent current of the output stage and increase the output current during large-signal operations [8].

Figure 3 shows the schematic of the proposed class-AB OTA. In the input stage of the proposed OTA, the current flowing through the M1 and M2 transistors are divided into M9, M13, M10, and M14. In the standby state, a significant portion of the drain-current of M2 flows into the current source M10. As a result, the small output current is generated by the current ratio of M14 and M34. Transistors M3-M6 and M11-M12 sense the input differential voltage and control the two voltage-controlled current sources M9 and M10. The dotted line at the bottom of Fig. 3 shows the slew-rate enhancement block. The proposed class-AB OTA has two cascaded G_m stages. In the first block G_{m1}, M3 and M4 receive differential inputs and convert them into current. The diode-connected M11 and M12 generate voltage through the received current. The voltage is converted back to current by M9 and M10. In the second block G_{m2}, M1 and M2 convert the input signal to current, similar to the operation of the G_{m1} block, but an additional current is injected from M9 and M10 of the G_{m1} block. The combined currents of M1, M2, M9 and M10 are converted to voltage by M13 and M14, and the voltage is mirrored to M33 and M34. The final output voltage is generated by the cascoded output stage.

The transconductance of the proposed class-AB OTA, G_m, and output resistance, R_{out}, can be expressed as follows [12]:

$$A_v = G_m \times R_{out} \tag{1}$$

$$\begin{aligned} G_m &= \frac{3}{2} \times g_{m1,2} \times \frac{A}{B} + \frac{3}{2} \times g_{m3,4} \times \frac{C}{D} \times \frac{A}{B} \\ &= \frac{3}{2} \times \frac{I_t}{V_{OD}} \times \frac{A}{B} \times \frac{(B+2C)}{(B+C+D)} \end{aligned} \tag{2}$$

$$\begin{aligned} R_{out} &= Ro_1 \| Ro_2 \| Ro_3 \\ Ro_1 &= g_{m37,38} \times r_{o37,38} \times r_{o35,36} \\ Ro_2 &= g_{m25,26} \times r_{o25,26} \times r_{o21,22} \\ Ro_3 &= g_{m29,30} \times r_{o29,30} \times r_{o33,34} \end{aligned} \tag{3}$$

where I_t is the tail current; V_{OD} is V_{GS}-V_{TH}, which indicates the overdrive voltage [10], [11]. The letters A, B, C, and D at the bottom of Fig. 3 represent the W/L ratio of each transistor. The size of M1 is equal to B+C, which is the sum of M9 and M13. The gain of the OTA can be adjusted by the W/L ratios of M9/M13 and M10/M14 using the above equations. The current through M9 and M10 is reused to increase the transconductance, and therefore the gain of the OTA.

The role of the bottom transistors M15-M18 is to generate a large drain-source voltage drop during the large-signal transient period. The increased gate-source voltage of M13 or M14 generates a significant output current by through the boosted current mirror operation. When the circuit settles

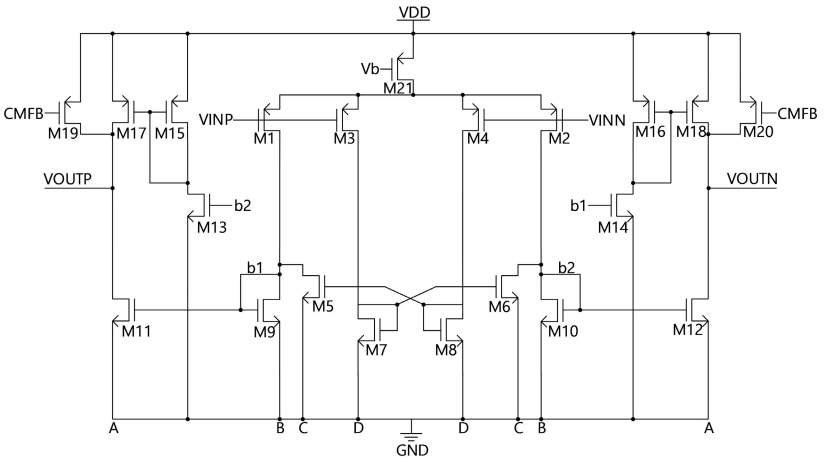


FIGURE 2. A conventional class-AB OTA.

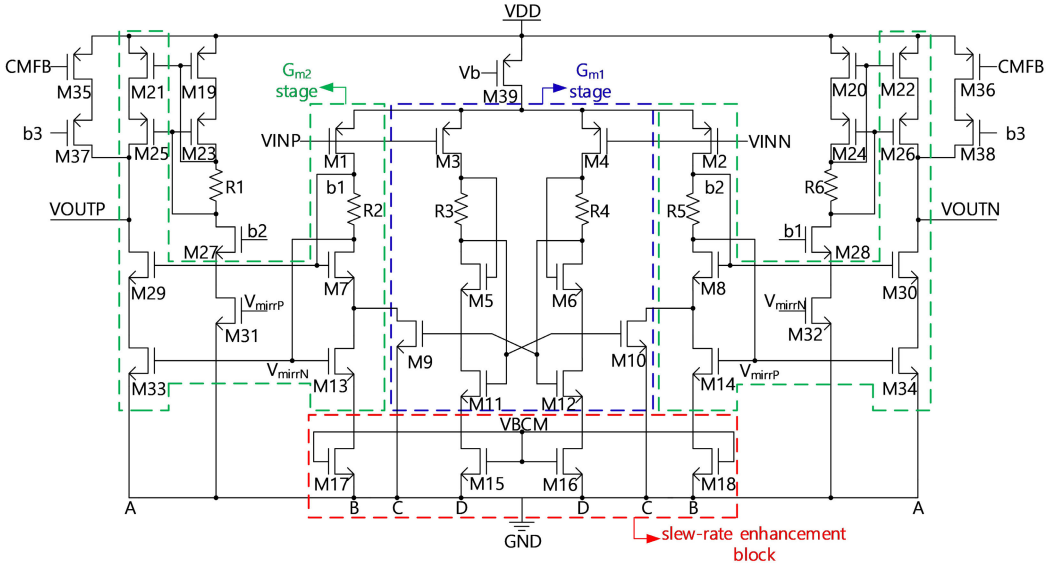


FIGURE 3. The proposed class-AB OTA.

down to steady-state conditions, the slew-rate enhancement transistors produce only a small drain voltage.

Figure 4 shows the drain-current versus drain-source voltage characteristic graph of the M15-M18 slew-rate enhancement transistors in Fig. 3. The transistor characteristics are similar to those of nonlinear resistors, which generate small drain-source voltages when the drain-current is small, and the drain-source voltages becomes large when the current increases [15]. The slew rate is improved by controlling the resistance and the voltage drop across it. In this article, the drain-source voltage range of the slew-rate enhancement transistor is from 2 mV to 320 mV. When the drain-source voltage is increased during a large-signal operation, a significant amount of current is mirrored to the output stage.

Figure 5 shows how the current-reference CMFB adjusts the slew-rate enhancement block. The CMFB circuit receives V_{mirrN}, and V_{mirrP} voltages and adjusts the slew-rate enhancement block. Owing to both the mismatch of the current mirrors, and the process, voltage, and temperature (PVT) fluctuations, the current ratio of the branches in the OTA may vary. The CMFB circuit senses V_{mirrN} and V_{mirrP} and generates the VBCM voltage so that the current through each branch of the proposed class-AB OTA stays within the predefined current ratio. The W/L size of the transistors M1, M2, and M3 of the CMFB block are exactly the same as those of the main amplifier M7, M13, M17 and M8, M14, M18, respectively. As a result, the current flowing through M13 and M14 in the OTA follows the IREF of the CMFB even with the PVT variations. The slew rate is improved by adjusting the

TABLE 1. Corner Model Simulation Results of the Proposed Class-AB OTA.

Corner	TT	FF	SS	TT	FF	SS	TT	FF	SS
Temperature (°C)	–40	–40	–40	27	27	27	125	125	125
UGBW (MHz)	194.3	214.0	171.4	172.5	188.5	154.2	146.6	161.0	131.4
Phase Margin (degree)	45.2	48.0	43.6	52.0	54.7	50.3	52.8	55.3	51.1
DC Gain (dB)	70.0	67.3	71.8	67.5	65.0	69.4	64.1	61.8	65.8

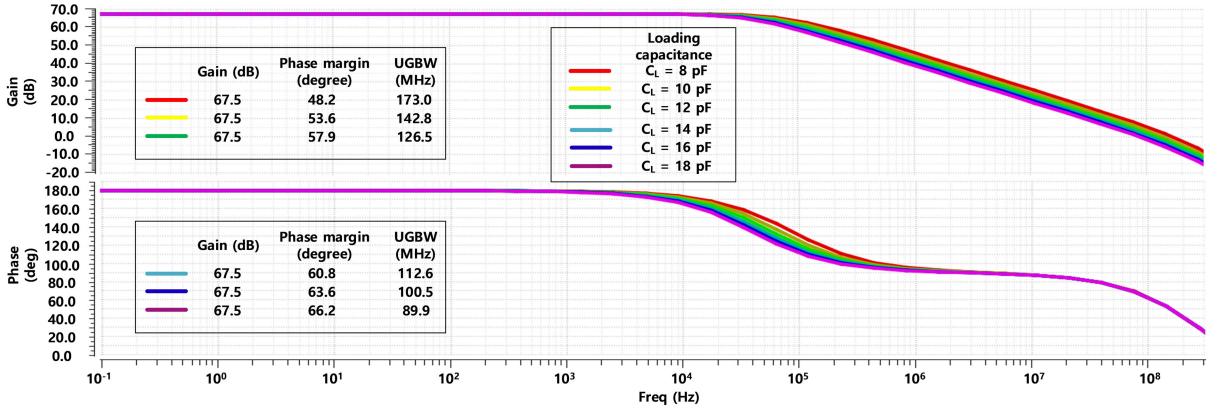


FIGURE 6. The open-loop AC simulation results of the proposed class-AB OTA.

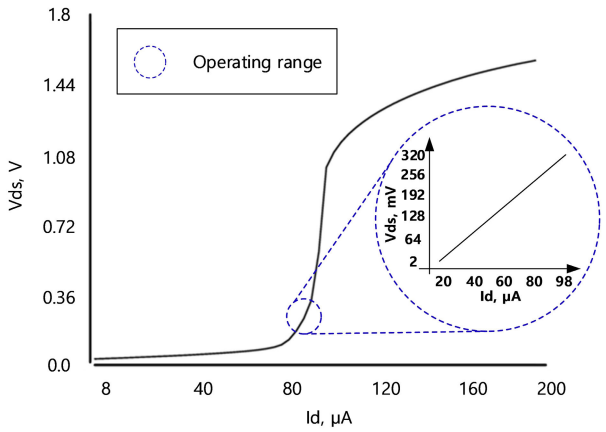


FIGURE 4. Drain-current versus drain-source voltage characteristic graph of a slew-rate enhancement transistor.

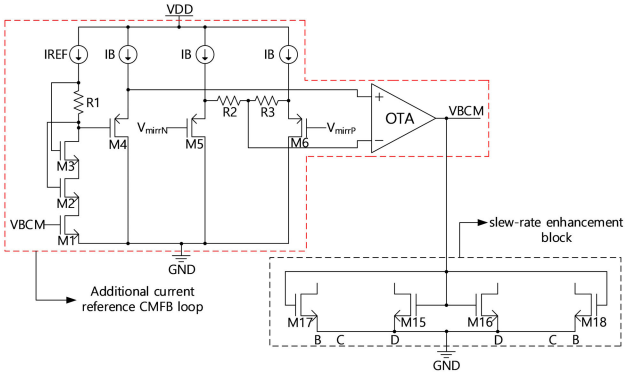


FIGURE 5. Current-reference CMFB to minimize the variation of the slew-rate enhancement block.

slew-rate enhancement block of the proposed class-AB OTA through the CMFB block Fig. 5.

B. PROPOSED CLASS-AB OTA SIMULATION RESULTS

Figure 6 shows the open-loop AC simulation results of the proposed class-AB OTA with 8pF, 10pF, 12pF, 14pF, 16pF, and 18pF load capacitors. In this article, an 8pF load capacitance is used. The proposed OTA AC simulation results show a DC gain of 67.5 dB, phase margin of 48.2 degrees, and UGBW of 172.5 MHz. It consumes less power than the conventional OTA but has a comparable DC gain, phase margin, and UGBW. Table 1 summarizes the AC simulation results of the OTA with different process and temperature corners.

Figure 7 shows the schematic of the switched-capacitor circuit with the proposed OTA. High-performance OTA is required for a fast and accurate operation. The clock signals for the switched-capacitor circuit are ϕ_1, ϕ_{1d}, ϕ_2, and ϕ_{2d}. Non-overlap timing is required so that the ϕ_1 and ϕ_2 switches are not turned on at the same time. Delayed clocks (ϕ_{1d}, ϕ_{2d}) are also generated to reduce the linearity problems caused by charge injection [10]. As shown in Fig. 7, the delay occurs only at the falling edge of the clock phase. To efficiently use the clock period, the falling clock edges are delayed, when the rising clock edges are synchronized [12], [13]. Here, C_{s1} and C_{DAC} are the sampling capacitors, and C_{I1} is an integrating capacitor.

Figure 8 shows the settling waveform of the class-AB OTA with and without a slew-rate enhancement block. The red line shows the waveform of the class-AB OTA with a slew-rate enhancement block, and the blue line is the waveform without the enhancement block. As shown in the figure, the class-AB OTA with a slew-rate enhancement block settles in a significantly shorter time than that without a slew-rate enhancement block. When the clock of the switched-capacitor is given by ϕ_1 and ϕ_2, the value of the load capacitance applied to the proposed OTA changes [14]. At the ϕ_1 clock, the equivalent load capacitance is 8pF, and at the ϕ_2, the equivalent load capacitance is 14pF. Figure 8 shows that settling is different between the ϕ_1 and ϕ_2 clocks. The proposed class-AB OTA provides excellent performance in terms of settling time and slew rate. The dotted line in Fig. 8 shows the non-overlapping period mentioned above. The OTA has a high UGBW of 172.5 MHz for the 12.8 MHz clock operation, and the circuit settles with sufficient accuracy [11].

In Fig. 8, $\triangle t_1$ and $\triangle V_1$ are the ramp waveform time and voltage changes, respectively, of the class-AB OTA with a slew-rate enhancement block, and $\triangle t_2$ and, $\triangle V_2$ are those without a slew-rate enhancement block. In general, a higher slew-rate is the better, although this is not always the case when the stability condition is not satisfied. When stability deteriorates, the overshoot/undershoot phenomenon occurs [10]. In the proposed OTA, such a phenomenon does not occur during the circuit operation.

The commonly used figures of merit, FOM_S and FOM_L, can be expressed respectively as follows [20]:

$$FOM_s = \frac{GBW \times C_L}{Power} \tag{4}$$

$$FOM_L = \frac{SR \times C_L}{Power} \tag{5}$$

where GBW is the gain-bandwidth, C_L is the loading capacitance, and SR is the slew rate. FOM_S and FOM_L are used to verify the small-signal and large-signal capabilities, respectively, among different amplifier topologies.

The proposed OTA's simulation results are summarized in Table 2. Owing to the designed slew-rate enhancement block, the OTA shows a better slew-rate performance than the other OTAs. To verify the performance of the OTA in a real circuit environment, the OTA is implemented in a switched-capacitor DSM circuit, which requires high-performance and high-precision analog blocks. A description of the implementation is described in the next part.

C. SC-DSM ARCHITECTURE APPLYING THE PROPOSED CLASS-AB OTA

This part describes the design of the SC-DSM with the proposed class-AB OTA. Figure 9 shows the SC-DSM architecture with the coefficient numbers. The cascade of integrators with feedforward (CIFF) architecture is used for low harmonic distortions [12]–[14]. The SC-DSM can process a 25 kHz signal bandwidth using a third-order modulator and a single-bit quantizer. It has an oversampling ratio (OSR) of 256 for the sampling frequency of 12.8 MHz.

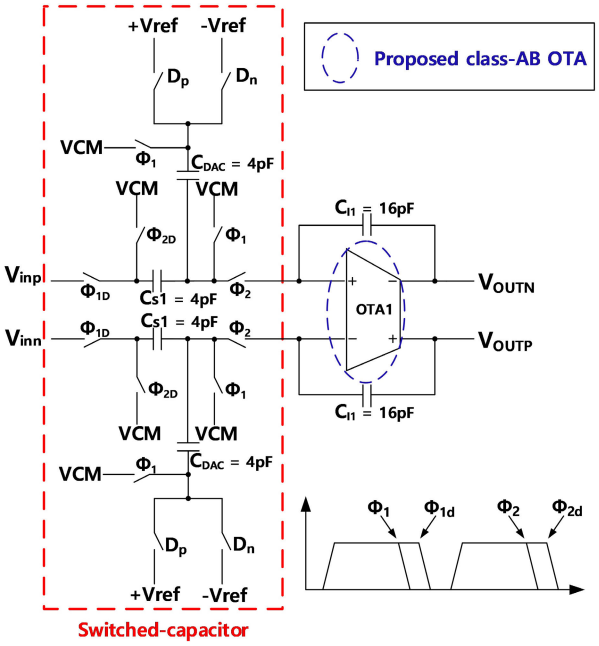


FIGURE 7. Switched-capacitor circuit with the proposed class-AB OTA.

The DSM architecture can be divided into CIFF architecture and cascade of integrators with feedback (CIFB) architecture. In the CIFF architecture, the input and the integrator signals are directly delivered to the quantizer through the feedforward paths. Here, the output voltage swing of each integrator decreases through the modulator's feedforward paths. Therefore, the voltage headroom requirements of the OTA are relaxed. In this article, the CIFF architecture is selected to validate the proposed OTA performance. For a stable operation, the peak gain of the noise transform function (NTF) should be less than 1.5 [11], [14].

As the SC-DSM requires a high resolution, OTAs should be designed with careful consideration of flicker noise. Figure 10 shows the transistors that affect flicker noise and the contribution chart in the proposed class-AB OTA. Among those that affect flicker noise, the input transistors are the most dominant. The larger the transistor size, the smaller the effect of flicker noise [10]. The chopper-stabilization technique is applied to reduce the input-referred noise of the OTA, in addition to the large transistor sizes. Chopping is applied to the input and output of the OTA of the first integrator, which is the most critical block in the DSM.

Figure 11 shows the overall schematic diagram of the SC-DSM. The dotted line in the figure represents the proposed OTA and chopping. The OTA is applied to the most important first integrator in the SC-DSM [12], [13]. The high slew rate and fast settling time of the OTA are important to SC-DSM. The performance of the proposed OTA is verified by designing and measuring the high-performance SC-DSM.

III. EXPERIMENTAL RESULTS

This section shows the experimental results of the designed SC-DSM with the proposed OTA inside of it. The third-order single-bit CIFF SC-DSM is designed and manufactured

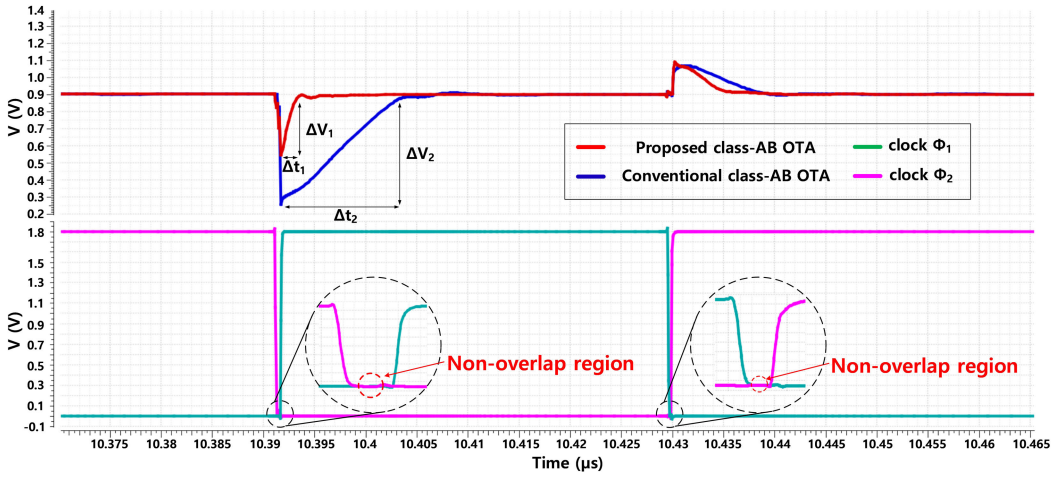


FIGURE 8. Comparison of the settling waveforms of the class-AB OTA with and without a slew-rate enhancement block.

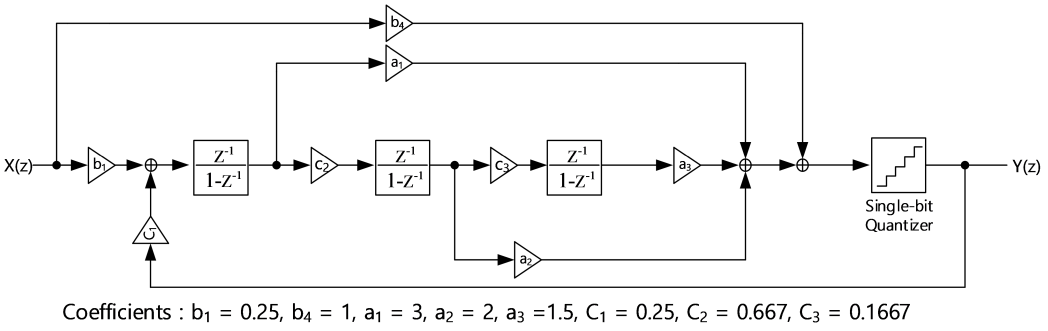
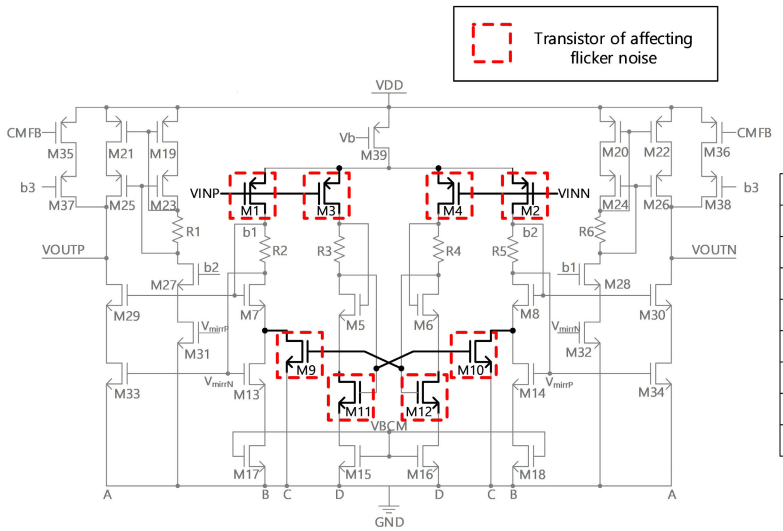


FIGURE 9. The third-order CIFF SC-DSM architecture.



Transistor	Noise contribution	% of total
M3	0.14	27.61
M4	0.14	27.61
M11	0.07	14.61
M12	0.07	14.61
M1	0.025	4.73
M2	0.025	4.73
M9	0.011	2.18
M10	0.011	2.18

FIGURE 10. Transistors affecting the flicker noise and contribution chart of the proposed class-AB OTA.

through a 0.18-μm complementary metal-oxide semiconductor (CMOS) process. Figure 12 shows the test bench of the SC-DSM chip with the proposed class-AB OTA. A signal generator, function generator, power supply, logic analyzer, and personal computer (PC) are used for the measurement. A fully differential input sine wave is generated using a signal

TABLE 2. Summary of the OTA Measurement Results and Performance Comparison.

Parameter	Conventional OTA*	Proposed OTA*	[16]	[17]*	[18]	[19]	[20]
Technology	0.18-μm	0.18-μm	0.18-μm	40-nm	0.18-μm	0.18-μm	0.18-μm
Supply voltage (V)	1.8	1.8	1.8	1.2	1.8	1.8	1.8
DC gain (dB)	66	68	72	51.5	98	54.9	105.5
Phase margin (degree)	48.7	48.2	50	59	71	79.8	53
Load capacitance (pF)	8	8	200	0.5	100	5.6	5
UGBW (MHz)	171	172.5	86.5	347	21	70.4	231.77
Slew-Rate (V/μs)	52.9	212.5	74.1	538.3	51	48.1	13.25
0.1 Settling Time (μs)	0.021	0.0042	–	0.01209	–	0.028	0.099
Power consumption (mW)	1.22	1.18	11.9	0.127	3	0.72	0.85
Area (mm^2)	0.034	0.036	0.070	0.391	0.053	3.0018	0.45
FOM_S (MHzpF/mW)	1,121	1,169	–	–	–	492.8	1,214
FOM_L ((V/μs)pF/mW)	346	1,440	1,245	–	–	336.7	78

*Simulation results.

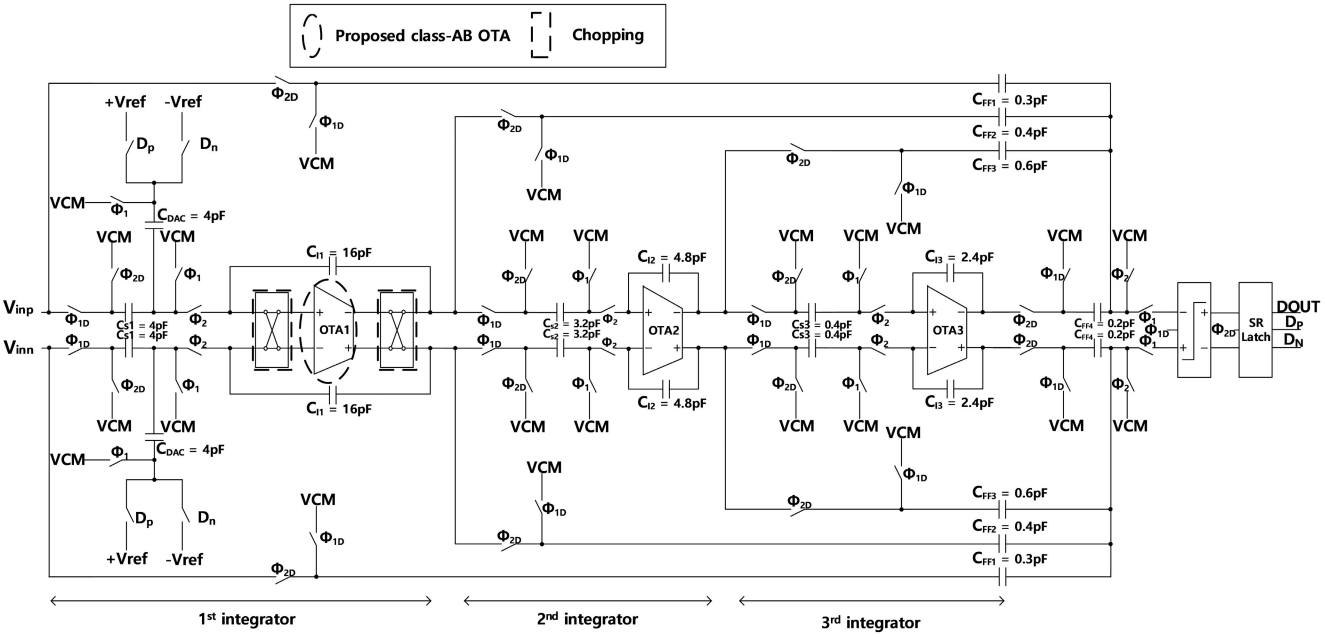


FIGURE 11. Schematic of the third-order CIFF single-bit SC-DSM.

generator. The clock signal is generated using a function generator. The generated clock frequency is 12.8 MHz. The digital outputs are stored in the memory of the logic analyzer and transferred to a PC for processing.

Figure 13 shows a microphotograph of the proposed OTA applied to an SC-DSM chip. The layout of the OTA and the switched-capacitor circuit of the SC-DSM is presented. The area of the OTA is 0.036 mm^2, and the total area of the SC-DSM is 1.19 mm^2. To improve the performance of the modulator, the layout uses a differential technique to reduce common-mode interference. The differential input transistors of the proposed OTA use a common-centroid layout technique to improve matching performance [10].

TABLE 3. Experimental Results of the Circuit for the SC-DSM.

Parameter	Value
Supply voltage (V)	1.8
Signal bandwidth (kHz)	25.0
Sampling frequency (MHz)	12.8
Power consumption (mW)	1.9
Peak SNR (dB)	90.7
Peak SNDR (dB)	90.1
Dynamic range (dB)	92.1

Figure 14 shows the measured digital output FFT spectrum of the SC-DSM chip. The number of samples is 64k, and the input frequency is 5.18 kHz. The chip measurement

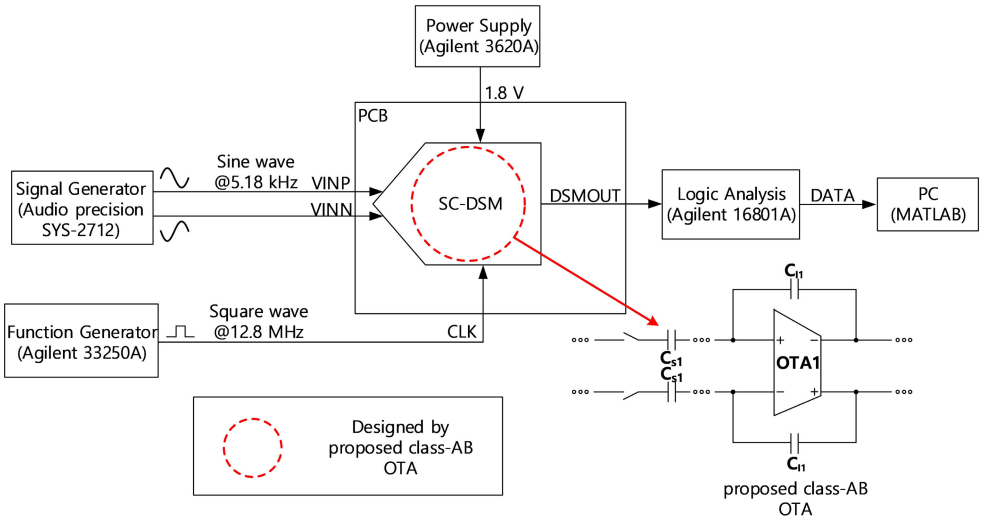


FIGURE 12. Test bench.

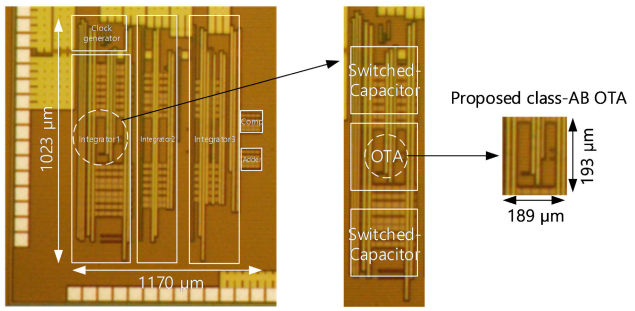


FIGURE 13. Chip microphotograph.

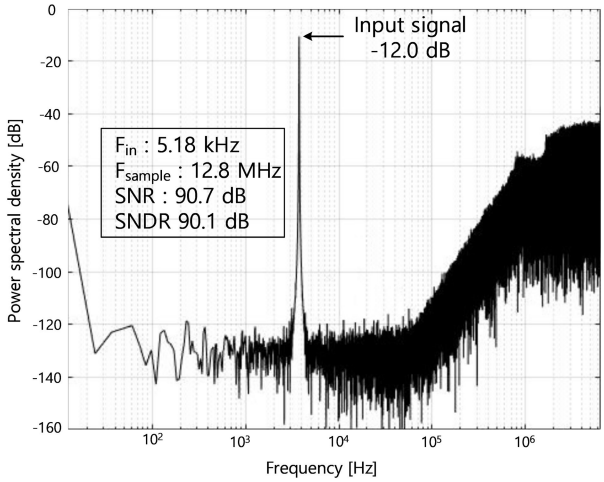


FIGURE 14. Measured output FFT spectrum of the SC-DSM chip.

results of the SC-DSM using the proposed OTA show a signal-to-noise ratio (SNR) of 90.7 dB, signal-to-noise and distortion ratio (SNDR) of 90.1 dB, and dynamic range (DR) of 92.1 dB. Table 3 summarizes the measured performance of the SC-DSM.

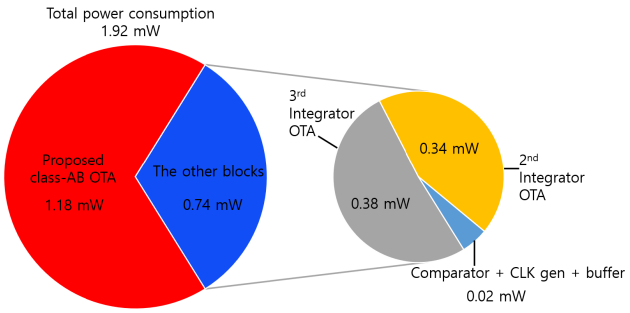


FIGURE 15. Power consumption of the proposed class-AB OTA and other blocks.

The proposed class-AB OTA consumes 1.18 mW of power. The power consumption of the other blocks is shown in Fig. 15. Most of the power consumption comes from the proposed OTA of the first integrator. As the OTA of the first integrator is the most important block for chip performance, 60 % of the total chip power is consumed by a single OTA. Using the proposed OTA, noise shaping is confirmed to works well, as shown in the digital output FFT spectrum of the SC-DSM. The performance of the proposed class-AB OTA is verified by high-performance measurements.

IV. CONCLUSION

The proposed class-AB OTA can be applied to the most widely used blocks in an analog design, such as switched capacitor circuits, oversampled delta-sigma data converters, and LDO regulators. In this article, the proposed OTA is used for the SC-DSM, in which the first integrator is the most important block for determining the performance of the overall circuit given that it consumes the most power. If the OTA of the first integrator has a poor slew rate and a low UGBW, harmonic distortions are observed at the digital output spectrum of the SC-DSM. For this reason, the performance of the

first integrator is improved using the class-AB OTA, which has good performance, high power efficiency, and improved slew rate. The current-reference CMFB loop for the proposed OTA resolves the vulnerability to PVT fluctuations because of the use of slew-rate enhancement transistors. By applying the chopper-stabilization technique to the first integrator, the noise proportional to 1/f, which is a problem when designing a high-accuracy circuit, is eliminated, thus improving the SNR and SNDR. The SC-DSM shows an SNDR of 90.1 dB and DR of 92.1 dB at a 25 kHz signal bandwidth when manufactured with a 0.18-μm CMOS process. These results confirmed the excellent performance of the proposed class-AB OTA applied to the SC-DSM, which requires high performance and high precision. The total power consumption is 1.18 mW for the proposed class-AB OTA at a 1.8 V supply voltage and 0.74 mW for the other blocks.

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JAEDO KIM (Graduate Student Member, IEEE) received the B.S. degree in electrical and electronic engineering from Hanyang University, Ansan, South Korea, in 2019, where he is currently pursuing the master's and Ph.D. degrees. His current research interests include low-power oversampled delta-sigma converters and mixed-signal integrated circuits.

SEOKJAE SONG (Graduate Student Member, IEEE) received the B.S. and M.S. degrees in electrical and electronic engineering from Hanyang University, Ansan, South Korea, in 2015 and 2017, respectively, where he is currently pursuing the Ph.D. degree. His current research interests include oversampled delta-sigma converters and mixed-signal integrated circuits.

JEONGJIN ROH (Senior Member, IEEE) received the B.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 1990, the M.S. degree in electrical engineering from Pennsylvania State University, in 1998, and the Ph.D. degree in computer engineering from The University of Texas at Austin, in 2001. From 1990 to 1996, he was with Samsung Electronics, Giheung, South Korea, as a Senior Circuit Designer for mixed-signal products. From 2000 to 2001, he was with Intel Corporation, Austin, TX, USA, as a Senior Analog Designer for delta-sigma data converters. In 2001, he joined the Faculty of Hanyang University, Ansan, South Korea. His research interests include power management circuits and oversampled delta-sigma converters.