

Received November 25, 2020, accepted December 9, 2020, date of publication December 11, 2020, date of current version December 28, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3044226

A Hybrid FCS-MPC With Low and Fixed Switching Frequency Without Steady-State Error Applied to a Grid-Connected CHB Inverter

ROBERTO O. RAMÍREZ¹, CARLOS R. BAIER¹, (Senior Member, IEEE), FELIPE VILLARROEL², JOSÉ R. ESPINOZA², (Senior Member, IEEE), JOSEP POU³, (Fellow, IEEE), AND JOSÉ RODRÍGUEZ⁴, (Life Fellow, IEEE)

¹Department of Electrical Engineering, University of Talca, Curicó 3344158, Chile

²Department of Electrical Engineering, University of Concepcion, Concepción 4030000, Chile

³School of Electrical and Electronic Engineering, Nanyang Technology University, Singapore 639798

⁴Department of Engineering Science, Universidad Andrés Bello, Santiago 7500971, Chile

Corresponding author: Roberto O. Ramírez (roramirez@utalca.cl)

This work was supported by the FONDECYT under Project 1201308, Project CONICYT/FONDAP/15110019, and Project CONICYT/DOCTORADO NACIONAL/21160928.

ABSTRACT This paper presents a new finite control set model predictive control strategy that, contrary to conventional approaches, achieves (i) zero steady-state error in the converter's AC current, and (ii) both fixed and lower harmonic spectrum, similar to that achieved by pulse width modulation based control schemes. These characteristics are attractive for medium and high voltage applications where high dv/dt is prohibitive and reduced switching losses are a must, or in applications that use passive filters and where a spread harmonic spectrum can cause resonances. The proposed strategy achieves dynamic results similar to those of conventional predictive control and a steady-state performance similar to that of a modulated control strategy. To do so, the strategy utilizes a modulated integral action to incorporate an input restriction into a conventional predictive control cost function. A grid-connected cascaded H-Bridge multilevel inverter is used to validate the strategy. Simulated and experimental results in both steady and transient states are presented to verify the proposed strategy's performance in the converter.

INDEX TERMS FCS-MPC, grid connected inverters, predictive control, PWM, spread spectrum, steady-state error, switching frequency.

I. INTRODUCTION

The efficient use of low-voltage semiconductors in high-voltage, high-power applications has been made possible thanks to multilevel converters [1]. These topologies have a series of advantages over traditional two-level converters such as lower device switching frequency, lower common-mode voltage, reduced dv/dt stress, and a low THD, among others [2], [3]. Nevertheless, these converters also present their own challenges related to their construction, control, reliability and scalability. Among multilevel converters, cascaded H-Bridge multilevel (CHB-ML) inverters have drawn attention thanks to their simple and scalable design, which enables them to handle higher power/voltage levels via cell stacking [4], [5].

The associate editor coordinating the review of this manuscript and approving it for publication was Tariq Masood^{id}.

Multiple control strategies have been proposed for CHB-ML inverters [6]–[9]; however, the strategies based on predictive control have gained ground due to (i) their easy and intuitive implementation, and (ii), the increased computing capacity of modern processors [10], [11]. Predictive control uses a model of the system to predict future behavior for each of its possible inputs (switching states). The input to be applied (or switching state) is selected through an optimization process that seeks to minimize a cost function made up of the desired control objectives [12]. In any power converter, the main control objective is to reduce the reference tracking error. Depending on the topology, a series of secondary objectives may be incorporated as well; these may include reducing the switching frequency [13], [14], balancing power between cells [15], [16], reducing the common-mode voltage, or minimizing the output voltage's jumps between non-adjacent levels [17], among others.

In CHB-ML converters, predictive control has proven good performance in terms of reference tracking. However, the results associated to secondary objectives such as cell voltage balancing, steady-state performance related to the switching frequency, and jumps between non-adjacent levels, are still open for study [17]–[22]. Indeed, the use of Finite Control Set Model Predictive Control (FCS-MPC) in CHB-ML converters naturally produces power imbalance among the converter's cells, as well as a spread high-frequency harmonic spectrum [23].

Several proposals have been described in the literature to reduce the spread spectrum. Early works, as [24], propose the use of an input restriction in the FCS-MPC cost function to penalize the input changes concerning previously applied states. This method allows to reduce the switching frequency, but it increases the steady-state error and keeps a spread spectrum. A more successful proposal based on input restrictions is made in [25], where the resulting algorithm allows achieving a harmonic spectrum concentrated at a desired frequency.

Most successful proposals are based on the so-called M2PC solution, where a duty cycle optimization is included. One of the first approaches is presented in [26], where a deadbeat solution is used to find the optimal voltage vector. However, this solution does not define which states are used to generate it, thus using a FCS-MPC cost function for this purpose. Finally, the solution is applied using space vector modulation (SVM). Results show a harmonic spectrum that is well defined over 5 kHz, but spread under this frequency. A similar approach is used in [27], where the results present a low current THD and torque ripple but without showing the resulting harmonic spectrum.

In [28] the deadbeat solution is used as voltage reference in the FCS-MPC cost function. In this case, additional control objectives are used to reduce the converter average switching frequency at steady-state. The proposal achieves better results than conventional FCS-MPC schemes, but requires a considerable computational burden due to the fuzzy logic stage used for tuning the cost function weighting factors. In [29] a direct deadbeat solution is implemented (SVM-DVC) without using an optimization stage. The method successfully fixes the harmonic spectrum at the desired frequency; however, the results are only valid at high sampling rates (20 kHz). The same approach is applied to an MMC converter in [30], achieving a well defined harmonic spectrum with low spread.

To avoid using the deadbeat solution, [31] proposes an FCS-MPC with two optimization stages. One is used to determine the converter states which minimize the control objectives desired, and the other is used to calculate the optimal duty cycles. An SVM stage is used to apply the vector calculated with the optimal duty cycles. Good results are achieved, fixing the harmonic spectrum at 10 kHz, but the harmonic distribution is similar to the shown in [26]–[29]. Another alternative is presented in [32], [33], where the objective is not to calculate the optimal state vector but instead an input sequence through an optimization prob-

lem. The proposal allows obtaining a concentrated harmonic spectrum at the desired frequency. To apply the strategy it is necessary to define the input sequences, which, in more complex converters, could not be straightforward.

The literature review shows that the previous solutions to concentrate the harmonic spectrum in FCS-MPC strategies have used deadbeat control to calculate directly the optimal converter's state. The proposals differ with each other in how they incorporate this information in the FCS-MPC algorithm to achieve the desired control objectives. Some directly use the voltage vector to generate the gating signals to the converter semiconductors, while others use this state as a reference in the optimization stage of the conventional scheme. However, it is important to emphasize that the starting point of these strategies is a prediction that depends on the system model; and therefore, under model mismatch or non-measurable disturbances, the state applied will not be necessarily the best one, generating in several cases steady-state error, despite having concentrated spectrum.

To concentrate the harmonic spectrum and avoid the steady-state error, this work proposes a hybrid FCS-MPC strategy that uses a linear controller with integral action to impose a PWM switching pattern through an input restriction on the FCS-MPC cost function. As a result, an operation with zero steady-state error and a well-defined harmonic spectrum is achieved. Hence, the proposal allows retaining characteristics of the predictive controller such as optimization and decoupled response, while improving its steady-state performance through well-known modulated linear controllers. To test the strategy, a single-phase CHB converter is considered whose control objectives are to regulate the output current and to operate with an even power distribution among cells. This last objective is typically solved using additional stages in the FCS-MPC algorithm [34]; however, as it will be shown in the following sections, this proposal naturally includes this operating condition.

This paper is organized as follows: Section II presents the model of the grid-connected single-phase CHB inverter. Then, Section III shows the conventional FCS-MPC scheme and the proposed hybrid scheme to improve its steady-state performance. Section IV shows simulated results that allow comparing the dynamic and stationary performance of the proposal with the conventional scheme. Section V shows the experimental waveforms obtained from a 3-cell single-phase CHB set-up connected to the grid. In Section VI previous results are discussed and compared with the current state of the art. Finally, the conclusions of this work are provided in Section VII.

II. GRID-CONNECTED CASCADE MULTILEVEL H-BRIDGE CONVERTER

A. DESCRIPTION OF THE CHB INVERTER

Fig. 1a shows a single-phase multilevel inverter assembled by n_c cells connected in series. Each cell is composed of an H-bridge inverter fed by a dc voltage whose origin is defined

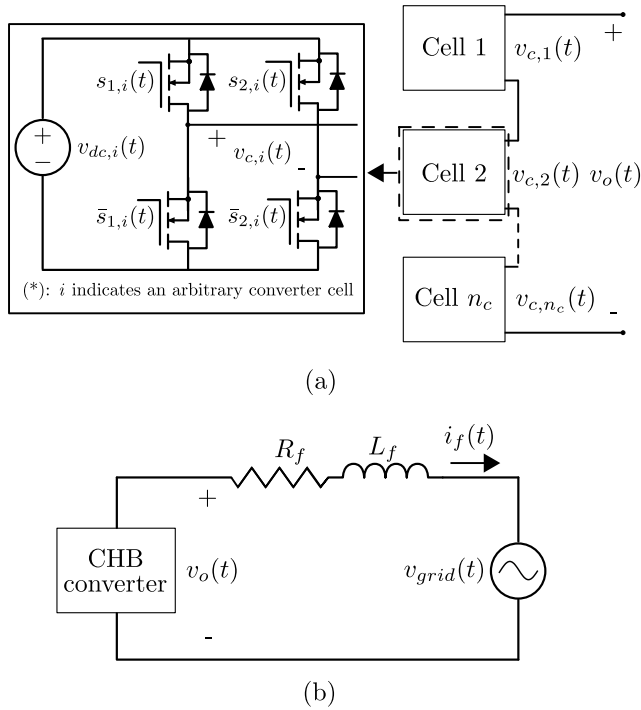


FIGURE 1. Cascade H-bridge converter. (a) Conventional topology; (b) grid-connected single-phase CHB scheme representation.

by the topology’s application [4]. The inverter output voltage v_o is equal to the sum of the output voltages of each one of the cells and can be expressed as,

$$v_o(t) = \sum_{i=1}^{n_c} v_{c,i}. \quad (1)$$

where $v_{c,i}$ is the ac voltage of cell i of the CHB inverter. The output voltage $v_{c,i}$ of any cell i of the system can be calculated as the product of the cell’s dc voltage and its respective switching function $s_{c,i}$. If the semiconductors are considered as ideal switches, the switching function can be expressed as a function of the inverter’s gating signals $\{s_1, s_2\}$ as,

$$s_{c,i}(t) = s_{1,i}(t) - s_{2,i}(t). \quad (2)$$

Thus, the output voltage of the CHB inverter can be rewritten as the sum of the switching functions of each cell as,

$$v_o(t) = \sum_{i=1}^{n_c} s_{c,i} v_{dc,i}(t). \quad (3)$$

In a single-phase H-bridge inverter, the state vector $\mathbf{s}=[s_1, s_2]^T$ has four possible values that correspond to the converter’s admissible switching combinations, Table 1. Therefore, a CHB inverter with n_c cells has a total of 2^{2n_c} admissible states [23].

B. SYSTEM MODEL

A single-phase CHB inverter, connected to the grid through an inductive filter, is used to explain the conventional FCS-MPC scheme and present the proposal of this work, Fig. 1b.

TABLE 1. H-bridge converter admissible states.

s_1	s_2	s_c	Output voltage
0	0	0	0
0	1	-1	$-v_{dc}$
1	0	1	v_{dc}
1	1	0	0

To implement both strategies a discrete model of the system is required, which can be directly obtained from the differential equations that describes its behavior. This model corresponds to,

$$\frac{di_f(t)}{dt} = \frac{1}{L_f} v_o(t) - \frac{R_f}{L_f} i_f(t) - \frac{1}{L_f} v_{grid}(t), \quad (4)$$

where v_{grid} is the grid voltage, v_o the output voltage of the converter, and the pair R_f, L_f correspond to the resistance and the inductance of the inductive filter, respectively. By applying the forward Euler approximation to (4), the predictive model for the proposed strategy is,

$$\tilde{i}_f(k+1) = a_d i_f(k) + b_d v_o(k) + e_d v_{grid}(k), \quad (5)$$

where $\tilde{i}_f(k+1)$ is the estimated filter current at the sampling time $k+1$ and,

$$a_d = (1 + T_s \frac{R_f}{L_f}), b_d = (T_s \frac{1}{L_f}), e_d = -(T_s \frac{1}{L_f}). \quad (6)$$

The discrete model presented in (5) is used in the following sections to formulate the proposed FCS-MPC control scheme that allows operating with zero steady-state error and a well-defined harmonic spectrum.

III. PROPOSED PREDICTIVE CONTROL

A. PREVIOUS WORKS

FCS-MPC uses the discrete model of the system to predict its future behavior in a defined prediction horizon. Its objective is to identify the control input \mathbf{u}_{opt} that allows achieving the best future performance, taking into consideration the desired control objectives and the restrictions imposed. In power converters, since the control inputs (converter states) are finite and discrete, it is possible to know the system’s response, in each sampling time, for all the possible inputs. Also, usually a prediction horizon equal to one is used because of the high computational burden associated with evaluating all converter states.

The described predictive control scheme is applied to the system shown in Fig. 1. At each sampling time, (5) is evaluated for each one of the N possible converter inputs. The optimal input \mathbf{s}_{opt} (optimal state) is given by,

$$\mathbf{s}_{opt} = \min_{j=1 \dots N} f(\tilde{i}_f(k+1), i_{ref}(k+1), (k+1|j)), \quad (7)$$

where $f(\cdot)$ is the predictive control cost function composed by the system’s control objectives and $i_{ref}(k+1)$ is the desired filter current reference. The converter state selected by (7) is applied in the next sampling time, where the process is repeated. Fig. 2 shows the algorithm’s flowchart where (i)

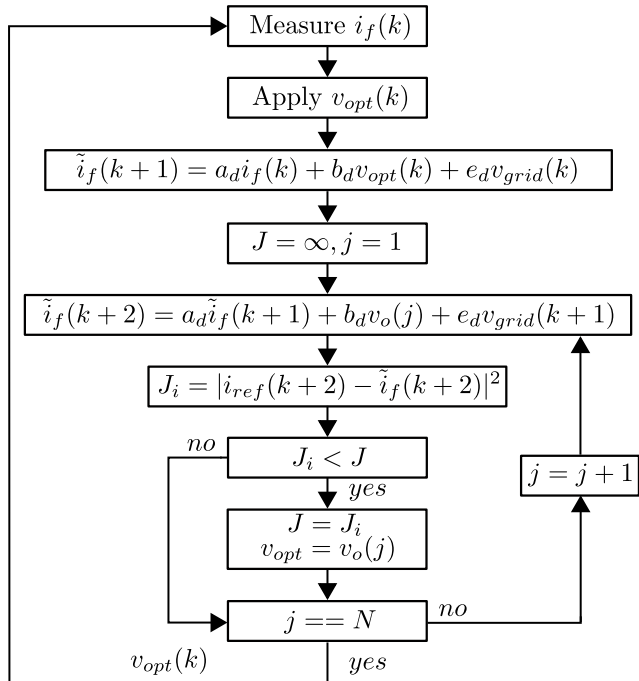


FIGURE 2. Conventional FCS-MPC flowchart applied to a grid-connected CHB inverter.

a delay compensation is used according to [35], and (ii) the control objective is to minimize the filter current tracking error.

When the algorithm shown in Fig. 2 is used, the resultant waveforms have a spread spectrum and the semiconductors average switching frequency depends on the selected sampling time. These characteristics are usually undesirable because they complicate the design of passive filters, excite resonances and increase the converter switching losses [11]. Moreover, the use of an FCS-MPC based controller does not ensure zero steady-state error due to the uncertainties present in the predictive model, which can be caused by parameter mismatch, non-measurable disturbances or too low sampling frequency [36].

Various strategies have been proposed in the literature to reduce and/or fix the switching frequency in controllers based on FCS-MPC [24]–[35], [37], [38]; being the strategy presented in [24], the simplest in terms of implementation and computational burden. This proposal uses an input restriction that penalizes the state change with respect to the optimal state selected in previous sampling time. This can be expressed considering an arbitrary cell i as,

$$\Delta s = (s_i(j) - s_i(k))^T (s_i(j) - s_i(k)), \quad (8)$$

where $s_i(k)$ is the applied state by cell i , and $s_i(j)$ corresponds to one of the converter’s future possible states. Despite (8) allows reducing the semiconductors’ average switching frequency, its use avoids (i) achieving zero steady-state error, and (ii) obtaining a periodical switching pattern with a well-defined harmonic spectrum around a fixed frequency.

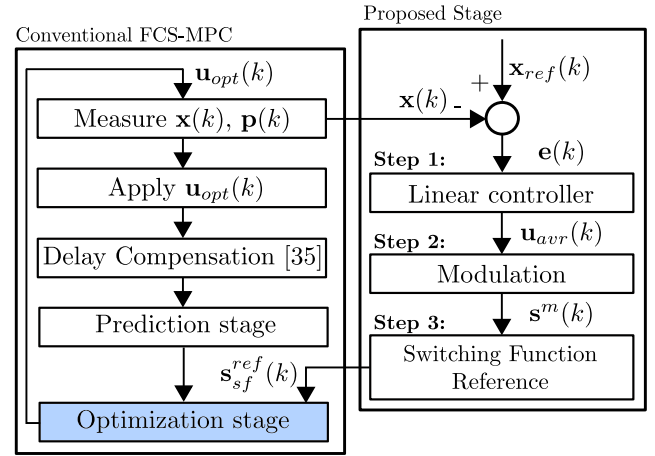


FIGURE 3. Proposed FCS-MPC. The blue box indicates the modified stage in the conventional FCS-MPC flowchart.

To solve the aforementioned problems, this work proposes using a linear controller with integral action to impose a PWM pattern on a conventional FCS-MPC controller. This strategy allows working with zero steady-state error and with a well-defined spectrum, without using extra-optimization stages or algorithms based on the deadbeat solution. Also, because the proposal does not change the FCS-MPC flowchart, and only requires adding a simple input restriction to the cost function, it can be implemented in any power converter that uses the conventional approach.

B. PROPOSED PREDICTIVE CONTROL

The switching frequency and harmonic distribution are defined by the carrier signal frequency in strategies that use a modulation stage to generate the semiconductors’ gating signals. In an FCS-MPC scheme, the control action is calculated in each sampling time regardless of the previously applied states. Thus, the controller does not achieve a well-defined switching pattern or spectrum on steady-state, neither zero error with respect to the desired reference [38]. Hence, for solving these problems, this work proposes using a linear controller with an integral action to generate an input restriction on the cost function of a conventional FCS-MPC scheme. This input restriction seeks to impose a PWM-like pattern on steady-state, which will allow operating with a fixed switching frequency, and thus a well-defined harmonic spectrum. Because a linear controller with integral action is used, the resulting pattern will also enable working with zero steady-state error. These characteristics are achieved without losing the attributes of an FCS-MPC scheme, such as fast and decoupled dynamic response, and optimization among multiple control objectives.

Fig. 3 shows the proposed FCS-MPC controller. This scheme can be analyzed as a linear controller working in parallel with the conventional FCS-MPC strategy. Both controllers are linked through the predictive controller optimization stage. In the proposal, three steps can be identified,

1) LINEAR CONTROLLER

The linear controller is used to find the optimal solution which allows achieving zero error on steady-state. If the reference signal is constant (i.e. with only dc component) on steady-state, the linear controller must have the correct number of poles at the origin to ensure zero error. On the other hand, if the reference signal is sinusoidal (i.e. with ac component), either a resonant controller or a coordinate transformation together with conventional integrators can be used [39]. The output of the linear controller corresponds to the average input \mathbf{u}_{avr} to the converter. Note that a solution based on the deadbeat controller can be used to calculate the value of \mathbf{u}_{avr} directly, such as [26], [29], [30]; however, the resulting controller is an open-loop solution which does not consider parameter mismatch or non-measurables-disturbances, so zero steady-state error cannot be ensured.

2) MODULATION STAGE

The output of the linear controller \mathbf{u}_{avr} must be modulated to obtain the converter discrete inputs. These inputs define the value of the converter state vector \mathbf{s}^m . Standard modulation techniques based on SVM or SPWM can be used for this purpose. The switching frequency and harmonic spectrum distribution are fixed according to the used modulation scheme. For example, if a SPWM solution is selected, the harmonics will be multiples of the carrier frequency.

3) SWITCHING FUNCTION REFERENCE

The converter state vector \mathbf{s}^m is used to calculate the reference converter switching function as,

$$\mathbf{s}_{sf}^{ref}(t) = f_{sf}(\mathbf{s}^m(t)), \quad (9)$$

where $f_{sf}(\cdot)$ is the relation between the converter states and the output voltage (or current) defined by the topology, e.g. for an H-bridge converter, $f_{sf}(\cdot)$ corresponds to the difference between the gating signals associated with the converter's upper semiconductors, as described in (2).

In steady-state, the value of \mathbf{s}^m is optimal if the error is zero. Under this condition, \mathbf{s}_{sf}^{ref} is the optimal switching function that allows the system to operate with zero steady-state error. The value of \mathbf{s}_{sf}^{ref} is used as a normalized voltage reference to define the following control objective in the cost function of the conventional FCS-MPC,

$$\Delta \mathbf{s} = (\mathbf{s}_{sf}^{ref}(j) - \mathbf{s}_{sf}(k))^T (\mathbf{s}_{sf}^{ref}(j) - \mathbf{s}_{sf}(k)), \quad (10)$$

where \mathbf{s}_{sf} is the value of the switching function for one of the j feasible converter states. Finally, the cost function used in the proposed FCS-MPC scheme corresponds to,

$$J = (\mathbf{x}_{ref} - \mathbf{x}(k+2))^T (\mathbf{x}_{ref} - \mathbf{x}(k+2)) + \lambda_{ss} \Delta \mathbf{s}, \quad (11)$$

where \mathbf{x}_{ref} is the desired reference and λ_{ss} is the weighting factor associated with the proposed input restriction.

C. APPLICATION TO THE SINGLE PHASE CHB CONVERTER

The proposed strategy is applied to the converter described in Section II to show its implementation. The control objectives are (i) tracking the converter output current i_f , and (ii) operating with even power distribution among cells. Herein, the previously defined steps will be described as they are applied to the single-phase CHB converter.

1) LINEAR CONTROLLER

The linear controller used to achieve zero error in steady-state is a proportional-resonant (PR) controller, as the reference signal is not constant on permanent regime. The PR controller z -transfer function is,

$$h_{re}(z) = K_r \frac{1 - z^{-1} \cos(\omega_o T_s)}{1 - 2z^{-1} \cos(\omega_o T_s) + z^{-2}} + K_p, \quad (12)$$

which can be rewritten as the difference equation (sampling time T_s),

$$m_i(k) = K_r [e(k) + e(k-1) \cos(\omega_o T_s)] + 2m_i(k-1) \cos(\omega_o T_s) - m_i(k-2) + K_p e(k), \quad (13)$$

where m_i is the output of PR controller; $e(k)$ is the error between the reference and the filter current at sampling time k ; K_r and K_p are the resonant and proportional linear controller gains, respectively; and ω_o is the fundamental frequency of the current reference.

The tuning procedure for K_p and K_r is based on comparing the Bode diagram of the open-loop transfer function h_{ld} with the Bode diagram of the canonical second-order system [40]. The discrete system transfer function, assuming a constant dc voltage corresponds to,

$$h_{sys} = \frac{\alpha z^{-1}}{1 - z^{-1} e^{\beta}}, \quad (14)$$

with,

$$\beta = -\frac{R_f}{L_f} T_s, \quad \alpha = \frac{1}{R_f} (1 - e^{\beta}). \quad (15)$$

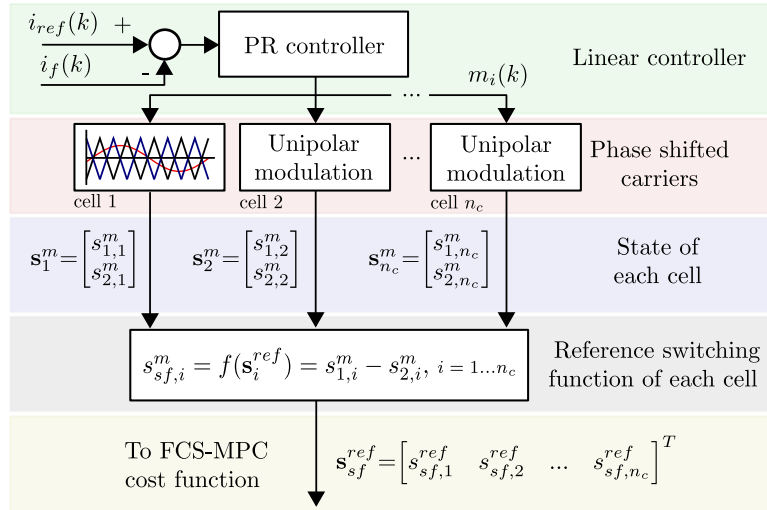
Thus, the h_{ld} transfer function considering the PR controller (13) is,

$$h_{ld}(z) = h_{re}(z) h_{sys}(z). \quad (16)$$

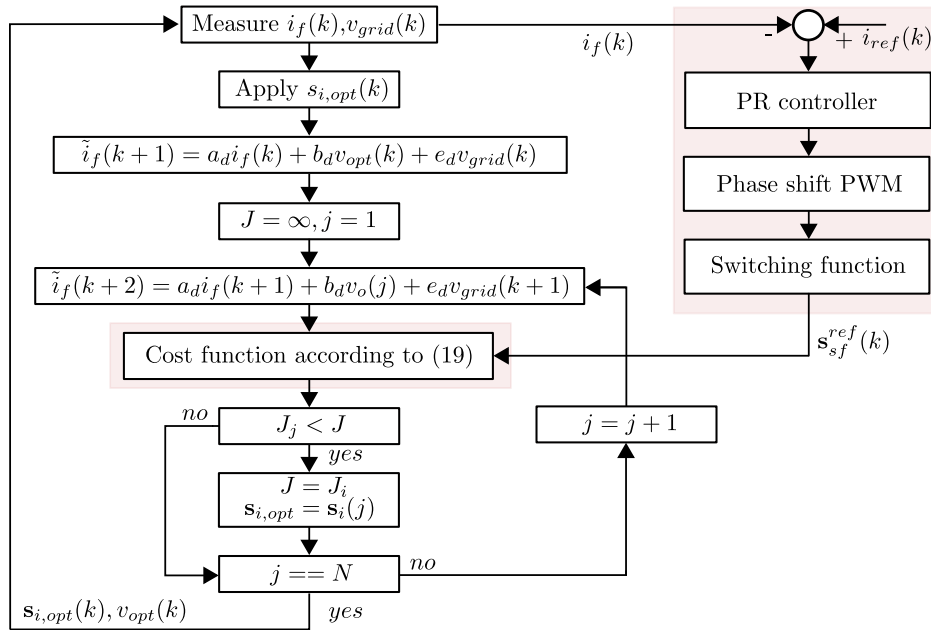
As the PR controller works in parallel to the FCS-MPC controller, it is important that the tuning does not interfere with the FCS-MPC controller dynamic. For a sampling time T_s , the fastest possible response is $2T_s$ (Nyquist frequency). Thus, the settling time will be selected to be in the range $4T_s$ - $10T_s$ as design criteria. Both simulation-based and experimental verification will be made in the following section.

2) MODULATION STAGE

The resonant controller output m_i is modulated using phase-shift PWM (PS-PWM), such as in a traditional CHB inverter [4]. The modulation results are the state vectors \mathbf{s}^m associated to each converter cell, Fig. 4a. Thus, \mathbf{s}_i^m is defined as the state vector of the arbitrary cell i .



(a)



(b)

FIGURE 4. Proposed FCS-MPC applied to a grid-connected CHB inverter. (a) Input restriction generation;(b) proposed algorithm flowchart (highlighted parts indicate a new or modified stage).

The state vector \mathbf{s}^m of each cell is used to calculate the value of the reference switching function $s_{sf,i}^{ref}$ according to (2) as,

$$s_{sf,i}^{ref} = f_{sf}(\mathbf{s}_i^m) = s_{1,i}^m - s_{2,i}^m, \quad (17)$$

where the values of $\{s_{1,i}^m, s_{2,i}^m\}$ for arbitrary cell i are obtained from the modulation stage. Finally, the proposed input restriction to be included in the FCS-MPC cost function is,

$$\Delta \mathbf{s} = (s_{sf,i}^{ref}(j) - s_{sf,i}(k))^2, \quad (18)$$

where $s_{sf,i}(j)$ is the switching function of a cell i for one of the j converter states. Finally, the cost function to be implemented

in the optimization stage will be,

$$J = (i_{ref} - i_f(k+2))^2 + \lambda_{ss} \Delta s, \quad (19)$$

The complete algorithm of the proposed FCS-MPC scheme is shown in Fig. 4b.

IV. SIMULATION RESULTS

The proposed control strategy is simulated for a grid-connected 3-cell CHB converter, Fig. 1. The scheme is evaluated using a carrier signal frequency of 5 p.u. with $\{K_p, K_r\} = \{2.1, 200\}$ and a weighting factor $\lambda_{ss} = 0.8$. The

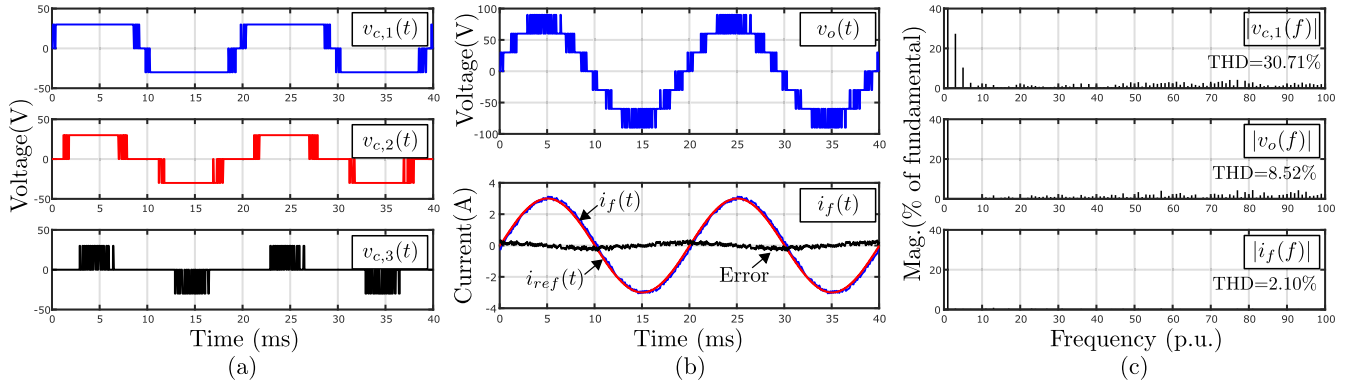


FIGURE 5. Simulation results for conventional predictive control. (a) Voltage of each cell; (b) output voltage and filter current; (c) harmonic spectra of the key waveforms.

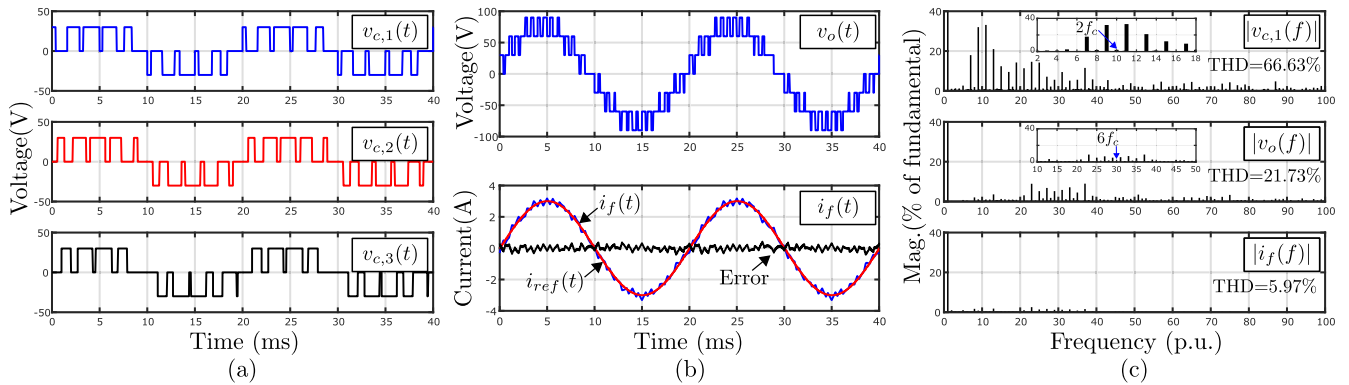


FIGURE 6. Simulation results for the proposed predictive control. (a) Voltage of each cell; (b) output voltage and filter current; (c) harmonic spectra of the key waveforms.

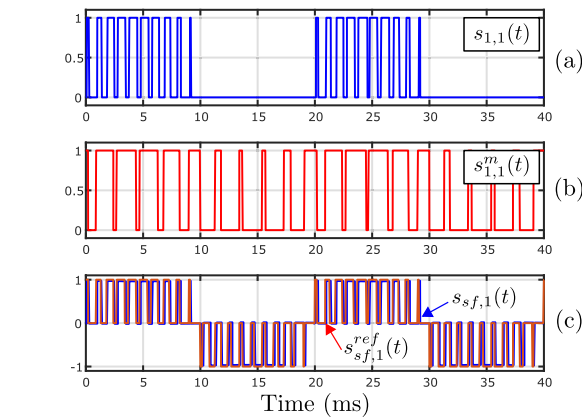


FIGURE 7. Simulation results. Comparison between the switching signal for $s_{1,1}^m$ obtained from the PR control and that applied by the proposed FCS-MPC scheme. (a) Switching signal applied by FCS-MPC; (b) switching signal proposed by modulation stage; (c) proposed and resulting switching function.

simulation parameters correspond to an inductive filter with an inductance of 12.6 mH and a resistance of 0.6 Ω ; a peak grid voltage of 64 V and a dc voltage per cell of 30 V. The sampling time used is 100 μ s and the current reference has an amplitude of 3 A.

TABLE 2. Fundamental cell voltage (50Hz) p.u. w.r.t $v_{dc} = 30$ V.

Voltage	Conventional FCS-MPC	Proposed FCS-MPC
	[11]	$f_c = 5$ p.u.
$v_{c,1}$	1.165	0.745
$v_{c,2}$	0.927	0.770
$v_{c,3}$	0.186	0.736
v_o	2.277	2.246

A. STEADY STATE PERFORMANCE

The system key waveforms when the conventional FCS-MPC algorithm (Fig. 2) is used are shown in Fig. 5. The results show an asymmetrical voltage per cell that leads to an uneven power-sharing among cells. Despite this, a seven-level voltage without jumps between non-adjacent levels is achieved on the converter output, Fig. 5b. The tracking error of the filter current reference has a magnitude of 0.83% with a phase error of -4.2° at fundamental frequency. The harmonic spectra of the output waveforms are shown in Fig. 5c, where the typical spread spectrum of a FCS-MPC implementation can be observed.

The steady-state performance of the proposed predictive control working with a carrier frequency of 5 p.u. is presented in Fig. 6. The results show that each cell operates with the

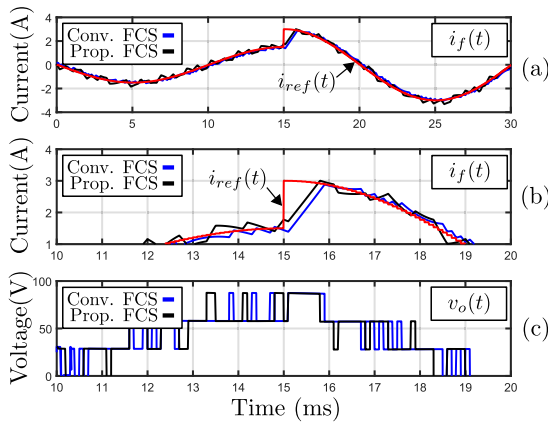


FIGURE 8. Simulation results. Dynamic response comparison between conventional and proposed FCS-MPC for a step-change in the current reference from 1.5 A to 3 A. (a) Filter current; (b) filter current zoom; (c) converter's output voltage.

same output voltage (Table 2) and their sum generates a 7-level voltage at the converter output, Fig. 6a,b. The value of the current error is 0.2% with a phase error of 0° at fundamental frequency due to the resonant action implemented by the linear controller, Fig.6b. In terms of THD values, the proposal has higher values because the harmonic spectra are shifted to lower frequencies by the selected carrier frequency, Fig.6c.

The key waveforms harmonic spectra are shown in Fig.6c. The voltage spectrum of the cell 1 is concentrated around 10 p.u. which is twice the carrier frequency, as unipolar modulation is used for each cell. In the case of the converter output voltage, its harmonic spectrum is concentrated around six-times the carrier frequency given that a PS-PWM scheme is used [4], [41]. These results show that the distribution of the harmonic spectrum is defined only by the modulation scheme used to generate the proposed input restriction.

Fig. 7 shows a comparison between the gating signal of the switch $s_{1,1}^m$ (cell 1) proposed by the linear controller and the one selected by the optimization stage of the FCS-MPC controller. The gating signal proposed by the PR controller does not necessarily match with the one applied by the FCS-MPC controller because the proposed input restriction is made over the switching function and not over the states. So, the optimization stage is free to select any converter state, as long as the resulting cost function is minimized. In steady-state, the error is zero because a resonant controller is used, so the optimization stage will select those states that generate the same switching function as a linear controller.

B. DYNAMIC PERFORMANCE

To compare the dynamic performance of the controllers, a step-change from 1.5 A to 3 A is made, Fig. 8. In both cases, the system attains the desired reference in 0.77 ms with the same dynamic response. In fact, both controllers select the same converter output voltage (input) during the transient response. Thus, the proposed scheme achieves the same fast

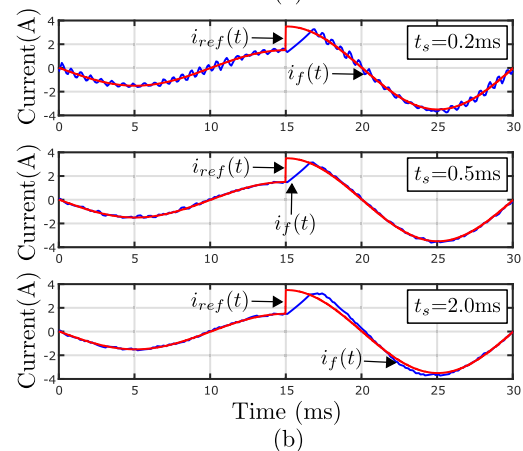
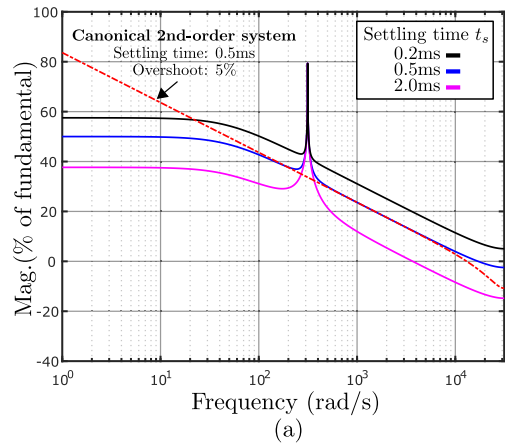


FIGURE 9. Simulation results. PR controller tuning. (a) Magnitude Bode; (b) Current dynamic performance.

dynamic response as the conventional one, but with improved steady-state performance.

C. SENSITIVITY TO THE LINEAR CONTROLLER PARAMETERS

The proposed scheme is evaluated for three different settling times $\{2T_s, 5T_s, 20T_s\}$ using the method described in Section III.C. Fig. 9a shows the open-loop frequency response of the system for each settling time studied. Fig. 9b shows the dynamic performance of each case. All of them attain the reference in 0.77 ms, being the most satisfactory response achieved with the second settling time. The other two cases are not considered because they have higher current ripple (first case) or have an overshoot response (third case). These results validate the design method proposed in Section III.C that recommends using a settling time in the range $4T_s$ - $10T_s$. Although this work proposes a specific tuning criterion for the linear controller, other methods, such as the ones presented in [42]–[46], can be used as well.

V. EXPERIMENTAL RESULTS

The proposed strategy is implemented on a grid-connected three-cell multilevel CHB converter, Fig. 10. The experimental set-up was built using three H-bridge inverter modules

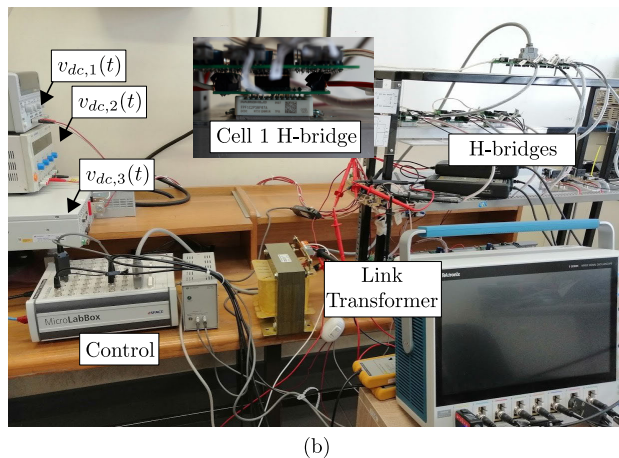
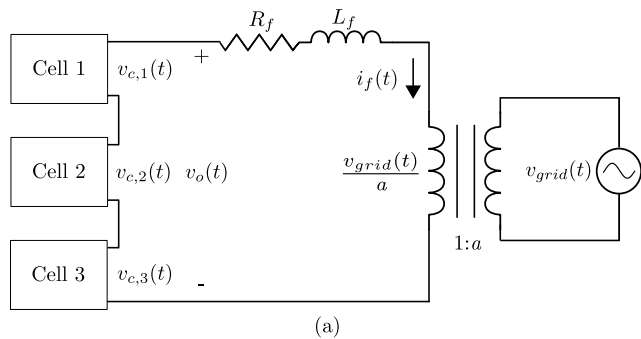


FIGURE 10. System used for the experimental tests. (a) Electrical diagram; (b) experimental setup.

TABLE 3. Experimental setup parameters.

Parameter	Description	Value
System		
v_{dc}	DC voltage	30 V
v_{grid}	Grid voltage	128 V
a	Transformer ratio	2
R_f	Filter resistance	0.6 Ω
L_f	Filter inductance	12.6 mH/6.3 mH
f_s	Sampling frequency	100 μ
Proposed controller		
f_c	Carrier frequency	250 Hz/5 p.u.
λ_{ss}	Input restriction weighting factor	0.8
K_p	Proportional gain	2.1
K_r	Resonant gain	200

(FPF1C2P5BF07A), an inductive filter, and a link transformer. The parameters of the system are shown in Table 3. The control algorithms were implemented in a dSpace MicroLabBox with a sampling time of 100 μ s. The dynamic and stationary performance of the proposed controller is compared with a conventional FCS-MPC using [47] to achieve an even power-distribution among cells. The proposal is evaluated for a carrier frequency of 5 p.u. and 7 p.u. using a PR controller tuned to achieve a settling time of 0.5 ms. All tests are performed for two filter inductance values (6.3 mH and 12.6 mH) to show the proposal versatility under different system configurations.

A. STEADY-STATE PERFORMANCE

The performance of the conventional FCS-MPC for both study cases is shown in Fig. 11. Independently of the value

TABLE 4. Fundamental cell voltage (p.u. w.r.t $v_{dc}=30$ V) for the tested inductance values.

Voltage	Conv. FCS-MPC	Prop. FCS-MPC	Prop. FCS-MPC
	using [47]	$f_c=5$ p.u.	$f_c=7$ p.u.
	6.3mH / 12.6mH	6.3mH / 12.6mH	6.3mH / 12.6mH
$v_{c,1}$	0.909 / 0.909	0.918 / 0.884	0.905 / 0.875
$v_{c,2}$	0.903 / 0.903	0.909 / 0.901	0.908 / 0.879
$v_{c,3}$	0.991 / 0.903	0.901 / 0.857	0.912 / 0.894
v_o	2.750 / 2.750	2.692 / 2.613	2.705 / 2.623

TABLE 5. Magnitude and phase error for filter current at fundamental frequency (50 Hz).

Control scheme	Mag. Error / Phase Error	
	$L_f=6.3$ mH	$L_f=12.6$ mH
Conventional FCS-MPC [47]	2.6% / 5.1°	1.83% / 4.4°
Proposed FCS-MPC		
$f_c = 5$ p.u.	0.2% / 1.2°	0.10% / 1.1°
$f_c = 7$ p.u.	0.8% / 1.0°	0.7% / 1.0°

TABLE 6. Average Switching Frequency p.u. w.r.t 50 Hz.

Control scheme	Value for a filter inductance of	
	$L_f=6.3$ mH	$L_f=12.6$ mH
Conventional FCS-MPC [47]	52	50
Proposed FCS-MPC		
$f_c = 5$ p.u.	10	10
$f_c = 7$ p.u.	14	13.3

of the filter inductance, the cells have the same fundamental output voltage, Table 4. The filter current tracks the reference of 3 A with a magnitude error of 1.83% (case 1), and 2.6% when the inductance is reduced to half (case 2). In terms of phase error, the current of case 1 has a delay of 4.4° with respect to the reference; while in case 2, the value obtained is 5.1°. In both cases, the phase error generates an oscillation in the current error waveform.

The key waveforms harmonic spectra for case 1 ($L_f = 12.6$ mH) are shown in Fig. 14a. The output voltage of cell 1 ($v_{c,1}$) presents a spread spectrum distributed around $f_s/6$ and $f_s/2$ with an average switching frequency per semiconductor (ASFS) of 2.6 kHz (52 p.u.). In the case of the converter output voltage and filter current, the harmonic spectra are distributed over 80 p.u. because of the voltage harmonic cancellation among cells.

Fig. 12 shows the performance of the proposed FCS-MPC for a carrier frequency of 5 p.u. The results show that all cells have the same fundamental voltage, which allows operating with symmetric power distribution among cells, Table 4. The waveforms are like the ones achieved using PS-PWM with the same carrier frequency. In case 1 ($L_f = 12.6$ mH), the current tracks the reference with a magnitude error of 0.1% and a phase error of 1.1%. Compared to the conventional FCS-MPC, the amplitude error is reduced 180%, and the phase error in 400%. Similar results are achieved for case 2, where the proposed scheme reduces 13 times the amplitude error and 4.25 times the phase error when compared with the conventional FCS-MPC, Fig. 12b.

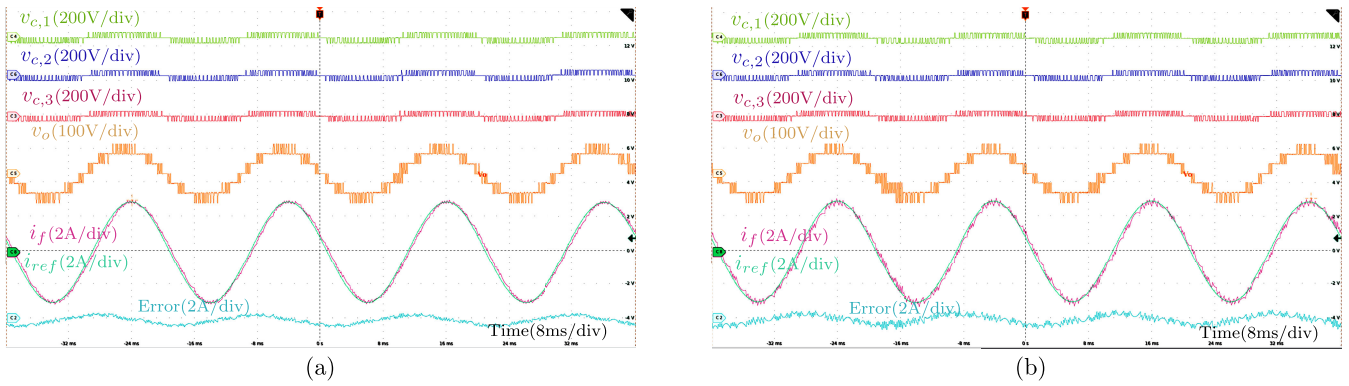


FIGURE 11. Experimental results for conventional predictive control using [47]. (a) Filter inductance 12.6 mH; (b) Filter inductance 6.3 mH.

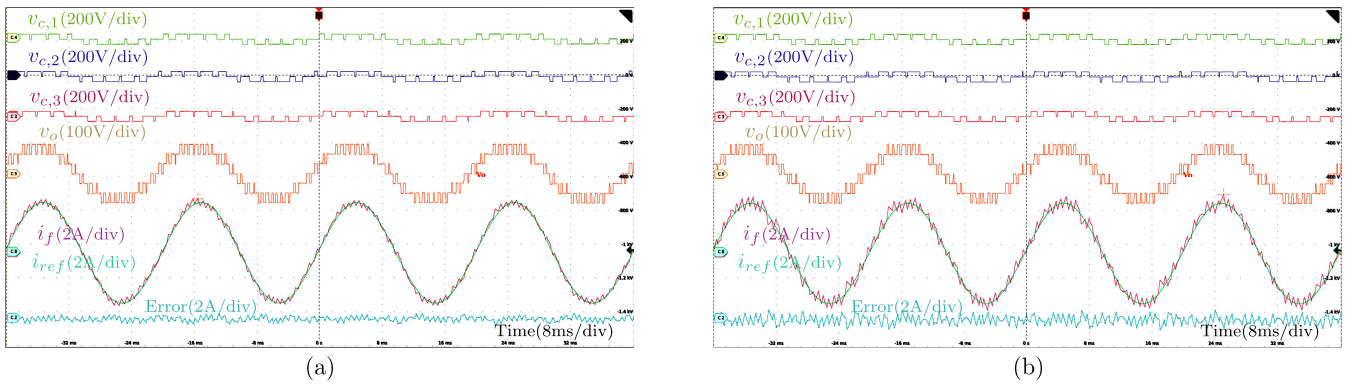


FIGURE 12. Experimental results for proposed predictive control ($f_c = 5$ p.u.). (a) Filter inductance 12.6 mH; (b) Filter inductance 6.3 mH.

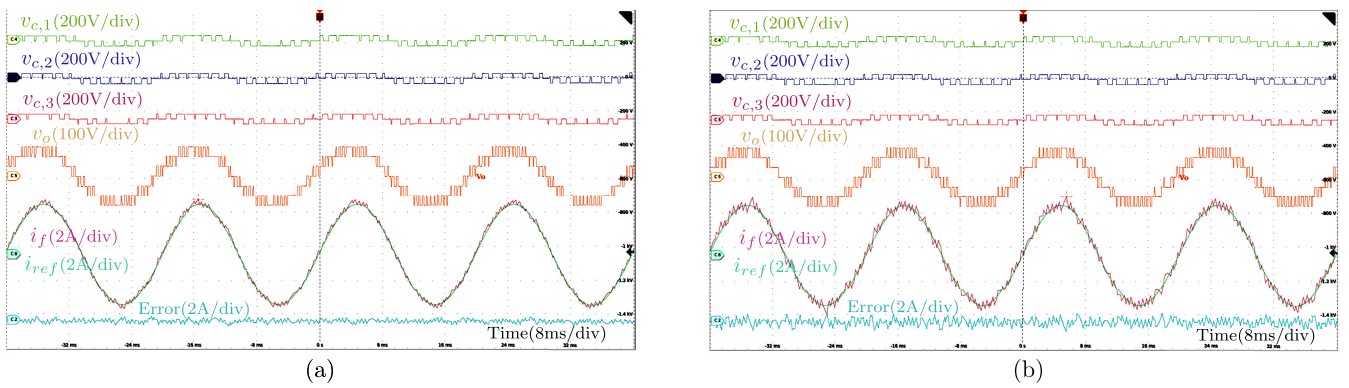


FIGURE 13. Experimental results for proposed predictive control ($f_c = 7$ p.u.). (a) Filter inductance 12.6 mH; (b) Filter inductance 6.3 mH.

The performance of the proposal for a carrier frequency of 7 p.u. (350 Hz) is shown in Fig. 13. The proposal allows operating with symmetric voltage among cells with a 7-level output voltage like a PS-PWM scheme, Table 4. The magnitude and phase errors are 0.7% and 1° for case 1, and 0.8% and 1° for case 2, respectively. The results are summarized in Table 5.

Fig. 14b,c show the harmonic spectra of the converter key waveforms for case 1, when carrier frequencies of 5 p.u. and 7 p.u. are used, respectively. In both cases, the voltage

harmonic spectrum of cell 1 is concentrated around twice the carrier frequency due to the unipolar modulation used. As expected, the converter output voltage harmonic spectrum is concentrated around six-times the corresponding carrier frequency ($n_c \cdot 2f_c$), just like a PS-PWM scheme for both carrier frequency values.

The average switching frequency per semiconductor for the different study cases and carrier frequencies are summarized in Table 6. When a carrier frequency of 5 p.u. is used the ASFS is 10 p.u., independently of the filter inductance

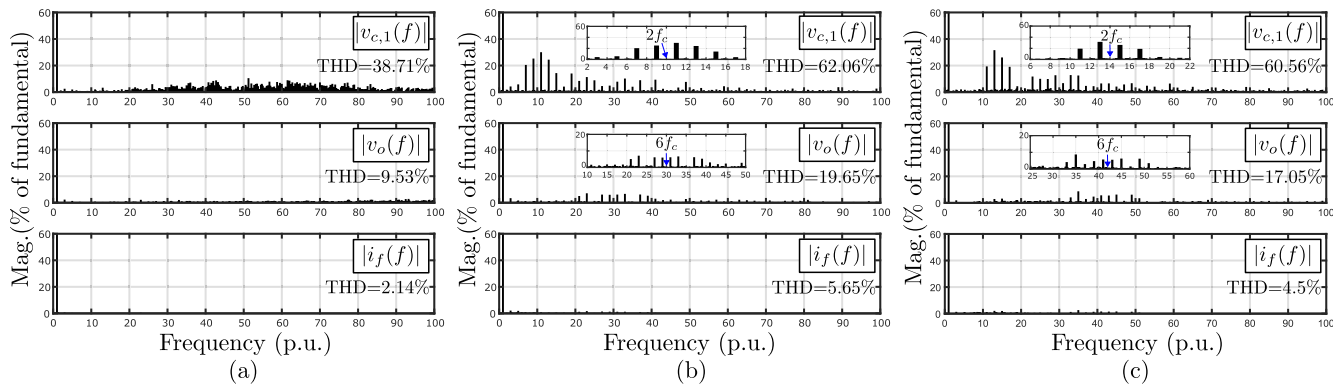


FIGURE 14. Experimental results for a filter inductance of 12.6 mH. Key waveforms harmonic spectra. (a) Conventional FCS-MPC using [47]; (b) proposed FCS with $f_c=5$ p.u.; (c) proposed FCS with $f_c=7$ p.u.

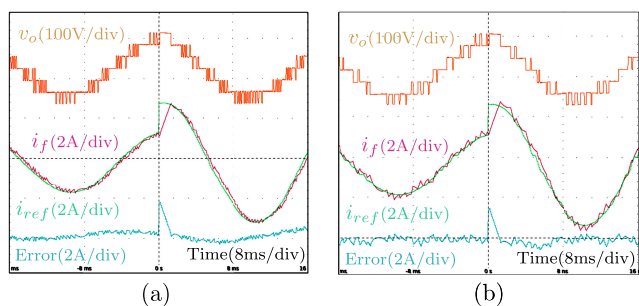


FIGURE 15. Experimental results. Dynamic performance for a step-change in the current reference from 1.5 A to 3 A when $L_f=12.6$ mH. (a) Conventional FCS-MPC using [47]; (b) proposed FCS-MPC.

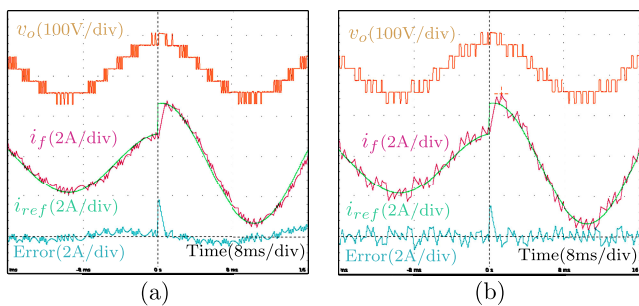


FIGURE 16. Experimental results. Dynamic performance for a step-change in the current reference from 1.5 A to 3 A when $L_f=6.3$ mH. (a) Conventional FCS-MPC using [47]; (b) proposed FCS-MPC.

used. This result is 5 times lower than the one achieved by the conventional scheme for the same sampling frequency. In fact, Table 6 shows that the ASFS is defined by the carrier frequency and its values are approximately equal to twice the carrier frequency.

The results show that the steady-state error is reduced in magnitude and phase independently of the value of the output filter and the carrier frequency. Furthermore, the key waveforms obtained by the proposed FCS-MPC are like those achieved through a PWM modulation-based scheme. A well-defined harmonic spectrum is obtained as is desired, which is centered around the desired carrier frequency.

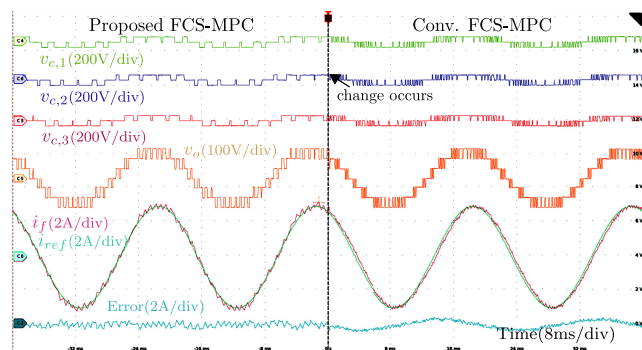


FIGURE 17. Experimental results. Change from the proposed FCS-MPC ($f_c=5$ p.u.) to the conventional predictive control using [47].

B. DYNAMIC PERFORMANCE

The dynamic performance of the proposal and conventional FCS-MPC is evaluated for a step-change in the current reference from 1.5 A to 3 A. The test is made for both study cases ($L_f = \{12.6 \text{ mH}, 6.3 \text{ mH}\}$) considering a carrier frequency of 5 p.u. (250 Hz). Fig. 15 shows the dynamic response for case 1. The results show that both, the proposed FCS.MPC and conventional FCS-MPC, attain the reference in 1.2 ms with the same filter current dynamic. Both control schemes apply the same converter output voltage when the change in the current reference is made. The same results can be observed in case 2 (6.3 mH), where both schemes show a dynamic response of 0.67 ms for the same voltage input, Fig. 16. In this case, the achieved response time is lower than in case 1 because the filter inductance is also lower. These results show that the proposed scheme improves the steady-state performance of the conventional FCS-MPC without deteriorating its fast dynamic response characteristic.

Fig. 17 illustrates the system performance under a change of the current control strategy. A controller change is considered from the proposed FCS-MPC with a carrier frequency of 5 p.u. to the conventional FCS-MPC scheme using [47]. A filter inductance value of 12.6 mH (case 1) is used for the test. Before the change, the system works with an even power distribution among cells, a low and constant switching frequency, and zero steady-state error. When the proposal is

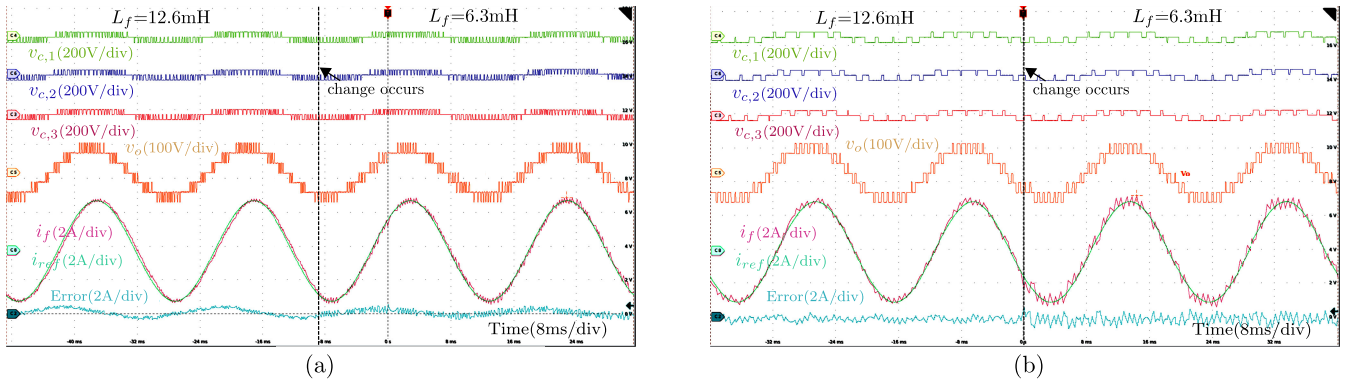


FIGURE 18. Experimental results for a change of -50% in the filter inductance value. (a) Conventional FCS using [47]; (b) proposed FCS-MPC.

deactivated, the error waveform starts to oscillate due to the phase difference between the current and its reference; while the voltage waveforms show an increase in the number of transitions between voltage levels due to the increase in the switching frequency.

C. PARAMETER SENSITIVITY

The performance of the conventional and proposed FCS-MPC under a variation of -50% in the inductance value is shown in Fig. 18. The filter current reference is 3 A and the change in the inductance value is from 12.6 mH to 6.3 mH. In both strategies the estimated inductance is 12.6 mH. The sampling frequency used is 10 kHz for both strategies, and the carrier frequency for the proposal is 250 Hz (5 p.u.). The PR controller parameters are $\{K_p, K_r\} = \{2.1, 200\}$, which are designed considering a inductance of 12.6 mH.

Fig. 18a shows the converter key waveforms for the conventional case. Before and after the change, there is a phase error between the filter current and the reference, which is independent of the inductance value. After the change, there is an increase in current THD from 2.14% to 4.1% due to the increase in the filter cut-off frequency. In the case of the proposal, before the inductance change, the current shows a higher ripple than the conventional case due to the reduced ASFS, Fig. 18b. After the change, the ripple increases from 5.65% to 9.7% as the harmonic components are nearer to the filter cut-off frequency. Although this natural ripple increases, the system can operate with zero steady-state error and a reduced switching frequency.

VI. DISCUSSION

Several predictive control strategies use the deadbeat solution to calculate the optimal input voltage vector to the system [26]–[30]. For instance, Table 7 shows a comparison between the proposed scheme to previous works based on FCS-MPC. These strategies differ among them in how this information affects the calculation of the converter gating signals. Mostly, these strategies use an output SVM stage to fix the harmonic spectrum. However, this not necessarily ensures zero steady-state error or a reduced switching frequency. The proposed

scheme also uses a modulation stage to fix the harmonic spectrum; but, in contrast to previous works, it is used to generate an input restriction on the optimization stage of the conventional FCS-MPC, being this controller the one who calculates the optimal gating signals. This method is similar to [28] where the input restriction is generated using the optimal voltage vector calculated with a deadbeat control approach. The major change with respect to this solution is the origin of the input restriction; if a deadbeat solution is used, the selection of the voltage vector is sensitive to model mismatch and/or non-measurable disturbances. To avoid this problem, the input restriction of the proposed FCS-MPC is evaluated with respect to the voltage vector obtained from a linear controller with integral action. This solution allows the system to work on steady-state with zero error and with a well-defined harmonic spectrum, due to the use of a PWM pattern in the input restriction.

The application of the proposal on a CHB inverter shows that it is possible to operate with zero steady-state error and a non-spread harmonic spectrum. The modulation stage is implemented with PS-PWM as this allows achieving an even power-distribution among cells and achieves a converter output voltage with a shifted harmonic spectrum without using additional stages. The proposal allows fast dynamic response, characteristic of conventional FCS-MPC, while at the same time retaining the desirable steady state behavior of modulation-based linear controllers. The best characteristics of each controller are retained in the proposed method. As the proposed method has both controllers running in parallel, a seamless transition is possible between the control actions, instead of using complex algorithms which are based on controller switching as [49].

The results show an increment in the THD value compared with the conventional case due to the reduction in the converter switching frequency, which causes a shift on the harmonic spectrum to lower frequencies. This produces an increment in the amplitude of the harmonics under 2550 Hz, which is used to calculate the THD. This can be confirmed comparing the spectrum in both cases, Fig. 14. Although the THD of the filter current increases, the system can operate

TABLE 7. Comparison among different MPC strategies.

Feature	PR controller	Conv. FCS-MPC [11]	Proposed FCS-MPC	Period Control [25]	M ² PC [26]	Input restriction [24]	Notch filter [48]
Switching Frequency	Carrier✓ frequency	Defined by sampling time	Carrier✓ frequency	Weighting factor tuning	SVM✓ frequency	Weighting factor tuning	Filter tuning
Dynamic response	Controller design	Controller	Fast✓	Fast✓	Fast✓	Medium	Medium
Optimization	No	Yes✓	Yes✓	Yes✓	Yes✓	Yes✓	Yes✓
Spread spectrum	No✓	Yes	No✓	Medium	Medium	Yes	Medium
Implementation	Simple✓	Simple✓	Simple✓	Medium	Medium	Simple✓	Medium
Even power distribution	Yes ✓	No	Yes✓	No	Yes✓	No	No

with a reduced switching frequency which in high power applications is key; keeping a operation with zero error on steady-state and a fixed harmonic spectrum. Moreover, in the particular case of CHB converter, the THD can be reduced by means of cell stacking, further shifting the harmonic components to higher frequencies.

Using a software-generated carrier signal is not the best solution for the modulation stage because it could increase the overall computational burden; however, because of the high computational capacity of the hardware used to implement the strategy, the resolution achieved (0.9° for $f_c=5$ p.u) is enough for good control performance. The proposed control scheme has a computational burden of $13.5 \mu\text{s}$ which, compared with the $13.2 \mu\text{s}$ of conventional FCS-MPC, corresponds to an increment of just 2.3%.

Although the control scheme was applied and tested in a CHB inverter, the proposal can be used in any power converter where a FCS-MPC strategy can be implemented. In this way, the converters could operate with a fixed spectrum and zero steady-state error, without losing the desirable characteristics of the FCS-MPC strategy such as optimization and fast dynamic response.

VII. CONCLUSION

This work presented a control strategy to improve the steady-state performance of FCS-MPC controllers. The proposal uses the modulated output obtained from a linear controller with integral action to achieve zero error on a steady-state. To evaluate the proposal, a grid connected single-phase CHB converter was considered. The results show that the proposal allows reducing 13 times the magnitude error and 4.25 times the phase error when compared with the conventional scheme for an output filter of 6.3 mH. These results were achieved with a harmonic distribution similar to a modulated scheme working at 500Hz and an even power-distribution among the converter's cells. These steady-state characteristics were obtained without sacrificing the characteristic fast dynamic response of the conventional FCS-MPC scheme or changing its basic algorithm's flowchart.

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ROBERTO O. RAMÍREZ received the B.Sc. and Engineer degrees (Hons.) in electronic engineering, and the M.Sc. and Ph.D. degrees in electrical engineering from the University of Concepción, Concepción, Chile, in 2010, 2012, 2013, and 2020, respectively.

Since 2018, he has been a Lecturer with the Department of Electrical Engineering, University of Talca, Curicó, Chile. His research interests include power converters, robotics, digital systems, and embedded systems.



CARLOS R. BAIER (Senior Member, IEEE) was born in Temuco, Chile, in 1979. He received the B.Sc., M.Sc., and D.Sc. degrees in electrical engineering from the Universidad de Concepción, Concepción, Chile, in 2004, 2006, and 2010, respectively. Since 2009, he has been a Professor with the Faculty of Engineering, Universidad de Talca, Talca, Chile, where he is currently a Teacher of industrial electronics. His research interests include improved control techniques for multilevel converters, emerging converters and strategies to inject power into the grid, and high-energy efficient improvements for medium-voltage converters.



FELIPE VILLARROEL received the B.Sc. and Engineer degrees (Hons.) in electronic engineering and the M.Sc. degree in electrical engineering from the University of Concepción, Concepción, Chile, in 2007, 2009, and 2012, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering, sponsored by a scholarship from the Chilean Research Foundation CONICYT. Since late 2012 until February 2016, he worked as a Hardware/Software Engineer with CADETECH

S.A., Concepción. His research interests include the modeling, simulation, and control of power converters, in particular predictive and nonlinear control techniques.



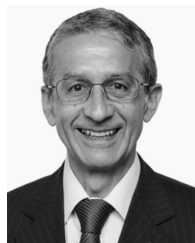
JOSEP POU (Fellow, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Technical University of Catalonia (UPC)-Barcelona Tech, in 1989, 1996, and 2002, respectively.

In 1990, he joined the Faculty of UPC as an Assistant Professor, where he became an Associate Professor in 1993. From February 2001 to January 2002 and from February 2005 to January 2006, he was a Researcher with the Center for Power Electronics Systems, Virginia Tech, Blacksburg. From January 2012 to January 2013, he was a Visiting Professor with the Australian Energy Research Institute, University of New South Wales (UNSW) Sydney, Australia. From February 2013 to August 2016, he was a Professor with UNSW Sydney. He is currently a Professor with Nanyang Technological University (NTU), Singapore, where he is also a Program Director of power electronics with the Energy Research Institute, NTU (ERI@N), and the Co-Director of the Rolls-Royce, NTU Corporate Lab. He has authored more than 340 published technical articles and has been involved in several industrial projects and educational programs in the fields of power electronics and systems. His research interests include modulation and control of power converters, multilevel converters, renewable energy, energy storage, power quality, HVdc transmission systems, and more-electrical aircraft and vessels. He received the 2018 IEEE Bimal Bose Award for Industrial Electronics Applications in Energy Systems. He is also an Associate Editor of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was the Co-Editor-in-Chief and an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.



JOSÉ R. ESPINOZA (Senior Member, IEEE) received the Engineering degree in electronic engineering and the M.Sc. degree in electrical engineering from the University of Concepción, Concepción, Chile, in 1989 and 1992, respectively, and the Ph.D. degree in electrical engineering from Concordia University, Montreal, QC, Canada, in 1997. Since 2006, he has been a Professor with the Department of Electrical Engineering, University of Concepción, where he is involved in

teaching and research in the areas of automatic control and power electronics. He has authored and coauthored more than 150 refereed journals and conference papers, and contributed to one chapter in the *Power Electronics Handbook* published in 2011 by Academic Press. He is currently an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS and the IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS.



JOSÉ RODRÍGUEZ (Life Fellow, IEEE) received the Engineer degree in electrical engineering from the Universidad Técnica Federico Santa María, Valparaíso, Chile, in 1977, and the Dr.-Ing. degree in electrical engineering from the University of Erlangen, Erlangen, Germany, in 1985. He has been with the Department of Electronics Engineering, Universidad Técnica Federico Santa María, since 1977, where he was a Full Professor and the President. Since 2015, he has also been the

President, and since 2019, he has also been a Full Professor with Universidad Andrés Bello, Santiago, Chile. He has coauthored two books, several book chapters, and more than 400 journal and conference papers. His research interests include multilevel inverters, new converter topologies, control of power converters, and adjustable-speed drives. He received a number of best paper awards from journals of the IEEE. He is also a member of the Chilean Academy of Engineering. In 2014, he also received the National Award of Applied Sciences and Technology from the government of Chile. In 2015, he also received the Eugene Mittelmann Award from the Industrial Electronics Society of the IEEE. From 2014 to 2019, he had been included in the list of Highly Cited Researchers published by Web of Science.

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