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A Multi-Cell 21-Level Hybrid Multilevel Inverter Synthesizes a Reduced Number of Components With Voltage Boosting Property

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ABSTRACT A multi-cell hybrid 21-Level multilevel inverter is proposed in this paper. The proposed topology includes two-unit; an H-bridge is cascaded with a modified K-type unit to generate an output voltage waveform with 21 levels based only on two unequal DC suppliers. The proposed topology's advantage lies in the fine and clear output voltage waveforms with high output efficiency. Meanwhile, the high number of output voltage waveform levels generates a low level of distortion and reduces the level of an electromagnetic interface (EMI). Moreover, it reduces the voltage stress on the switching devices and gives it a long lifetime. Also, the reduction in the number of components has a noticeable role in saving size and cost. Regarding the capacitors charging, the proposed topology presents an online method for charging and balancing the capacitor's voltage without any auxiliary circuits. The proposed topology can upgrade to a high number of output steps through the cascading connection. Undoubtedly this cascading will increase the power level to medium and high levels and reduce the harmonics content to a neglectable rate. The proposed system has been tested through the simulation results, and an experimental prototype based on the controller dSPACE (DS-1103) hardware unit used to support the simulation results.

INDEX TERMS 21-Level Multilevel Inverter (MLI), hybridization, modified K-type inverter, online charging, self-balancing, voltage boosting inverter, Total Harmonic Distortion (THD).

I. INTRODUCTION

Recently, MLIs gained wide fame as a member of the family of the DC/AC converters, and make a revolution in the industrial field. This is caused by the smart features presented by these converters over the traditional converters and the huge number of applications such as FACTS, grid-connected renewable energy applications, electric vehicles, and mining [1]–[3]. The MLIs present some of the good features which make it the best choice for the consumers such as, the high number of steps in the output voltage waveforms reduce the voltage stress on the switching devices and gives it a long lifetime. On the other hand, the high number of steps in the voltage waveform reduces the harmonics content. It makes the waveforms closer to the sinusoidal shape. Also, it reduces the level of EMI. The reduction in the THD level reduces the size of the filter components, which in turn reduces the size and cost of the system and enhances the overall efficiency. Always the MLIs present a reduction in the number of components if compared with the conventional converters. This makes it more compact and easy to be packaged; consequently, the percentage of reliability enhances [4], [5].

MLIs are very common in the range of medium and high power applications. This can be achieved by applying a series connection between multiple units either with a combination of similar units as in modular multilevel converters cases. References [3], [6], or a cascaded connection between different MLIs topologies as in hybrid systems [7], [8]. Some of the MLI's topologies present voltage boosting ability that aids in the voltage amplification in some industrial applications. [9]–[11].

Basically; the MLIs have been classified into three main members, the flying capacitor multilevel inverters (FCMLIs), the Neutral Point Clamped multilevel inverters (NPCMLIs), and the cascaded H-bridge multilevel

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inverters (CHBMLIs) [12]–[17]. For the NPC, it needs a set of power diodes with a different rating. Because of the different applied voltage in the same inverter, these topologies are suffering from voltages balancing issues, especially increasing the system capacity. So, the inverter needs an additional number of switches, capacitors, and diodes, which increases the system losses, cost, and size [18]. The FCMLIs also have some constraints such as the high number of bulky capacitors with its charging and balancing difficulties [19]. Moreover, increasing the output power range will increase the number of capacitors in the system, which leads to a high level of losses and big size for the system. In the case of the CHB, it needs many DC sources, which increases the total cost of the system. In the case of extending the system for maximizing the range of the output power, the number of DC sources will increase more and more [20].

Generally, the main target of any MLI topology is saving the cost by reducing the number of switches, the DC suppliers, and reducing the harmonics content in the output waveforms. These are the main issues that usually face the researchers in this field. In [21]–[24] the authors used an H-bridge unit as a polarity generation block of the output waveforms which, increasing the number of switches, and increasing the system complexity and size. In [10], [11] The topologies didn't depend on the HB in the structure and used a unique loop for each level based on the proposed topologies' switching devices. Both of these topologies ensure 13-Level in the output voltage waveform. Different topologies also follow the same technique of removing the HB unit, such as ST-type and E-type, which are presented in [25] and [26] respectively.

In [24], [27], 9 levels, and 11 levels multilevel inverters are presented respectively. However; these topologies use separated DC sources which increases the cost. A 33-level MLI has been presented in [28]. This topology also lacks the DC sources' reduction, which represents the most expensive part of any topology. In [20] a cascaded Multilevel inverter with a series connection of novel H-Bridge has been presented. This topology presents a cascaded system that can be extended to many units based on the cascaded units connected in series. However, it has many switches and DC sources, which means an increment in the system size and cost.

The hybrid multilevel topologies represent one of the successful techniques to increase the number of steps in the output waveforms with a slight increment in the number of switching devices and the feeding DC sources. A combination of the FC MLI and CHB MLI topology has been presented in the hybrid system in [29]. A 15L hybrid system MLI has been presented in [30] based on a series and parallel conversion of dc voltage sources. However, this topology uses four DC sources in the input sources, which increases the total cost and also increases the system size. A 19-level MLI topology has been presented in [31]. This system consisted of a switched-capacitor converter and a floating-capacitor-based (FCB) unit. Another hybrid connection of two sub-units has been illustrated in [32] to generate a 7-Level Multilevel Inverter. In [33] hybrid combination of two sub-units has been presented for system expansion. So this connection can be extended to a cascaded connection system aiming to increase the number of steps in the output voltage waveform; also, a self-balancing controlling scheme has been in addition to eliminating the odd multiples of switching frequency in the output voltage frequency spectrum. However, the system controlling scheme is very complex, and also, the system uses many switching devices to generate the desired number of levels.

This paper presents a multi-cell 21-Level hybrid Multi-Cell Based Modular Multilevel inverter with voltage boosting property. The proposed MLI topology ensures a reduced number of switching devices, diodes, and DC sources to generate the desired output voltage waveform levels. The proposed topology presents a reduction in DC suppliers' number by replacing the real DC suppliers with virtual DC suppliers represented in the chargeable DC capacitors. Those capacitors will keep charging and discharging based on an online method for charging and balancing through a charging loop. In the stand-alone power stations, the electrical power range needs to be raised to medium or high power levels. The proposed topology covers this point by connecting multiple units in a cascaded connection. This will raise the output power range to a sufficient level and reduce the level of the harmonic content in the output voltage waveforms to a neglectable level. It also will reflect on reducing the size of the input filter component of the proposed topology. The proposed topology has been tested in two cascaded connection forms either by duplication of the H-bridge unit or by duplication of the modified k-type unit.

Structurally, this paper starts with a brief introduction and survey for the most influential MLI topologies. The proposed 21-Level hybrid MLI has been introduced in section II; this section includes the configuration of the presented topology and the level generation process and the different switching modes and the capacitors charging loops. In section III, the proposed topology has been compared to the reported topologies to achieve this topology's uniqueness in terms of the number of switching devices, the number of DC sources, and the number of generated levels. The cascading process for the proposed topology has been introduced in section IV, with its two connection scenarios. The value of the capacitance of the capacitors and the power losses calculations have been presented in section V. Results, and discussions introduce in section VI. It is divided into simulation results and supported by the experimental results, and both of them describe the performance of the proposed system well. Finally, a conclusion of the introduced work has been drawn.

II. PROPOSED SINGLE PHASE 21-LEVEL HYBRID MULTILEVEL INVERTER TOPOLOGY

This section presents the proposed hybrid MLI topology in terms of the topology configuration to show the structures for the different units in the hybrid system. Also, the process of generating the different steps in the output waveform

presents in the same section. Besides, the proposed method for charging the capacitors in the proposed topology has been discussed.

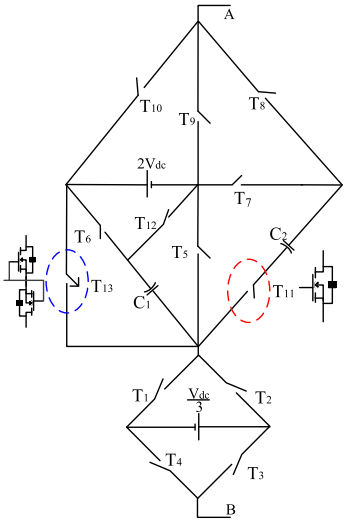

FIGURE 1. Proposed hybrid MLI topology.

A. PROPOSED TOPOLOGY CONFIGURATION

The proposed hybrid Multi-Cell 21-Level multilevel inverter has been presented in Figure. 1. The term ''hybrid'' refers to the the combination of two different units connected in cascade, an H-bridge with its classical (four switches and a separate DC source). The second unit is the modified K-Type unit. This unit uses ten switching devices, another separate DC source, and two chargeable DC capacitors acting as virtual DC suppliers. So in total, the system uses fourteen switching devices, two DC suppliers, and two chargeable DC capacitors to generate an output voltage waveform with 21 steps. The idea of using the virtual DC suppliers (which represents in the capacitors) keeps the number of the DC suppliers as lower as possible, which reduces the total cost of the topology and keeps it compactable. The proposed structure has also been designed well to prevent the possibility of forming any closed loop for the DC link.

The H-bridge unit generates an output voltage with three levels (+VdcH, 0, −VdcH); these outputs will be loaded into the output voltage of the second unit, which in turn generates an output voltage waveform with seven levels so that the total voltage waveform will be formed in the shape of the 21-Level output voltage waveform. The second unit has the name of (K-Type) because the switches of this unit have been arranged in the ''Kite'' shape, shortened to K-type. [10], [11].

B. LEVEL GENERATION AND SWITCHING MODES

The proposed topology generates an output voltage waveform with 21 steps, including 10 positive levels, 10 negative levels, and zero levels. These levels are formed through the switching devices based on a unique switching case for each level, generating a different 21 switching cases. Figure. 2 illustrates the different switching cases for all the 21-level cases. These cases have been summarized in Table. 1 present the active switches and DC suppliers for each case from the presented cases.

It is noticed from the proposed structure that there are sets of switches that aren't allowed to turn on in the same instant otherwise;, a short circuit will taking place. These sets are (T_9, T_{10}), (T_6, T_{12}), (T_5, T_{12}), and (T_6, T_{13}). The presented switching scheme in Table. 1 prevent each set of these pair switches from being turned on at the same time. The number of turning on times per one cycle for each switch has been mentioned in Table.1 it is noticed from this statistic that the maximum and the minimum number of turning on times are 7 and 1 respectively, which ensures low switching stress, especially in the low switching frequency operation.

C. PROCESS OF CAPACITORS CHARGING

In order to reduce the cost of the proposed topology as low as possible, the number of DC suppliers employed in the system should keep optimum. Hence, the real DC sources were replaced with virtual DC sources represented by a chargeable DC capacitor.

The chargeable DC capacitor should keep continuous charging and discharge during the running time. This paper proposed an online charging loop for the capacitors, which means that the capacitors' charging process will take place during the process of levels generating. The charging loop for both the capacitors in the K-Type unit (C_1&C_2) has been illustrated in Figure. 3. This loop provides a closes path between the $2V_{dc}$ and the capacitors (C_1&C_2). Also, the charging process has been mentioned in Table. 1 and the symbols C and D in the Table. 1 refer to the charging and discharging cases of the capacitors, respectively. The capacitors charging process is taking place during generating the levels (+2, +3, and +4) (see Figure. 2). During this time, the capacitors should be charged with V_{dc} for each capacitor based on the charging loop presented in Figure. 3.

III. COMPARATIVE STUDY BETWEEN THE PROPOSED TOPOLOGY AND THE OTHER EXISTING MLI TOPOLOGIES

In order to highlight the features of the proposed topology in reducing the number of the components and generates an output voltage waveforms with a low level of harmonics. This section presents a comparative studies between the proposed topology and a set of pre-invented MLIs topologies [10], [25], [26], [31], [34]–[38]. This study compares the main parameters of the structure such as the number of DC suppliers, drives, switches, and capacitors for each topology. Figure. 4 indicates the comparative studies for the number of switches, number of capacitors, number of DC suppliers, and the number of drives circuits in terms of the number of levels. For these statistics, the proposed topology presents a perfect performance in reducing the number switching devices which reflects in reducing the level of losses and switch stress and enhances efficiency.

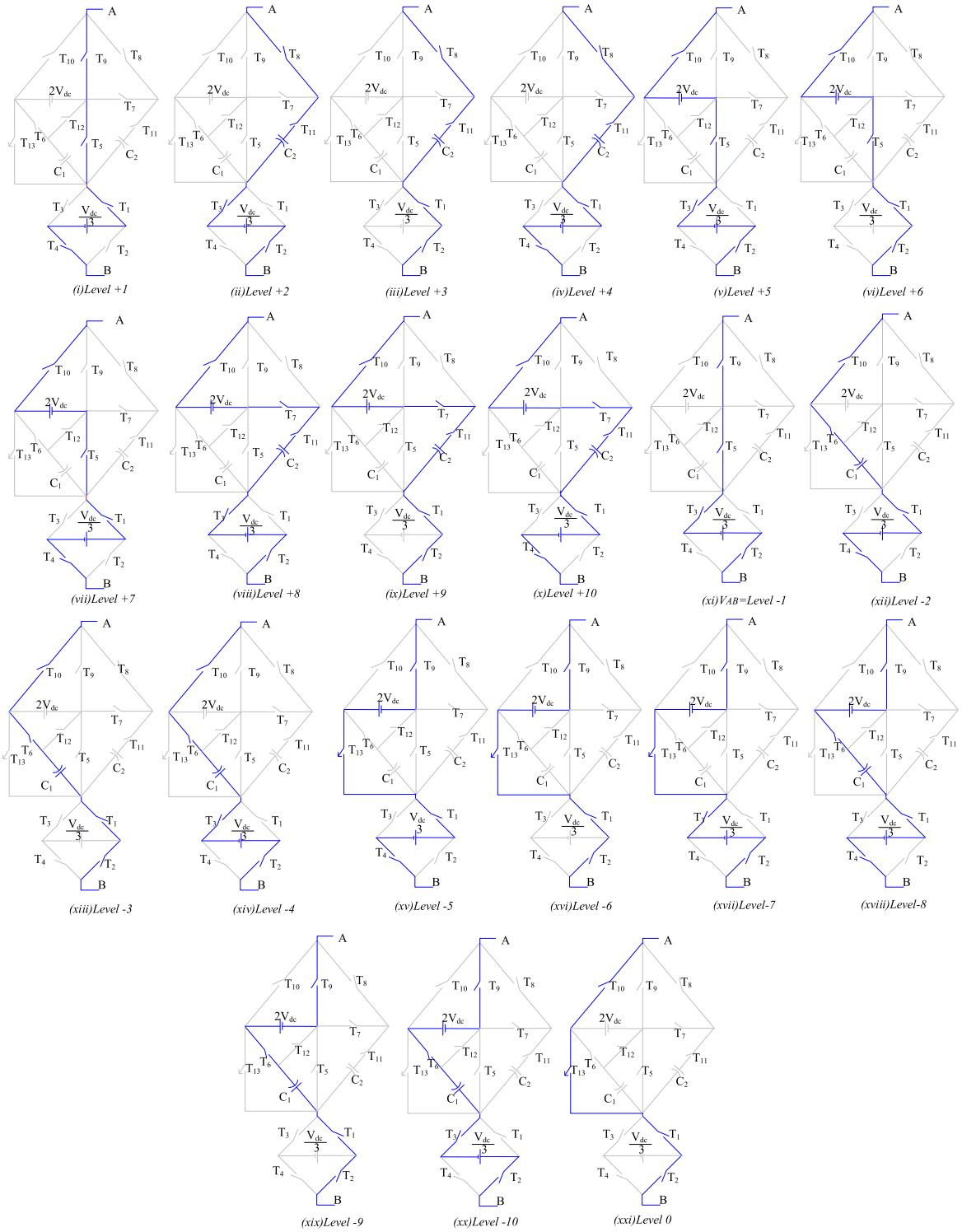

FIGURE 2. Different switching cases of the proposed topology.

One of the promising advantages of the proposed topology is that it uses a reduced number of DC suppliers as shown in Figure. 4-a. This reduction in the number of suppliers helps in reducing the total cost of the topology and gives a compact shape to the system. The proposed topology introduces a reasonable number of driving circuits which illustrates in Figure 4-b. compared with the other topologies this reduction helps in reducing the size of the system and makes it packageable. Dramatically, this reduction in the driving circuit helps the control circuit to be unloaded which gives a

TABLE 1. Different switching cases of the proposed topology.

		T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	C_1	C_2
POSITIVE HALF LEVELS	+10	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	---	D
	+9	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	---	D
	+8	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	---	D
	+7	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	---	---
	+6	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	---	---
	+5	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	---	---
	+4	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	C	C
	+3	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	C	C
	+2	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	C	C
	+1	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	---	---
ZERO	0	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	---	---
NEGATIVE HALF LEVELS	-1	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	---	---
	-2	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	D	---
	-3	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	D	---
	-4	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	D	---
	-5	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	---	---
	-6	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	---	---
	-7	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	---	---
	-8	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	D	---
	-9	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	D	---
	-10	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	D	---
ON TIMES PER CYCLE FOR EACH SWITCH		7	7	7	7	2	3	1	1	3	3	2	1	2		

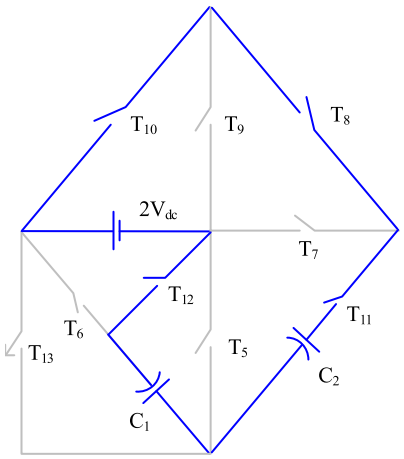

FIGURE 3. Capacitors charging loop.

fast response of the system. Compared to the other topologies in the comparison the proposed topology presents a reduction in the number of the switching devices, this reduction reduces the level of the losses associated with these switches and this gives a Satisfying percentage of efficiency. The comparison of the number of switches shows in Figure. 4-c.

Furthermore; the proposed topology uses a reduced number of capacitors compared with the other topologies that used the capacitors as a Virtual DC-link; this reduction in the capacitors appeared in the Figure. 4-d when it compared to the other MLIs topologies. In addition to the lack of using an auxiliary circuit for the charging process which supports the Uniqueness of the proposed topology.

Also, the comparison studies the number of components per pole for each topology from the different topologies [10], [31], [39]–[45]. This parameter has been studied in order to dedicate the most economical topology which uses the less number of components per pole. Consequently, this topology achieves low cost and high efficiency. This parameter has been calculated through the following formula:

$$N_{Com/Lev} = \frac{N_{Sup} + N_C + N_T + N_{Sw} + N_D + N_A}{N_P} \quad (1)$$

where:

$N_{Com/Lev}$: Number of components per pole for each level in the output voltage waveform.

N_{Sup}: number of Dc power suppliers that used to feed the topologies.

N_C: Number Capacitors in the proposed topology.

N_T: Number of transformers.

N_{Sw}: Number of switching devices.

N_D: Number of diodes in the converter circuit.

N_P: number of levels in the voltage waveform per pole.

N_A: Any auxiliary components in the converter circuit.

As mentioned above that this parameter has been used to predict the most economical topology that scores less cost and high reliability.

Table. 2 presents the numbers of the different components for the proposed topology and the other topologies and also the calculated values for the parameter $N_{Com/Lev}$ based on the (1). The references used in the comparison have been chosen accurately so that it use only Two DC suppliers as input suppliers as the same as the proposed topology. The presented data confirmed the superiority of the proposed topology over the other MLIs topologies when it achieves the most optimal design to generate the desired number of

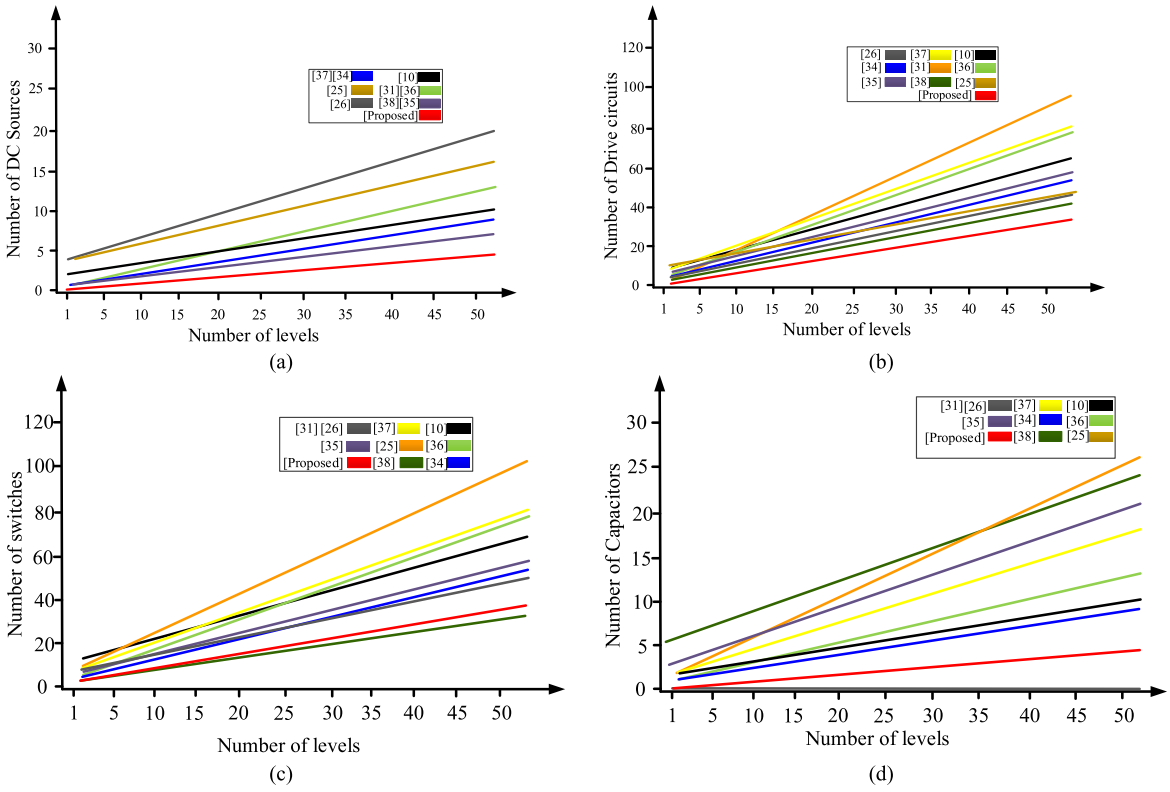

FIGURE 4. Comparative studies between (a) number of DC sources (b) number of drive circuits (c) number of switching devices (d) number of capacitors and its relations with the number of levels in the output waveform.

TABLE 2. Comparison between the proposed MLI topology and pre-invented topologies.

Ref	*lev*	N_{Sup}	N_C	N_T	N_{Sw}	N_D	N_P	N_A	$N_{Com/Lev}$
[41]	9	2	1	0	12	0	5	0	3
[39]	13	2	1	0	11	1	7	0	2.14
[10]	13	2	2	0	14	0	7	0	2.57
[40]	11	2	1	0	11	0	6	0	2.33
[42]	9	2	2	0	9	4	5	0	3.4
[43]	25	2	4	0	10	12	13	0	2.15
[44]	9	2	0	0	10	0	5	0	2.4
[31]	19	2	4	0	12	6	10	0	2.4
[45]	5	2	0	0	8	0	3	0	3.33
Pro	**21**	**2**	**2**	**0**	**14**	**0**	**11**	**0**	**1.63**

levels in the output voltage waveform with a reduced number of components which ensures a reduction in the total power losses and enhances the system reliability. Figure. 5 shows the Circle graph of the parameter $N_{Com/Lev}$ for the compared topologies.

Another feature for the proposed topology is the ability to present an output boosting stage for the output voltage. This boosting stage will help in maximizing the output voltage without adding a boosting circuit for this purpose. Consider the summation of the real input DC sources and the maximum amplitude of the 21L output voltage waveform, so the formula for the boosting factor that achieved from proposed topology is illustrated as follow:

$$\gamma = \frac{V_{o,Max}}{\sum V_{in}} \tag{2}$$

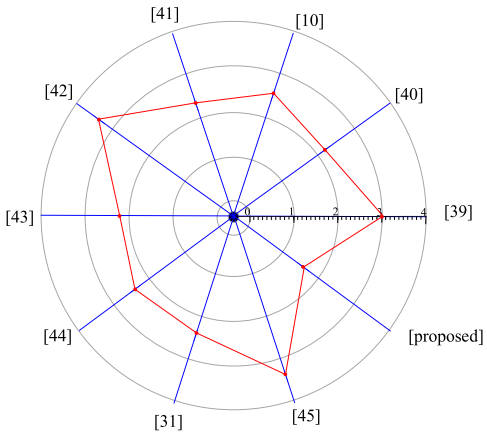

FIGURE 5. Circle graph of the parameter $N_{Com/Lev}$.

where γ is the boosting factor, $V_{o,max}$ is the maximum amplitude for the output voltage waveform and the denominator contains the summation of the real input DC sources. Based on the formula in (2) the calculated value for the boosting factor achieved by the proposed topology is 1.71. Table.3 presents a Comparative study between the proposed 21L MLI topology and some of the suggested MLIs topologies.

Regrading to the statistics on the previous table the proposed MLI topology achieves a stepping up for the input voltage compared to almost of the MLIs topologies in the

TABLE 3. Comparison between the proposed MLI topology and other topologies based the voltage boosting capability.

ref	N_{Sup}	*Nc*	*Nsw*	N_{lev}	*Boosting factor γ*
[46]	1	3	10	7	(No)1
[47]	2	3	14	9	(No)1
[48]	1	4	16	17	(No)1
[49]	2	2	12	17	(Yes)2
[50]	3	3	14	25	(No)1
[25]	4	0	12	17	(No)1
[10]	2	2	14	13	(Yes)2
[11]	2	4	14	13	(No)1
[34]	1	1	6	7	(No)1
proposed	**2**	**2**	**14**	**21**	**(Yes)1.71**

comparison except for the references [10], [49], [51] which records a step-up ratio slightly higher than the presented topology, but the proposed topology still beats these references in the other performance parameters that were mentioned earlier.

IV. CASCADED CONNECTION OF THE PROPOSED HYBRID TOPOLOGY

To satisfy the load demand and generates a proper level of the output power which upgrades to medium and high ranges, so the proposed topology can achieve this by connecting multiple units in a cascaded connection. This cascaded connection not only will increase the size of the delivered power, but also will reduce the level of noises in the output waveform to a neglectable level of noises. Increasing the number of steps in the output voltage waveform due to the cascaded connection helps in reducing the amount of THD and enhances the quality of the output waveforms. The voltage stress on the switches will reduce too. In the proposed topology, the amplification of the power range can be performed through two scenarios. The first scenario is to connect the modified K-Type unit in series with multiple units of H-bridge unit, and the second scenario is performed by connecting a single H-bridge unit in series with several units of the modified K-Type unit. Each scenario of these scenarios for series connection has a unique formula to calculate the number of the levels in the output voltage waveforms based on the number of the series units in the system. In case of H-bridge cascading, so the number of steps in the output voltage can be calculated from the following formula ($N_{level} = (7*3^m)$ where $m = 1, 2, 3 \ldots\ldots$) where m represents the number of H-bridge units in the system. On the other hand with the K-type unit cascading the output voltage levels ($N_{level} = (3*7^m)$ where $m = 1, 2, 3 \ldots\ldots$) where m represents the number of K-type units in the system. Figure. 6 illustrates the different cascaded connections based on pre-discussed scenarios.

V. POWER LOSSES AND CAPACITANCE CALCULATIONS

The total losses in any power electronics device represented by the summation of the switching losses conduction losses,

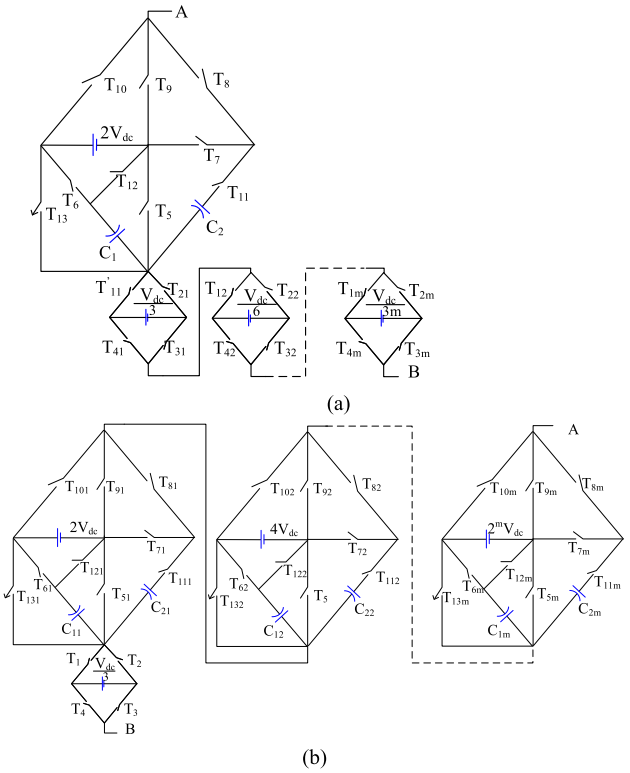

FIGURE 6. The different scenarios for the cascaded connection (a) Single modified K-Type unit with multiple HB units (b) Single HB unit with multiple K-Type units.

and the ripple losses. The conduction losses are defined as the amount of losses that leakages during the operating interval of this device. Due to the anti-parallel diode operation for almost of switches, so both the transistor and the diode have a conduction loss [52]. Hence; the calculation of the conduction losses include the conduction losses related to diodes and the conduction losses related to transistors, the average conduction losses power calculations summarized in the following equations:

$$P_{cond\_sw} = \frac{1}{T}\int_0^T (V_{sw} + R_{sw} * i^{\beta}(t)) * i(t)dt \quad (3)$$

$$P_{cond\_D} = \frac{1}{T}\int_0^T (V_D + R_D * i(t)) * i(t)dt \quad (4)$$

where: V_{sw}, V_D, R_{sw}, and R_D are the on-state voltage and resistance of the switching devices and diodes and the parameter β is related to the switching device, and i(t) is the current passing through the devices. Noteworthy that the total conduction losses equal to the summation of equations (3) & (4).

It is worth to point that the switching losses are defined as the losses power per each electronic device during the periods of turning this item ON or OFF [27]. The equation that used to calculate the switching power losses during both on and off periods are stated as follow:

$$P_{on} = \frac{1}{T}\int_0^{t_{on}} V(t) * i(t)\, dt = \frac{1}{6T} * V_{sw} * I * t_{on} \quad (5)$$

$$P_{off} = \frac{1}{T}\int_0^{t_{off}} V(t) * i(t)\, dt = \frac{1}{6T} * V_{sw} * I * t_{off} \quad (6)$$

where t_{on} and t_{off} are the turn-on and off times, respectively. V_{SW} and I are the voltage and current through the switch. So the generated pulses have been calculated carefullyand taking into account the most available reduction in the number of switching times, this helps in reducing the switching losses to keep the total losses in the circuit as low as possible.

The ripple losses represents the losses that depleted due to the ripple capacitor's voltage ΔVc and this amount of losses is formulated as follow:

$$P_{ripple} = 0.5 * C * \Delta V_c^2 * f \quad (7)$$

where P_{ripple} represents the ripple losses and f is the switching frequency. as the output power increases, the ripple losses as well as the the conduction losses has the biggest impact to controlling the overall losses and efficiency.

To prevent the occurrence of high-voltage ripples across capacitors, also for the optimum design of the proposed topology, so the optimal value of the capacitance of capacitors should be calculated carefully. For calculating the capacitance of each capacitor so the longest discharging cycle (LDC) of each capacitor must be detected. This parameter refers to the longest period that the capacitor takes to discharge energy toward the load in one cycle. Besides, the allowable level of voltage ripple for each capacitor [53], [54]. Based on the scheme presented in Table. 1 which represents the switching cases during a complete cycle. It is noticed that the capacitor C1 discharges its energy during the levels −2, −3, −4, −8, −9, and −10 with a percentage 14.12% of the total energy dissipated per one cycle. And C2 discharges its stored energy during the levels 2, 3, 4, 8, 9, and 10 with a percentage of 14.12% of the total energy dissipated per one cycle. Based on the rating of the inverter as well as the allowable level of voltage ripple so the optimal value of the capacitance can be calculated as follow:

$$E_{cn} = 0.5 C_n \Delta V^2 \quad (8)$$

$$E_{cn} = kE \quad (9)$$

where E_{cn} represented the stored energy in the capacitor, E is the total rated energy of the converter, k is the percentage of the energy that shared by each capacitor and ΔV is the allowable voltage ripple level ripple:

$$C_{opt\_n} \geq \frac{E_{cn}}{0.5\Delta V^2} \quad (10)$$

According to (10) the ripple in the output voltage will decrease within increasing the value of capacitance if the other parameters are kept constant.

VI. RESULTS AND DISCUSSIONS

The performance of the proposed 21L hybrid MLI topology has been verified based on two ways; firstly, the simulation verification performed through the simulation software (MATLAB /SIMULINK) environment and the simulation validation have applied for the single unit and the cascaded connection system. For the second way of verification, an experimental prototype has been built, and the captured results support the simulation results. Both the simulation and experimental verification presents a convincing performance through the presented results. The simulation, as well as experimental results, have been presented as follow.

A. SIMULATION RESULTS

The proposed topology has been implemented based on the simulation parameters presented in Table. 3. As follow the simulation results that were picked from the simulation file.

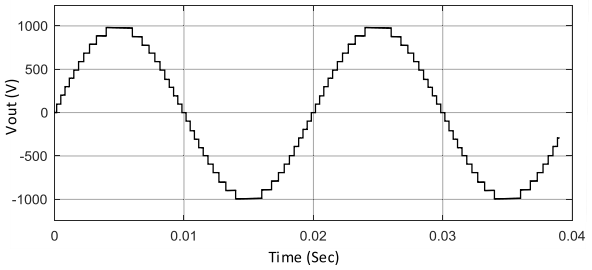

FIGURE 7. 7 21L MLI output voltage waveform.

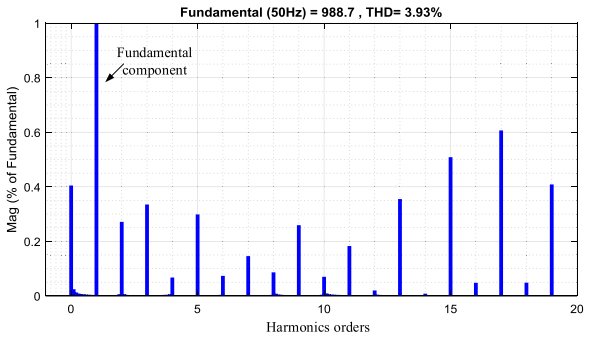

FIGURE 8. FFT analysis of the 21L output voltage waveform.

Figure. 7 presents the 21-Level output voltage waveform. Thanks to the high number of steps, the generated output voltage waveform is clear, fine, and close to the sinusoidal shape. For studying the level of harmonics content in the output waveform, an FFT analysis has been applied for the voltage waveform, and it recorded a low level of noise (3.93%). This reduction has its influence in reducing the size of the smoothing filter. The FFT analysis for the output voltage waveform has been illustrated in Figure. 8. The capacitors voltages attributed to the output voltage waveform have been illustrated in Figure. 9. It seems from the figure that the voltages of the capacitors are aligned to the desired value with a small amount of voltage ripple, which ensures a fixed and balanced voltage in the output side. The output voltage and load current have been shown in Figure. 10. The load current seems pure and free of harmonics; this will prevent the inverter from injecting any harmful harmonics orders to the

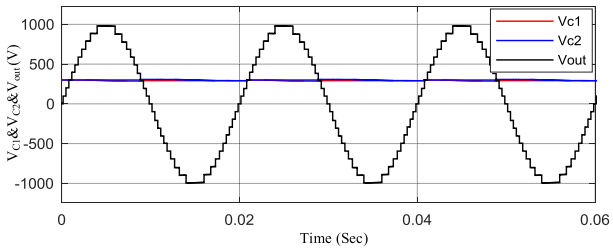

FIGURE 9. Capacitor voltages and the output voltage waveform.

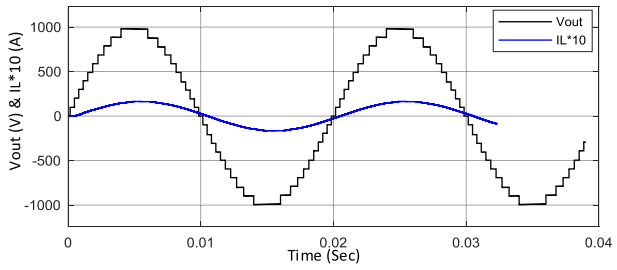

FIGURE 10. Output voltage and load current waveforms.

load, especially in the dynamic loads which suffering from mechanical malfunctions when it is exposed to such harmful harmonics.

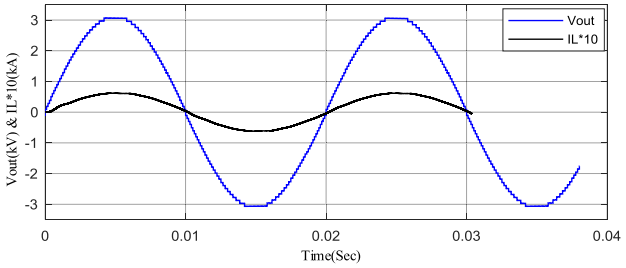

FIGURE 11. 63L cascaded system output voltage and load current.

As a complement to the study, the proposed MLI topology has been tested under the cascaded connection. The sequence for this test has been performed under the two scenarios of cascaded connection (Single HB unit with multiple K-Type units and single modified K-Type unit with multiple HB units) for simplicity the multiplication will be only two units for each type. Figure. 11 shows the output voltage waveform as well as the load current waveform for the cascaded connection (2HB+K). According to the formula that was presented previously to calculate the number of steps in the output voltage waveform, the voltage waveform, in this case, should have 63 steps which are achieved in the presented figure. The high number of steps in voltage waveform helps in reducing the level of THD and records only (1.78%) for the output voltage waveform, which makes the waveform closer to the sinusoidal shape. The FFT analysis of the voltage waveform has been shown in Figure. 12. Figure. 13. presents the output voltage for the different units in the cascaded system.

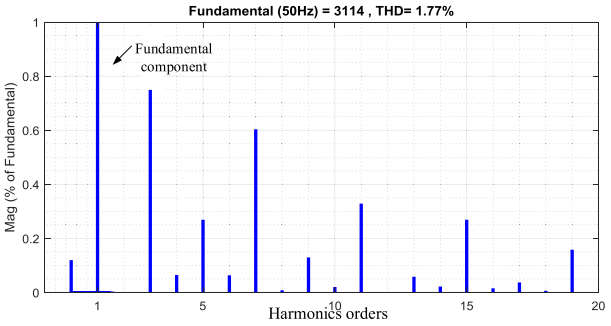

FIGURE 12. FFT analysis of the 63L output voltage waveform.

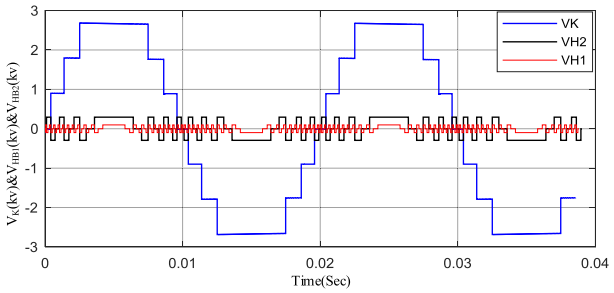

FIGURE 13. Output voltages of 2HB+K cascaded system units.

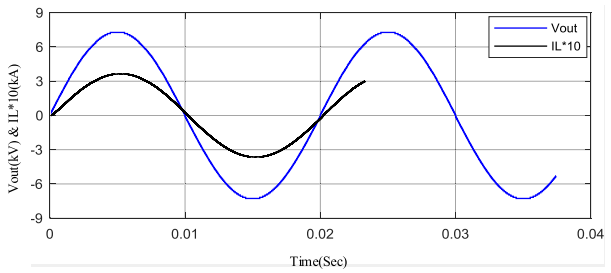

FIGURE 14. 147L cascaded system output voltage and load current.

In the case of the second connection scenario in the cascaded system, the connected units are an H-Bridge unit that is cascaded with two K-type units (HB+2K). The output voltage waveform and the load current have been presented in Figure. 14. The waveforms presented are perfect and look free of any harmonics content. According to the formula for calculating the number of steps in the output voltage waveform the output voltage should contain 147 steps as the same as presented in the figure. This high number of steps in the waveform makes the signal more closely to the sinusoidal shape and has a neglectable value of THD (0.73%). The FFT analysis for the output voltage waveform under the second case of cascaded connection has been illustrated in Figure. 15. The voltages of the different units in the cascaded system (HB+2K) have been shown in Figure. 16.

B. EXPERIMENTAL RESULTS

The performance of the proposed 21L MLI topology has been tested through the simulation results in the previous

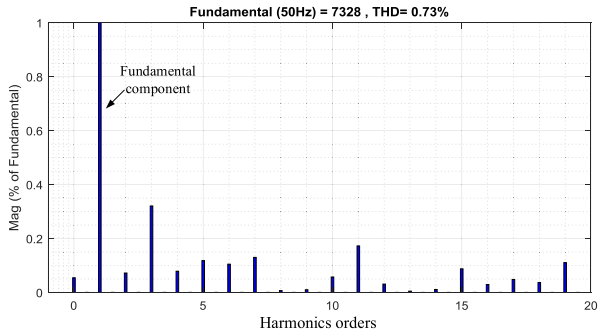

FIGURE 15. FFT analysis of the 147L output voltage waveform.

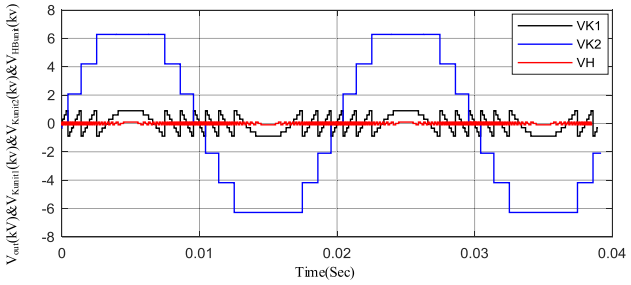

FIGURE 16. Output voltages of Asymmetrical cascaded system units.

subsection and to support these simulation results of the proposed topology. So an experimental prototype has been built, taking into account the configuration parameters that mentioned in Table. 4. The system has been controlled based on the controller hardware unit (dSPACE DS1103). The experimental system has been tested, and the following results have been captured and presented as follows.

TABLE 4. Simulation parameters of the proposed hybrid MLI topology.

OUTPUT LEVELS	*21-LEVEL*	
INPUT VOLTAGE	V_{dc1}=100V	V_{dc2}=600v
CAPACITOR VOLTAGE	V_{C1}=300V	V_{C2}=300V
CAPACITANCE VALUE	C_1>3600uf	C_2> 3600uf
LOAD PARAMETERS	L= 5mH	R=12 Ω

TABLE 5. Experimental configuration parameters of the proposed hybrid MLI topology.

	Hybrid MLI system	*Cascaded MLI system*
switches	IRFP460	
Capacitors	4700uf-50v- LLS1H472MELB	
Input sources	V_{HB}= 8v V_K= 48v	V_{HB1}= 3 v,V_{HB2}= 9 v V_K =54 v
Output levels	21	63
Controller	dSPACE **DS1103** hardware unit.	
Load	R=28	L=70mH

The photography of the proposed hybrid system setup has been shown in Figure. 17. The output voltage waveform for

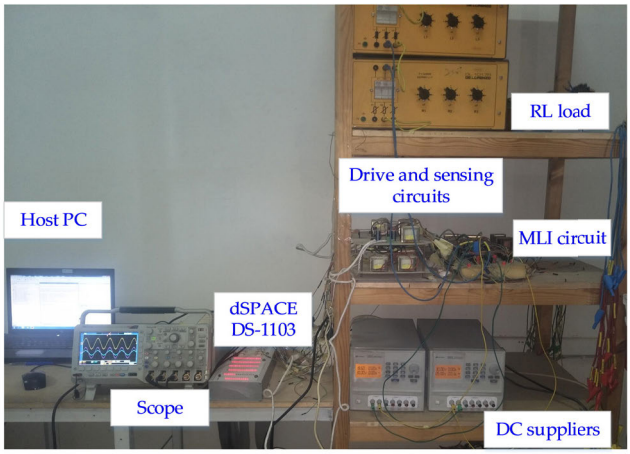

FIGURE 17. Photograph of the experimental setup.

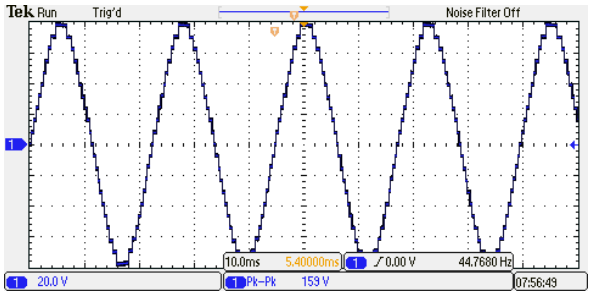

FIGURE 18. 21L Hybrid MLI system output voltage waveform.

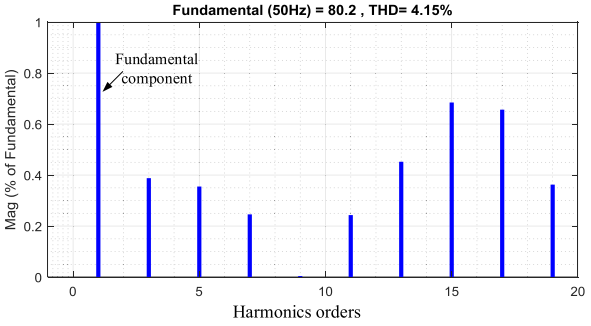

FIGURE 19. FFT analysis for the 21L output voltage waveform.

the proposed 21L hybrid MLI topology has been illustrated in Figure. 18. The generated output voltage is clear, fine, and looks very near to the sinusoidal shape. The high number of output steps lead to a reduction in the value of THD, which is related to the output voltage. The FFT analysis of the output voltage is shown in Figure. 19. The reduction in the harmonics contents helps in reducing the size of the filter components. Consequently; both the size and the cost of the system are reduced. The output voltage waveform, load voltage and load current have been presented in Figure. 20. It is noticed from the figure that the load current is aligned to the load voltage and both the waveforms look fine and free of harmonics which validate unity power factor operation for

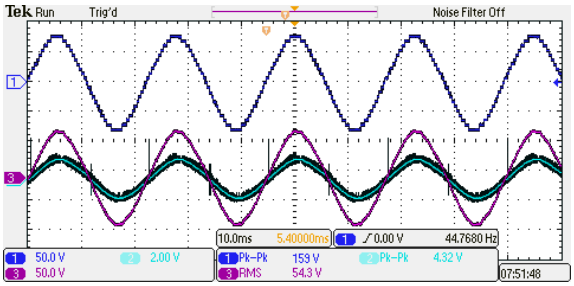

FIGURE 20. Output voltage load voltage and current.

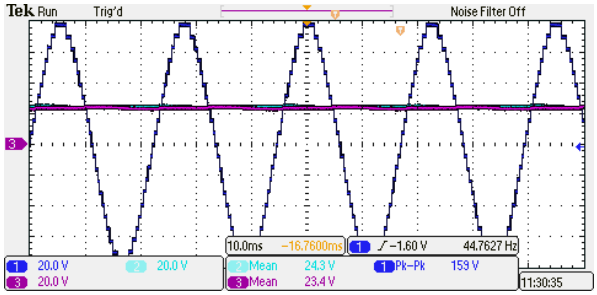

FIGURE 21. Capacitors voltages and the output voltage waveform.

the system. Figure. 21 shows the voltages of the capacitors attributed to the output voltage waveform. The capacitor's voltages look constant with a small amount of ripple voltage. This output capacitor voltage supports strongly the proposed technique for charging and balancing the capacitor's output voltage.

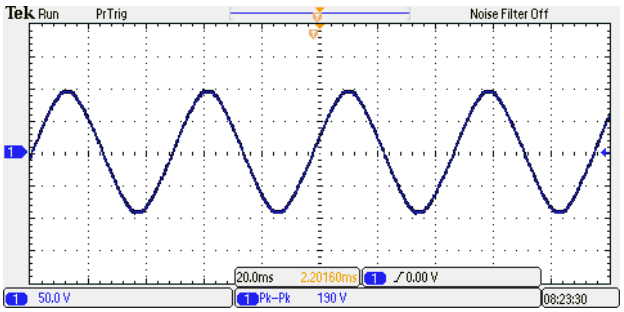

FIGURE 22. Cascaded system output voltage waveform.

In case of verifying the experimental results for the cascaded MLI system, the 63L cascaded MLI system has been chosen. The system has been built by repeating the H-bridge unit, and the values of the input DC sources have been mentioned in Table. 4. Figure. 22 presents the output voltage waveform of the cascaded system. The increase in the number of the steps in the output voltage waveform makes it finer and closer to the sinusoidal shape with a neglectable amount of harmonics content, and this appears in the load current and voltage that presented in Figure. 23. The output voltage of the three units in the tested system has been presented in Figure. 24.

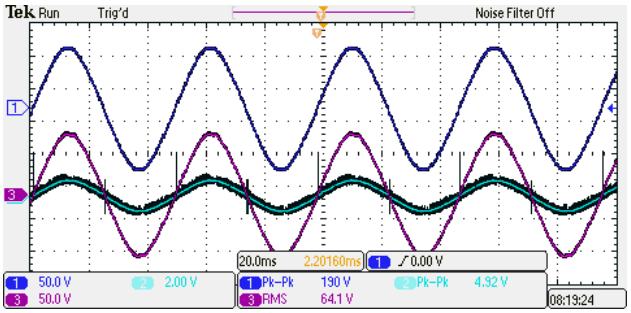

FIGURE 23. Output voltage waveform and load voltage and current.

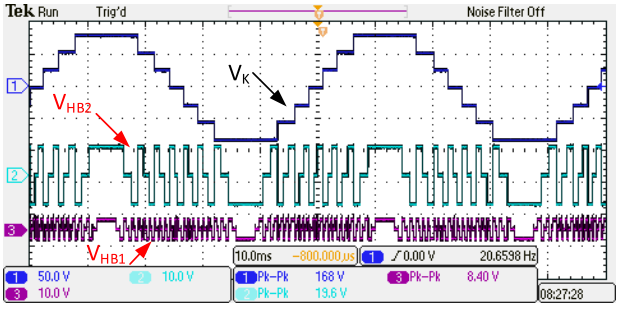

FIGURE 24. Output voltages of the different units in the cascaded system.

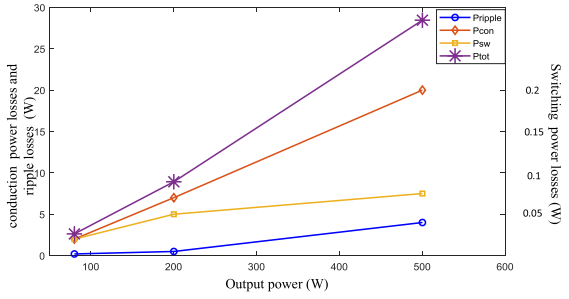

FIGURE 25. Conduction, switching, and ripple losses at different output power values.

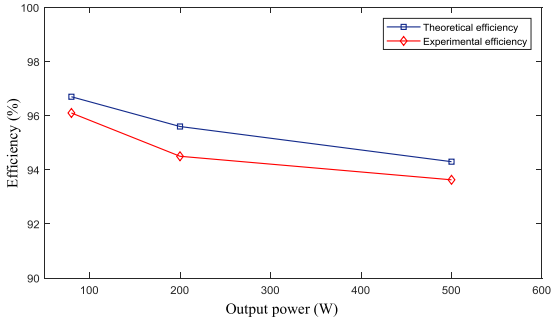

FIGURE 26. Theoretical and experimental efficiency.

The formulas for the conduction, switching, and ripple losses that presented in (3–7) have been used to calculate the different losses, as well as the total power losses based on the level of the output power and the datasheet of the

power switch. Hence the system efficiency can be calculated. Figure. 24 presents the total losses in the proposed system represented by the conduction losses, switching losses, and the ripple losses. These losses used to calculate the system overall efficiency. The theoretical and the experimental efficiencies have been illustrated in Figure. 25. The range of the system efficiency is located between (96–94)% with an average value of 95% which ensures high efficiency for the proposed MLI topology.

VII. CONCLUSION

The work in this paper presented a hybrid multilevel inverter that consisted of a series connection between two units (an HB unit with a modified K-Type unit). This combination generates an output voltage waveform with 21 steps. This high number steps in the output voltage help in reducing the level of noises in the output voltage and reduced the stress in the switching devices, which on the one hand generating fine and clear waveforms and on the other hand reduces the harmonic content in the waveforms to a deficient level (satisfying the harmonics standard IEEE519). Economically, the structure of the proposed topology presented an optimal design in terms of reducing the number of switches and DC sources which in turn enhancing the system reliability by reducing the inverter cost. For the capacitors charging process, the paper presents an online method for charging and balancing the capacitor voltages without any auxiliary circuits for that. This helps in the continuous operation of the charging and discharging process for the capacitor without disturbing the process of generating the output voltage. The proposed topology supports the modularity process in order to maximize the range of output power to the medium and high level, and the paper presented two scenarios for the series connection 2HB+K and HB+2K both the cases raise the level of the output power and enhances the system performance to achieve high efficiency. Due to the dependence on multi DC sources, this topology is suitable for renewable energy applications; DC sources are abundant. The hybrid renewable energy sources application will be more appropriate between all the renewable energy applications because the proposed topology-based mainly on two unequal DC suppliers, which will be available easily in the hybrid renewable energy sources.

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