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Hybrid Nonisolated Active Quasi-Switched DC-DC Converter for High Step-up Voltage Conversion Applications

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ABSTRACT This paper deals with a hybrid non-isolated active quasi-switched dc-dc converter with a high-boost voltage gain, which is applicable for the high step-up low power applications. By using fewer number of components in circuit topology, the proposed converter can provide higher-gain voltage with a small duty cycle, which can reduce the voltage stress and conduction loss on power switches. In addition, it draws continuous input current, has lower diode voltage stress and lower passive component voltage ratings. The operating principles and key waveforms in continuous conduction mode and discontinuous conduction mode are presented. Small-signal dynamic analysis, parameter design guideline, power loss calculation, and characteristics comparison with other non-isolated converters have been completed. Finally, a 250W hardware prototype is constructed and the experimental results are presented to verify the feasibility of the proposed converter.

INDEX TERMS Dual switches, high voltage gain, non-isolated dc-dc converter, switched-capacitor, switched-boost network.

I. INTRODUCTION

With the large consumption of traditional fossil energy and the increasing awareness of environmental protection, the development and utilization of renewable energy sources, such as solar, wind, and fuel cells, has become more and more important. However, the output voltage of the distributed renewable energy sources is relatively low, which is far away from the desired dc-link voltage level of grid-connected inverters [1], [2]. Therefore, a high step-up dc-dc converter is required to boost the low voltage of renewable energy sources into a constant and high level dc-bus voltage, as shown in Fig. 1. While in other low power industrial applications, such as TV-CRTs, medical X-ray equipment systems, battery-powered LED lighting systems and automobile high-intensity discharge headlamps, the dc/dc converter with high voltage conversion ratio is also required.

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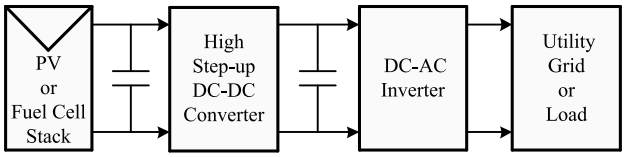


FIGURE 1. Typical schematic of the two-stage power-conversion system.

Many high boost dc-dc converter topologies have been developed and investigated to produce high voltage gain, which can be divided into two categories: isolated and non-isolated circuit topologies. For the isolated and coupled-inductor based topologies [3]–[7], a high frequency transformer or a coupled-inductor is used to boost the output voltage gain by choosing appropriate turn ratio and operating duty cycle; however, the stored energy in leak inductance is another negative impact, which should be solved by additional snubber circuits [8], [9].

Among the non-coupled-inductor type dc-dc converter topologies, traditional boost converter is one of the most commonly used topology. Theoretically, its output voltage gain can be infinite when the operating duty cycle is approaching to one. However, the switch turn-off time will be very narrow, which will induce large current ripple of the input and output current [10]. In addition, the peak current flow through the power switch will become very large, and the conduction power loss will be increased dramatically. Therefore, the output voltage gain of traditional boost converter is limited, which cannot meet the requirements of the practical industrial applications.

In order to produce higher voltage gain without an extremely high operating duty cycle, conventional boost converters can be cascaded in series [11]; however, the system's size and cost will be increased due to many elements and control units are used in the topology. By introducing voltage multiplier cells into the traditional boost converter, some high step-up dc-dc converters are developed in [12], [13]. Converters adopting interleaved configuration and voltage lift techniques have been presented in [14], [15], which can produce high-gain voltage and reduce the voltage and current stresses. Moreover, by utilizing switched-inductor (SL) cells to replace the conventional inductors, some nonisolated high-gain SL dc-dc converters have been proposed in [16], [17]. Similarly, switched-capacitor (SC) units can also be applied to dc-dc converter topologies, as presented in [18]–[20], to further increase the output voltage gain. By combining the active switch network with the traditional SL and SC cells, a multicell switched-inductor/switched-capacitor based active network converters (SL/SC-ANCs) are developed in [21], [22], which can provide high voltage gain with low voltage stress across switches and diodes.

However, the operating duty cycle range of the above boost-based nonisolated dc-dc converters is wide, which is varied from 0 to 1. In this case, a larger duty cycle will be utilized to produce a higher voltage gain, which will induce high conduction power loss accordingly on active power switches. In order to reduce the operating range of the switches' duty cycle to (0, 0.5), impedance source networks, such as Z-source network [23] and switched-boost network [24], have been applied to dc-dc converter topologies. In [25], a PWM discontinuous input current Z-source dc-dc converter is proposed, which has higher voltage gain than traditional boost converter. To improve the input current profile, some high voltage gain quasi-Z-source dc-dc converters are presented in [26], [27]. By changing the connection way between the load and the traditional Z-network, a high-gain voltage common grounded Z-source dc-dc converter is proposed in [28]. By combining several traditional (quasi-)Z-source networks in different ways, a family of hybrid Z-source boost dc-dc converters [29] are developed, which have further enhanced the output voltage boost capability. Similarly, by introducing switched-capacitor, switched-inductor or voltage multiplier cells into the switched-boost network, several new high step-up switched-boost dc-dc converters are put forward in [30], [31], respectively, but at the cost of too many components used in the circuit topology.

In this paper, a new hybrid nonisolated active quasi-switched dc-dc converter with high step-up voltage conversion ratio is proposed, as shown in Fig. 2, which has the following main advantageous features: high output voltage gain with a small duty cycle, low voltage stress across power switches and output diode, simple structure and easy to control. Section II gives a detailed steady-state operating principle analysis of the proposed converter in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Small-signal dynamic performance is analyzed in Section III. The comprehensive characteristics comparison between the proposed topology and other well known structures will be performed in Section IV. In addition, the detailed power loss analysis and efficiency comparison are presented in Section V. Then, in Section VI, experimental results are shown to verify the theoretical analysis. Finally, Section VII draws a conclusion.

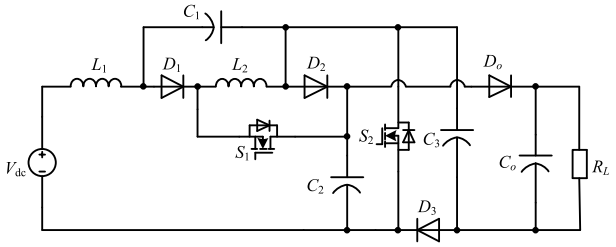


FIGURE 2. The topological configuration of the proposed converter.

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

This section presents the detailed operating principle analysis of the proposed converter in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Both switches S_1 and S_2 are turned on and off at the same time. To simplify the operating principle analysis in both CCM and DCM, the following conditions are assumed: 1) all components are ideal and lossless; 2) all capacitors, inductors and resistors are linear, time invariant and frequency independent; 3) the capacitance value of all capacitors are large enough to maintain the constant capacitor voltage; 4) inductor currents iL1 and iL2 are all increased or decreased linearly.

A. CIRCUIT ANALYSIS IN CCM

The proposed converter operates in CCM can be divided into two operating modes: 1) mode1 and 2) mode 2. Fig. 3(a) shows the key waveforms of the proposed converter in CCM. The corresponding equivalent circuits of the proposed converter during CCM are shown in Fig. 4(a) and (b), respectively.

1) Mode 1 [t_0-t_1, Fig. 4(a)]: In this operating mode, switch S_1 and S_2 are turned on simultaneously. Diode D_o is forward-biased, while diodes D_1, D_2 and D_3 are reverse-biased.

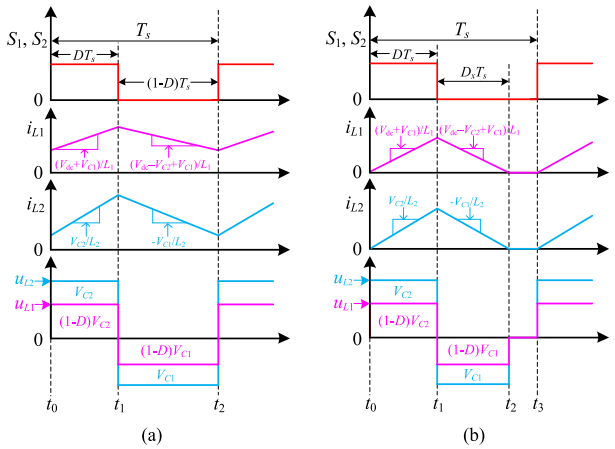


FIGURE 3. Key waveforms of the proposed converter: (a) CCM, (b) DCM.

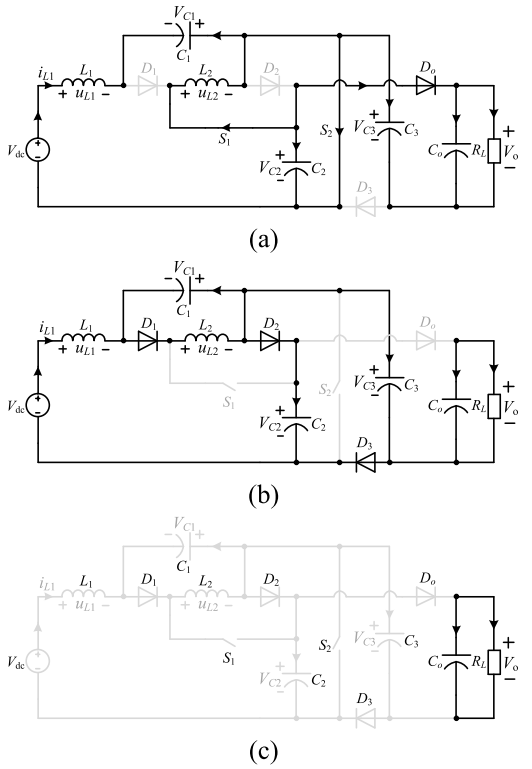


FIGURE 4. Operating modes of the proposed converter: (a) Mode 1, (b) mode 2, (c) mode3 in DCM.

The time interval of this mode is DT, where D and T are the duty cycle and switching period, respectively. Inductors L_1, L_2 are charged while capacitors C_1, $C_2$and C_3 are discharged. There are three loops in this states: 1) loop 1 consists of $V_{\rm dc}$, L_1, C_1 and S_2, in which $V_{\rm dc}$ and C_1 discharge the energy to L_1 through S_2; 2) loop2 is composed of C_2, S_1, L_2 and S_2, capacitor C_2 charges L_2 through S_1 and S_2; 3) loop 3 is consisted of C_2, D_o, C_o, R_L, C_3 and S_2, where C_2 and C_3 are connected in series to discharge the energy to C_o and R_L through D_o and S_2. By applying Kirchhoff's voltage law (KVL) to Fig. 4(a), the following equations can be derived:

$$L_1\frac{di_{L1\_on}}{dt} = V_{dc} + V_{C1} \quad L_2\frac{di_{L2\_on}}{dt} = V_{C2} \tag{1}$$

$$V_o = V_{C2} + V_{C3} \tag{2}$$

2) Mode 2 [t_1-t_2, Fig. 4(b)]: In this state, switch S_1 and S_2 are all turned off, diodes D_1, D_2 and D_3 are forward-biased, diode D_o is reverse-biased. The time interval of this operating mode is (1-D)T. Inductor L_1, L_2 are discharged, while capacitor C_1, C_2 and C_3 are charged. There are four loops in this state: 1) loop 1 consists of $V_{\rm dc}$, L_1, D_1, L_2, D_2 and C_2. $V_{\rm dc}$, L_1 and L_2 are connected in series to discharge the energy to C_2; 2) loop 2 is composed of L_2, C_1 and D_1. Inductor L_2 discharge the energy to capacitor C_1; 3) loop 3 is consisted of $V_{\rm dc}$, L_1, D_1, L_2, D_2, C_3 and D_3. $V_{\rm dc}$, L_1 and L_2 charges C_3 through D_1, D_2 and D_3; 4) loop 4 is composed of C_o and R_L. C_o discharges the energy to load R_L. Similarly, by applying KVL in Fig. 4(b), the following formula can be derived as:

$$\begin{cases} L_1\dfrac{di_{L1\_off}}{dt} = V_{dc} - V_{C2} + V_{C1} \\ L_2\dfrac{di_{L2\_off}}{dt} = -V_{C1}V_{C2} = V_{C3} \end{cases} \tag{3}$$

In steady-state, by using the inductors' volt-second balance principle during one switching period. From (1) to (3), it has

$$\begin{cases} D\left(V_{dc} + V_{C1}\right) + (1-D)\left(V_{dc} - V_{C2} + V_{C1}\right) = 0 \\ DV_{C2} - (1-D) \quad V_{C1} = 0 \end{cases} \tag{4}$$

Solving equation (4), the steady-state capacitor voltage and the output voltage V_o can be obtained as,

$$\begin{cases} V_{C1} = \dfrac{D}{1-3D+D^2}V_{dc} \quad V_{C2,3} = \dfrac{1-D}{1-3D+D^2}V_{dc} \\ V_o = V_{C2} + V_{C3} = \dfrac{2\,(1-D)}{1-3D+D^2}V_{dc} \end{cases} \tag{5}$$

From (5), the output voltage gain of the proposed converter in CCM can be derived as,

$$G_{CCM} = \frac{V_o}{V_{dc}} = \frac{2\,(1-D)}{1-3D+D^2} \tag{6}$$

B. CIRCUIT ANALYSIS IN DCM

The proposed converter will operate in discontinuous conduction mode when light loads are used. Fig. 3(b) shows the key waveforms of the proposed converter in DCM. In this situation, there are three operating modes and the equivalent circuit diagrams are shown in Fig. 4(a)-(c), respectively.

1) Mode 1 [t_0-t_1, Fig. 4(a)]: This operating mode is same as the mode 1 in CCM. From (1), the peak-to-peak value of inductor current i_{L1}, i_{L2} in mode 1 is

$$\Delta i_{L1} = \frac{V_{dc} + V_{C1}}{L_1}DT_s \quad \Delta i_{L2} = \frac{V_{C2}}{L_2}DT_s \tag{7}$$

2) Mode 2 [t_1-t_2, Fig. 4(b)]: The corresponding equivalent circuit schematic diagram is shown in Fig. 4(b). The time interval of this operating mode is D_xT_s. Inductor voltage u_{L1}, u_{L2} can be calculated by using (3).

Mode 2 in DCM ends when the inductor current i_{L1}, i_{L2} are reduced to zero.

3) Mode 3 [t_2-t_3, Fig. 4(c)]: Switch S_1 and S_2 are still turned off, and inductor currents are reduced to zero, as shown in Fig. 4(c). The stored energy in capacitor C_o is discharged to load R_L, and the inductor voltages in this mode are also zero.

Based on the assumption of power circuit is lossless, the average inductor currents I_{L1}, I_{L2} are derived as

$$\bar{I}_{L1} = \bar{I}_{in} = \frac{V_o^2}{RV_{dc}} \quad \bar{I}_{L2} = \frac{D + D_x}{D_x}\bar{I}_{L1} \tag{8}$$

The discontinuous conduction mode occurs with the following condition,

$$\bar{I}_{L1} - \Delta i_{L1}/2 \le 0 \quad \bar{I}_{L2} - \Delta i_{L2}/2 \le 0 \tag{9}$$

Substituting (7) and (8) into (9), the boundary condition between CCM and DCM can be obtained as,

$$\frac{2L_1}{RT_s} \le \frac{D\left(1 - 3D + D^2\right)}{4} \quad \frac{2L_2}{RT_s} \le \frac{D\left(1 - 3D + D^2\right)}{4} \tag{10}$$

Assuming $L_1 = L_2$ and denoting $K = 2L/RT_s$, $K_{\text{crit}} = D(1\text{-}3D + D^2)/4$, Fig. 5 shows the plot of K_{crit} as a function of duty cycle D at the CCM and DCM boundaries. When $K > K_{\text{crit}}$, the proposed converter operates in CCM; when $K < K_{\text{crit}}$, the converter operates in DCM.

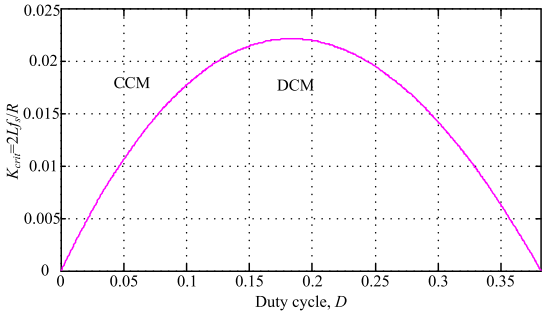


FIGURE 5. CCM/DCM boundary condition of the proposed converter.

In DCM operating mode, from Fig. 4(a), the average inductor current can be calculated as,

$$\begin{cases} \bar{I}_{L1} = \dfrac{D + D_x}{2}\Delta i_{L1} = \dfrac{D + D_x}{2}\dfrac{V_{dc} + V_{C1}}{L_1}DT_s \\ \bar{I}_{L2} = \dfrac{D + D_x}{2}\Delta i_{L2} = \dfrac{D + D_x}{2}\dfrac{V_{C2}}{L_2}DT_s \end{cases} \tag{11}$$

According to the volt-second balance property of inductor L_1, L_2 in DCM, and solving (8) and (11), one can obtain the following formulas,

$$V_{dc} + V_{C1} = \frac{D_x}{D + D_x}V_{C2} \Rightarrow D_x = \frac{D\left(V_{dc} + V_{C1}\right)}{V_{C2} - V_{C1} - V_{dc}} \tag{12}$$

Due to $V_{C2} = V_o/2$, and substituting (12) into (8), the expression of D_x can be derived as

$$D_x = \frac{4L_1 G_{DCM}}{RDT_s} \tag{13}$$

Therefore, from (8), (11), (12) and (13), the output voltage gain of the proposed converter in DCM can be obtained as

$$G_{DCM} = 1 + \frac{D^2}{4K} + \frac{1}{2}\sqrt{4 + \frac{6D^2}{K} + \frac{5D^4}{4K^2}} \tag{14}$$

Based on (14), Fig. 6 shows the output voltage gain curve G_{DCM} with variation of the duty cycle D for the proposed converter in DCM. From this figure, it can be seen that the output voltage gain in DCM is higher than that of in CCM, and the voltage gain decreases with K increases. When $K > 0.022$, the proposed converter operates in CCM mode.

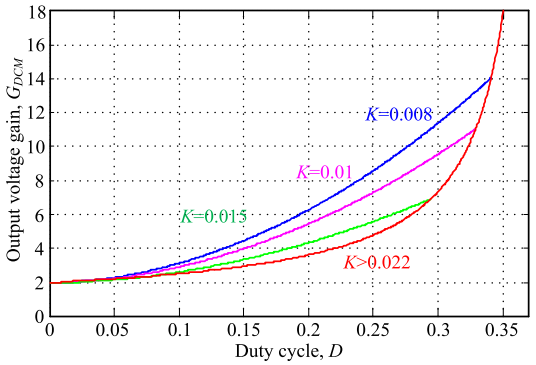


FIGURE 6. Relationship between DCM output voltage gain and duty cycle D.

Based on the aforementioned DCM operating principle analysis, the average inductor current I_{L1} and I_{L2} are

$$\bar{I}_{L1} = \frac{DD_x T_s G_{DCM} V_{dc}}{4L_1} \quad \bar{I}_{L2} = \frac{(D + D_x)\, DT_s G_{DCM} V_{dc}}{4L_2} \tag{15}$$

Therefore, the inductor power loss of the proposed converter in DCM mode can be calculated by:

$$P'_{rL} = \bar{I}_{L1}^2 r_L + \bar{I}_{L2}^2 r_L \tag{16}$$

The capacitor power loss of the proposed converter in DCM mode can be calculated by

$$\begin{aligned} P'_{rC} &= \bar{I}_{C_{1-\text{RMS}}}^2 r_C + \bar{I}_{C_{2-\text{RMS}}}^2 r_C + \bar{I}_{C_{3-\text{RMS}}}^2 r_C + \bar{I}_{C_{o-\text{RMS}}}^2 r_C \\ &= \frac{D\,(D + D_x)}{D_x} I_{L1}^2 r_C + \frac{1 - D}{D}\left(\frac{G_{DCM} V_{dc}}{R_L}\right)^2 r_C \\ &\quad + \frac{(D + D_x)\left(1 - D + D^2\right)^2}{4DD_x} I_{L2}^2 r_C \\ &\quad + \frac{(D + D_x)\left(1 - 3D + D^2\right)^2}{4DD_x\,(1 - D)^2} I_{L1}^2 r_C \end{aligned} \tag{17}$$

The total diode power loss of the proposed converter in DCM mode can be expressed as

$$P'_{D-loss} = V_F\left[D_x \bar{I}_{L2} + \frac{1 - D + D^2}{2}\bar{I}_{L2} + \frac{1 - 3D + D^2}{1 - D}\bar{I}_{L1}\right] \tag{18}$$

The total MOSFET power loss of the proposed converter in DCM mode can be calculated by

$$\begin{aligned} P'_{mosfet} &= P'_{conduction} + P'_{switching} \\ &= \frac{V_{dc}\bar{I}_{L1}\left(t_{on}+t_{off}\right)f_s}{2\left(1-3D+D^2\right)}\cdot\left(\frac{D}{1-D}+\frac{1+D-D^2}{2D}\right) \\ &\quad + \frac{4D^2+\left(1+D-D^2\right)^2}{4D\left(1-D\right)^2}r_{DS}\bar{I}_{L1}^2 \end{aligned} \tag{19}$$

Based on the above power loss analysis of inductors, capacitors, diodes and MOSFETs. The total power loss of the proposed converter in DCM mode can be expressed as

$$P'_{total-loss} = P'_{rL} + P'_{rC} + P'_{D-loss} + P'_{mosfet} \tag{20}$$

Then, the efficiency of the proposed converter in DCM can be calculated by

$$\begin{aligned} \eta &= \frac{P_{in}-P'_{total-loss}}{P_{in}} = 1-\frac{P'_{total-loss}}{P_{in}} \\ &= 1-\frac{P'_{rL}+P'_{rC}+P'_{D-loss}+P'_{mosfet}}{V_{dc}\bar{I}_{L1}} \end{aligned} \tag{21}$$

III. SMALL-SIGNAL DYNAMIC ANALYSIS

For simplicity, we assume that $L_1 = L_2 = L$, and choosing capacitor voltages and inductor currents as the state-variables, the input voltage V_{dc} as the input variable. Based on the state-space averaging method in [28], by separating ac components, and after Laplace transformation, the small-signal transfer function of the proposed converter can be obtained as

$$\begin{cases} sL_1\hat{i}_{L1}(s) = V_{C2}\hat{d}(s) + \hat{u}_{dc}(s) + \hat{u}_{C1}(s) - (1-D)\hat{u}_{C2}(s) \\ sL_2\hat{i}_{L2}(s) = (V_{C1}+V_{C2})\hat{d}(s) + D\hat{u}_{C2}(s) - (1-D)\hat{u}_{C1}(s) \\ sC_1\hat{u}_{C1}(s) = -I_{L2}\hat{d}(s) - \hat{i}_{L1}(s) + (1-D)\hat{i}_{L2}(s) \\ sC_2\hat{u}_{C2}(s) = \left[(2D-1)I_o/D/(1-D) - (2-D)I_{L2}\right]\hat{d}(s) \\ \qquad\qquad -D\hat{i}_{L2}(s) - 2\hat{u}_{Co}(s)/R_L + (1-D)\hat{i}_{L1}(s) \\ sC_o\hat{u}_{Co}(s) = I_o\hat{d}(s)/D \end{cases} \tag{22}$$

where the symbol "^" denotes the small-signal perturbations of the equilibrium points of state variables. Solving the above small-signal state equation (22) with the input voltage perturbation $u_{dc}(s) = 0$, the transfer function from control duty cycle $d(s)$ to capacitor voltage $V_{C2}(s)$ can be derived as

$$\begin{aligned} G_{vd}(s) &= \left.\frac{\hat{u}_{C2}(s)}{\hat{d}(s)}\right|_{\hat{u}_{dc}(s)=0} \\ &= \frac{b_3s^3+b_2s^2+b_1s+b_0}{a_4s^4+a_3s^3+a_2s^2+a_1s+a_0} \end{aligned} \tag{23}$$

where $b_3 = [(2D\text{-}1)I_o/D/(1\text{-}D)\text{-}(2\text{-}D)I_{L2}]L^2C_1$, $b_2 = LC_1[(1\text{-}2D)V_{C2}\text{-}DV_{C1}\text{-}2LI_o/R/D/C_o]$, $b_1 = L[(2D\text{-}1)(2\text{-}2D+D^2)I_o/D/(1\text{-}D)\text{-}(5\text{-}6D+3D^2\text{-}D^3)I_{L2}]$, $b_0 = (2\text{-}2D+D^2)[(1\text{-}2D)V_{C2}\text{-}V_{C1}\text{-}2LI_o/R/D/C_o]$, $a_4 = L^2C_1C_2$, $a_3 = a_1 = 0$, $a_2 = LC_1(1\text{-}2D+2D^2) + LC_2(2\text{-}2D+D^2)$, $a_0 = (1\text{-}2D+2D^2)(2\text{-}2D+D^2)\text{-}(1\text{-}D)^2(1+D)^2$.

Based on the transfer function in (23), the bode diagram of the proposed converter with the parameters in Section VII-A is plotted in Fig. 7. From this figure, it can be observed that the slope inclination is about −20dB/dec on the crossing frequency, which indicates that the stability of this open-loop system can be guaranteed. In order to realize stable operation under input voltage or load changes, the voltage loop control strategy with a PI controller is used, as shown in Fig. 8.

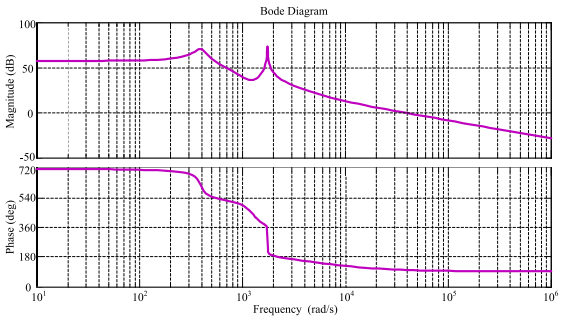


FIGURE 7. Bode diagram of the control-to-capacitor voltage transfer function $G_{vd}(s)$ of the proposed converter.

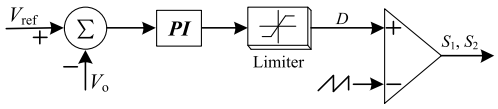


FIGURE 8. PI-voltage loop control strategy for the proposed converter.

IV. PARAMETER DESIGN GUIDELINE

Generally, the parameter design of passive/active components in a converter mainly depends on their rated voltage and rated current. Hence, the voltage and current stress of each element are deduced at first in this section.

A. VOLTAGE STRESSES ON SWITCHES AND DIODES

As shown in Fig. 4(b), switch S_1 and S_2 are all turned off, the voltage stress across S_1, S_2 are derived as

$$\begin{cases} V_{S1} = V_{C1} = \dfrac{D}{1-3D+D^2}V_{dc} \\ V_{S2} = V_{C3} = \dfrac{1-D}{1-3D+D^2}V_{dc} \end{cases} \tag{24}$$

Similarly, from Fig. 4(a) and (b), the diode voltage stress of $D_{1\text{-}3}$ and D_o are

$$\begin{cases} V_{D1} = V_{C1} + V_{C2} = \dfrac{V_{dc}}{1-3D+D^2} \\ V_{D2} = V_{D3} = V_{Do} = \dfrac{1-D}{1-3D+D^2}V_{dc} \end{cases} \tag{25}$$

B. CURRENT STRESSES ON SWITCHES AND DIODES

When S_1 and S_2 are all turned on, as shown in Fig. 4(a), the peak current across S_1 is equal to the current flow through inductor L_2. By applying kirchhoff's current law (KCL),

the current stress through S_1 and S_2 are

$$\begin{cases} i_{S1} = I_{L2} = \dfrac{I_{L1}}{1-D} = \dfrac{P_o}{(1-D)\,V_{dc}} \\ i_{S2} = \dfrac{1+D-D^2}{2D\,(1-D)} I_{L1} = \dfrac{\left(1+D-D^2\right) P_o}{2D\,(1-D)\,V_{dc}} \end{cases} \tag{26}$$

In mode 2, as shown in Fig. 4(b), diode D_1, D_2 and D_3 are all forward-biased, the peak current through D_1, D_2, D_3 can be expressed as

$$\begin{cases} i_{D1} = I_{L2} = \dfrac{P_o}{(1-D)\,V_{dc}} \\ i_{D2} = \dfrac{\left(1-D+D^2\right) P_o}{2\,(1-D)^2\,V_{dc}} i_{D3} = \dfrac{\left(1-3D+D^2\right) P_o}{2\,(1-D)^2\,V_{dc}} \end{cases} \tag{27}$$

The current stress flow through diode D_o can be derived as

$$i_{Do} = \frac{\left(1-3D+D^2\right) P_o}{2D\,(1-D)\,V_{dc}} \tag{28}$$

C. PARAMETER DESIGN OF INDUCTORS

As shown in Fig. 4(a), S_1 and S_2 are all at ON state in mode 1, inductor L_1 is charged by V_{dc} and C_1, inductor L_2 is charged by C_2. The corresponding inductor current ripple di_L can be expressed as, $di_L = x_L\%I_L$, where $x_L\%$ is the permitted fluctuation range of the inductor current. Then, from (1), the inductor L_1 and L_2 can be described as

$$L_1 = \frac{(V_{dc}+V_{C1})\,DT_s}{x_L\%I_{L1}} \quad L_2 = \frac{DT_sV_{C2}}{x_L\%I_{L2}} \tag{29}$$

Substituting the expression of V_{C1}, V_{C2}, I_{L1} and I_{L2} into (29), the required inductance value of L_1 and L_2 can be calculated by

$$L_1 = L_2 = \frac{DR_L\left(1-3D+D^2\right)}{4x_L\%f_s} \tag{30}$$

where f_s is the switching frequency of switch S_1, S_2, i.e., $f_s = 1/T_s$.

D. PARAMETER DESIGN OF CAPACITORS

Based on the equivalent circuit of Fig. 4(a), by applying kirchhoff's current law, the current flow through capacitor C_1, C_2 and C_3 can be expressed as

$$i_{C1\_on} = C_1\frac{\Delta u_{C1}}{\Delta t} = -I_{L1}$$

$$i_{C2\_on} = -I_{L2} - \frac{\left(1-3D+D^2\right) I_{L1}}{2D\,(1-D)} \tag{31}$$

$$i_{C3\_on} = C_3\frac{\Delta u_{C3}}{\Delta t} = -\frac{\left(1-3D+D^2\right) I_{L1}}{2D\,(1-D)} \tag{32}$$

where the capacitor voltage ripple $\Delta u_C = x_C\%V_C$, and $x_C\%$ is the permitted fluctuation range of the capacitor voltage, $\Delta t = DT_s$. Substituting the inductor current expression into (31) and (32), the required capacitances of C_1, C_2 and C_3 for the proposed converter can be calculated by

$$\begin{cases} C_1 = \dfrac{4\,(1-D)^2}{\left(1-3D+D^2\right) R_Lx_C\%f_s} \\ C_2 = \dfrac{2\left(1-D+D^2\right)}{\left(1-3D+D^2\right) R_Lx_C\%f_s} C_3 = \dfrac{2}{R_Lx_C\%f_s} \end{cases} \tag{33}$$

As shown in Fig. 4(b), when S_1, S_2 are turned off, diode D_o is reverse-biased, the current flow through capacitor C_o is equal to the load current I_o, then

$$i_{Co\_off} = C_o\frac{\Delta u_{Co}}{(1-D)\,T_s} = -\frac{V_o}{R_L} \tag{34}$$

where $\Delta u_{Co} = x_C\%V_o$. Therefore, from (34), the capacitance of the output capacitor C_o can be derived as follows,

$$C_o = \frac{1-D}{R_Lx_C\%f_s} \tag{35}$$

E. PARAMETER DESIGN OF SWITCHES AND DIODES

Normally, the parameter selection of power switches and diodes are based on their current and voltage stress, respectively, as tabulated in Table 1.

TABLE 1. Voltage and current stress of the proposed converter.

Parameter	Voltage Stress	Parameter	Current Stress
C_1	$\frac{D}{1-3D+D^2}V_{dc}$	L_1	$\frac{2\ 1-D}{1-3D+D^2}I_o$
C_2	$\frac{1-D}{1-3D+D^2}V_{dc}$	L_2	$\frac{2}{1-3D+D^2}I_o$
C_3	$\frac{1-D}{1-3D+D^2}V_{dc}$	D_1	$\frac{2}{1-3D+D^2}I_o$
D_2, D_3	$\frac{1-D}{1-3D+D^2}V_{dc}$	D_2	$\frac{1-D+D^2}{2\ 1-D\ ^2}I_{L1}$
D_1	$\frac{1}{1-3D+D^2}V_{dc}$	D_3	$\frac{1-3D+D^2}{2\ 1-D\ ^2}I_{L1}$
D_o	$\frac{1-D}{1-3D+D^2}V_{dc}$	D_o	$\frac{1}{D}I_o$
S_1	$\frac{D}{1-3D+D^2}V_{dc}$	S_1	$\frac{2}{1-3D+D^2}I_o$
S_2	$\frac{1-D}{1-3D+D^2}V_{dc}$	S_2	$\frac{1+D-D^2}{2D\ 1-D\ ^2}I_{L1}$

V. PERFORMANCE COMPARISON WITH OTHER NON-ISOLATED HIGH STEP-UP DC-DC CONVERTERS

A. COMPARIOSN OF NUMBER OF COMPONENTS

Table 2 shows the comparison of number of passive and active components used in these high boost converters. From this table, it can be found that the proposed converter has two less inductors than 3-Z-Boost converter [16] and SH-SLC [17], one less inductor than the SL-qZSC [26], HQZSC [27] and the converter in [20]. In addition, it has less number of capacitors than the DIESC-converter [19], HQZSC [27] and converter in [20], but a little more than the SH-SLC, 3-Z-Boost and SL-qZSC. Besides, the proposed topology has the minimum number of diodes used in power circuit.

TABLE 2. Comparison of voltage and current stresses for these non-isolated high boost converters.

	SL-qZSC[26]	DIESC-SC Converter[19]	Converter in [20]	3-Z-Boost[16]	SH-SLC[17]	HQZSC[27]	Proposed Converter
Inductor	3	2	3	4	4	3	2
Capacitor	3	5	6	2	1	7	4
Diode	5	4	5	9	7	5	4
Switch	1	1	2	1	2	1	2
Voltage Gain(G)	$\frac{1+D}{1-2D-D^2}$	$\frac{2+D}{1-D}$	$\frac{2+D}{1-D^2}$	$\left(\frac{1+D}{1-D}\right)^2$	$\frac{1+3D}{1-D}$	$\frac{2+D}{1-2D}$	$\frac{2-2D}{1-3D+D^2}$
Switch Voltage Stress	GV_{dc}	$(G+1)V_{dc}/3$	$V_{dc}/(1-D)$ $V_{dc}/(1-D)^2$	GV_{dc}	$(1+G)V_{dc}/2$	$\frac{V_{dc}}{1-2D}$	$GV_{dc}/2$ $GDV_{dc}/(2-2D)$
Switch Current Stress	$\frac{3+D}{1+D}I_{in}$	$\frac{G-1}{G}I_{in}$	I_{in} $\frac{-2-15G+2+3G\sqrt{1+12G}}{DG\ 1+6G-\sqrt{1+12G}}I_{in}$	$\frac{G+2\sqrt{G}+1}{G}I_{in}$	$\frac{G+3}{2G}I_{in}$	$\frac{1+3D\ I_{in}}{D\ 2+D}$	$I_{in}/(1-D)$ $\frac{1+D-D^2}{2D\ 1-D}I_{in}$
Voltage Stress of D_o	GV_{dc}	$(G+1)V_{dc}/3$	$V_{dc}/(1-D)^2$	GV_{dc}	$(1+G)V_{dc}$	$\frac{V_{dc}}{1-2D}$	$GV_{dc}/2$
Voltage Stress of Other Diodes	GV_{dc} $(1-D)GV_{dc}/(1+D)$ $DGV_{dc}/(1+D)$	$(G+1)V_{dc}/3$	$V_{dc}/(1-D)$ $V_{dc}/(1-D)^2$	$\sqrt{G}-1\ V_{dc}/2$ $G-\sqrt{G}\ V_{dc}/2$ $\sqrt{G}V_{dc}\ V_{dc}$ $G-\sqrt{G}\ V_{dc}$	$(G-1)V_{dc}/4$ V_{dc}	$\frac{V_{dc}}{1-2D}$	$GV_{dc}/(2-2D)$ $GV_{dc}/2$
Inductor Current Stress	I_{in} $I_{in}/(1+D)$	I_{in} I_{in}/G	I_{in}/G $-1+\sqrt{1+12G}\ I_{in}/\ 2G$ $\frac{2G+1-\sqrt{1+12G}}{2G}I_{in}$	$G+\sqrt{G}\ I_{in}/2$ $1+\sqrt{G}\ I_{in}/2$	$\frac{G+3}{4G}I_{in}$	I_{in} I_{in}/G	I_{in} $\frac{1}{1-D}I_{in}$

And the total number of the components used in this proposed circuit is less than those of the other six high step-up dc-dc converters.

B. COMPARIOSN OF OUTPUT VOLTAGE GAIN

The output voltage gain of the proposed converter is plotted in Fig. 9 and compared with those of the other six high boost topologies. The expressions of the ideal output voltage gain are shown in Table 2. From this figure, it can be seen that the proposed converter has the highest output voltage gain than those of the other high boost converters through the whole duty cycle range.

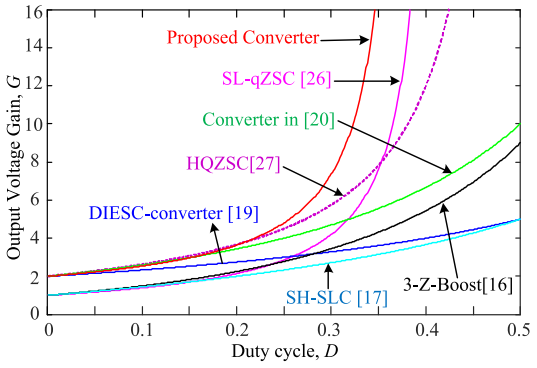
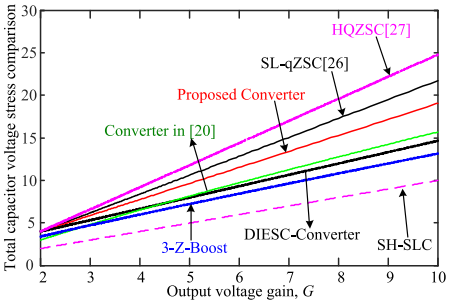


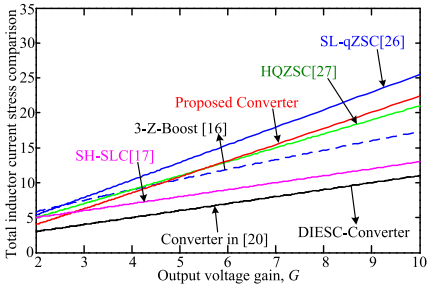
FIGURE 9. Output voltage gain comparison among these high step-up converters.

C. COMPARISON OF VOLTAGE AND CURRENT STRESSES

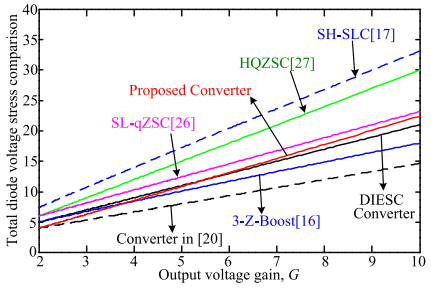
For these high boost dc-dc converter topologies, their corresponding voltage and current stresses of passive and active elements are summarized in Table 2. Based on this table, the total capacitor voltage stress is compared in Fig. 10(a), it can be found that the proposed converter has lower capacitor voltage stress than SL-qZSC and the HQZSC, but a little higher than those of the other four topologies. The total inductor current stress of the proposed method, as shown in Fig. 10(b), is lower than the SL-qZSC, but higher than that of the DIESC-converter, 3-Z-Boost converter, SH-SLC and the converter in [20]. The total diode voltage stress comparison between the proposed topology and the other converters is presented in Fig. 10(c). From Fig. 10(c), the proposed topology has lower diode voltage stress than the SH-SLC, HQZSC and SL-qZSC, but a little higher than that of the 3-Z-Boost converter and the converter in [20]. Fig. 10(d) depicts the total switching voltage stress comparison among these high boost converters. From this figure, it can be found that for obtaining the same output voltage gain G, the proposed circuit



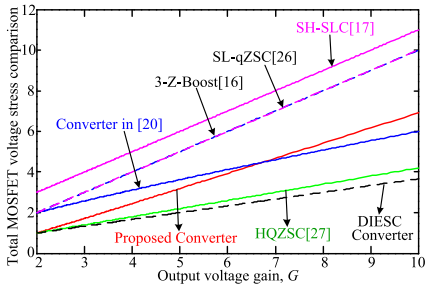
(a)



(b)



(c)



(d)

FIGURE 10. Voltage and current stress comparison among these high boost converters. (a) Total capacitor voltage stress comparison, (b) Total inductor current stress comparison, (c) Total diode voltage stress comparison, (d) Total switching voltage stress comparison.

has lower switching voltage stress than SH-SLC, SL-qZSC and the 3-Z- Boost converter, but a little higher than that of the DIESC-converter and the HQZSC [27].

VI. POWER LOSS ANALYSIS AND EFFICIENCY COMPARISON IN CCM

For the proposed converter, the total power loss consists of capacitor loss, inductor loss, diode loss and the active power switch loss, which will be calculated in detail in the following, respectively.

A. ACTIVE POWER SWITCH LOSS

The current flow through switch S_1, S_2 during ON and OFF state can be obtained from Fig. 4(a) and (b),

$$\begin{aligned} i_{S1} &= \begin{cases} I_{L2}, & (0, DT_s) \\ 0, & (DT_s, T_s) \end{cases} \\ &\Rightarrow \begin{cases} I_{S1(\mathrm{AVG})} = DI_{L2} = \dfrac{D}{1-D} I_{L1} \\ I_{S1(\mathrm{RMS})} = \sqrt{D} I_{L2} = \dfrac{\sqrt{D}}{1-D} I_{L1} \end{cases} \end{aligned} \tag{36}$$

$$\begin{aligned} i_{S2} &= \begin{cases} \dfrac{1+D-D^2}{2D(1-D)} I_{L1}, & (0, DT_s) \\ 0, & (DT_s, T_s) \end{cases} \\ &\Rightarrow \begin{cases} I_{S2(\mathrm{AVG})} = \dfrac{1+D-D^2}{2(1-D)} I_{L1} \\ I_{S2(\mathrm{RMS})} = \dfrac{1+D-D^2}{2\sqrt{D}(1-D)} I_{L1} \end{cases} \end{aligned} \tag{37}$$

where I_{L1} is the average current of inductor L_1, $I_{L1} = V_o \cdot V_o/R_L/V_{dc}$.

From (36)-(37), the total switching power loss and conduction power loss of S_1, S_2 can be expressed as

$$\begin{aligned} P_{switching} &= \frac{t_{on} + t_{off}}{2} f_s \left(V_{S1} i_{S1} + V_{S2} i_{S2} \right) \\ &= \frac{V_{dc} I_{L1} \left(t_{on} + t_{off} \right) f_s}{2\left(1 - 3D + D^2\right)} \cdot \left(\frac{D}{1-D} + \frac{1+D-D^2}{2D} \right) \end{aligned} \tag{38}$$

$$\begin{aligned} P_{con} &= I_{S1(\mathrm{RMS})}^2 r_{DS} + I_{S2(\mathrm{RMS})}^2 r_{DS} \\ &= \frac{4D^2 + \left(1 + D - D^2\right)^2}{4D(1-D)^2} r_{DS} I_{L1}^2 \end{aligned} \tag{39}$$

where f_s is the switching frequency, t_{on} and t_{off} are the turn-on and turn-off delay times of switch S_1 and S_2, r_{DS} is the drain-to-source resistance of these two power switches.

B. DIODE POWER LOSS

Based on the operating principle analysis in Section II, the average and RMS values of diode currents can be derived as

$$\begin{cases} I_{D1(\mathrm{AVG})} = (1-D) I_{L2} = I_{L1} \\ I_{D1(\mathrm{RMS})} = \sqrt{1-D} I_{L2} = \dfrac{\sqrt{1-D}}{1-D} I_{L1} \\ I_{D2(\mathrm{AVG})} = \dfrac{1-D+D^2}{2(1-D)} I_{L1} \\ I_{D2(\mathrm{RMS})} = \sqrt{1-D} \cdot \dfrac{1-D+D^2}{2(1-D)^2} I_{L1} \\ I_{D3(\mathrm{AVG})} = \dfrac{1-3D+D^2}{2(1-D)} I_{L1} \\ I_{D3(\mathrm{RMS})} = \sqrt{1-D} \cdot \dfrac{1-3D+D^2}{2(1-D)^2} I_{L1} \\ I_{Do(\mathrm{AVG})} = \dfrac{1-3D+D^2}{2(1-D)} I_{L1} \\ I_{Do(\mathrm{RMS})} = \sqrt{1-D} \cdot \dfrac{1-3D+D^2}{2D(1-D)} I_{L1} \end{cases} \tag{40}$$

The power loss associated with forward voltage drop V_F is

$$\begin{aligned} P_{V_F\_loss} &= I_{D1(\mathrm{AVG})}V_F + I_{D2(\mathrm{AVG})}V_F + I_{D3(\mathrm{AVG})}V_F \\ &\quad + I_{Do(\mathrm{AVG})}V_F \\ &= \frac{5 - 9D + 3D^2}{2\,(1-D)}V_F I_{L1} \end{aligned} \tag{41}$$

The diodes' ohmic power loss associated with the internal forward resistance r_D is

$$\begin{aligned} P_{r_D\_loss} &= I^2_{D1(\mathrm{RMS})}r_D + I^2_{D2(\mathrm{RMS})}r_D + I^2_{D3(\mathrm{RMS})}r_D \\ &\quad + I^2_{Do(\mathrm{RMS})}r_D \\ &= \left[\frac{1}{1-D} + \frac{\left(1-3D+D^2\right)^2}{4D\,(1-D)^2}\right. \\ &\quad \left. + \frac{\left(1-D+D^2\right)^2 + \left(1-3D+D^2\right)^2}{4\,(1-D)^3}\right] I^2_{L1}r_D \end{aligned} \tag{42}$$

Therefore, the total diode power loss can be expressed as

$$P_{D\_loss} = P_{V_F\_loss} + P_{r_D\_loss} \tag{43}$$

C. INDUCTOR POWER LOSS

The approximate RMS value of the inductor current i_{L1} and i_{L2} can be derived as

$$\begin{aligned} I_{L1(\mathrm{RMS})} &= \frac{V_o^2}{R_L V_{dc}} = \frac{G^2_{CCM}V_{dc}}{R_L} \\ I_{L2(\mathrm{RMS})} &= \frac{I_{L1(\mathrm{RMS})}}{1-D} = \frac{G^2_{CCM}V_{dc}}{(1-D)\,R_L} \end{aligned} \tag{44}$$

Thus, the total inductor power loss can be expressed as

$$P_{rL\_loss} = I^2_{L1(\mathrm{RMS})}r_L + I^2_{L2(\mathrm{RMS})}r_L = \frac{2 - 2D + D^2}{(1-D)^2}I^2_{L1}r_L \tag{45}$$

where r_L is internal resistance of inductors.

D. CAPACITOR POWER LOSS

From Fig. 4(a) and Fig. 4(b), the current flow through capacitor C_1, C_2, C_3 and C_o during ON and OFF states can be obtained as

$$\begin{aligned} i_{C1} &= \begin{cases} -I_{L1}, & (0, DT_s) \\ \dfrac{D}{1-D}I_{L1}, & (DT_s, T_s) \end{cases} \\ i_{C2} &= \begin{cases} -\dfrac{1-D+D^2}{2D}I_{L2}, & (0, DT_s) \\ \dfrac{1-D+D^2}{2\,(1-D)}I_{L2}, & (DT_s, T_s) \end{cases} \\ i_{C3} &= \begin{cases} -\dfrac{1-3D+D^2}{2D\,(1-D)}I_{L1}, & (0, DT_s) \\ \dfrac{1-3D+D^2}{2\,(1-D)^2}I_{L1}, & (DT_s, T_s) \end{cases} \end{aligned} \tag{46}$$

$$i_{Co} = \begin{cases} \dfrac{1-D}{D}\cdot\dfrac{V_o}{R_L}, & (0, DT_s) \\ -\dfrac{V_o}{R_L}, & (DT_s, T_s) \end{cases} \tag{47}$$

Based on (46) and (47), the approximate RMS value of capacitor currents can be derived as

$$\begin{aligned} I_{C1(\mathrm{RMS})} &= \sqrt{\frac{D}{1-D}}I_{L1} \\ I_{C2(\mathrm{RMS})} &= \frac{1-D+D^2}{2\sqrt{D\,(1-D)}}I_{L2} \\ I_{Co(\mathrm{RMS})} &= \sqrt{\frac{1-D}{D}}\frac{V_o}{R_L} \end{aligned} \tag{48}$$

$$I_{C3(\mathrm{RMS})} = \frac{1-3D+D^2}{2\,(1-D)\sqrt{D\,(1-D)}}I_{L1} \tag{49}$$

Denoting the capacitor's equivalent series resistance (ESR) is r_C. Then, the total capacitor conduction power loss is

$$\begin{aligned} P_{r_C\_loss} &= I^2_{C1(\mathrm{RMS})}r_C + I^2_{C2(\mathrm{RMS})}r_C + I^2_{C3(\mathrm{RMS})}r_C \\ &\quad + I^2_{Co(\mathrm{RMS})}r_C \\ &= \left[\frac{D}{1-D} + \frac{1-D}{DG^2_{CCM}}\right. \\ &\quad \left. + \frac{\left(1-D+D^2\right)^2 + \left(1-3D+D^2\right)^2}{4D\,(1-D)^3}\right] I^2_{L1}r_C \end{aligned} \tag{50}$$

where G_{CCM} is the output voltage gain of the proposed converter in CCM.

Based on (38), (39), (43), (45), (50) and the internal parasitic parameters in Table 3, the power loss calculation results for these high step-up dc-dc converters are depicted and compared in Fig. 11. From Fig. 11(a), it can be found that the inductor power loss of the proposed converter is lower than that of the SL-qZSC, HQZSC [27] and the 3-Z-Boost converter, but a little higher than that of the SH-SLC, DIESC-converter and the converter in [20]. Fig. 11(b) shows the capacitor power loss comparison. From this figure, it can be seen that the proposed topology has lower capacitor loss than the SL-qZSC and the HQZSC [27], but higher than that of the SH-SLC, 3-Z-Boost, DIESC-converter and the converter in [20]. The diode and MOSFET power loss comparison results are shown in Fig. 11(c) and Fig. 11(d), respectively. From Fig. 11(c), the proposed topology has a lower diode loss than the SL-qZSC, HQZSC and the converter in [20], but higher than that of the SH-SLC, 3-Z-Boost and the converter in [20]. It can be seen that from Fig. 11(d), the proposed method has a lower MOSFTE loss than the SL-qZSC, HQZSC and the 3-Z-Boost converter, but a little higher than the DIESC, SH-SLC and the converter in [20]. Fig. 11(e) shows the power loss distribution percentage of the proposed converter, it can be found that for obtaining higher output voltage gain G, the major power losses come from inductors, MOSFETs and capacitors. Therefore, based on the above power loss analysis (29)–(43) and Table 3,

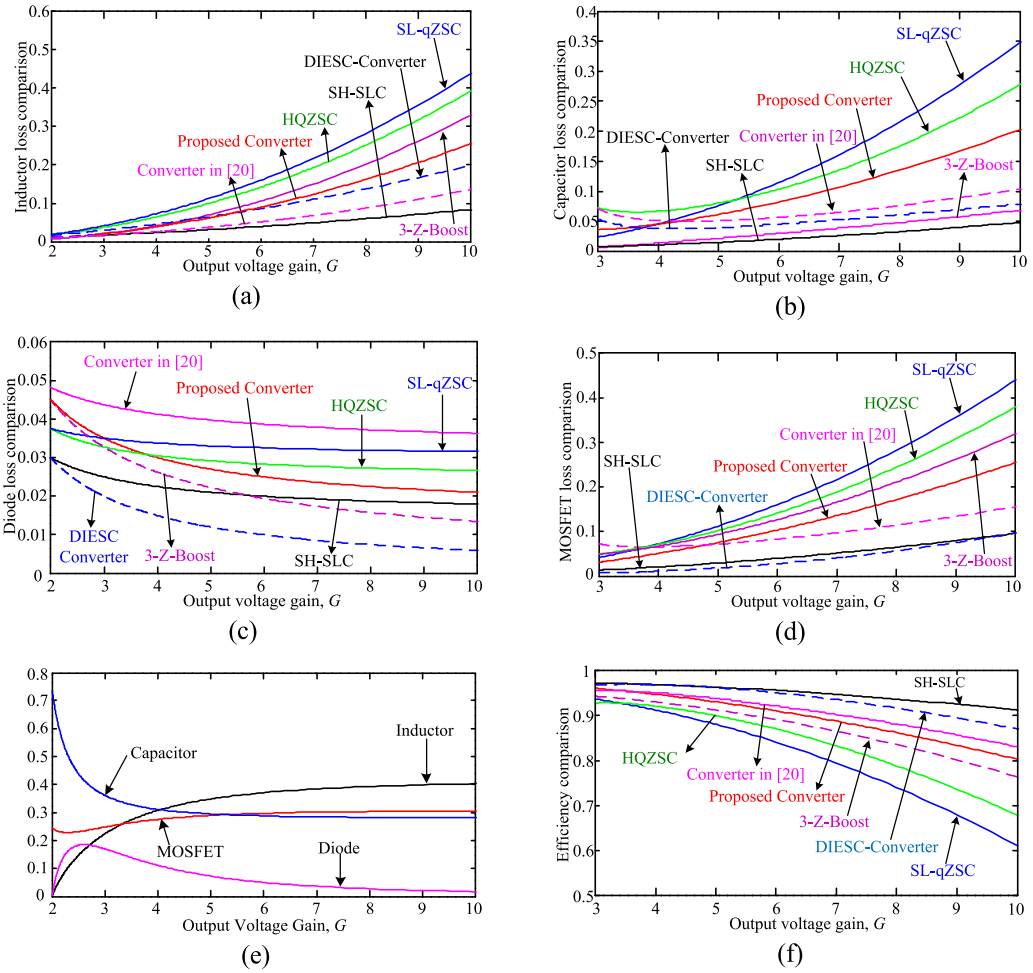


FIGURE 11. Power loss analysis and efficiency comparison. (a) Inductor loss comparison. (b) Capacitor loss comparison. (c) Diode power loss comparison. (d) MOSFET power loss comparison. (e) Loss distribution percentage of the proposed converter. (f) Efficiency comparison.

the calculated efficiencies for these high step-up converters are compared and plotted in Fig. 11(f). From this figure, it can be found that the proposed converter has a higher efficiency than that of the SL-qZSC, HQZSC and 3-Z-Boost converter, but lower than those of the other three topologies (SH-SLC, DIESC [19] and the converter in [20]).

VII. SIMULATION AND EXPERIMENTAL VERIFICATIONS

A. SIMULATION RESULTS

To verify the properties of the proposed active quasi-switched dc-dc converter, a Matlab/Simulink simulation was performed with the following parameters: input voltage $V_{\rm dc}$ = 20V, $L_1 = L_2 = 220$uH, $C_1 = C_2 = C_3 = 100\mu$F, output filter capacitor $C_{\rm o} = 220\mu$F. The switching frequency is $f_s = 30$ kHz, duty cycle $D = 0.28$ and load resistance $R_L = 50\Omega$.

Fig. 12 show the simulation results for the proposed converter when $V_{\rm dc} = 20$V, $D = 0.28$. From Fig. 12(a), it can be seen that the inductor currents (i_{L1} and i_{L2}) are increased and decreased linearly during ON and OFF states, respectively.

TABLE 3. Parasitic parameters for power loss analysis.

Parameters	Values
Parasitic resistance of inductors (L_1, L_2)	0.12Ω
Core of inductors	KS300125A(142nH/N^2)
ESR of capacitors (C_1, C_2, C_3, $C_{\rm o}$)	100mΩ
Diodes (MBR30200F)	200V, 30A, $V_{F(\max)}$=0.9V
MOSFET S_7 (FQA90N15)	150V, 90A, $r_{DS(\max)}$=0.018Ω

And the converter operates in continuous conduction mode (CCM). Capacitor voltages V_{C1}, $V_{C2}(= V_{C3})$ are pumped up to 23.4V and 60.4V, respectively. And the output voltage $V_{\rm o}$ is boosted to 120.8V, which is the total of the capacitor voltages V_{C2} and V_{C3}. These are in good agreement with the calculated values from (4). From Fig. 12(b), the switching voltage stress of S_1 and S_2 are 23.4V and 60.4V, the simulated diode voltage stress are $V_{D1} = 83.8$V, $V_{D2} = V_{D3} = V_{\rm Do} = 60.4$V, which are coincident with the theoretical calculated values

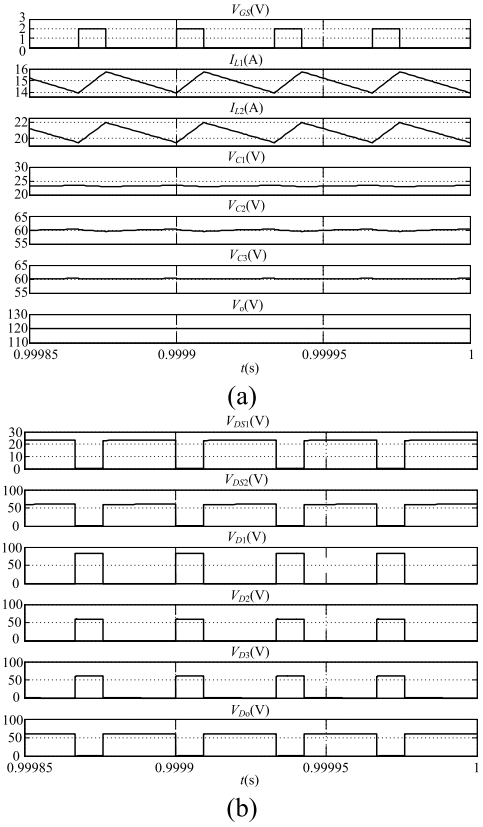


FIGURE 12. Simulation results of the proposed converter when $V_{dc} = 20V$, $D = 0.28$. From top to bottom: (a) gate-source driving voltage V_{GS}, inductor current-i_{L1}-i_{L2}, capacitor voltage-V_{C1}-V_{C2}-V_{C3}, output voltage-V_o; (b) drain-source voltage of S_1, S_2, diode voltages-V_{D1}-V_{D2}-V_{D3}-V_{Do}.

from (17)-(18). Therefore, it can be concluded that the above simulation results are fit well with the theoretical analysis.

B. EXPERIMENTAL RESULTS

To verify the above steady-state analysis and simulation results, experimental test was performed for the proposed topology. The circuit components' values and types used in the prototype are same as the aforementioned simulation parameters. The two MOSFETs are FQA90N15 (150V, 90A, $r_{DS(\max)} = 0.018\Omega$), and the four power diodes are MBR30200F (200V, 30A, $V_{F(max)} = 0.9V$). All the power MOSFETS are driven by the 2BB0108T basic board with driver 2SC0108T.

Fig. 13 shows the measured experimental results for the proposed converter when $V_{dc} = 20V, D = 0.28$. In Fig. 13(a), from top to bottom, the waveforms are the gate-source voltage V_{GS}, inductor currents (i_{L1}, i_{L2}) and output voltage V_o. From this figure, it can be observed that input current is continuous, when switch S_1 and S_2 are turned ON, the inductor currents are increased. Otherwise, the inductor currents are decreased. The measured output voltage V_o is about 110V, which is slightly lower than the calculated value due to the nonidealities of components. The experimental capacitor voltages are

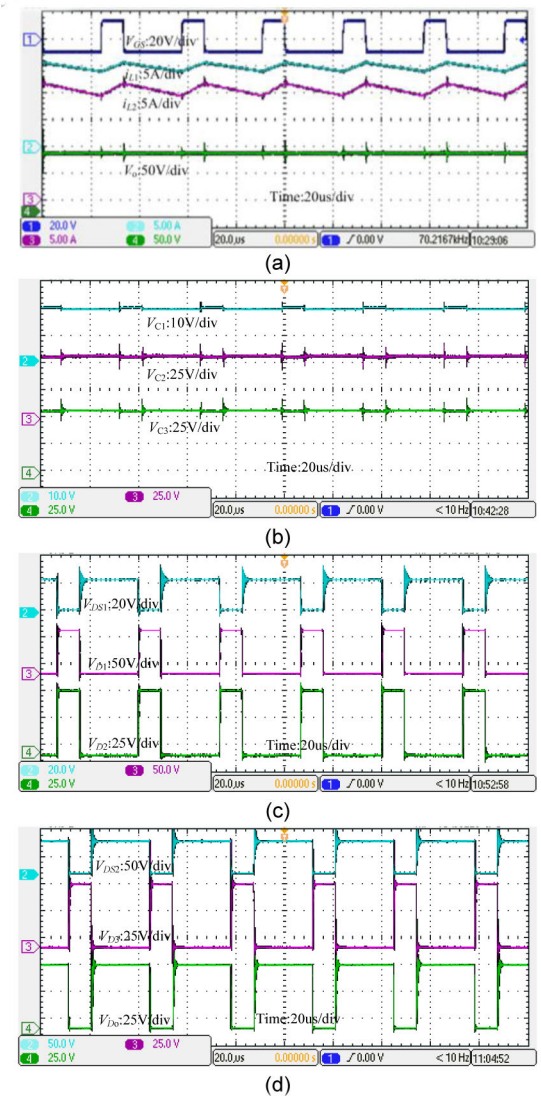


FIGURE 13. Experimental results of the proposed converter when Vdc = 20V, D = 0.28. From top to bottom: (a) gate-source voltage V_{GS} of S_1, S_2, inductor currents (i_{L1}, i_{L2}) and output voltage V_o; (b) Capacitor voltages V_{C1}, V_{C2} and V_{C3}; (c) Switching voltage stress V_{DS1} and diode voltage (V_{D1}, V_{D2}); (d) Switching voltage V_{DS2} and diode voltage stress (V_{D3}, V_{Do}).

measured and shown in Fig. 13(b). It can be observed that the voltage of capacitor C_1 (V_{C1}), C_2 and C_3 ($V_{C2} = V_{C3}$) are boosted to 20V and 55V, respectively, which are a little lower than the theoretical value due to the parasitic parameters of passive and active elements. Fig.13(c) and (d) presents the measured experimental switching voltage stress waveforms of S_1, S_2 and diodes D_1, D_2, D_3 and D_o. It can be seen that when S_1, S_2 are turned on, diode D_1, D_2 and D_3 are reverse biased. The voltage stress of diode D_1 is about 80V, while for diode D_2, D_3 and D_o, the voltage stress is about 60V, which are much smaller than the output voltage. When S_1 and S_2 are turned off, the measured switching voltage stress is about 23V and 60V, respectively, which are lower than the above diode voltage stress. Therefore, the switches and diodes with

low voltage rating can be used to decrease the size and loss of the converter. In addition to the voltage stress waveforms of diodes and switches, the experimental results of diode current stresses and switching current stresses are presented in Fig.14. From this figure, when switch S_1, S_2 are ON, diodes D_1, D_2, D_3 are reverse blocking, D_o is forward biased. And the measured current stresses are all in good agreement with theoretical analysis.

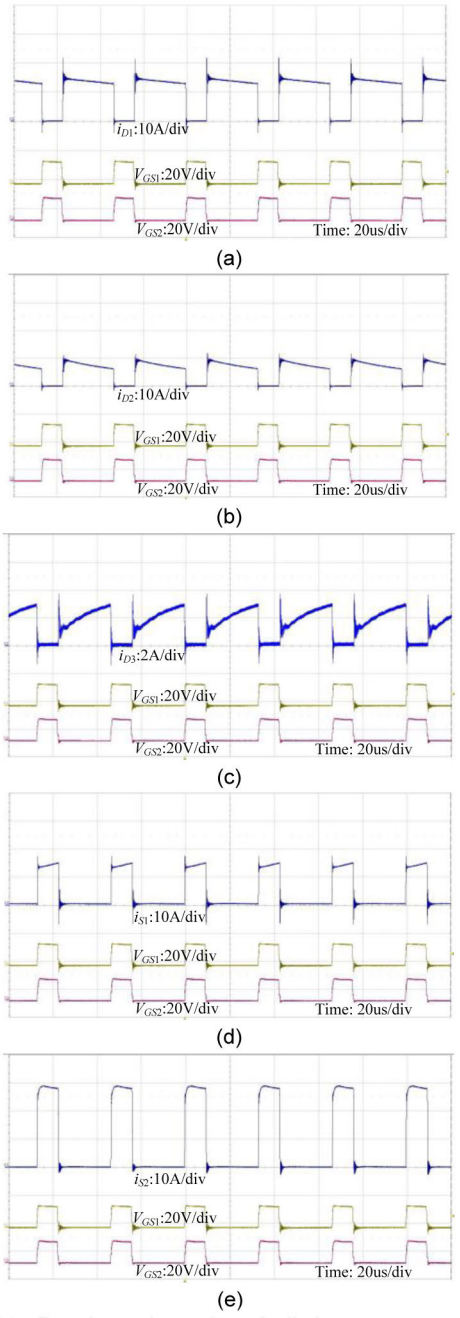


FIGURE 14. Experimental results of diode current stresses and switching current stresses when $V_{dc} = 20V$, $D = 0.28$. (a) Diode current stress i_{D1}; (b) Diode current stress i_{D2}; (c) Diode current stress i_{D3}; (d) Switching current stress i_{S1}; (e) Switching current stress i_{S2}.

The theoretical and experimental output voltage gain of the proposed circuit is plotted and compared in Fig. 15. From this figure, it can be found that the experimental results are lower than that of the theoretical values because the parasitic effects of the components are neglected in theoretical calculation, while these cannot be ignored in practical applications. Moreover, the difference between the theoretical values and the experimental results are increased when the operating duty cycle D is increasing. This is due to the fact that the conduction losses of active/passive components will be high when the shoot-through time interval is large.

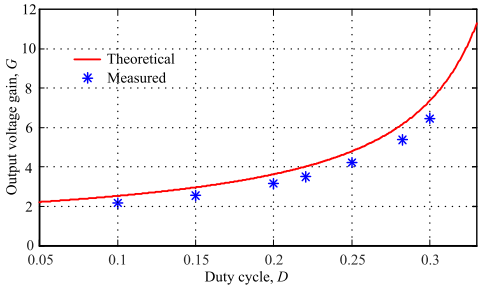


FIGURE 15. Output voltage gain comparison between theoretical and experimental values.

The experimental efficiency of the proposed converter in CCM mode is measured and plotted in Fig. 16, with different output power under $V_{dc} = 20V$ and $V_{dc} = 12V$. From this figure, it can be seen that the maximum measured efficiency is 92.6%, and the efficiency is higher with the increase of input voltage, this is owing to the low conduction loss when small duty ratio can be utilized with higher input, which is helpful to improve the system efficiency.

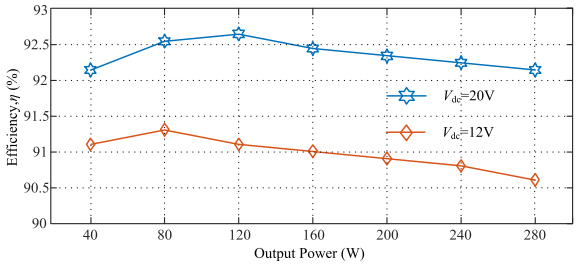


FIGURE 16. Measured converter efficiency versus different output powers.

In CCM mode, based on the loss-related parameters in Table 3 and the power loss analysis in Section IV. The detailed loss distribution analysis in devices under the rated operating condition when $V_{dc} = 20V$, $D = 0.28$ has been depicted in Fig. 17. From this figure, it can be observed that the total power loss is about 19.4W, and the major losses come from inductors, MOSFETs and capacitors, and their corresponding loss distribution percentage are 36.2%, 29.8% and 25.7%, respectively.

According to the DCM circuit analysis in Section II-B, when $K = 2L/R_L T_s < 0.022$, the proposed converter

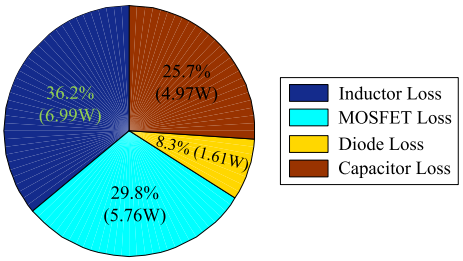


FIGURE 17. Calculated power loss distribution in devices under the rated operating condition of $V_{dc} = 20V$, $D = 0.28$.

operates in DCM mode. Under the operating condition of $R_L = 50\Omega$ and $f_s = 30$kHz, the inductance of L_1 and L_2 should satisfy $L_1 = L_2 = L < 18.3$uH. Therefore, we choose $L_1 = L_2 = 15$uH, $V_{dc} = 20$V, $f_s = 30$kHz, $R_L = 50\Omega$ and $D = 0.28$ to implement the DCM verification. And Fig. 18 shows the corresponding DCM experimental results. From Fig. 18(a), one can find that the inductor current reduces to zero during one switching cycle, and the converter operates in discontinuous conduction mode. Fig. 18(b)-(f) shows the diode current stresses and the switching current stresses, respectively. The experimental results of capacitor voltages and output voltage under DCM condition are presented in Fig. 18(g)-(h), which shows a good agreement with the-oretical analysis.

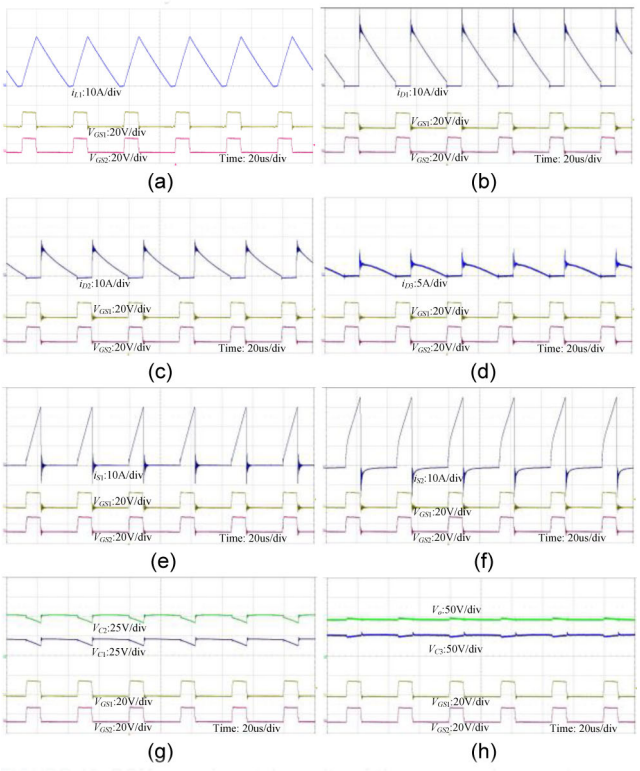


FIGURE 18. DCM experimental results of the proposed converter when $L_1 = L_2 = 15$uH, $V_{dc} = 20$V, $f_s = 30$kHz, $R_L = 50\Omega$ and $D = 0.28$. (a) Inductor current stress i_{L1}; (b) Diode current stress i_{D1}; (c) Diode current stress i_{D2}; (d) Diode current stress i_{D3}; (e) Switching current stress i_{S1}; (f) Switching current stress i_{S2}; (g) Capacitor voltage V_{C1} and V_{C2}; (h) Capacitor voltage V_{C3} and output voltage V_o.

Based on the small-signal dynamic analysis in Section III, a PI controller, $G_c(s) = 0.001 + 0.038/s$, is designed and utilized in the voltage loop control strategy of Fig. 8, which aims to evaluate the dynamic response performance of the proposed converter. The close-loop dynamic experimental results of the output voltage V_o and output current i_o under the load transient variation between full load and half load are measured and shown in Fig. 19. It can be seen that with the proper design of the PI controller, the output voltage of the proposed converter is stable and insensitive to the load step change.

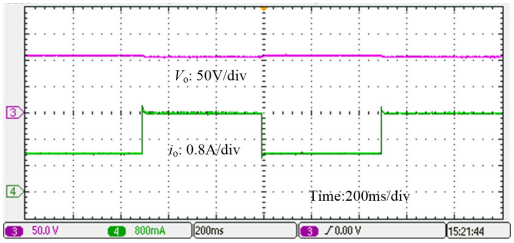


FIGURE 19. Experimental dynamic response with the load transient variation between full load and half load.

Besides, the dynamic response of the proposed converter when the input voltage varies from 20V to 30V have been presented in Fig. 20. Fig. 20(a) and Fig. 20(b) shows the simulation and experimental results, respectively. From top to bottom, the presented waveforms are the output current i_o, the input voltage V_{dc} and the output voltage V_o. From this figure, one can find that when the input voltage changes from 20V to 30V, the output voltage and output current have the overshoot and keep stable fast at 110V and 2.2A, respectively.

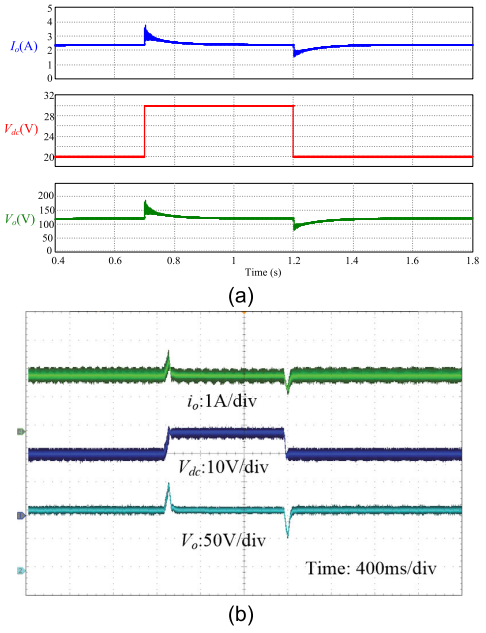


FIGURE 20. Dynamic response when the input voltage varies from 20V to 30V. (a) Simulation results; (b) Experimental results.

Comparing Fig. 20(a) and 20(b), it can be observed that the experimental dynamic performance results with the input voltage variation are fit well with the simulation results.

VIII. CONCLUSION

A hybrid non-isolated active quasi-switched dc-dc converter is proposed in this paper for high step-up voltage conversion applications. The features of the proposed topology are as follows: continuous input current, high output voltage gain with a small duty ratio for the reduction of conduction power loss, simple structure and easy to control. The voltage stress on diodes and MOSFETs are low, which is beneficial to the system efficiency and cost. The operating principle, CCM and DCM circuit analysis have been discussed in detail, and the small-signal dynamic analysis is also presented. In addition, a comprehensive performance comparison between the proposed topology and other non-isolated high step-up dc–dc converters are addressed. Finally, corresponding experimental results have been given to verify the analysis and merits of the converter. Thence, it would be suitable for the low power high step-up applications, such as TV-CRTs, medical X-ray equipment systems, battery-powered LED lighting systems and automobile high-intensity discharge headlamps, where dc/dc converter with high voltage conversion ratio is also required.

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