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Electrical Performance and Stability Improvement of p-Channel SnO Thin-Film Transistors Using Atomic-Layer-Deposited Al_2O_3 Capping Layer

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ABSTRACT The incorporation of an atomic-layer-deposited Al_2O_3 capping layer was proposed as an effective method to enhance the electrical performance and stability of p-channel SnO thin-film transistors (TFTs). The SnO TFT with the Al_2O_3 capping layer demonstrated better electrical characteristics, such as higher field-effect mobility ($\mu_{FE} = 1.7$ cm^2/V·s), smaller subthreshold swing ($SS = 2.9$ V/dec), and larger current on/off ratio ($I_{ON/OFF} = 1.6 \times 10^4$), than the pristine SnO TFT ($\mu_{FE} = 1.5$ cm^2/V·s, $SS = 3.8$ V/dec, and $I_{ON/OFF} = 6.9 \times 10^2$). Furthermore, the Al_2O_3-capped SnO TFT exhibited significantly enhanced electrical stability under an applied negative-gate-bias stress compared to the pristine device. The observed phenomena were mainly attributed to the decreased number of oxygen-vacancy-induced hole trap states within the SnO owing to diffused hydrogen from the atomic-layer-deposited Al_2O_3 layer. Our experimental results thus demonstrate that incorporating the atomic-layer-deposited Al_2O_3 capping layer is a simple and effective method for improving the electrical characteristics of p-channel SnO TFTs.

INDEX TERMS P-channel SnO TFTs, Al_2O_3 capping layer, atomic layer deposition (ALD), oxygen vacancy, hydrogen.

I. INTRODUCTION

Since the first report on indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFTs) by Nomura *et al.* in 2004, oxide TFTs have progressed rapidly and are being widely used to fabricate the backplanes of large-area flat-panel displays [1]. However, most of the available research on oxide TFTs were conducted on n-channel devices, such as the IGZO TFTs, which has prevented the implementation of complementary logic circuits composed of both n- and p-channel oxide TFTs [2]–[8]. Complementary logic circuits have advantages over electronic circuits composed of only n-channel transistors, in terms of density of integration and power consumption [9]–[11]. Therefore, development of high-performance p-channel oxide TFTs can expand the application of oxide TFTs beyond flat-panel displays. Until now, several kinds of p-type oxide semiconductors have been studied as the channel materials for p-channel oxide TFTs [12]–[16]. Among them, SnO is considered as one of the most promising channel materials for p-channel oxide TFTs. Although SnO has the narrow process window [17], it has the potential for high hole mobilities stemming from the hybridization of the pseudo-closed Sn 5s and O 2p orbitals in the valence band [18], [19]. However, numerous subgap states inside the SnO thin film have hindered the fabrication of high-performance p-channel TFTs using SnO as the channel material [20]–[23].

Metal or metal-oxide-based capping layers have been frequently used to enhance the electrical performances and stabilities of n-channel oxide TFTs [24]–[27]. However, there have been very few studies on the effects of capping layers on the electrical properties of p-channel oxide TFTs. Very recently, our group reported that the Ni or Pt capping layer can increase the field-effect mobility (μ_{FE}) of the p-channel SnO TFTs [28], [29]. However, except for the μ_{FE}, other electrical properties such as the subthreshold swing (SS), threshold voltage (V_{TH}), current on/off ratio ($I_{ON/OFF}$) of the SnO TFTs did not change significantly or were rather deteriorated after forming the Ni or Pt capping layer. In the

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present work, we show that the formation of an atomic-layer-deposited Al_2O_3 capping layer can significantly improve the electrical performance and stability of p-channel SnO TFTs for the first time. A systematic study was conducted to understand the physical mechanism responsible for the observed phenomenon, and defect termination by the diffused hydrogen in the SnO channel layer from the Al_2O_3 capping layer is suggested as the cause of this behavior.

II. EXPERIMENTS

A. DEVICE FABRICATION METHODS

Experiments were performed using the bottom-gate top-source/drain electrode TFTs, where an n^+-Si wafer was employed as the substrate and gate electrode. A 40-nm-thick layer of thermal SiO_2 grown by the dry oxidation process was used as the gate dielectric, and a 14-nm-thick SnO_X thin film was formed on the SiO_2/n^+-Si substrate using a radio frequency (RF) magnetron sputter with a metallic Sn target (3-inch-diameter, 99.999% purity). The sputtering conditions are as follows: RF power of 70 W, deposition pressure of 3 mTorr, Ar/O_2 ratio of 90/4 (sccm/sccm), and substrate at room temperature (RT). The deposition condition of the thin film was carefully selected because Sn and SnO_2 are more stable phases than SnO [17]. In addition, we considered that the percentage of metallic Sn in the thin film increases as the RF power increases [30]. The as-deposited SnO_X thin films on the SiO_2/n^+-Si substrate were thermally annealed in air for 30 min at 180 °C. After the post-deposition annealing process, the source/drain electrodes were formed with 60-nm-thick indium-tin-oxide (ITO) using a direct current (DC) magnetron sputter. The channel and electrodes were patterned using the photolithography and lift-off processes. The fabricated TFTs were then divided into three groups. The TFTs in the first group were capped with 75-nm-thick Al_2O_3 thin films. These films were applied by the atomic layer deposition (ALD) method at 200 °C for 10 h using trimethylaluminum (TMA, $Al(CH_3)_3$) and water (H_2O) as precursors. The TFTs in the second group were annealed at 200 °C for 10 h in a vacuum environment to ensure that they were exposed to the same thermal budget as those in the first group. The TFTs in the third group were not subjected to any further treatment. Finally, all TFTs were passivated by a 2-μm-thick layer of SU-8 using the procedure described in our previous work [31]. Fig. 1(a) shows the schematic of the fabricated Al_2O_3-capped TFT.

B. DEVICE CHARACTERIZATION METHODS

The structural properties and chemical compositions of the SnO_X thin films were examined using X-ray diffraction (XRD, Dmax2500/PC, RIGAKU) and X-ray photoelectron spectroscopy (XPS, PHI 5000 Versa Probe, ULVAC-PHI). Time-of-flight secondary ion mass spectrometry (TOF-SIMS, TOF-SIMS5, ION-TOF GmbH) was used to determine the amount of hydrogen in the Al_2O_3 and SnO_X thin films. The electrical characteristics of the TFTs were measured using a semiconductor parameter analyzer

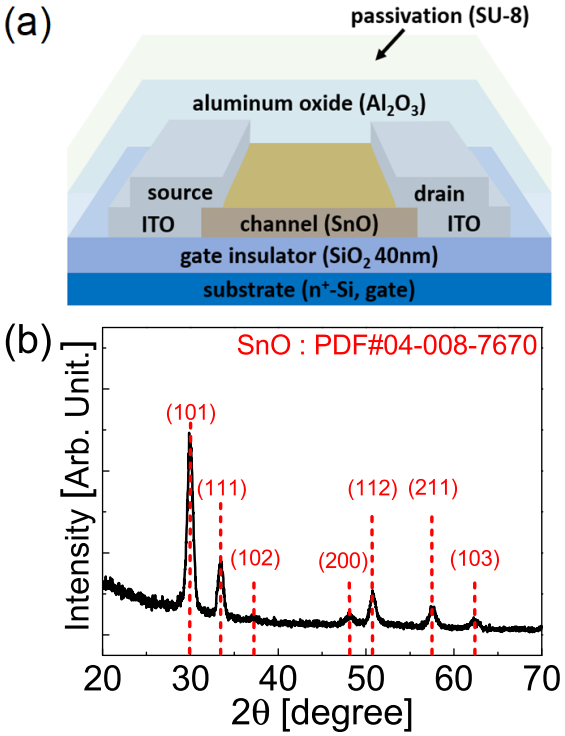

FIGURE 1. (a) Schematic view of the fabricated Al_2O_3-capped SnO TFT; (b) XRD patterns of the SnO_X thin film formed on the SiO_2/n^+-Si substrate.

(4156C, Agilent) at RT in the dark in a vacuum environment to avoid the effects of ambient conditions on the characteristics of the SnO TFTs.

III. RESULTS AND DISCUSSION

Fig. 1(b) displays the XRD patterns of the 14-nm-thick SnO_X thin film formed on the SiO_2/n^+-Si substrate. Clear diffraction peaks are observed in the XRD spectrum, which indicates that the deposited SnO_X thin film has a polycrystalline phase. The XRD peaks in Fig. 1(b) correspond to the (002), (101), (103), (110), (112), (200), and (211) planes of the SnO phase (powder diffraction file (PDF) card number 04-008-7670) [32], implying that the SnO is the dominant phase in the deposited SnO_X thin film. The crystallite size was calculated to 11.6 nm from the peak (101) of the XRD spectra based on the Debye-Scherrer equation.

Figs. 2(a) and (b) depict the representative transfer curves of the pristine, additionally vacuum-annealed, and Al_2O_3-capped SnO TFTs (width/length $(W/L) = 500\ \mu m/500\ \mu m$) on the semi-logarithmic and linear scales, respectively, where V_{GS}, V_{DS}, and I_D are the gate-to-source voltage, drain-to-source voltage, and drain current, respectively. Measurements were obtained by scanning for V_{GS} in the range of 15 to −20 V at $V_{DS} = -1$ V for all TFTs. In this work, μ_{FE} was determined from the maximum transconductance at a V_{DS} of −1 V using the following equation:

$$\mu_{FE} = \frac{Lg_m}{WC_iV_{DS}} \quad (1)$$

TABLE 1. Electrical Parameters Extracted From the Pristine, Vacuum-Annealed, and Al_2O_3-Capped SnO TFTs. Electrical Characterization was Conducted for 5 Devices per Each Type of TFT.

	parameter	sample 1	sample 2	sample 3	sample 4	sample 5	average
pristine TFT	μ_{FE} (cm^2/V·s)	1.5	1.5	1.5	1.5	1.5	1.5
	V_{TH} (V)	6.4	6.8	6.2	6.7	6.4	6.5
	SS (V/dec)	3.7	3.9	3.8	3.9	3.6	3.8
	$I_{ON/OFF}$	7.0×10^2	7.2×10^2	6.7×10^2	6.5×10^2	6.9×10^2	6.9×10^2
vacuum-annealed TFT	μ_{FE} (cm^2/V·s)	1.4	1.4	1.4	1.3	1.3	1.4
	V_{TH} (V)	7.2	7.4	7.1	7.5	7.5	7.3
	SS (V/dec)	3.7	3.7	3.5	3.8	3.5	3.6
	$I_{ON/OFF}$	1.1×10^3	9.5×10^2	1.2×10^3	1.2×10^3	1.0×10^3	1.1×10^3
Al_2O_3-capped TFT	μ_{FE} (cm^2/V·s)	1.7	1.7	1.6	1.7	1.7	1.7
	V_{TH} (V)	2.7	2.8	2.4	2.9	2.8	2.7
	SS (V/dec)	2.9	3.0	2.9	3.0	2.8	2.9
	$I_{ON/OFF}$	1.9×10^4	1.7×10^4	1.5×10^4	1.4×10^4	1.5×10^4	1.6×10^4

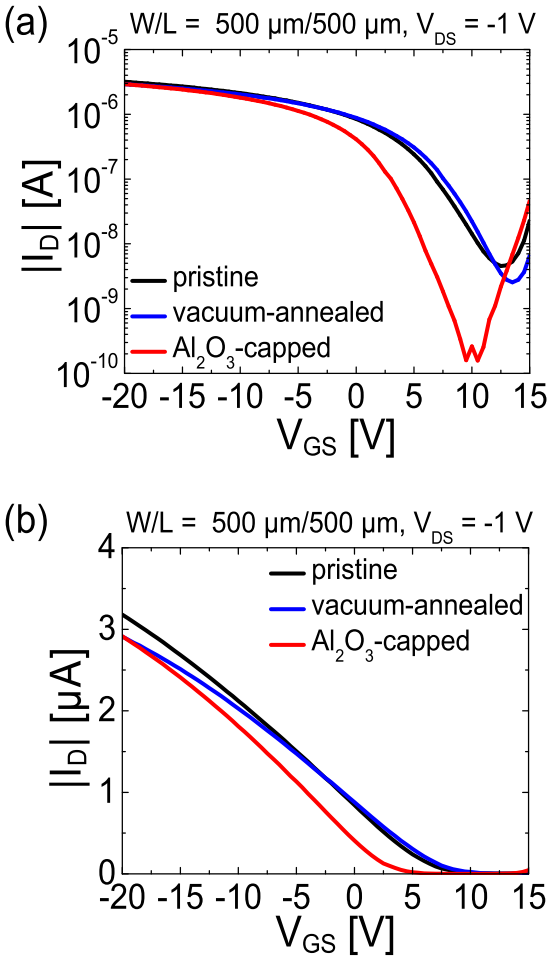

FIGURE 2. Representative transfer curves of the pristine, vacuum-annealed, and Al_2O_3-capped SnO TFTs in the (a) semi-logarithmic and (b) linear scale.

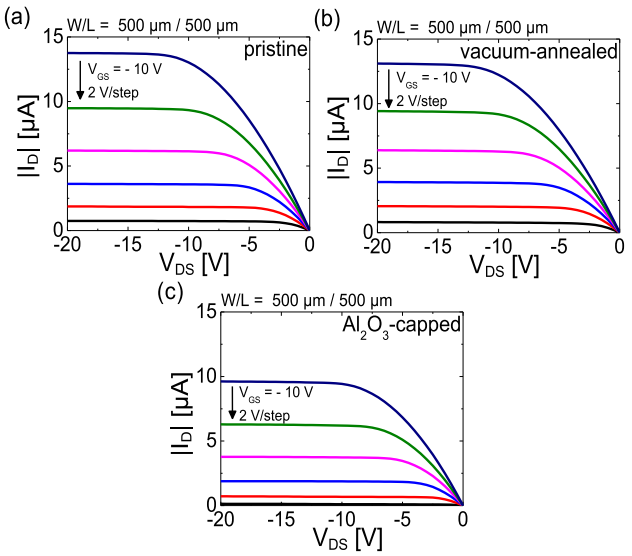

FIGURE 3. Output curves measured from the (a) pristine, (b) vacuum-annealed, and (c) Al_2O_3-capped SnO TFTs.

where C_i is the capacitance of the gate dielectric per unit area and g_m is the transconductance whose value can be obtained by the equation of $g_m = dI_D/dV_{GS}$. Here, C_i was determined as 8.63×10^{-8} F/cm^2 considering the dielectric constant (= 3.9) and thickness (= 40 nm) of the gate insulator. The SS was calculated using the subthreshold region data in Fig. 2(a) based on the following equation:

$$SS = \frac{dV_{GS}}{d(\log I_D)} \tag{2}$$

and V_{TH} was obtained by finding the intercept of the linearly extrapolated linear-scale transfer curve with the V_{GS} axis. From the figures, it is clear that the Al_2O_3 capping layer enhances the μ_{FE} and reduces the SS of the SnO TFT. Furthermore, the capping increases the $I_{ON/OFF}$ and shifts the V_{TH} in the negative direction. Transfer curves measured from the additionally vacuum-annealed SnO TFT exhibit similar shapes as those of the pristine TFT, implying that the additional thermal budget provided during the deposition of the Al_2O_3 thin film can be excluded from the possible mechanisms responsible for the enhanced electrical performance of the Al_2O_3-capped SnO TFT. Table 1 summarizes the electrical parameters extracted from three types of SnO TFTs. The electrical parameters of each type of SnO TFT

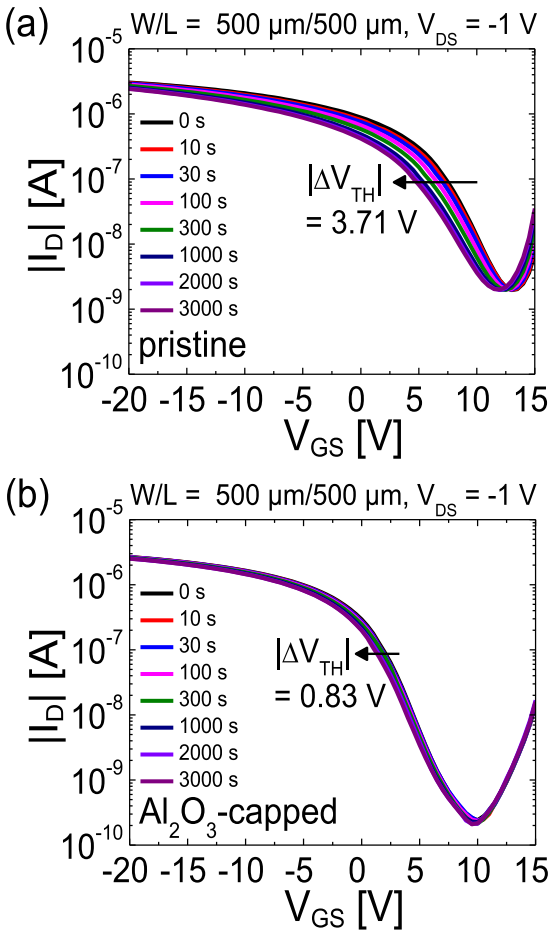

FIGURE 4. Time dependence of representative transfer curves for (a) pristine and (b) Al_2O_3-capped SnO TFTs under an application of the constant bias stress of $V_{GS} = -15$ V and $V_{DS} = -1$ V.

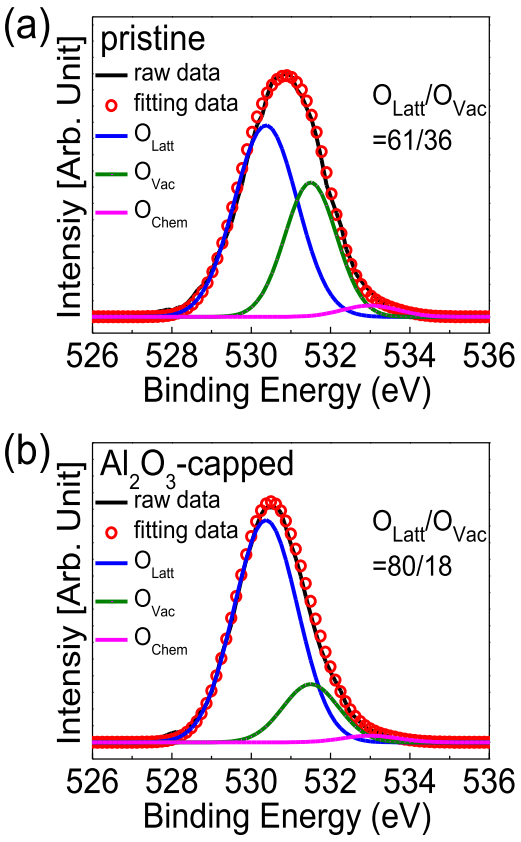

FIGURE 5. XPS O1s spectra of the SnO thin-film (a) without and (b) with an Al_2O_3 capping layer obtained in the middle of the SnO thin-film.

were obtained from five devices that were randomly selected among TFTs fabricated from different batches. The results in table 1 show that every type of SnO TFT exhibits an excellent uniformity. Figs. 3(a)-(c) display the output curves measured from the pristine, vacuum-annealed, and Al_2O_3-capped SnO TFTs, respectively. Fig. 3 shows that output curves obtained from all SnO TFTs exhibit clear pinch-off and solid saturation. The lower saturation current of the Al_2O_3-capped SnO TFT than that of other SnO TFTs at the same V_{GS} are due to the negatively shifted V_{TH} value of the Al_2O_3-capped SnO TFT.

Figs. 4(a) and (b) present the time dependences of the transfer curves for the pristine and Al_2O_3-capped SnO TFTs under a constant-bias stress of $V_{GS} = -15$ V and $V_{DS} = -1$ V, respectively. Fig. 4 shows that the transfer curves shift toward the negative direction with an increase in the stress time for both TFTs. A large threshold voltage shift ($|\Delta V_{TH}|$) of 3.71 V is observed for the pristine SnO TFT after stress application for 3,000 s. However, the Al_2O_3-capped SnO TFT exhibits a significantly smaller value of $|\Delta V_{TH}|$ (= 0.83 V) compared to the pristine one after being exposed to the same duration of stress. The results in Fig. 4 show that the Al_2O_3 capping layer formed by ALD improves not only the electrical performance but also the electrical stability of the p-channel SnO TFTs. In the p-channel oxide TFTs, both the negative-bias-stress stability and *SS* characteristics in the transfer curves degrade with an increase in the subgap densities of the states within the bulk oxide semiconductor or at the gate dielectric/metal oxide interface [33]–[38]. Furthermore, the carrier transport of the p-channel SnO TFT is dominated by the trap-limited conduction at RT [23], thus, the high density of subgap states decreases the μ_{FE} in SnO TFTs. Therefore, the experimental results in Figs. 2 and 4 show that the number of subgap states in the SnO was effectively reduced by the Al_2O_3 capping layer.

To investigate the physical mechanism responsible for the observed electrical performance and stability improvement of the Al_2O_3-capped SnO TFTs, SnO thin films with and without the Al_2O_3 capping layer were characterized by XPS and TOF-SIMS, respectively. Figs. 5(a) and (b) respectively show the XPS O1*s* spectra obtained at the middle of the SnO thin films without and with the Al_2O_3 capping layer. The Ar^+ ion beam was used to sputter the Al_2O_3 and SnO thin films before the XPS characterization. The XPS spectra were deconvolved into three sub-peaks originating from the lattice oxygen (O_{Latt}), oxygen vacancies (O_{Vac}), and chemisorbed and dissociated oxygen (O_{Chem}) using a Gaussian function; here, the binding energies of the O_{Latt}, O_{Vac}, and O_{Chem} components were fixed at 530.4 eV, 531.5 eV, and 533.0 eV,

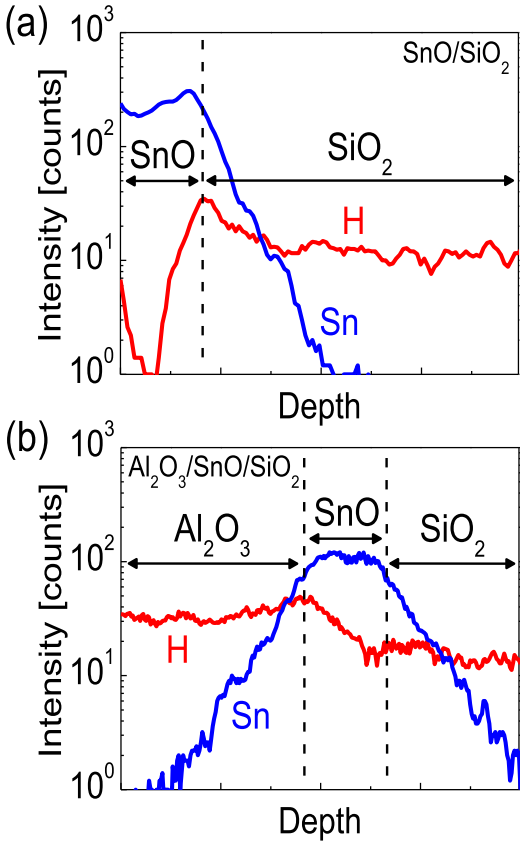

FIGURE 6. TOF-SIMS depth profile of tin and hydrogen for (a) SnO/SiO_2 and (b) $Al_2O_3/SnO/SiO_2$ samples.

respectively [39]. Fig. 5 shows that the area percentage of the O_{Vac} is significantly lower in the SnO thin film with the Al_2O_3 capping layer (O_{Latt}:O_{Vac} = 80:18) than in the pristine SnO thin film (O_{Latt}:O_{Vac} = 61:36). In previous works on the p-type SnO semiconductor, O_{Vac} was reported to generate the hole trap states located approximately 0.24 eV above the valence band maximum within the SnO [40], [41]. The XPS results in Fig. 5 show that the formation of the atomic-layer-deposited Al_2O_3 capping layer enhances the electrical characteristics of the p-channel SnO TFT by reducing the number of hole trap states originating from the O_{Vac} in the SnO.

Figs. 6(a) and (b) display the TOF-SIMS depth profiles of tin and hydrogen for the SnO/SiO_2 and $Al_2O_3/SnO/SiO_2$ samples, respectively. It can be clearly observed that the hydrogen intensity in the SnO thin film is higher in the $Al_2O_3/SnO/SiO_2$ sample than the SnO/SiO_2 sample. This phenomenon can be attributed to hydrogen diffusion from the atomic-layer-deposited Al_2O_3 thin film to the SnO thin film during the ALD process at 200 °C. The Al_2O_3 thin film deposited by the ALD method using TMA and H_2O as precursors might contain the hydrogen as a result of incomplete removal of the hydroxyl groups during the surface reaction, especially when formed at low temperatures [42]. Fig. 6(b) shows that the atomic-layer-deposited Al_2O_3 layer on the SnO thin film contains a non-negligible amount of hydrogen, as expected. In a recently published paper by Lee *et al.*, the authors showed that hydrogen could eliminate the hole trap states originating from the O_{Vac} by forming Sn-H bonds in the SnO [41]. The hydrogen in the thermal SiO_2 is considered to be caused by the hydrogen contained in the hydrogen chloride gas introduced into the furnace during the dry oxidation process [43]. The relatively higher amount of hydrogen in the SnO near the SiO_2 than near the surface in the SnO/SiO_2 sample is possibly attributed to the hydrogen diffused from the SiO_2 during the post deposition annealing process. The TOF-SIMS results in Fig. 6 demonstrate that a hydrogen-induced decrease in the hole trap concentration in the SnO could be a plausible mechanism responsible for the electrical performance and stability improvement of the atomic-layer-deposited Al_2O_3-capped p-channel SnO TFTs.

IV. CONCLUSION

In this work, we successfully demonstrate the improved electrical performance and stability of p-channel SnO TFTs using an Al_2O_3 capping layer formed via the ALD method. Electrical properties of μ_{FE} = 1.7 $cm^2/V{\cdot}s$, SS = 2.9 V/dec, V_{TH} = 2.7 V, and $I_{ON/OFF}$ = 1.6 × 10^4 were observed for the Al_2O_3-capped SnO TFT, and these values were superior to those of the pristine SnO TFT (μ_{FE} = 1.5 $cm^2/V{\cdot}s$, SS = 3.8 V/dec, V_{TH} = 6.5 V, and $I_{ON/OFF}$ = 6.9 × 10^2). Furthermore, the SnO TFT with the Al_2O_3 capping layer exhibited significantly smaller $|\Delta V_{TH}|$ (= 0.83 V) than the pristine SnO TFT ($|\Delta V_{TH}|$ = 3.71 V) under the constant-bias stress conditions V_{GS} = −15 V and V_{DS} = −1 V applied for 3,000 s. From the XPS and TOF-SIMS characterizations, a smaller amount of O_{Vac} and larger amount of hydrogen were observed for the Al_2O_3-capped SnO thin film than the pristine SnO thin film. The passivation of the O_{Vac}-induced hole trap states by the diffused hydrogen from the Al_2O_3 capping layer is hereby suggested as the physical mechanism responsible for the observed phenomenon.

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