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Power Quality Improvement in HVDC MMC With Modified Nearest Level Control in Real-Time HIL Based Setup

SADDAQAT ALI[1], JAHANGEER BADAR SOOMRO[1], MAHNOOR MUGHAL[1], FAHEEM AKHTER CHACHAR[1], SYED SABIR HUSSAIN BUKHARI[1,2], (Member, IEEE), AND JONGSUK RO[2]

[1]Department of Electrical Engineering, Sukkur IBA University, Sukkur 65200, Pakistan
[2]School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 06974, South Korea

Corresponding author: Jongsuk Ro (jongsukro@gmail.com)

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ABSTRACT The Modular Multilevel Converter (MMC) is the best topology for medium and high voltage applications. The performance of MMC and the quality of the output waveform completely depends on the control applied. Nearest Level Modulation (NLM) is the conventional method used to control MMC that produces N+1 (N is the number of submodules per arm) AC output voltages. This article proposes a modified NLM control method for the MMC, which produces 2N+1 level which is twice the number of levels produced by conventional NLM. The proposed method is easy to implement and is extended in the article to produce a 4N+1 output voltage level which is never done in the literature. The THD of the output waveform is reduced to more than one-fourth compared to conventional NLM. The cost of switching devices, capacitors and size of circuit is also reduced to one-fourth for 4N+1 output waveform compared to conventional NLM. The method is verified through LabVIEW Multisim Co-simulation and real-time simulation using Field Programmable Gate Array (FPGA) based NI PXI.

INDEX TERMS Modified NLC, power quality, HVDC MMC, hardware-in-loop simulation.

I. INTRODUCTION

The concept of the Modular multilevel converter was introduced in 2003 [1], after that it has been adopted as the art of technology in the high-voltage and high-power applications, such as high-voltage direct current (HVDC) transmission, power derives, and STATCOM [2]–[5]. The fundamental topology for MMC submodules (SMs) is half-bridge (HB) [6]. To optimize the cost of the converter and to improve the quality and performance of MMC, various SMs topologies and control techniques are being developed [7]–[10].

In the literature, many control techniques such as pulse width modulation (PWM), space vector control, and selective harmonic elimination (SHE) have been introduced and used to control the MMC [11]–[16]. For a step wave modulation, mainly SHE and NLM are used since they have some common features such as low switching frequency and N+1 levels. In HVDC applications where the switching frequency used in the converter is limited, the NLM is adapted since, the NLM with its attractive advantages such as being simple to implement, natural capacitor voltage balancing and not involving complex mathematics to find particular firing angle as in SHE, is used majorly [17]–[19]. In NLM, the arm voltages generated are taken as reference and are fed back to the modulator to generate the pulses for all the SMs present in the upper and lower arm of the MMC. The sinusoidal arm voltage references are converted to the staircase waveform using the nearest integer method and then using the conventional sorting algorithm, the SMs are inserted and bypassed depending upon their voltage, the arm current polarity, and the level of voltage required [20]–[21].

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It has been observed that to increase the number of levels and improve the quality of output waveform the number of SMs is to be increased every time, which in practice increases the number devices i.e. capacitors and switches, cost and complexity of the MMC [22]. In order to improve the quality of the waveform without any additional switching devices, using the same number of SMs, this article proposes a modified NLM method with the output levels raised up to 2N+1. The proposed method is further extended using the same methodology to produce 4N+1 output levels and Total Harmonic Distortion (THD) of the output waveform reduces $1/4^{th}$ of the previous results taken using the conventional NLM method.

The proposed method compared to other previous modified methods has many advantages in terms of simplicity, easy implementation and power quality. For instance, in [23] the circuit of the MMC is reduced and power quality is improved using binary, trinary, and modified MMC-based topology, but their algorithm involves complex calculation and THD is higher compared to our proposed modified NLC. The reference [24] proposes an improved NLC algorithm with a reduced number of SMs but their results are limited to offline simulation and involves complex calculation compared to our proposed method. The work presented in [25] shows a modified NLM method and claims less THD but their work lacks experimental verification and THD is more compared to our results. The authors of [26] presented level increased NLM modulation with a reduced number of SMs and THD but their method involves too much calculation compared to our proposed method and THD reduction for 11 level is also less compared to our proposed method. In [27]–[30] different authors presented ways of increasing AC output voltage levels, decreasing THD, and increasing the power quality but their method cannot be extended to achieve 4N+1 level AC output voltage as compared to our proposed method.

The control is implemented in LabVIEW and the model is designed in Multisim to obtained offline simulation results using LabVIEW Multisim co-simulation platform and the results are taken using modified NLM and compared with conventional NLM technique with the different number of levels in the output waveform. The real-time results are obtained using FPGA based controller compact RIO (CRIO) and NI PXI system. The article is organized as follows: Working principle of MMC is discussed in section II. Section III introduces the conventional NLM method. In section IV, the modified NLM method is introduced and analyzed. Section V presents the offline and real-time simulation results.

II. WORKING PRINCIPLE OF MMC

The Single-phase MMC circuit shown in Fig. 1 consists of the upper arm and lower arm connected through inductors. Each arm has N connected SMs in series and each SM consists of two switches and a capacitor connected across them. Applying Kirchhoff's voltage law (KVL) in the upper and lower

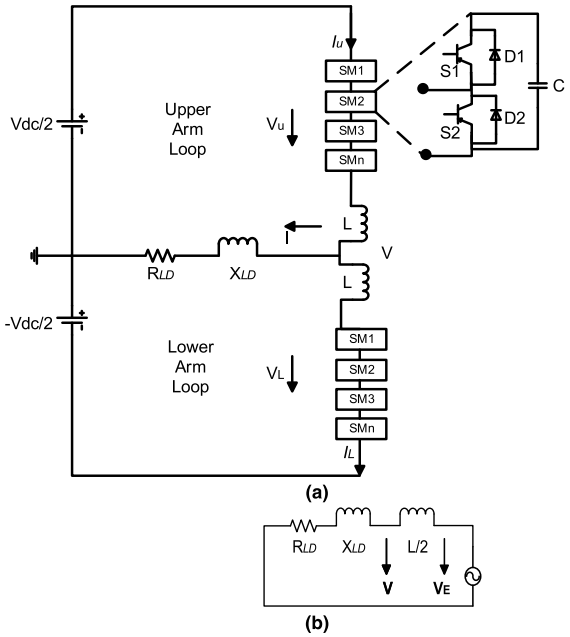

FIGURE 1. (a) Single-phase MMC circuit diagram; (b) equivalent circuit of the MMC.

loop in Fig. 1 we will get:

$$V = \frac{1}{2}V_{dc} - V_U - L\frac{di_U}{dt} \tag{1}$$

$$V = -\frac{1}{2}V_{dc} + V_L + L\frac{di_L}{dt} \tag{2}$$

And applying Kirchhoff's current law (KCL) to find the output current:

$$i = i_L - i_U \tag{3}$$

The equivalent circuit of MMC is shown in Fig. 1(b). Using equation (1) and (2) the output voltage will be

$$V = \frac{1}{2}(V_L - V_U) + \frac{1}{2}L\frac{di}{dt} \tag{4}$$

From equation (3) it is clear that the ac equivalent voltage can be expressed as

$$V_E = \frac{1}{2}(V_L - V_U) \tag{5}$$

Generally, the ac equivalent voltage can be shown as

$$V_E^{ref} = \frac{mV_{dc}}{2}\cos(\omega t) \tag{6}$$

In equation (6) m is the modulation index with $0 < m < 1$ and ω is the angular frequency. N submodules are used in the circuit using the conventional NLM method so, the below equation is satisfied on the dc side.

$$V_{dc} = V_L + V_U \tag{7}$$

Reference voltages for the upper and lower arm can be expressed by

$$V_U^{ref} = \frac{V_{dc}}{2}[1 - m\cos(\omega t)] \tag{8}$$

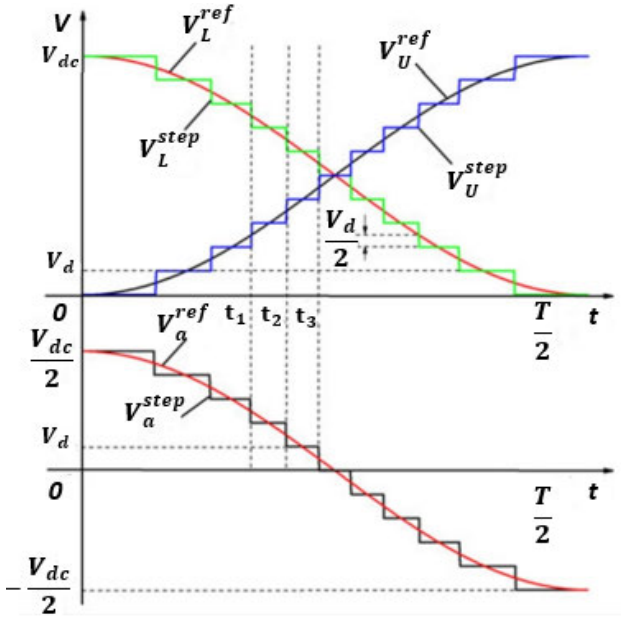

FIGURE 2. Conventional NLM switching pattern.

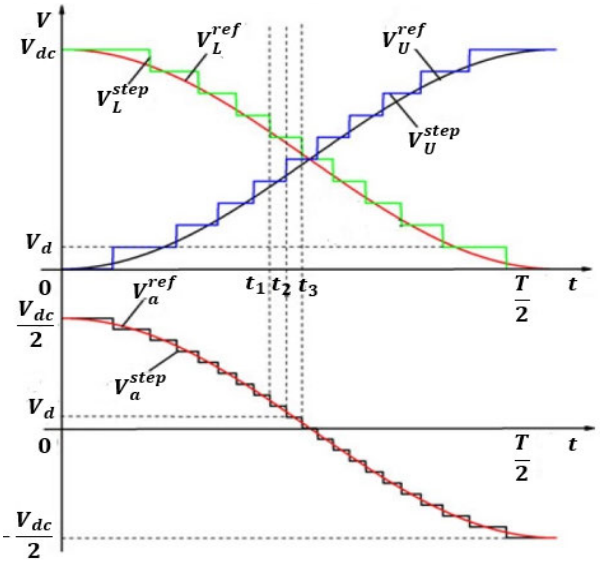

FIGURE 3. Modified NLM Method.

$$V_L^{ref} = \frac{V_{dc}}{2}[1 + m\cos(\omega t)] \tag{9}$$

III. CONVENTIONAL NLM METHOD

In conventional NLM the number of submodules to be inserted is calculated by

$$N_U = round_{0.5}\frac{V_{dc}}{2V_d}(1 - m\cos(\omega t)) \tag{10}$$

$$N_L = round_{0.5}\frac{V_{dc}}{2V_d}(1 + m\cos(\omega t)) \tag{11}$$

where V_d is the SM capacitor voltage at any instant. The round function is used to round the real number into the nearest available integer according to its decimal fraction. If the decimal fraction of the argument is less than 0.5 then the argument will be rounded to previously available integer otherwise if it is greater than 0.5 then it will be rounded to the next available integer. To understand the switching states two cases [t_1 to t_2, t_2 to t_3] are analyzed and shown in Fig. 2. In the first case [t_1 to t_2], assuming $V_L^{step} = MV_d$ then the reference values of arm voltages and equivalent inner voltage of the phase at $t = t_1$ can be shown as (12) and (13) respectively.

$$\begin{cases} V_L^{ref} = (M + 0.5)V_d \\ V_U^{ref} = [(N - M - 1) + 0.5]V_d \end{cases} \tag{12}$$

$$V_E^{ref} = (M - 0.5N + 0.5)V_d \tag{13}$$

In the first scenario, the step waves of arm voltages and equivalent inner voltage are expressed as

$$\begin{cases} V_L^{step} = MV_d \\ V_U^{step} = (N - M)V_d \end{cases} \tag{14}$$

$$V_E^{step} = (M - 0.5N)V_d \tag{15}$$

In the second scenario from t_2 to t_3 reference values of arm voltages and equivalent inner voltage are expressed as

$$\begin{cases} V_L^{ref} = [(M - 1) + 0.5]V_d \\ V_U^{ref} = [(N - M) + 0.5]V_d \end{cases} \tag{16}$$

$$V_E^{ref} = (M - 0.5N - 0.5)V_d \tag{17}$$

The step waves of arm voltages and equivalent inner voltages are shown as

$$\begin{cases} V_L^{step} = (M - 1)V_d \\ V_U^{step} = (N - M + 1)V_d \end{cases} \tag{18}$$

$$V_E^{step} = (M - 0.5N - 1)V_d \tag{19}$$

Comparing (15) and (19), it can be observed that the step height in V^{step} is V_d. Since the positive and negative DC voltage limits are $\pm 0.5V_{dc}$, the maximum level in equivalent inner voltage is equal to $V_{dc}/V_d + 1$.

IV. PROPOSE MODIFIED NLM METHOD

The modified NLM method is based on introducing a small phase shift in reference waveform for either upper or lower arm in each phase of the three-phase MMC. Fig. 3 depicts the proposed modified N LM method in which the reference waveform of the lower arm has a phase shift compared to the waveform of the upper arm reference waveform. The equations in modified NLM for reference voltage and staircase waveform respectively can be expressed as shown in (20) and (21) for 2N+1 AC output voltage levels.

$$V_L^{ref} = \frac{V_d}{2}(1 + m\cos(\omega t + \beta)) \tag{20}$$

$$V_L^{step} = round_{0.5}\frac{V_d}{2}(1 + m\cos(\omega t + \beta)) \tag{21}$$

where β can found using the algorithm shown below in Fig. 4.

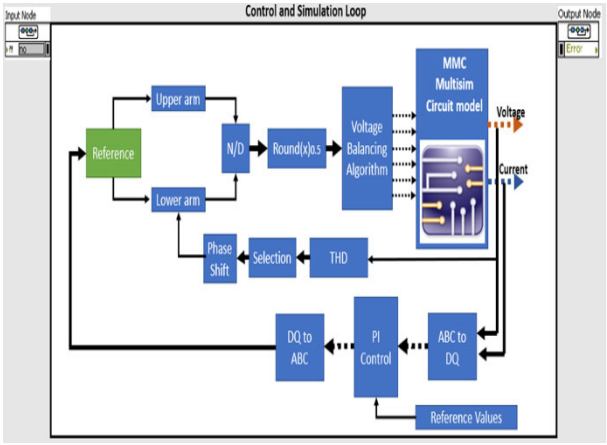

FIGURE 4. Proposed Modified NLM in LabVIEW Multisim Co-simulation.

The proposed algorithm is implemented in LabVIEW for co-simulation as shown in Fig. 4. The THD of the voltage is measured and it is fed to the selection block where the THD from the previous iteration is available. Based on the THD the phase shift is changed either increased or decreased. If the THD of the current iteration is less than the previous iteration the phase is increased and vice versa. The variations in system such as load variation, temporary faults and transients causes the variation in β angle. The optimum value of β (phase shift) in modified NLC was found to be in the range of 9.5 degrees to 11 degrees.

The proposed method using the same concept of introducing phase shift in the reference waveform can now be extended to produce 4N+1 output levels. As shown in Fig. 5(b) from t_1 to t_3, if the waveform (2N+1) is taken as a reference waveform then a phase shifted waveform from this reference waveform can be used to control either upper or lower arm which will produce 4N+1 output levels. This process is further illustrated in Fig. 5(a) and Fig 5(b).

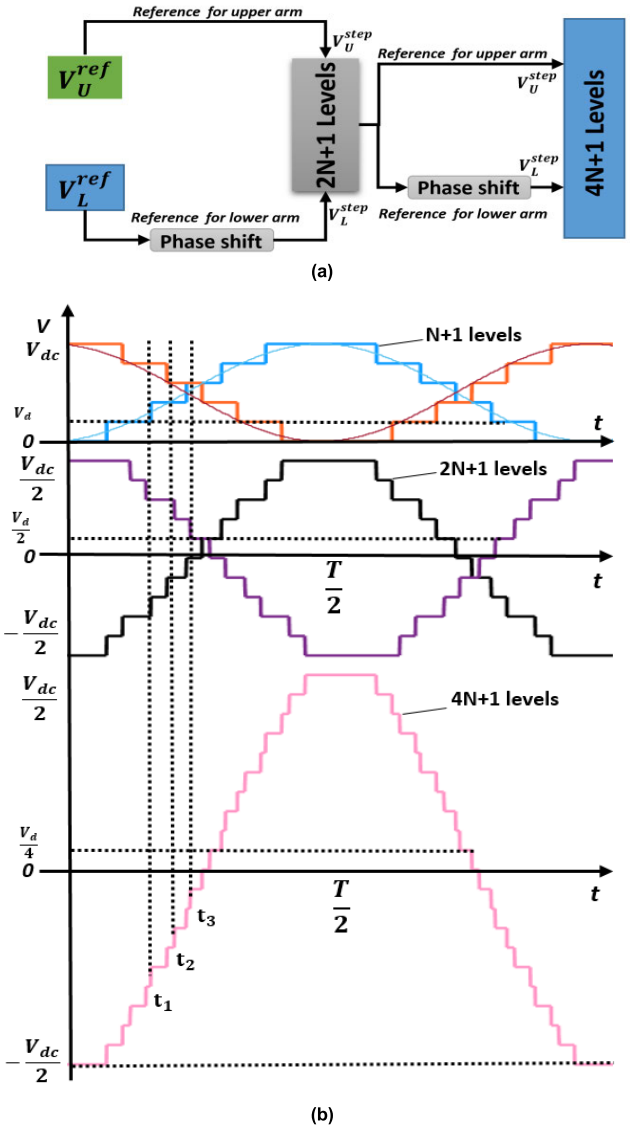

FIGURE 5. Modified NLM for 4N+1 Output levels, and (b) Modified NLM Method for 4N+1 Levels.

V. LABVIEW MULTISIM CO-SIMULATION AND REAL-TIME SIMULATION RESULTS

In order to validate the proposed method the offline results are obtained using LabVIEW Multisim co-simulation and for real-time simulation results, NI PXI and cRIO are used.

A. LABVIEW MULTISIM CO-SIMULATION RESULTS

To obtain offline simulation results LabVIEW Multisim co-simulation platform is used in which the conventional and modified NLC is designed once and used for both offline and real-time simulation. The methodology obtained for offline and real-time simulation of three-phase MMC used is shown in Fig. 6. To show the effectiveness of the modified NLM method, both conventional and modified NLM methods are implemented in simulations, and results are obtained.

The parameters used in implementing three-phase MMC are shown in table 3 and results are obtained for different levels of output voltage and current waveform for N+1 and 2N+1 level. The modified NLC algorithm is activated at 0.03 sec. When using conventional NLM the THD of the output voltage and current is 12.1% and 7.46% respectively for N+1 level (N=5). With modified NLM the THD of output voltage and current is 5.98% and 4.35% respectively for N+1 level (N=5). Different levels of AC output voltage and current as shown from Fig. 7 to Fig. 14 are obtained using LabVIEW Multisim co-simulation and their comparison is shown in Table 1. It is highly important to ensure that power flow through the sub module is zero over a certain period of time to maintain capacitor voltages constant. If the capacitor voltages are diverging and are not kept at a fixed value, this will result in non-sinusoidal output waveform. Capacitor voltages are balanced before and after Modified NLC control is activated as shown in Fig. 15.

B. REAL-TIME SIMULATION RESULTS

The circuit of three-phase MMC is loaded in NI PXI which is an FPGA-based floating-point solver that is used to burn

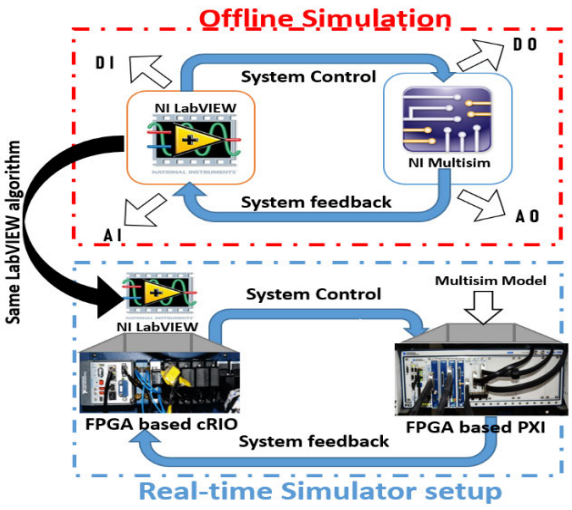

FIGURE 6. Methodology for offline and real-time simulation.

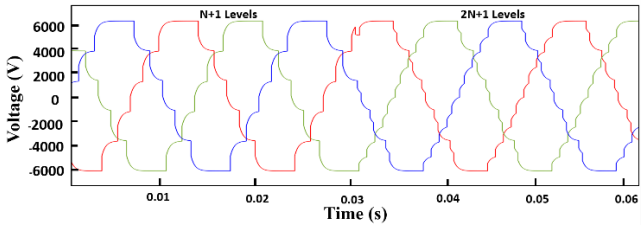

FIGURE 7. Three-phase output voltage waveforms with 6 levels and 11 levels.

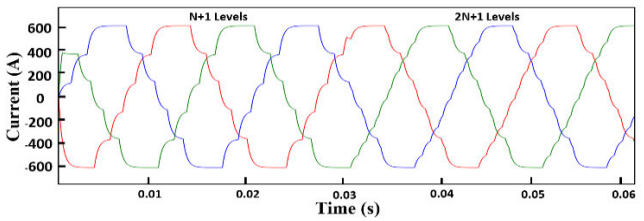

FIGURE 8. Three-phase output current waveform with 6 levels and 11 levels.

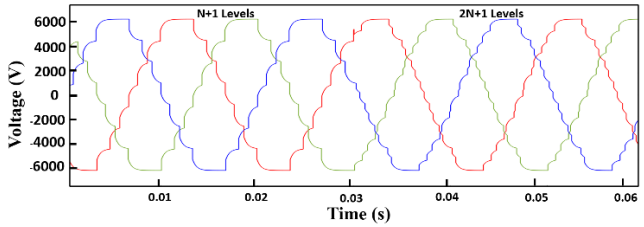

FIGURE 9. Three-phase output voltage waveforms with 8 levels and 15 levels.

electrical circuit on the FPGA automatically with a step size of nanoseconds. The architecture of hardware-in-loop (HIL) setup is previously shown in Fig. 6. The conventional and modified NLC algorithm is burned on CRIO which is an FPGA based controller with hot swappable input/output modules. The CRIO uses analog and digital input/output modules

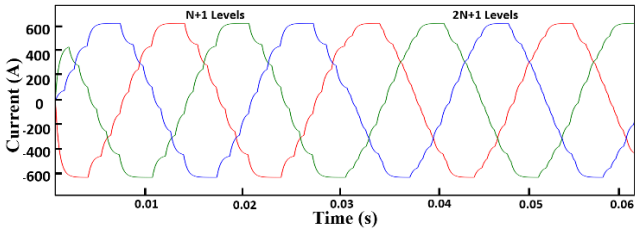

FIGURE 10. Three-phase output current waveform with 8 levels and 15 levels.

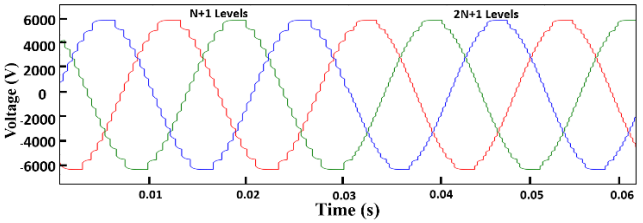

FIGURE 11. Three-phase output voltage waveforms with 16 levels and 33 levels.

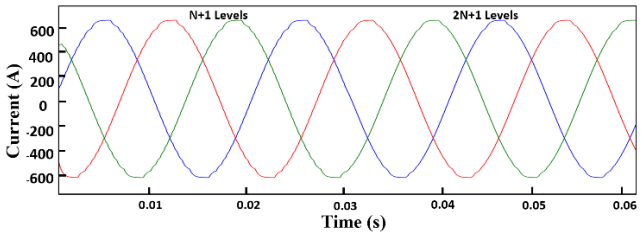

FIGURE 12. Three-phase output current waveform with 16 levels and 33 levels.

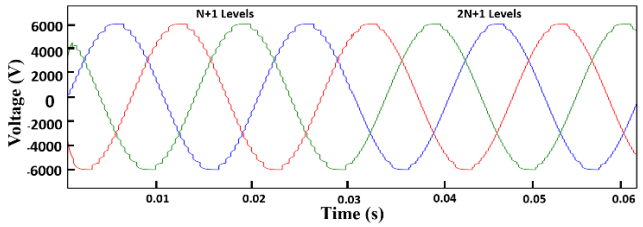

FIGURE 13. Three-phase output voltage waveforms with 22 levels and 43 levels.

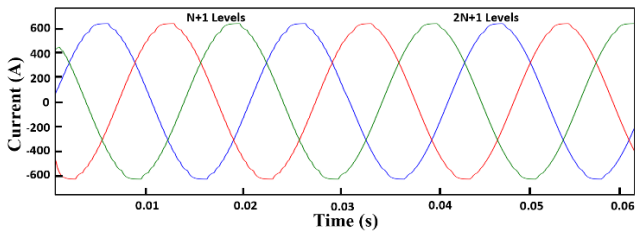

FIGURE 14. Three-phase output current waveform with 22 levels and 43 levels.

to control and monitor the three-phase MMC running in NI PXI. The conventional and modified NLC is used to control and obtained the real time results for voltage and current of

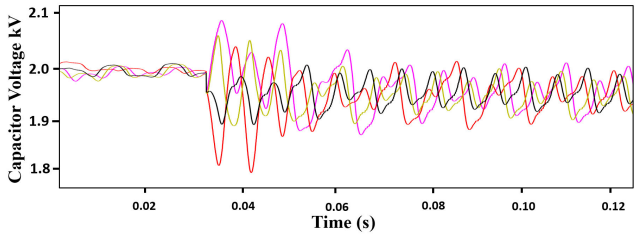

FIGURE 15. SM capacitor voltages.

TABLE 1. Comparison of THD w.r.t SMs Using Convention and Modified NLC.

Number of SMs	Voltage %THD		Current %THD	
	Conventional NLC	Modified NLC	Conventional NLC	Modified NLC
5	12.1	5.98	7.46	4.35
8	7.92	4.23	4.22	2.76
15	3.64	1.79	1.6	0.75
21	2.35	1.05	0.84	0.39

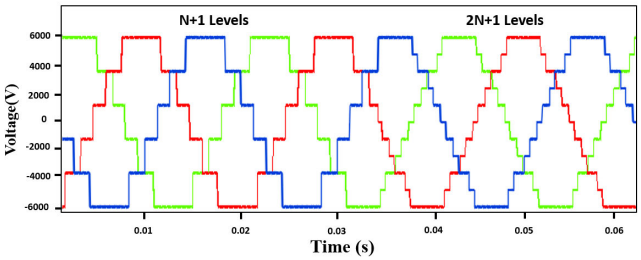

FIGURE 16. Three-phase output voltage waveforms with 6 levels and 11 levels.

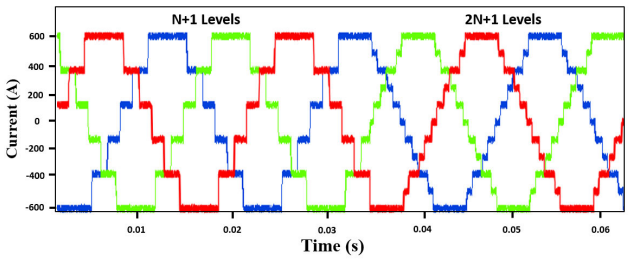

FIGURE 17. Three-phase output current waveform with 6 levels and 11 levels.

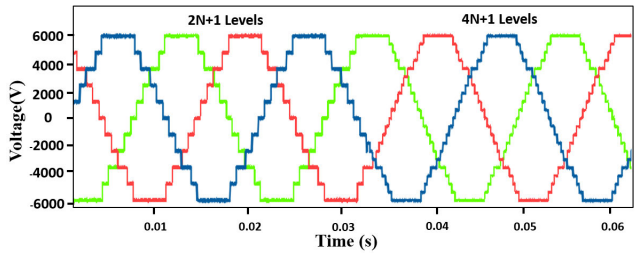

FIGURE 18. Three-phase output voltage waveforms from 11 levels (2N+1) to 21 levels (4N+1) with N=5 (number of SMs).

three phase MMC for 2N+1 level as shown in Fig. 16 and 17 respectively. The Modified NLM is further extended to

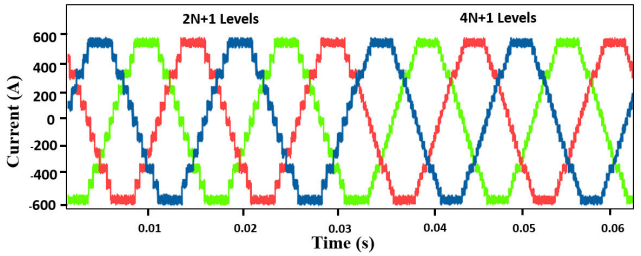

FIGURE 19. Three-phase output current waveform from 11 levels (2N+1) to 21 levels (4N+1) with N=5 (number of SMs).

TABLE 2. Comparison of THD in Offline and Real-Time Simulation.

Setup		Voltage %THD			Current %THD		
	N	N+1	2N+1	4N+1	N+1	2N+1	4N+1
Offline simulation	5	12.1	5.98	2.75	7.46	4.35	1.30
Real-time Simulation	5	12.35	6.23	2.82	7.92	6.38	1.42

TABLE 3. Offline and Real-Time Simulation Parameters.

Item No.	System Parameters	Values
1	Rated power	10 MVA
2	Vac grid voltage	4.16 kV
3	Vd	8 kV
4	Rated Frequency	50 Hz
5	SM_Cap (Submodule capacitance)	5000 uF
6	L_arm (Arm inductance)	5 mH
7	L_val (Line inductance)	3 mH
8	R_line (Line resistance)	0.003 Ω

increases the number of levels obtained in Fig. 15 and 16 from 2N+1 levels to 4N+1 levels as shown in Fig. 17 and 18. It can be observed that the THD of the output voltage decreases from 12.35% with N+1 level to 2.82% with 4N+1 level in real-time simulation (N=5). Moreover, the current THD decreases from 7.92% with N+1 level to 1.42% with 4N+1 level in real-time simulation (N=5). The THD for output voltage and current is slightly higher in real-time simulation results as compared to offline simulation results, due to fundamental switching frequency and step size of nanoseconds in real-time simulation. The THD in offline and real-time simulation for N+1, 2N+1, and 4N+1 output levels is also compared in table II to show the effectiveness of the modified NLC method.

VI. CONCLUSION

Usage of more submodules, capacitors, and increased total harmonic distortion poses a limitation for conventional NLM

control for MMC to its wide range of applications including HVDC. Therefore, Modified NLC is proposed in this research work which reduces the number of submodules, capacitors, and improves the power quality. It is concluded that as compared to conventional NLM, the Modified NLC can produce 2N+1 output voltage levels and can also be extended to produce up to 4N+1 output voltage levels. Efficacy of proposed modified NLC for MMC is verified using both offline and real-time simulation results using LabVIEW-Multisim Co-Simulation and laboratory setup of power hardware in the loop. Finally, the results in terms of THD are compared for N+1, 2N+1, and 4N+1 levels using offline and real-time simulation.

REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf.*, vol. 3, Jun. 2003, p. 6.

[2] S. Ali, J. Badar, F. Akhter, S. S. H. Bukhari, and J. Ro, "Real-time controller design test bench for high-voltage direct current modular multilevel converters," *Appl. Sci.*, vol. 10, no. 17, p. 6004, Aug. 2020.

[3] M. Espinoza-B, R. Cardenas, J. Clare, D. Soto-Sanchez, M. Diaz, E. Espina, and C. M. Hackl, "An integrated converter and machine control system for MMC-based high-power drives," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2343–2354, Mar. 2019.

[4] M. T. Bina, "A transformerless medium-voltage STATCOM topology based on extended modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1534–1545, May 2011.

[5] H. Saad, J. Peralta, S. Dennetiere, J. Mahseredjian, J. Jatskevich, J. A. Martinez, A. Davoudi, M. Saeedifard, V. Sood, X. Wang, J. Cano, and A. Mehrizi-Sani, "Dynamic averaged and simplified models for MMC-based HVDC transmission systems," *IEEE Trans. Power Del.*, vol. 28, no. 3, pp. 1723–1730, Jul. 2013.

[6] A. Marzoughi, R. Burgos, D. Boroyevich, and Y. Xue, "Investigation and comparison of cascaded H-bridge and modular multilevel converter topologies for medium-voltage drive application," in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Oct. 2014, pp. 1562–1568.

[7] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Trans. Power Del.*, vol. 30, no. 1, pp. 385–394, Feb. 2015.

[8] J. Lyu, X. Cai, and M. Molinas, "Optimal design of controller parameters for improving the stability of MMC-HVDC for wind farm integration," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 40–53, Mar. 2018.

[9] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 316–324, Jan. 2011.

[10] L. Zhang, A. State University, Y. Zou, J. Yu, J. Qin, V. Vijay, G. G. Karady, D. Shi, and Z. Wang, "Modeling, control, and protection of modular multilevel converter-based multi-terminal HVDC systems: A review," *CSEE J. Power Energy Syst.*, vol. 3, no. 4, pp. 340–352, Dec. 2017.

[11] G. S. Konstantinou, M. Ciobotaru, and V. G. Agelidis, "Analysis of multicarrier PWM methods for back-to-back HVDC systems based on modular multilevel converters," in *Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Nov. 2011, pp. 4391–4396.

[12] G. Konstantinou, V. Agelidis, and M. Ciobotaru, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *IET Power Electron.*, vol. 6, no. 1, pp. 96–107, Jan. 2013.

[13] A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "A space-vector PWM-based voltage-balancing approach with reduced current sensors for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2734–2745, May 2016.

[14] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel Back-to-Back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[15] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.

[16] X. Li, Q. Song, W. Liu, and J. Li, "Capacitor voltage balancing control by using carrier phase-shift modulation of modular multilevel converters," *Zhongguo Dianji Gongcheng Xuebao(Proc. Chin. Soc. Elect. Eng.)*, vol. 32, no. 9, pp. 49–55, 2012.

[17] P. M. Meshram and V. B. Borghate, "A simplified nearest level control (NLC) voltage balancing method for modular multilevel converter (MMC)," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 450–462, Jan. 2015.

[18] G. Tae Son, H.-J. Lee, T. Sik Nam, Y.-H. Chung, U.-H. Lee, S.-T. Baek, K. Hur, and J.-W. Park, "Design and control of a modular multilevel HVDC converter with redundant power modules for noninterruptible energy transfer," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1611–1619, Jul. 2012.

[19] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[20] F. Martinez-Rodrigo, D. Ramirez, A. B. Rey-Boue, S. De Pablo, and L. C. Herrero-de Lucas, "Modular multilevel converters: Control and applications," *Energies*, vol. 10, no. 11, p. 1709, 2017.

[21] H. Saad, T. Ould-Bachir, J. Mahseredjian, C. Dufour, S. Dennetiere, and S. Nguefeu, "Real-time simulation of MMCs using CPU and FPGA," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 259–267, Jan. 2015.

[22] L. Lin, Y. Lin, Z. He, Y. Chen, J. Hu, and W. Li, "Improved nearest-level modulation for a modular multilevel converter with a lower submodule number," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5369–5377, Aug. 2016.

[23] A. Alexander and M. Thathan, "Modelling and analysis of modular multilevel converter for solar photovoltaic applications to improve power quality," *IET Renew. Power Gener.*, vol. 9, no. 1, pp. 78–88, Jan. 2015.

[24] W. Zhao, K. Yang, and G. Chen, "An improved nearest-level-modulation of modular multilevel converter—STATCOM," in *Proc. IEEE 11th Int. Conf. Power Electron. Drive Syst.*, Jun. 2015, pp. 219–223.

[25] Q. Liu, A. Chen, C. Du, and C. Zhang, "A modified nearest-level modulation method for modular multilevel converter with fewer submodules," in *Proc. Chin. Autom. Congr. (CAC)*, Oct. 2017, pp. 6551–6556.

[26] P. Hu and D. Jiang, "A level-increased nearest level modulation method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1836–1842, Apr. 2015.

[27] A. A. Gebreel and L. Xu, "Power quality and total harmonic distortion response for MMC with increasing arm inductance based on closed loop-needless PID controller," *Electr. Power Syst. Res.*, vol. 133, pp. 281–291, Apr. 2016.

[28] P. Mishra and M. M. Bhesaniya, "Comparison of total harmonic distortion of modular multilevel converter and parallel hybrid modular multilevel converter," in *Proc. 2nd Int. Conf. Trends Electron. Informat. (ICOEI)*, May 2018, pp. 890–894.

[29] A. Shojaei and G. Joos, "An improved modulation scheme for harmonic distortion reduction in modular multilevel converter," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, Jul. 2012, pp. 1–7.

[30] Y. Deng, M. Saeedifard, and R. G. Harley, "An improved nearest-level modulation method for the modular multilevel converter," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Mar. 2015, pp. 1595–1600.

SADDAQAT ALI received the B.E. degree in electrical engineering from Sukkur IBA University, in 2018, where he currently pursuing the M.E. degree. From 2018 to 2019, he was a Research Assistant with the PHIL Lab, Sukkur IBA University. He is currently a Subject Specialist Electrical with the IBA Community College. His research interests include HVDC converters, power quality, and DC microgrid.

JAHANGEER BADAR SOOMRO received the B.E. degree in electronics engineering from Mehran UET, Jamshoro, and the M.E. degree in electrical power system from Mehran UET. He is currently pursuing the Ph.D. degree in electrical engineering from Sukkur IBA University, Pakistan. He is also an Assistant Professor and a Principle Investigator of power hardware with the Loop Lab, Electrical Department, Sukkur IBA University. His research interests include the power quality analysis of power converters, PWM techniques to control power converters, PWM inverters, and the real time simulation of power converters.

MAHNOOR MUGHAL received the B.E. degree in electrical engineering from Sukkur IBA University, Pakistan, in 2018. She is currently pursuing the master's degree in power systems. She is also serving as a Faculty (as Lab Engineer) for the Department of Electrical (Power) Engineering, Sukkur IBA University, Pakistan. Her research interests include HVDC systems, electrical machines, and power system quality and control.

FAHEEM AKHTER CHACHAR received the master's degree in electrical and electronics engineering with Entrepreneurship from the University of Nottingham, U.K., in 2011, and the Ph.D. degree in energy systems from The University of Edinburgh, U.K. He was a Trainee Engineer with Universal Cables Industries Ltd. In February 2010, he joined Sukkur IBA University. He has published article in international Springer journal and also presented articles in international conferences. He has also been presenting and participated in international seminars. His current research interests include the integration of offshore wind farms to onshore AC grid through VSC-HVDC technology.

SYED SABIR HUSSAIN BUKHARI (Member, IEEE) received the B.E. degree in electrical engineering from the Mehran University of Engineering and Technology, Jamshoro, Pakistan, in 2009, and the Ph.D. degree from the Department of Electronic Systems Engineering, Hanyang University, South Korea, in 2017. In December 2016, he joined as an Assistant Professor Sukkur IBA University. He is currently a Research Professor with Chung-Ang University, Seoul, South Korea, under the Korean Research Fellowship (KRF) Program. His current research interests include electric machine design, power quality, and drive controls.

JONGSUK RO received the B.S. degree in mechanical engineering from Han-Yang University, Seoul, South Korea, in 2001, and the Ph.D. degree in electrical engineering from Seoul National University (SNU), Seoul, in 2008.

From 2008 to 2012, he conducted research at the Research and Development Center, Samsung Electronics as a Senior Engineer. From 2012 to 2013, he was with the Brain Korea 21 Information Technology, SNU, as a Postdoctoral Fellow. In 2013, he conducted research at the Electrical Energy Conversion System Research Division, Korea Electrical Engineering & Science Research Institute as a Researcher. From 2013 to 2016, he was with the Brain Korea 21 Plus, SNU, as a BK Assistant Professor. In 2014, he was with the University of Bath, Bath, U.K. He is currently an Associate Professor of the School of Electrical and Electronics Engineering, Chung-Ang University, Seoul. His research interests include the analysis and optimal design of next-generation electrical machines using smart materials such as electromagnet, piezoelectric, and magnetic shape memory alloy.