Performance-Issues-Mitigation-Techniques for On-Chip-Antennas – Recent Developments in RF, MM-Wave, and Thz Bands With Future Directions

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ABSTRACT The need for a compact, economical, and low-power wireless system has given birth to the System-on-Chip (SoC) concept viable of a multitude of innovative applications. On-Chip-Antennas (AoCs) are an integral part of the SoC based wireless system and have got a remarkable attention since last one decade. In contrary to off-chip-antennas, AoCs are fabricated and integrated on the same substrate where the other components of the wireless system are fabricated. This integration results in several challenges besides highly desired benefits. The most serious challenge is the degradation in AoC's key performance metrics, i.e. gain and radiation efficiency because of low-resistivity and high-permittivity of the Silicon substrate which is the optimized choice for the AoC design. This triggers a need for the use of novel methods for the mitigation of these performance issues. Consequently, a variety of such innovative methods have been proposed in the literature. However, a critical description on the recent developments in these methods at one place to facilitate a wide range of researchers is missing. Therefore, this article presents a well-organized and systematic survey on the recent advancements of the AoC's performance-issues-mitigation-methods for wireless applications in Radio Frequency (RF), Millimeter-Wave (MM-Wave), and Terahertz (THz) bands for the first time. A concise description of future directions with respect to AoCs performance enhancement methods is also part of this article. It is anticipated that the critical presentation of these methods will make this article a valuable guide for a wide spectrum of researchers, who want to adventure with the tough task of high performance AoC design. In addition, it is envisioned that this article will pave a promising path for a further dominance of the AoCs in RF, MM-Wave, and THz regions.

INDEX TERMS Antennas-on-chip, CMOS, gain, integrated circuits, MM-wave, mitigation techniques, recent developments, RF, radiation efficiency, system-on-chip, SiGe BiCMOS, THz.

I. INTRODUCTION

Owing to enormous technological innovations in transistors scaling, integrated circuits (ICs) and fabrication processes, the world has seen a revolution in wireless systems over the last 20 years [1], [2]. The requirement to integrate various wireless systems has led to the development of multi-standard, flexible software defined radios and cognitive radio systems [3]–[7] in a small form-factor. This has pushed the need to develop miniaturized digital and analog/Radio Frequency (RF) systems [1]. In future, this trend of ever-escalating integration demand is likely to grow as

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predicted in [8] because of the emergence of novel wireless applications such as universal radios, 5G, 6G and beyond technologies [9]–[13]. It is because of this tendency that SoC integration method has got special interest recently, where all sections (digital microprocessor core, analog mixed signal, RF front-end, and antenna) of modern wireless systems are integrated on a single chip, as shown in Figure 1. Compared to alternative integration methods, i.e. Multi-chip module and System-in-Package (SiP), System-on-chip (SoC) offers several benefits such as abating the need of off-chip interconnects and packaging processes. In particular, SoC mitigates major issues associated with SiP [1], [14]–[18], which originate mainly because of the use of bond wires in SiP based systems. Some of such issues include: loss [19],
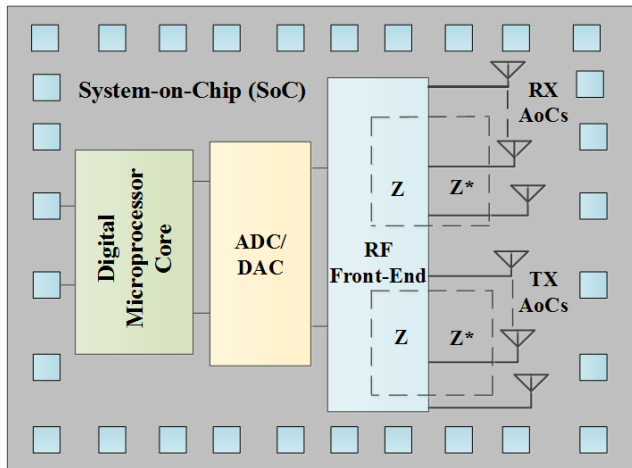
FIGURE 1. Pictorial representation of a SoC integration based wireless communication system: there is no need of lossy off-chip interconnects, i.e. bond wires. The shown multiple AoCs can be used for beamforming, which will be a pivotal part of MIMO based 5G wireless systems. The AoCs and RF front-end are conjugately matched in the figure.

radiation leakage, unintended parasitics, difficulty in realizing and modelling of bond wires [1], [20]–[25], unreliability [22], significant degradation in system's performance at Millimeter-Wave (MM-Wave) frequencies [25], and fabrication tolerance [2]. The inductance of the bond wire and capacitance of the bond pads form a bandpass filter which limit the systems' bandwidth. Consequently, bond wire free packaging is highly desirable to achieve superior system performance, especially for MM-Wave Complementary Metal Oxide Semiconductor (CMOS) based systems design [26], which SoC method promises (Figure 1) along with other benefits. The antennas, which are essential part of a wireless SoC based system, are integrated on the same chip without a need of bond wires and called as "Antennas–on–Chip (AoCs)".

AoCs offer several advantages compared to their conventional off-chip counterparts. First, they eliminate the need of an impedance matching network between RF front-end and antenna since both can be co-designed in such a way that their impedances are conjugately matched [1], as shown in Figure 1. This practice not only leads to a significant reduction in the overall system's profile, but also results in a lower cost. Second, they avoid the need of lossy and unpredictable interconnects between the impedance matching network and antenna/RF front-end section; these interconnects cause a substantial decline in the system loss, especially at MM-Wave. Lesser loss means an improved Signal-to-Noise Ratio (SNR) of the system [27]. Third, they promise a high power-efficiency of the system because of the reduced dielectric losses and minimum reflection of the signal [28]. Fourth, they enable an easy and hassle-free integration of the system's components [15]. Fifth, they help in achieving a higher system bandwidth [29] as they introduce smaller parasitic losses because of the absence of the metal interconnects. Sixth, they make the design cycle of the wireless system shorter [30] since they enable a co-design approach of the antenna and

RF front-end section, thus ensuring a significant reduction in the design steps of the wireless system.

The AoC implementation in MM-Wave frequency bands (30 GHz – 300 GHz) which have got distinctive consideration recently [21], [23], [31] are very well-suited because of two major reasons. First, the antenna size is compact at these frequencies because of the smaller form-factor [21]. Second, Si based CMOS technologies, the preferred choice for AoC design, haves proved their potential for MM-Wave applications with the innovative developments [15], [20], [21], [23], [32] and transition frequency (f_t) and unity-power-gain frequency (f_{max}) of Si based transistors have now surpassed 300 GHz. Several MM-Wave frequency bands find their use in a plethora of different valuable applications. The unlicensed 60 GHz band, for example, can be used for Wireless personal area network, (WPAN), radiometry, radio astronomy, broadband radio communication [14], [17], [32]–[35] and short range wireless communications with high data rates and frequency reuse benefits [36], [37]. MM-Wave radars are gaining importance in numerous applications like industrial, automotive, remote control sensing, material characterization, imaging, and security systems [22], [29], [38]. In D-band (110 GHz – 170 GHz), the radar sensors and wireless communication are attractive applications [39]. A MM-Wave chip-to-chip communication [40] such as clock distribution for microprocessors is another such application.

Furthermore, another favorable band for AoC is Terahertz (THz) region which is gaining popularity for various applications such as astronomy, high data rate wireless communication, short range radar systems imaging, quality control, airport security, skin cancer detection, and wireless networking for smart homes [41]–[43]. Latest advancements in the cut-off frequency of low-cost CMOS technology have also made its use possible for THz region applications [41], [42], [44]. The significance of AoCs has been vastly enhanced with the emergence of a variety of the state-of-the-art applications. Some most prominent applications include: the MM-Wave transceivers for multiple-input-multiple-output (MIMO) based 5G wireless systems (e.g. Figure 1 which shows a simplistic view of this), IoT wireless devices and systems, wireless sensor network nodes, biomedical implants, RF energy harvesting, wireless power transfer, smart city, wearable devices, autonomous automobiles, unmanned aerial vehicles, as explained in [45]. Small satellite based wireless systems is another emerging application in this regard [46]. The miniaturization, low-cost, low-loss, and low-power dissipation are the fundamental requirements for the success of all these applications. However, one of the biggest obstacles in the way of AoCs' use for these applications is the performance issues of AoCs. AoCs exhibit a degraded performance, i.e. gain and radiation efficiency in comparison with the off-chip antennas because of the reasons stated in the following paragraph.

CMOS has achieved the status of the mainstream IC technology for MM-Wave and THz wireless SoC applications and is preferred due to its low-cost, low-power, and better
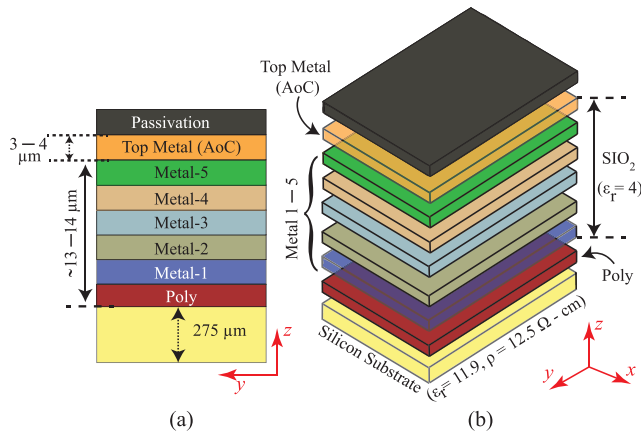
FIGURE 2. Typical six metal layers CMOS chip environment over the silicon substrate (a) Cross sectional view and (b) 3-D representation.
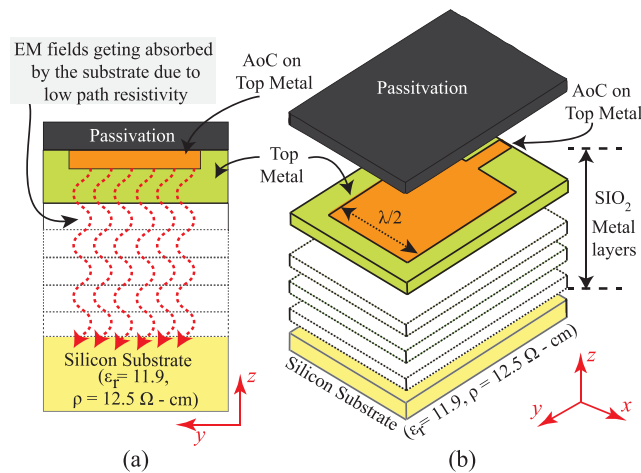

FIGURE 3. Impact of low resistivity and high permittivity of Si based technologies substrate on AoC performance; (a) cross sectional view, (b) 3-D view: low resistivity causes a large proportion of AoC radiations to get absorbed into Si substrate, thus degrading the radiation efficiency of AoC.

high-frequency performance based benefits [2], [20]–[23], [31], [32], [34], [41], [44], [47] along with the BiCMOS technology [23], [38]. Moreover, Si based technologies have got remarkable improvements in terms of f_t and f_{max} values as a result of tremendous scaling and their f_{max} has now reached 570 GHz [48]. Optimized for the other components of the SoC based wireless systems, these technologies are not favorable for AoC design because of the values of the permittivity and resistivity of their substrates. Typical commercial CMOS technology substrate has high permittivity ($\varepsilon_r \approx 11.7$) and low resistivity (10 Ω-cm) [1], [2], [14], [15], [17], [18], [21], [22], [24], [29], [30], [32], [34], [36], [37], [41]. These values are beneficial for wireless ICs in several ways. For instance, they prevent the latch up problem in ICs [1], [27]. However, these values are not suitable for a high performance AoC design. A clear understanding of this can be seen in Figure 2 and 3. As seen in Figures 2 and 3, the thickest metal (top metal) of a standard CMOS process is most often utilized

for AoC implementation. Due to small distance (≈ 16 μm) between the top metal and Si substrate and low resistivity of Si substrate, AoC radiations/ElectroMagnetic (EM) waves find a low resistive path through the substrate and a major percentage of these EM waves gets lost in it (Figure 3). The result is lesser EM radiations into the air, causing a drastic degradation in AoC's performance (gain and efficiency). In contrary, these values are suitable for other components of wireless transceiver such as High-Power Amplifier (HPA) since a high performance HPA needs a substrate which prevents the signal to get radiated outside the substrate as less as possible. So, an opposite set of performance criteria for the antenna and other components of transceiver system in terms of Si substrate properties is the major challenge. Moreover, high permittivity of Si substrate espouses surface waves and high back radiations which severally degrade AoC's radiation efficiency [1], [2], [14], [15], [17], [19], [49], as shown in Figure 3 (a). Hence, these values degrade the gain, directivity, and radiation efficiency (i.e. performance) of AoC and thus make CMOS substrate a lossy one for AoC design [1], [2], [14], [15], [17], [20]–[22], [24], [25], [29], [31], [32], [35], [42], [47]. This, thus, dictates the need for innovative performance- issues-mitigation-techniques for AoCs.

In order to overcome the AoCs performance issues, various performance-issues-mitigation-methods have been proposed and successfully applied to AoCs. A very brief description of few of these methods is part of several research articles on AoCs as a literature review component. However, this discussion is constrained because of a variety of factors. First, the discussion is often in a specific context and lacks the critical review aspect of these methods. Second, a large majority of these articles are focused on a specific performance-issues-mitigation-method. Third, the discussion is not profound and only intended to give a short outline of few of the methods. Therefore, existing discussion of performance issue in AoC and their mitigation do not lead to the fruitful results for the researchers. Fourth, the existing discussion does not provide a comparative analysis of different existing methods. Fifth, the description of the method is generally not organized and well-structured so that relevant researchers can take advantage to set the design goals while designing high performance AoC. Sixth, these articles are void of the detail of the various improved versions of the already existing methods. Finally, several novel methods have been introduced in the recent literature, which need to be described for the benefit of the researchers. This, therefore, triggers a dire need of presenting a critical review of all of these innovative methods at one place in order to enable the relevant researchers and readers to not only grasp and apply these methods, but also inspire them to come up with the state-of-the-art performance enhancement methods in future. Keeping these dynamics in mind and a gap in the literature, this article presents a systematic and coherent survey of the recent developments with respect to the AoCs performance-issues- mitigation-techniques in RF, MM-Wave, and THz regions.
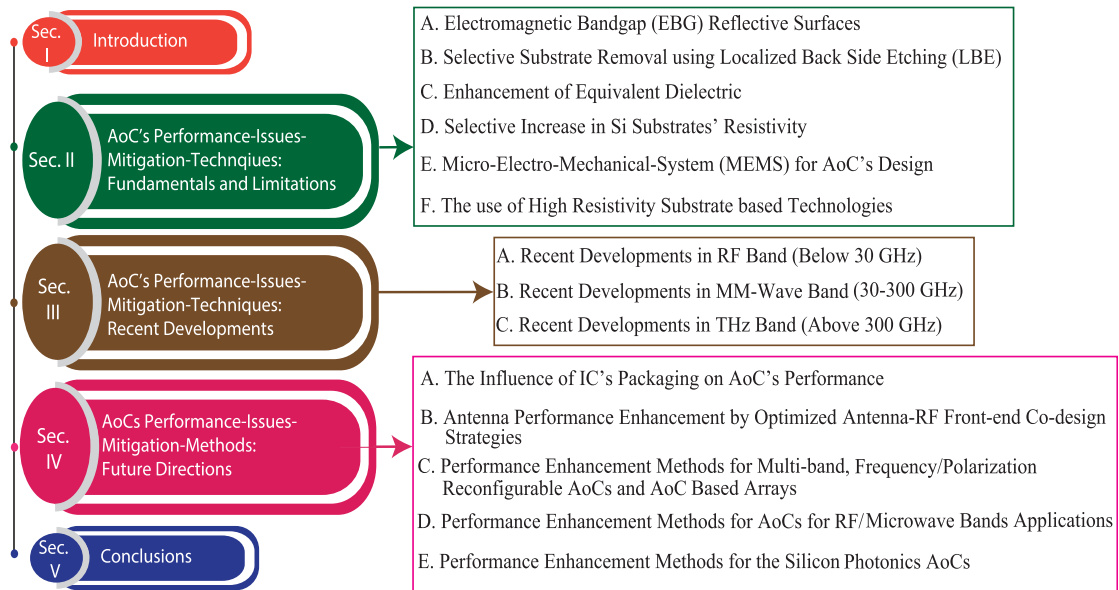
A. Electromagnetic Bandgap (EBG) Reflective Surfaces

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Sec. II — AoC's Performance-Issues-Mitigation-Technqiues: Fundamentals and Limitations

Sec. III — AoC's Performance-Issues-Mitigation-Techniques: Recent Developments

Sec. IV — AoCs Performance-Issues-Mitigation-Methods: Future Directions

Sec. V — Conclusions

FIGURE 4. Graphical representation of this article's outline.

This article is organized as follows: Section II delineates the fundamentals and limitations of some widely used methods for the mitigation of AoCs performance issues. Section III describes the recently proposed solutions of the challenges and issues associated with the AoC's performance, i.e. AoC performance-issues-mitigation-techniques in RF, MM-Wave, and THz bands. A brief discussion about few future directions with respect to the AoCs performance-issues-mitigation-techniques is part of section IV. This article is summarized with the conclusion section. To facilitate the reader for a smooth and easy follow-up of this article, a graphical outline is also provided in Figure 4, which also depicts the major contributions resulting from this article.

II. AoC's PERFORMANCE-ISSUES-MITIGATION: FUNDAMENTALS AND LIMITATIONS OF SOME WIDELY USED TECHNIQUES

The literature survey shows several methods which have been utilized widely for the mitigation of AoCs performance issues, especially in the recent years. In particular, it has been observed from the literature review that some methods have been extensively utilized in this regard. It is essential, therefore, to provide a concise overview of such methods in order to familiarize the readers with their fundamentals and associated limitations before actually presenting the recent developments in performance-issues-mitigation-methods for AoCs. This section endeavors to do the same and describes the above-mentioned concepts in a concise and effective way. After comprehending the basics and limitations of these widely utilized methods with the help of this section, the readers will be in a better position to follow the section III of this article, which critically presents the recent developments in AoC performance enhancement methods. This way, this section sets up a platform for the section III.

A. ELECTROMAGNETIC BANDGAP (EBG) REFLECTIVE SURFACES

Planar metamaterials, having subwavelength thickness, provide spatial variations in electromagnetic (EM) wave with scattering phases, amplitudes, and polarizations. These metamaterials, also referred as artificial engineered materials, considerably suppress unavoidable losses in EM structures. Another similar terminology, 'Electromagnetic Band Gap (EBG)' has also become popular in the research community. The use of EBGs or metamaterials for performance enhancement of AoCs is one of the most attractive choices. The EBG surfaces generally consist of metallic-dielectric array of periodic structures and symbolize an artificially realized material. The EBG surfaces, when introduced in a design, have the ability to suppress surface waves and produce bandstop or bandgap transmission and reflection characteristics at a particular frequency band [50]. Because of this property, they can be introduced in a lossy Si material to modify its transmission and reflection characteristics and to improve the gain and radiation efficiency of the AoC. Some other metamaterials providing prevention/assistance in the propagation of EM wave in a specific frequency band are: artificial magnetic conductors, high impedance surfaces, frequency selective surfaces, partially reflective surfaces, and negative refractive index materials. These artificial objects are usually classified under the broad terminology of EBGs. The brief detail of each category with respect to their use for AoC performance issues mitigation is provided below.

1) ARTIFICIAL MAGNETIC CONDUCTORS (AMCs)/HIGH IMPEDANCE SURFACES (HIS)

This is one of the most widespread and ancient technique [14], which is especially used in broadside AoCs in

order to increase their radiation efficiency [17]. The concept is illustrated in Figure 5, which shows that this technique inhibits the signal/EM field entering the substrate using the AMC between antenna and Si substrate. This AMC acts as a High Impedance Surface (HIS) for the incident wave coming from the antenna towards the substrate. This incident wave gets in phase wave reflection from the incorporated AMC and results in a constructive interference between incident and reflected wave. Consequently, an increased EM field into the air boosts AoC performance.
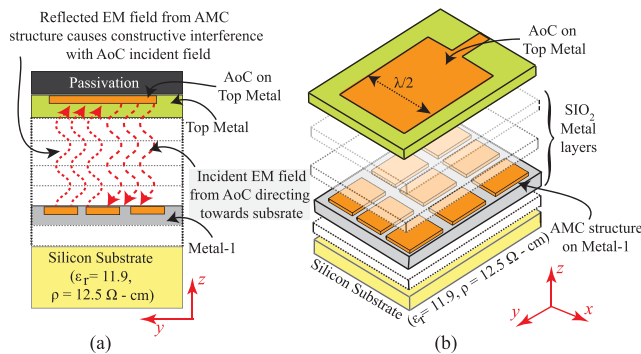

FIGURE 5. Illustration of the periodic AMC utilization for AoC performance enhancement: (a) a cross-sectional view showing the formation of constructive interference because of the AMC in AoC, and (b) 3-D view; AMC structure is implemented on metal 1 layer of the process technology in majority of the practical designs; however, its placement may be optimized as per AoC orientation to get in phase reflection.

The incorporation of periodic AMC structures provides enhanced performance in AOCs; however, careful study of AMC inspired AOCs revealed few limitations of these structures. For example, AMCs add some extra chip area [34], [51] which increases overall system cost [52] and hardware complexity. In addition, some power is still lost in the Si substrate since the ground plane of the AMC is usually designed underneath the Si substrate [30]. Also, MM-Wave based systems (specially 5G) needs wideband antennas, however the metamaterials such as AMC and HIS are narrow band in nature. Furthermore, AMCs based AoCs with ground plane underneath the Si substrate needs post-processing, which results in additional cost and increased design complexity.

2) FREQUENCY SELECTIVE SURFACES (FSS) AND PARTIALLY REFLECTIVE SURFACES (PRS)

Similar to the AMC, the FSS has the capability to control the transmission and reflection characteristics of the incident EM waves [18] if positioned between AoC and Si substrate. However, this method also has some limitations. The main disadvantage is its large area consumption. Moreover, AoC's performance may deteriorate due to small distance between different layers of modern Si processes [18] despite FSS incorporation. One possible solution of the issues associated with the FSS can be the incorporation of the partially reflecting surface (PRS) between AoC and Si substrate, which is another similar technique like AMCs.

In standard CMOS processes, the lowest metal acts an isolator between the antenna and lossy Si substrate, which results in antenna radiation performance boost. However, presence of a small gap between the metal plane and the antenna results in a small antenna radiation resistance and thus reduced gain. To solve this issue and enhance the antenna gain, the PRS is usually placed between the antenna and lossy Si substrate. Unlike AMC and FSS, PSR can be designed in such a way that it handles the amount of the reflected power, as well as decides the resonance frequency of the antenna [18]. In addition, PSR ensures a modestly lower reflection of the antenna's incident waves compared to AMC and FSS, which means a little percentage of the incident waves are still absorbed by the substrate.

B. SELECTIVE SUBSTRATE REMOVAL USING LOCALIZED BACK SIDE ETCHING (LBE)

To avoid system cost and power lost issues in AoCs and improve its radiation efficiency, one effective way is to locally remove the lossy Si substrate around the AoC using a post-processing method [19], [21], [53]. This method is called as 'Micromachining or LBE'. The concept is shown in Figure 6, where area under the AoC in the Si substrate is etched using the LBE process to suppress losses created by the Si substrate.
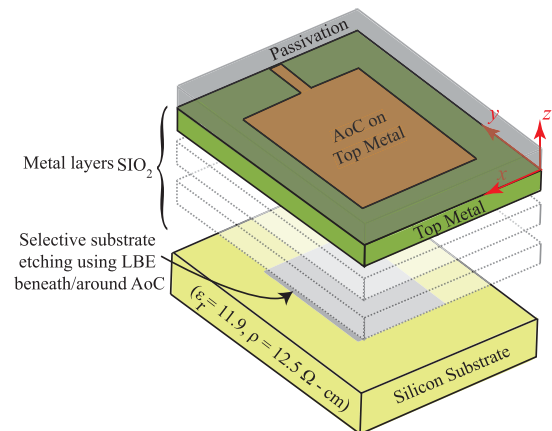

FIGURE 6. The use of micromachined LBE concept for efficiency enhancement of AoC; 3-D view. Si substrate beneath and around the AoC has been removed, thus mitigating the effect of lossy Si substrate.

This method, like others, does have its own disadvantages, which include extra assembly efforts and mechanical instability of the backend process [19], resulting in complex fabrication and degraded flexibility in antenna design [54]. Moreover, an increased cost and reduced system level integration are other limitations [14], [17], [36] due to post-processing requirements [47], [53], [55]. In addition, this process is incompatible with the majority of standard CMOS processes [34], who do not have an in-built support for LBE.

C. ENHANCEMENT OF EQUIVALENT DIELECTRIC

The radiation efficiency of the AoC can also be enhanced by either adding or increasing the equivalent dielectric of lossy

Si substrate and three famous methods practically employed. A brief detail of these is given below.

1) LENS INTEGRATED ANTENNA (LIA)

Originating from [56], LIA is the oldest performance enhancement technique for AoCs performance issues mitigation. Here, a Si lens is placed beneath the lossy Si substrate [18], [34] to add the dielectric. After manufacturing, Si lens is glued with the IC containing the AoC with the help of an electrically insulating adhesive material, as shown in Figure 7. The thickness of electrically insulating adhesive material may affect overall electrical properties of the design. However, with the use of an adhesive thinner than Si chip and lens, this affect can be made insignificant [57]. This is validated by using a 5 μm thick adhesive in [57] and less than 10 μm in [19], which has minimized this affect. Also, the placement/configuration of lens needs special care depending on the application [57]. Furthermore, LIA's gain is directly proportional to the lens size [19], [57]. As an added benefit, LIA also provides reasonably high bandwidth [57]. In general, on-chip LIA provides high efficiency–bandwidth product compared to other such methods [19].
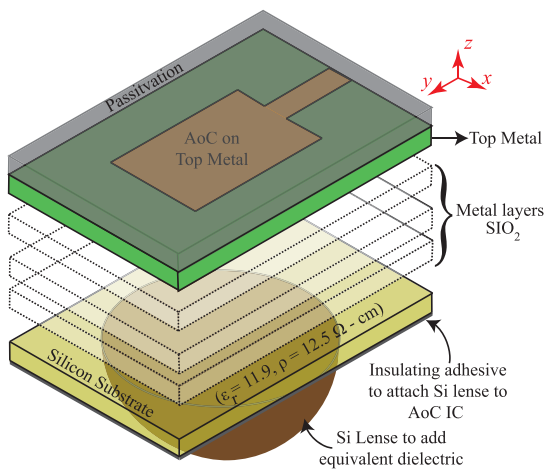

FIGURE 7. A 3D view of Si lens application for performance enhancement of an AoC. The Si lens adds the permittivity of the Si substrate, which in turn mitigates the loss and enhances AoC efficiency.

The LIA method has several disadvantages. First, this is not part of the standard CMOS processes [34]. Second, this method needs post-processing which not only increases the cost, but also makes this technique a hybrid version of the AoC and the Antenna-in-Package [18]. Third, the lens itself is also costly and often needs special mounting mechanisms [55].

2) DIELECTRIC RESONATOR ANTENNA (DRA)

DRA is a another practiced AoC gain enhancement technique [18], [58]. In order to increase the equivalent dielectric, a DRA made up of a low-loss dielectric material is placed above the Si substrate with an appropriate feeding structure with the help of an epoxy glue material, as shown in Figure 8.
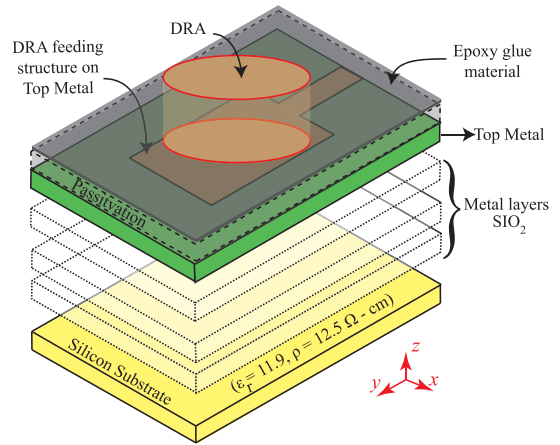

FIGURE 8. Representation of DRA employment for AoC performance issues mitigation; 3-D view. Only one DRA has been used here; a vertical stack of DRAs are generally used for this purpose. DRA generally consists of a low loss material. Here, cylindrical DRA has been utilized; other shapes such as rectangular and cubic can also be used. The feeding of the DRA which has been done by a patch here can also be done from other methods, i.e. diploe, etc.

The excitation of appropriate modes in DRA and absence of surface waves along with the metallic losses are major reason for performance enhancement in the AoCs. The advantages of DRA include compactness, wide bandwidth, and lower conductive loss [59]. However, the DRA integration is incompatible with modern CMOS processes [58]. Therefore, this incompatibility increases fabrication complexity significantly and develops mechanical instability issues.

3) ARTIFICIAL DIELECTRIC SUPERSTRATE (ADS)

The third such technique is ADS. An Artificial Dielectric (AD) is a high permittivity material which, if inserted in a host material, can enhance the equivalent permittivity of that material. A 3D view of ADS insertion on host material is depicted in Figure 9. The EM waves radiate efficiently
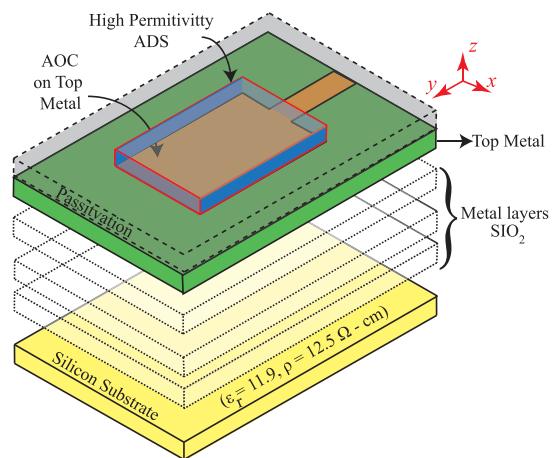

FIGURE 9. The use of ADS for AoC performance enhancement; 3-D view, high permittivity ADS enhances the equivalent dielectric constant of the low permittivity Si substrate, which in turns increases the radiation efficiency of AoC.

from the ADS based AoCs due to the enhanced equivalent permittivity. The use of multiple Artificial Dielectric Layers (ADLs) as a superstrate is more beneficial in this regard, but with an increased chip area. ADLs generally consist of periodic metallic structures, which are non-resonant [60]. Figure 10 shows ADLs, where periodic structures are embedded in a host dielectric. The ADLs arrangement results in a medium, which stimulates a homogenous anisotropic substrate [60]. The use of ADLs for AoC performance enhancement is shown in Figure 11. The main advantage offered by ADLs superstrate compared to a real dielectrics superstrate is that it does not permit surface waves [61] and enhances overall gain of the AoC along with the miniaturization. However, ADLs, being not part of the standard Si processes [55], restricts their practical employability in the AoCs.
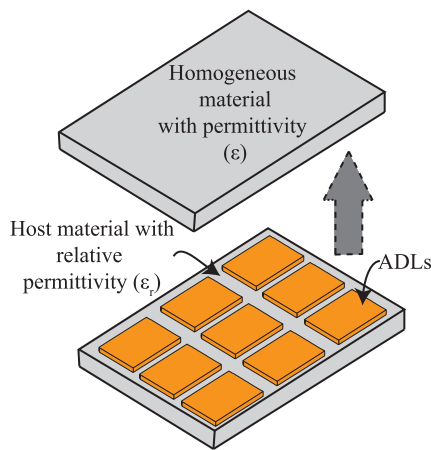

FIGURE 10. ADLs embedded in a medium with relative permittivity (ε_r) to get an equivalent homogeneous medium.
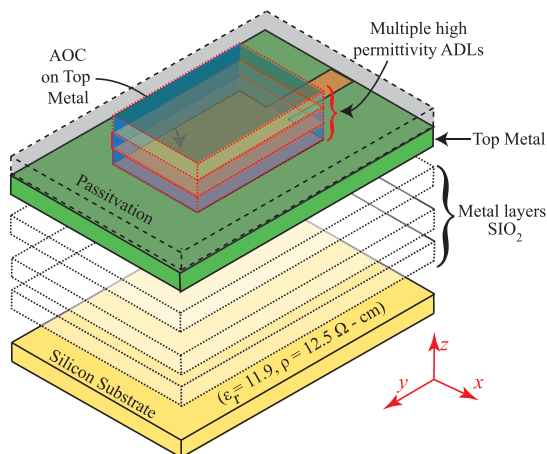

FIGURE 11. AoC performance enhancement by ADLs; 3-D view. Here, symmetric ADL structures with high permittivity have been used above the AoC.

D. SELECTIVE INCREASE IN SI SUBSTRATES' RESISTIVITY

As described in section II, low resistivity in Si based technologies is one of the main reasons for AoC's poor performance.

If somehow, the resistivity of the Si substrate can be increased or alternatively conductivity can be decreased in the vicinity of the AoC, its performance will get boosted. Helium-3 Ion Irradiation and Proton Implantation are the conventionally practiced methods used for increasing resistivity in Si substrates. These methods are discussed briefly as follows:

1) HELIUM -3 ION IRRADIATION

In Helium -3 Ion Irradiation, a portion of low resistivity Si substrate near the AoC is irradiated with the help of Helium -3 Ion technique. This irradiation increases overall resistivity of Si substrate and hence, enhances AoC's radiation efficiency. The concept of this irradiation technique is briefly depicted in Figure 12. Like other methods, this method also has some disadvantages. These include higher cost because of the need of special irradiation process and relatively less immunity to the loss due to the surface channels. However, the irradiation of only selective area makes these issues less severe for this application.
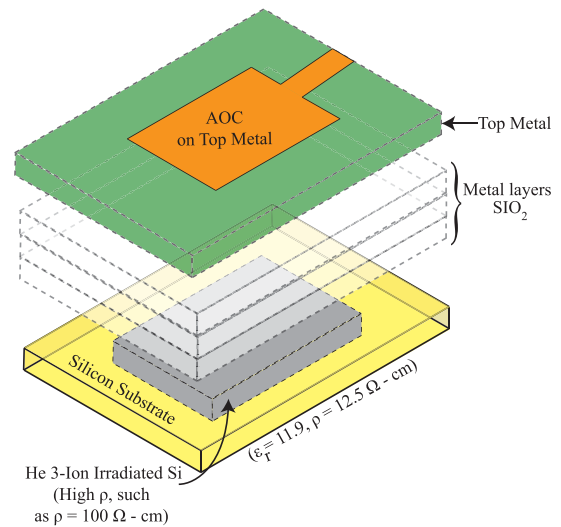

FIGURE 12. Helium 3-ion irradiation based AoC; 3-D view. A rectangular region of low resistivity Si substrate in close vicinity of AoC has been irradiated with the help of Helium 3-ion irradiation method and hence enhanced EM waves radiate into air from AoC because of the mitigation of the loss associated with low resistivity Si substrate.

2) PROTON IMPLANTATION

Like Helium -3 Ion Irradiation method, proton implantation can also enhance AoC's efficiency by increasing the resistivity of Si substrate [14], [17], [34], [36], [62]. A high dose of high energy protons is implanted in the desired area to change substrate doping profile for increasing its resistivity in selective antenna area. High cost and lower systems integration are key issues associated with this technique [14], [17], [36]. These issues arise due to its incompatibility with the standard CMOS processes [34]. In addition, the need for high dose amount ($> 10^{15}\ cm^2$) for proton implantation [51] is another major reason for high cost. Therefore, this method has very limited use for AoC's performance enhancement applications.

E. MICRO-ELECTRO-MECHANICAL-SYSTEM (MEMS) FOR AoC's DESIGN

MEMS is an emerging choice for an efficient AoC design. Apart from the efficiency, antennas inspired from MEMS are low-cost, can be easily fabricated [64], and can provide nanometer level precision. Thus, they are considered highly promising [64] for AoC system design. Moreover, with the help of the Focused Ion Beam (FIB) process, which is a part of recently developed MEMS technology, 3D antennas can be fabricated, as evident from [64] in which fabrication of 3-D helical antennas are made possible. However, the major challenges associated with MEMS are stiction and reliability as described in [65], [66]. To abate these issues, a detailed failure analysis is essential which can enable proposing suitable mitigation methods for stiction and reliability of MEMS [66], [67].

F. USE OF HIGH RESISTIVITY SUBSTRATE BASED TECHNOLOGIES

A popular method to get high performance AoCs is to use high resistivity substrate-based technologies instead of standard low resistivity Si substrate-based technologies. Although, the use of high resistivity substrate-based technologies enhances the AoC performance significantly, it offers other limitations and drawbacks. Substrate-on-Insulator (SOI) CMOS technology falls in this category, which has attracted a substantial attention for the design of AoC in recent days. The resistivity of SOI CMOS substrate is significantly higher than bulk CMOS or SiGe BiCMOS substrate, which results in high efficiency AoCs. However, SOI CMOS is costly than bulk CMOS. In addition, SOI CMOS does not mitigate substrate surface waves generation [58], which is a key factor for the AoC performance degradation, especially at MM-Wave. Another popular technology, which is being utilized for AoC performance enhancement is Si substrate Glass Integrated Passive Device (GIPD), whose glass substrate offers high resistivity silicon substrate (loss tangent = 0.0005, $\varepsilon_r = 11.9$, $\rho > 3$ kΩ-cm) and low-cost [63]. The configuration of Si substrate based GIPD technology is shown in Figure 13. The AoC designed in this technology can be integrated with the active circuits designed using 180 nm and 90 nm CMOS processes with a possibility of other processes in the future. However, low integration level with respect to standard Si based technologies is a major issue associated with this technology.
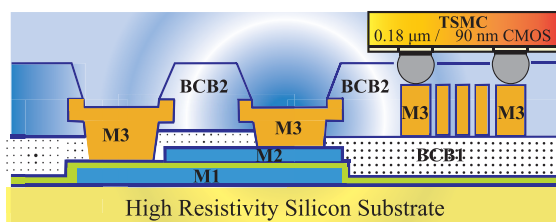

FIGURE 13. High resistivity Si substrate based GIPD technology: Configuration [63].

Magnesium oxide (MgO) is another high resistivity substrate-based technology, which have found application in AoCs design more recently [68], [69]. Although the use of MgO provides a high performance AoC, but it is less attractive than standard low resistivity Si based technologies when it comes to high integration level and low cost. In addition, it is more useful for wireless applications which involves large temperature variations because of its stable performance over a wide temperature range. Indium Phosphide (InP) [70] is yet another technology, which is utilized to get highly efficient AoCs because of its high resistivity-based substrate. InP technology facilitates substrate thinning [71], which is also an effective way of increasing AoC performance. Moreover, InP technology mitigates the substrate modes because of its low dielectric loss tangent [72]. Furthermore, it is favorable for high speed wireless communication based AoCs at MM-Wave because of its higher transition and maximum oscillation frequencies [71]. Low integration level is major drawback of InP substrate in comparison with standard Si based technologies.

III. AoC's PERFORMANCE-ISSUES-MITIGATION-TECHNIQUES: RECENT DEVELOPMENTS

Several methods to mitigate AoCs performance issues have been proposed in recent years. This section endeavours to showcase the most recent advancements in this regard with the aim of a critical evaluation of each method. The recent advancements in the AoCs performance-issues-mitigation-methods have been divided into three categories: RF, MM-Wave, and THz bands. The detail of recent developments in each category is provided below:

A. RECENT DEVELOPMENTS IN RF BAND (Below 30 GHz)

1) USE OF MINIATURIZED FSS TO ACT AS A METASURFACE SUPERSTRATE FOR AoC

In [73], a compact FSS structure based cover, consisting of an AMC and a PRS, has been designed and placed over the 10 GHz AoC chip. The designed FSS structure based cover acts as a metasurafce superstrate for the AoC. The outcome is the enhanced performance of CMOS process based AoC with a 9 dBi rise in the gain. The proposed approach is attractive because its potential can be increased with a rise in the number of elements of the PSR used in the FSS structure-based cover, which permits achieving a more bandwidth besides gain enhancement. In addition, this method is more promising at MM-Wave and THz bands, where a large number of PSR elements can be added without a fear of significant increase in AoC dimensions, resulting in a substantial surge in the gain and bandwidth of the AoC.

2) USE OF HIGH-RESISTIVITY FERRITE LAYER BETWEEN AoC AND SiO$_2$ LAYER

In [74], the authors have proposed a miniaturized AoC at 0.915 GHz for biomedical applications with an innovative performance enhancement method. The authors have utilized

a thin film of CoZrO material-based ferrite between the radiating layer and SiO_2 layer. The ferrite material is characterized by high resistivity ($\approx 10^4$ Ω-cm), which limits the penetration of antenna EM waves into lossy substrate. In addition, the CoZrO material exhibits frequency dependent magnetic properties and low-quality factor, acting as reactive elements for the top metal and substrate. The interaction of these reactive elements with the reactive elements of substrate and top metal results in a reduction in reactive losses. This method has provided an enhancement of $\approx$ 10.5 dBi in gain and 32 % in radiation efficiency of the antenna. The use of the same method in [75] for a slotted patch AoC using 180 nm CMOS process has resulted a 12.28 dBi raise in the gain and 22 % increase in the radiation efficiency.

3) HYBRID APPROACH FOR THE DESIGN AND INTEGRATION OF ANTENNA

An innovative hybrid design and integration methodology for highly efficient AoCs has been presented in [76] for 27.5 GHz – 29.5 GHz band. The selected structure for the antenna is stacked patch backed by a cavity and it has been implemented using air-filled substrate integrated waveguide (SIW) technology. The hybrid approach makes use of both, on-chip and off-chip structures for the design and integration of antenna. The antenna feeding network and metal based air-filled cavity have been designed on-chip, while stacked patch has been designed off-chip on Rogers RO4350B PCB material supporting the chip. As per measured results, the AoC exhibits a peak gain of 7.3 dBi at 28.5 GHz and radiation efficiency of more than 90 % in the whole band. Other advantages of the proposed technique include smaller chip-area because of stacked patch geometry, and mitigation of the electromagnetic interference issues between the antenna and RF front-end because of the achievement of the high isolation between both by metallizing the air-filled cavity.

4) USE OF SYMMETRICAL LAYERS FOR MULTIPATH INTERFERENCE MITIGATION IN AoC BASED INTER-CHIP WIRELESS COMMUNICATION

In [77], the authors have proposed a method to mitigate the multipath interference issue for wireless inter-chip communication by introducing symmetrical layers in the vicinity of transmitting and receiving AoCs, which results in a significant increase in the transmission gain ($|S_{21}|$). In inter-chip wireless communication, it is known that the level of transmitted signal is reduced at the receiver side because of the destructive interference at the receiver side owing to the multipath transmission of signal from transmitter to receiver. The authors, knowing that the medium of signal propagation can be managed on the chip during the design phase, have introduced symmetrical silicon layers which sandwich the transmitting and receiving AoCs. Because of the symmetrical silicon layers, the AoCs radiate symmetrically and multipath destructive interference issue is mitigated. The concept of signal transmission in unsymmetrical vs. the

proposed symmetrical layers is shown in Figure 14. The use of these symmetrical layers for two 18 GHz linear dipole AoCs, placed 2 cm apart at low-resistivity Si substrate, cancels the effect of multipath interference, which is depicted in form of 10 dB enhancement in transmission gain ($|S_{21}|$) in comparison with signal transfer using unsymmetrical layers.
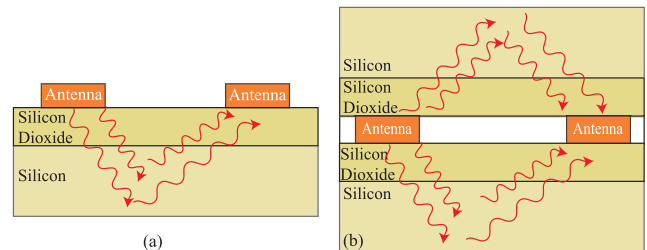

FIGURE 14. The signal transfer in unsymmetrical vs. proposed symmetrical layers for inter-chip wireless communication with the help of AoCs [77]. (a) Unsymmetrical layer structure and (b) Symmetrical layer structure.

5) USE OF SOI CMOS TECHNOLOGY

In [78], the authors have design a dipole AoC using 180 nm SOI CMOS process (conductivity ≥ 0.1 S/m), which achieves a maximum radiation efficiency of 28 % at 17 GHz and a peak gain of 2.2 dBi at 10 GHz without the use of any AoC performance enhancement method. Because of the low conductivity of the SOI substrate, the performance of AoC is not deteriorated significantly in comparison with the standard CMOS processes. The designed AoC resulted in the development of a novel, battery-less, mm-sized dielectric sensor with wireless power capability. The miniaturization of the sensor has been enabled by the transmitting and receiving AoCs.

In [79], ultra-low-loss trap-rich RF-SOI wafers ($\rho > 3000$) have been proposed for the design of highly efficient AoC in ultrawide band (6 GHz – 10 GHz). To validate the usefulness of the proposed technology, monopole antennas are designed using the proposed RF-SOI wafers ($\rho > 3000$), bulk silicon ($\rho = 10$-20) wafer, and high resistivity silicon ($\rho > 4000$) wafers. The results shows that RF-SOI wafers based AoC achieves better performance in terms of RF losses than other antennas. The effectiveness of the technology is further verified by demonstrating 6.2 GHz wireless communication with the help of proposed technology based two AoCs, placed apart at a distance of 1 m as well as 2 m. The transmission gains ($|S_{21}|$) of -33.2 dB and -40.8 dB have been reported at 1 m and 2 m, respectively.

6) USE OF VERTICAL CAVITY

In [49], a vertical cavity is etched at the bottom of the Si substrate for a monopole with two-tier structure patch AoC to boost its gain in Ultra Wide Band. The antenna is implemented in high dielectric constant Si material; it is compatible with MEMS technology fabrication processes, and delivers peak gain from 1.73 dBi to 5.12 dBi.

TABLE 1. Recent developments in AoCs performance-issues-mitigation-techniques at RF bands (below 30 GHz).

Ref.	Performance-Issues-Mitigation-Method	Antenna Type	Freq. (GHz)	Technology	Dimensions	Peak Gain (dBi) / Incr. in Gain (dBi)	$\eta_{rad}(\%)$ / Inc. in $\eta_{rad}(\%)$
[73]	Miniaturized FSS cover to act as metasurface superstrate	Patch	10	CMOS	96×96 mm^2	14.14 / 9	NR / NR
[81]	High resistivity substrate	Monopole	24	High resistivity substrate ($\rho \geq$ 8 kΩ-cm, $\varepsilon_r =$ 11.8, thickness = 675 μm	$3.8 \times 4 \times 0.676$ mm^3	−3 / NR	NR / NR
[74]	High resistivity Ferrite loading	Spiral like shape	0.915	Silicon	15×15.4 mm^2	−33.5 / 10.5	86 / 32
[76]	Hybrid integration (on-chip and off-chip antenna structure)	Cavity backed stacked patch	28.5	SIW	$0.49 \lambda_{min} \times 0.49 \lambda_{min}$	7.3 / NR	90.9 / NR
[75]	Thin CoZrO ferrite metal layer b/w AoC and SIO$_2$	Slot	0.915	180 nm CMOS	$15 \times 15.4 \times 0.306$ mm^3	NR / 12.28	86 / 22
[78]	SOI CMOS	Dipole	9.8	180 nm SOI CMOS	NR	2.2 / NR	28 / NR
[79]	Trap-rich high-resistivity SOI	Monopole	6	RF SOI	NR	NR / NR	NR / NR
[49]	Cavity at back of substrate	Monopole with two-tier structure patch	3.14 − 12.4	Si Substrate	$16 \times 25 \times 0.4$ mm^3	1.73 − 5.12 / NR	NR / NR
[80]	Partial shield layer between AoC and substrate	Meandered loop	11	Low − ρ Si Wafer	12×2 mm^2	−29.2 / 4	NR / NR

7) USE OF PARTIAL SHIELD LAYER BETWEEN AoC AND LOSSY SI SUBSTRATE

In [80], the authors have utilized a partial shield Aluminium layer between an 11 GHz compact meandered loop AoC and lossy Si substrate to enhance performance. The partial shield layer acts similar as an AMC and protects the migration of AoC EM field towards substrate. Consequently, AoC gain is enhanced by 4 dBi. This is one of those AoCs which make use of both, the antenna miniaturization method and performance enhancement method – a necessity for antennas at RF band.

Table 1 presents a summary of the recent developments in AoCs performance-issues-mitigation-techniques. Various observations can be made from Table 1. First, the number of AoCs with performance enhancement methods in RF bands (upto 30 GHz) is very low. One possible reason is that RF AoCs also need employment of innovative antenna miniaturization methods besides performance enhancement methods in comparison with MM-Wave and THz band AoCs, thus making the challenge two-folds. Table 1 also shows one AoC which utilizes both the methods, i.e. meandering as antenna miniaturization method and partial shield layer as performance boost method. Second, the maximum enhancement of the gain in this band, resulting by applying AoCs performance issues methods, is 12.28 dBi. This gain rise has been provided by the use of thin CoZrO ferrite metal layer between AoC and SIO$_2$ as a performance-issues-mitigation-method to a 0.915 GHz AoC. However, AoC's peak gain achieved after applying this method is not reported. Third, 32 % is the

maximum rise in the radiation efficiency of the AoC after applying high-resistivity Ferrite loading as performance-issues-mitigation-method. Fourth, SIW and high-resistivity substrate technologies have also been utilized for the design of AoCs in this band besides Si-based technologies. Fifth, the minimum and maximum frequencies for which performance enhancement methods have been employed in this band are 0.915 GHz and 28.5 GHz, respectively. Sixth, unlike MM-Wave and THz bands, the use of famous methods that are responsible for performance enhancement, i.e. methods described in section II of this article is rare. The possible reasons of this trend include large antenna size and fabrication complexity at RF frequencies with application of popular performance enhancement methods. Seventh, no dual-band AoC with a performance enhancement method is reported in RF band. Given the fact that the demand of high performance dual-band RF AoCs has grown recently because of a few state-of-the-art applications such as wireless power and data transfer, EM energy harvesting, the use of novel performance-issues-mitigation-techniques for such AoCs is the need of the hour.

B. RECENT DEVELOPMENTS IN MM-WAVE BAND (30-300 GHz)

1) USE OF ELECTROMAGNETIC BAND-GAP REFLECTIVE SURFACES

(a) **Symmetric vs. Asymmetric AMCs:** Usually, symmetric AMCs are utilized for the performance boost of

AoCs. However, the authors in [14] have demonstrated that the use of the asymmetric AMC offers better performance enhancement as compared to conventional symmetric AMC since the asymmetric AMC shows lower insertion loss than symmetric AMC, when used as a ground plane for a feeding circuit. The reason behind a better performance of the asymmetric AMC is its ability to solve the discontinuity issue - an issue inherently present in symmetric AMC. To validate this concept, the authors simulated a 50 Ω microstrip line of same dimensions with both, symmetric and asymmetric AMC as a ground plane. As per simulation results, the insertion loss of asymmetric AMC is 2 dB/mm lesser than the symmetric AMC. In addition, the authors have verified this by simulating a 60 GHz triangular AoC with both, symmetric and asymmetric AMC, which shows that the gain and radiation efficiency of asymmetric AMC based AoC is better than symmetric AMC based AoC across entire band of interest (57 GHz – 64 GHz). At 60 GHz, the gain of asymmetric AMC based AoC is 2 dBi more than symmetric AMC, while $\approx$ 20 % rise in the radiation efficiency is observed. Based on these verifications, the authors used the asymmetric AMC for the design and fabrication of a 60 GHz circular AoC using 180 nm CMOS process, which produces radiation efficiency, gain, and front-to-back ratio (FBR) of 49 %, 0.25 dBi, and 12.8 dB, respectively. The authors in [82] have also utilized asymmetric AMC for a V-band polarization reconfigurable AoC design using 180 nm CMOS process and achieved 1 dBi increase in the gain and 10 % rise in the radiation efficiency. Several other AMCs-based AoCs at MM-Wave are reported in recent literature whose detail can be seen in Table 2.

(b) **Thin Metasurface to act as a radiator without a need of post-processing:** Inspired by the AMC-based AoCs, several new variants have been proposed by the authors in recent literature which mitigate the limitations associated with AMC-based solutions. One of them is metasurface-based AoCs. In [2], the authors have proposed a novel metasurface-based AoC at 94 GHz using 6 metal-layers 180 nm SiGe BiCMOS process. Instead of placing AMC at the lowest metal, i.e. metal 1 and ground plane below the AoC as is done in a majority of the AMC-based AoCs, the authors have placed the ground plane at metal 1 and designed an extremely thin dogbone-shaped metasurface by patterned metal 5, metal 6, and vias in between without placing any antenna/radiator. The metasurface is designed in such a way that it acts as a radiator itself instead acting as a reflector or high-impedance surface, thus mitigating the need for any other radiating element in contrary to other AMC-based AoCs. The ground plane at metal 1 acts as a shield for the EM waves coming towards the Si substrate. The antenna, without a need of post-processing, achieves a peak gain of −2.5 dBi and an impedance bandwidth of more than 10 GHz.

(c) **FSS without a need of post-processing:** The use of the FSS can provide significant gain improvement as explained in section II of this article. In a majority of FSS-based AoCs, the ground plane is placed beneath the Si substrate. As a result, a small percentage of antenna EM waves is still dissipated into Si substrate. In addition, it requires post-processing. Both limitations can be solved with the proposal of an FSS structure without any ground plane beneath the Si substrate. The authors in [30] have proposed such a method for a 94 GHz bow-tie slot AoC using 7 metal-layers 130 nm SiGe BiCMOS process. The AoC is modelled on the top metal, while an E-shaped FSS structure is designed on metal 1. A gain enhancement of 0.79 dBi has been achieved without the use of any ground plane.

(d) **PRS-antenna co-design approach:** Like FSS, the use of PRS boosts the AoC performance substantially. The use of PRS becomes more effective if PRS-AoC co-design methodology exists, which could ensure achieving an optimized performance as well as chip-area for the antenna. In [18], such a co-design approach has been proposed for the design of a V-band triangular monopole AoC using 130 nm SiGe BiCMOS process with 7 metal-layers. The AoC is realized on the top metal. The unit cell of PSR is constructed by 2 floating dipole arrays, i.e. array 1 and array 2. Dipole array 1 makes use of metal layer 4 and 5; two adjacent identical geometries on metal layer 4 and 5 are connected through vias. Dipole layer 2, having same geometry as array 1 except a minor modification, is realized by connecting metal layer 1, 2, and 3 through vias. The PSR dimensions are optimized in order to get high performance and smaller chip-area. The co-design approach results in a 90 % reflection of the incident EM waves (i.e. the waves coming from the AoC towards Si substrate). The proposed methodology provides radiation efficiency and gain boost of 17 % and 1.98 dBi, respectively with an overall chip-area of 0.868 mm^2 including Ground-Signal-Ground pads.

2) USE OF LOCALIZED BACK SIDE ETCHING (LBE)

(a) **Built-in-support for LBE in few commercial SiGe BiCMOS Processes:** The removal of Si substrate using LBE method for AoC performance enhancement has gained popularity recently since few commercially available standard SiGe BiCMOS processes, such as IHP's 130 nm SiGe BiCMOS, have now provided built in support for LBE. In [21], a D-band Micromachined end-fire quasi yagi-udda antenna was design using 130 nm SiGe BiCMOS process having commercially built in LBE support. The antenna obtains a good gain of 4.7 dBi and radiation efficiency of 72 – 76 %. Moreover, the good reliability of AoC was confirmed by successful post-processing of LBE process and repeatable measured results, with and without guard rings. Because of these advantages, it is justified to say that the end-fire

TABLE 2. Recent developments in AoCs performance-issues-mitigation-techniques at MM-Wave bands (30-300 GHz).

Ref.	Performance-Issues-Mitigation-Method	Antenna Type	Freq. (GHz)	Technology	Chip Size	Peak Gain (dBi) / Incr. in Gain (dBi)	$\eta_{rad}(\%)$ / Inc. in $\eta_{rad}(\%)$
[14]	Asymmetric AMC	Circular Patch	60	180 nm CMOS	1.22 mm^2	–0.25 / 1	49 / NR
[82]	Asymmetric AMC	Polarization reconfigurable Dipole	V-band (55-75)	180 nm CMOS	NR	NR / 1	NR / 10
[2]	Metasurface	Leaky wave	94	180 nm SiGe BiCMOS	2.6 mm^2	–2.5 / NR	NR / NR
[30]	FSS	Bowtie slot	94	130 nm SiGe BiCMOS	0.066 mm^3	–1.94 / 0.79	NR / NR
[22]	Selective removal of Si substrate using LBE	double folded dipole	122	130 nm SiGe BiCMOS	NR	6 / NR	54 / NR
[21]	LBE	Quasi yagi-udda	135 − 165	130 nm SiGe BiCMOS	4 mm^2	3.5 − 5.1 / NR	72 − 76 / NR
[84]	Selective removal of Si substrate using LBE	folded dipole	120	130 nm SiGe BiCMOS	NR	3 − 5 / NR	NR / NR
[114]	Selective removal of Si substrate using LBE	Dipole	77	SiGe BiCMOS	NR	4.1 / NR	NR / NR
[83]	Post-processed Si substrate to act as a pseudo lens	Stacked Open slot	180	130 nm SiGe BiCMOS	NR	2.8 / 1	NR / NR
[44]	Si hemispherical lens	Annular slot	240	130 nm SiGe BiCMOS	NR	NR / NR	52 − 42 / NR
[38]	Si hemispherical lens	Dipole	110 − 140	SiGe BiCMOS	NR	1.8 − 4 / NR	NR / NR
[69]	Si hemispherical lens	gold thin film	160, 640	(MgO) substrate	NR	9.7 / NR and 19.9 / NR	NR / NR
[87]	Periodic hemispherical lenses	Monopole	60	BiCMOS	NR	1 / NR	65 / 20
[88]	spherical DRA	Microstrip	69	Benzocyclobutene substrate	NR	8.4 / NR	72 / NR
[39]	DRA	waveguide horn	140 (130 − 150)	130 nm CMOS	NR	18.9 / NR	45 / NR
[89]	Micromachined cylindrical DRA	CPW structure	60	high resistivity silicon	NR	7 / NR	79.35 / NR
[90]	rectangular DRA	slot	24, 40	65 nm bulk CMOS	2.5 × 2.5 × 2.5 mm^3	–1 / 8, 0 / 9	41 / NR, 31 / NR
[115]	cylindrical DRA	Microstrip resonator	80	NR	NR	NR / NR	65 / NR
[52]	ADS with permittivity near to Si	Yagi-udda	94	Si process (Thickness = 600 μm)	NR	0.4 / NR	67 / NR
[95]	quartz ADS	dipole	108 − 114	180 nm SiGe BiCMOS	0.136 mm^2	2.7 / NR	45 / NR
[96]	ADLs	slot	60	CMOS	NR	3.6 / 6.2	32.5 / 18.5
[20]	Helium -3 Ion Irradiation	Dipole	60	CMOS	NR	2.7 / NR	48 / 43
[24]	Helium -3 Ion Irradiation with a vertical reflector	Folded Dipole	140	40 nm CMOS	NR	–2.7 / NR	NR / NR
[97]	Proton Implantation	Cylindrical DRA	60	180 nm CMOS	NR	–1.1 / NR	22.6 / NR
[27]	MEMS	Monopole	50 − 67	CMOS compatible Polymer MEMS fabrication process	NR	–2.5 / NR	NR / NR
[98]	MEMS	Leaky wave	60	Si compatible MEMS fabrication process	NR	12.2 / NR	90 / NR
[99]	Elevation of AoC array from lossy Si-substrate using MEMS	5 × 5 array	60	Si compatible MEMS fabrication process	156.25 mm^2	19.7 / NR	BW = 2 GHz
[36]	asymmetric AMC + MNZ-MM lens	Circular	60	CMOS	NR	2.8 / 3.3	35 / 9
[17]	planar arc reflector + etching of equal corrugations	Tapered slot Vivaldi	60	180 nm CMOS	0.785 × 0.93 mm^2	–0.4 / 4.4	32 / NR
[54]	appropriate Si thickness + process provided loaded dielectric	Quasi Yagi-Udda	140	130 nm SiGe BiCMOS	0.9 × 0.7 mm^2 (without supported structure)	4.1 / NR	83 / NR

TABLE 2. *(Continued.)* Recent developments in AoCs performance-issues-mitigation-techniques at MM-Wave bands (30-300 GHz).

[109]	Cavity in PCB package + optimized PCB interconnects	Monopole	60	BiCMOS Qubic4X	NR	2 / NR	45 / NR
[100]	AMC + superstrate	Monopole	77	180 nm CMOS	NR	2.4 / 9.1	54.37 / 22.1
[101]	three rectangular slits + arc reflector + circular metal-strips to act as an additional director	Tapered slot Vivaldi	60	180 nm CMOS	0.7×0.940 mm^2	−1.9 / 2.25	24 / 7.5
[116]	Quartz substrate	Microstrip	91.5 − 98.5	SiGe BiCMOS	NR	0.7 − 3.9 / NR	48 / NR
[108]	DRA + Half-mode Cavity based feeding	DRA	135	CMOS	0.7×0.9 mm^2	3.7 / NR	62 / NR
[117]	AMC	Quasi-Yagi	60	180 nm CMOS	$2.45 \times 1.8 \times 0.3$ mm^3	−2.64 / NR	16.8 / NR
[118]	LBE	Slot	70 − 110	250 nm SiGe BiCMOS	NR	0 / NR	64 / 29
[119]	AMC	2×2 Monopole array	60	90 nm CMOS	3.1×3.8 mm^2	−5 / 4	15 / 9
[51]	Helium-3 Ion Irradiation	Dipole	60	65 nm CMOS	0.48 mm^2	−4.1 / 3	59 / 33
[102]	High resistivity substrate + DRA + off-chip PCB ground	Loop	67	180 nm high resistivity CMOS (ρ = 1000 Ω-cm)	0.7×1.25 mm^2	7.8 / NR	96.7 / NR
[24]	Vertical metallic reflector + Helium -3 Ion Irradiation	Folded dipole	140	40 nm CMOS	7.5×7.5 mm^2	−2.7 / 5	NR / NR
[105]	SOI CMOS + Off-chip reflector	Frequency reconfigurable	29.5 − 51	180 nm SOI CMOS	1.1×1.7 mm^2	2.2 / NR	NR / NR
[91]	DRA for 2 × 1 array	Half-mode cavity	130	Standard CMOS	NR	6.3 / NR, 7 / NR	NR / NR
[91]	DRA for 4 × 1 array	Half-mode cavity	130	Standard CMOS	NR	7 / NR, 8.2 / NR	NR / NR
[120]	Dual polarized spherical DRA	Microstrip loop	105	Benzocyclobutene (BCB) dielectric (h = 24 μm, ε_r = 2.55	NR	9 / NR	80 / NR
[63]	High resistivity substrate based GIPD	Log periodic dipole	94	GIPD	NR	4 / NR	90 / NR
[121]	AMC	Monopole	77	180 nm CMOS	NR	1.7 / 8.4	42.52 / 27.51
[92]	DRA for on-chip feeding of RCA	Resonant cavity antenna (RCA)	V-band	NR	NR	17.8 / 10	70 / NR
[92]	DRA for on-chip feeding of RCA	Resonant cavity antenna (RCA)	W-band	NR	NR	18.4 / 10.8	70 / NR
[86]	Selective removal of Si substrate using LBE	Folded Dipole	165	130 nm SiGe BiCMOS	1.88 mm^2	5 / NR	65 / NR
[86]	Selective removal of Si substrate using LBE	Patch	165	130 nm SiGe BiCMOS	1 mm^2	6 / NR	> 70 / NR
[122]	Selective removal of Si substrate using LBE	Differential Patch	160	130 nm SiGe BiCMOS	NR	7 / NR	60 / NR
[123]	SOI CMOS	Loop	68	45 nm SOI CMOS	NR	3.7 / NR	83 / NR
[123]	SOI CMOS	Slot	68	45 nm SOI CMOS	NR	3.8 / 2.83	85 / 39
[123]	SOI CMOS	Dipole	68	45 nm SOI CMOS	NR	3.9 / 2.83	88 / NR
[103]	Dielectric Superstrate + parasitic substrate	DRA	60	High resistivity Si (ρ = 2000 Ω-cm)	NR	12.4 / 3.9	81.6 / 2
[104]	AMC + superstrate + Fresnel lens	Monopole	77	180 nm CMOS	1.5×1.5 mm^2	8.3 / 22.10	NR / NR
[124]	AMC	Patch monopole	60	180 nm CMOS	0.9×2.1 mm^2	1.53 / 1.16	48 / 12
[125]	AMC	Triangular Monopole	38	28 nm CMOS	0.95×4.75 mm^2	−1.75 / 5.15	22 / 15.70
[126]	AMC	Double-layer dipole	235	65 nm CMOS	250×410 mm^2	0 / 1	63 / NR

TABLE 2. *(Continued.)* Recent developments in AoCs performance-issues-mitigation-techniques at MM-Wave bands (30-300 GHz).

Ref	Technique	Antenna	Freq	Process	Size	G/BW	Eff
[33]	AMC	Loop with cut gap	60	180 nm CMOS	1.5 × 1.5 × 0.3 mm³	−3.2 / 1.1	**NR / NR**
[37]	AMC	Patch with 2 parasitic elements	60	180 nm CMOS	1.65 × 1.63 mm²	0.12 / NR	NR / NR
[127]	AMC	Dipole	94	SiGe BiCMOS	NR	4.8 / 15.8	NR / NR
[128]	AMC	Folded monopole	60	CMOS	3 mm²	4.87 / 3.6	58.11 / 18.24
[129]	AMC	Planar monopole	220	180 nm CMOS	NR	9.8 / NR	NR / NR
[18]	PRS	Triangular Monopole	60	130 nm SiGe BiCMOS	1.1 × 0.78 mm²	1.42 / 1.98	41 / 17
[85]	Selective removal of Si substrate using LBE	Folded dipole	120	130 nm SiGe BiCMOS	NR	3 − 5 / NR	NR / NR
[97]	Cylindrical DRA	Microstrip line feed	60	180 nm CMOS	NR	−1.10 / NR	22.6 / NR
[34]	2 AoCs based MIMO structure with common ground plane	Monopole and IFA	60	65 nm CMOS	0.70 × 0.35 mm²	−3.8 / NR, −6.1 / NR	NR / NR, NR / NR
[110]	Slots radiators on ground plane	Patch	60	90 nm CMOS	0.8 × 0.8 mm²	−1.1 / NR	65 / NR
[111]	Metal tiles to act as AMC	Monopole	60	Si process with 6 metal layers	NR	NR / 3.3	21 / 10
[112]	Ground metals on PCB to act as a reflector	V-shaped patch	33	28 nm digital CMOS	0.66 × 0.85 mm²	2.24 / 9.8	44 / 37.3
[54]	optimized Si thickness and process provided loaded dielectric	Yagi-Udda	140	130 nm SiGe BiCMOS	0.9 × 0.75 mm²	4.1 / NR	83 / NR
[54]	optimized Si thickness and process provided loaded dielectric	1 × 2 array of Yagi-Udda	140	130 nm SiGe BiCMOS	2 × 0.85 mm²	7 / NR	72 / NR
[93]	High order DRA	CPW patch with backside cavity	270	0.1 μm GaAs	NR	6.4 / 4	75 / 22
[60]	ADS + High resistivity substrate	Double slot	300	High resistivity silicon	NR	3.9 / 2	NR / NR
[61]	ADS	Dipole	280	Si process	NR	6.8 / NR	87 / 51
[68]	High resistivity substrate + Hemispherical lens	2-elements ring slot array	300	MgO + High resistivity substrate	NR	13.5 / NR	NR / NR
[106]	High resistivity NTN layer	Flipped zero-order	60	180 nm CMOS with NTN	1.175 × 1.375 mm²	−10.6 / 1.1	NR / NR
[106]	High resistivity NTN layer + metallic walls around AoC	Flipped zero-order	60	180 nm CMOS with NTN	1.475 × 0.875 mm²	−9.6 / 2.6	NR / NR
[107]	High-resistivity substrate	Slots on ground supply plane of SoC	60	High-resistivity substrate (ρ = 7 kΩ-cm)	NR	NR / NR	92 / NR
[107]	Si substrate thinning upto 17.5 μm	Slots on ground supply plane of SoC	60	Thin Si substrate	NR	NR / NR	61 / NR
[58]	Low permittivity locally formed Si substrate	Dipole	49.2	Locally formed Si substrate on a standard Si substrate	NR	−13 / 11	NR / NR
[113]	Inkjet Printing as a post-processing for CMOS chip	Monopole	24	180 nm CMOS with inkjet printing	NR	NR / NR	NR / NR
[130]	Dual-mode DRA	H slot feeding	120	55 nm CMOS	NR	6 / NR	58 / NR
[130]	Dual-mode DRA	H slot feeding	120	55 nm CMOS	NR	6.9 / NR	60 / NR
[131]	Hemispherical Lens	Leaky slot	250	130 nm SiGe BiCMOS	NR	16.9 / NR	NR / NR

AoC at MM-Wave can be designed using standard commercially available BiCMOS process with built in LBE support, which can show performance comparable to off-chip antennas.

(b) **Methods to mitigate chip mechanical instability issue of LBE:** Recently, one useful method has been proposed which mitigates the instability issue associated with the LBE-based AoCs. In [22], the authors proposed a solution of this issue for the design of two double-folded dipole antennas for a 122 GHz radar sensor using an innovative selective LBE method. To ensure stability of the AoCs, only a small portion of lossy Si substrate around the antennas was removed using LBE instead of eradicating all the substrate. However, a small decrease in the gain and bandwidth of AoCs was noticed as a result of selective removal of substrate in comparison with the full substrate removal. A good gain of 6 dBi and radiation efficiency of 54 % were achieved, thus proving the efficacy of this solution. The same selective LBE technique was also utilized in [84] and [85] in order to solve mechanical instability issue, where 120 GHz double-folded AoC provides a good peak gain of 3 – 5 dBi using 130 nm SiGe BiCMOS process. Likewise, the selective removal of Si substrate using LBE for two D-band AoCs, implemented using 130 nm SiGe BiCMOS process, has also been employed in [86]. Consequently, a folded dipole AoC achieves a peak gain of 5 dBi and radiation efficiency of 45 %, while the patch AoC obtains a peak gain of 6 dBi and radiation efficiency of above 60 %. In all above-mentioned methods, the AoC is realized by the top metal and ground plane is on the bottom metal.

3) METHODS RELATED TO ENHANCEMENT OF EQUIVALENT DIELECTRIC OF ANTENNA SUBSTRATE

(a) **The use of Lens**

(i) **Post-processed Si substrate to act as a pseudo lens:** A lens is glued beneath the AoC (called as LIA) as a post-processing step in order to enhance its performance as described in section II of this article. However, to achieve high gain and bandwidth simultaneously is one of the major constraints of this method. In [83], the authors have proposed a novel method to solve this issue for a 180 GHz stacked open-slot AoC using 130 nm SiGe BiCMOS process. Instead of using a lens as a post-processing step after fabrication, the Si substrate was post-processed in such a way that it acts itself as a reflector or pseudo lens, i.e. the Si substrate directly radiates the energy. The concept is shown in Figure 15 to highlight the difference of the direction of main beam between the conventional LIA and the proposed method. The gain enhancement of 1 dBi and relative bandwidth rise of around 3 % was obtained compared to the same antenna designed with the conventional lens. This method can alleviate
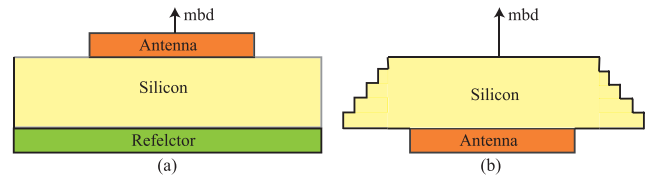

FIGURE 15. The difference of main beam direction (mbd) between (a) traditional LIA and (b) novel pseudo-lens structure [83] (a) with reflector and (b) without reflector. Here, lens is written as a reflector as it reflects the energy.

the other disadvantages associated with LIA such as the cost of the lens and its mounting setup.

(ii) **The use of Si hemispherical lens for dual-band AoC:** Si hemispherical lens is the mostly used lens type for AoC performance enhancement applications. The authors have utilized a high resistivity (ε_r = 11.9) Si hemispherical lens, attached to the back side of the 0.5 mm thick Magnesium Oxide (MgO) substrate, for the performance enhancement of a gold thin-film based dual-band AoC in [69]. The dual-band operation was achieved using well-designed twin slots and optimized matching characteristics were obtained with the help of a well-matched coplanar waveguide-based network. The AoC operates at 160 GHz and 640 GHz with a gain of 9.7 dBi at 160 GHz and 19.9 dBi at 640 GHz. The excellent coupling features of designed AoC, achieved using lens, have enabled the development of a state-of-the-art high temperature coefficient superconducting based 4th harmonic mixer for sub-THz wireless and sensing applications. This is the only dual-band AoC, which operates in MM-Wave as well as in THz band. Few other recent examples of the use of hemispherical lens for MM-Wave AoC performance enhancement can be found in Table 2.

(iii) **The use of periodic hemispherical lenses on top of the IC package to change its effective permittivity:** In [87], the authors have proposed an innovative approach of enhancing the beam-width and radiation efficiency of a 60 GHz single chip FMCW radar based AoCs without effecting their gain. The method makes use of the fact that a change in the dielectric characteristics of the package material, which protects the radar IC, results in variations of surface field distributions of the radar IC. These changes in field distributions on the surface of radar IC can be exploited to vary the far-field radiation characteristics and thus enhance the beam-width and radiation efficiency of the AoCs. In order to change the dielectric characteristics of the epoxy material of the radar IC package, the authors have designed novel periodic hemispherical lens structures, which are placed on top of the epoxy cover of the already designed radar chip integrated with transmitting and receiving AoCs. The outcome is 20 % and 8 % rise in the

radiation efficiency of transmitter AoC and receiver AoC respectively, and 60 % raise in the 3-dB beam-width. The fabrication of periodic lenses, however, is a challenging task since periodic lenses need a special mold for the expxy of radar IC. In addition, the top of these lenses should be flat to facilitate straightforward picking and placement of the radar chip.

(b) **The use of DRAs**

(i) **The use of DRA with accurate alignment and test-ing characteristics:** The DRAs for the use of per-formance enhancement of AoCs face a few issues. Some of these issues include: DRAs accurate posi-tioning with respect to the excitation body, DRAs large size, and an inability of the active circuits to be tested before DRAs are mounted. The solution of these issues has been proposed in [88] at 69 GHz with the help of a novel spherical DRA. The excita-tion has been done by a miniaturized half-wavelength microstrip resonator circuit, which is constructed in a 24 μm thick benzocyclobutene layer on top of a low-resistivity silicon substrate. To ensure an accu-rate alignment of the proposed spherical DRA with respect to the microstrip feed, a square crate is etched, with a high lateral accuracy, into benzocyclobutene layer near the microstrip feed. As a result, the DR sphere falls into this crate after gluing and self-aligns itself. As a shunt resonant circuit is formed by microstrip feed from line to ground and this resonant circuit exhibits a high impedance without the sphere, the microstrip feed can be designed in such a manner that it formulates a 50 Ω coplanar Ground-Signal-Ground probe pads. These pads can be utilized for the on-wafer testing of circuits before the placement of the spherical DR. Besides above-mentioned advan-tages, the proposed spherical DRA achieves a good gain of 8.4 dBi and radiation efficiency of 72 %.

(ii) **The use of DRA for chip-to-waveguide horn antenna to achieve high gain:** In [39], the authors have proposed a novel method to boost the gain of CMOS-based antennas. The solution is based on the observation that the gain of an AoC is enhanced significantly if it is first transitioned to waveg-uide which then acts as a feed for the radiating horn antenna. The proposed antenna geometry con-sists of an on-chip substrate-integrated-waveguide cavity-based DRA, a chip-to-waveguide transition, and a horn antenna. First, an on-chip antenna, backed by substrate-integrated-waveguide cavity, with a rect-angular radiation patch is designed using 130 nm CMOS process. This on-chip antenna feeds the DRA operating at TE_{110}^{δ} mode. DRA, made up of Al_2O_3 with dielectric constant of 9.8, is glued to on-chip antenna with the help of an epoxy material. DRA, then, excites the dominant mode (TE_{10}) of the rect-angular waveguide and transfers the power efficiently.

Rectangular waveguide feeds the horn antenna, which radiates the power into the air. The proposed approach provides radiation efficiency of 45 % and a good gain of 18.9 dBi.

(iii) **The use of DRA which is made-up of the same material as of the feeding circuit material:** In a majority of DRAs designed for performance enhance-ment of Si-based AoCs, the material of the DRA is not the same as of its feeding circuit. This results in a hybrid integration, which offers several issues such as large chip-area, misalignment of DRA with the feed-ing circuit, high cost, high probability of mechanical instability of the chip, etc. The design in [89] has proposed a 60 GHz on-chip micromachined cylin-drical DRA using high-resistivity ($\rho = 2000 \ \Omega$-cm) silicon process which uses same material for both, the feeding circuit and DRA. To make the design cost-effective and simpler, the DRA is fed by a copla-nar waveguide. In addition, the feeding structure is at the back side of the Si substrate in order to enable the construction of DRA and feeding structure on a single Si wafer. The micromachining fabrication process is utilized for the fabrication of the proposed antenna on double-sides high-resistivity Si wafers. One side of the wafer is etched up-to a depth of 400 μm with the help of a deep reactive ion etching process, while the backside is un-etched to act as a substrate for the feeding structure. The feeding structure is realized, first by performing copper-coating of the backside and then patterning the copper using dry etching. The antenna achieves good performance with a gain of 7 dBi and radiation efficiency of 79.35 %.

(iv) **The use of DRA for a dual-band AoC:** The use of DRA for the performance enhancement of multi-band AoCs has not been very common. In [90], a rect-angular DRA has been used for the performance enhancement of a dual-band coplanar waveguide fed rectangular slot AoC using 65 nm CMOS pro-cess which operates at 24 GHz and 40 GHz. First, the coplanar waveguide fed on-chip antenna is pro-posed which is comprised of two concentric ring slots. These slots enable dual-band operation. To enhance the performance, the slot AoC is loaded with a rect-angular DRA of a high dielectric constant $\varepsilon_r = 9.6$. The field of dual-band slot antenna is coupled with the DRA mode in a concentrated configuration. The use of DRA increases the peak gain of slot antenna by 8 dBi at 24 GHz and 9 dBi at 240 GHz.

(v) **The use of DRA arrays:** The use of DRA arrays can provide more performance enhancement for AoC than single DRA element. However, the use of DRA arrays for this purpose is rare yet. Recently one method has been proposed in [91] for a 130 GHz AoC using standard CMOS process, where 2×1 and 4×1 DRA arrays have been proposed. The feeding of both the arrays, in the dominant and higher order modes, has

been done with a half-mode cavity using a Wilkinson divider arrangement without the balanced resistor. 2×1 array achieves a peak gain of 6.3 dBi if backed by a $TE_{\delta 11}$ DR and 7 dBi if backed by $TE_{\delta 13}$ DR. Similarly, 4×1 array achieves a peak gain of 7 dBi if backed by a $TE_{\delta 11}$ DR and 8.2 dBi if backed by $TE_{\delta 13}$ DR. The comparison of 2×1 DRA array based AoC with the single element DRA based AoC shows a 2.5 dBi more gain in the array based AoC than the single element based AoC.

(vi) **The use of DRA for on-chip feeding of the resonant cavity antennas:** To get high directivity, large bandwidth, excellent performance, straightforward antenna assembly, and miniaturization simultaneously for MM-Wave AoCs is a tough task. In [92], the authors have proposed an innovative method to solve this challenge for one V-band and one W-band resonant cavity AoC with the help of DRA. First, they have selected resonant cavity antennas for on-chip operation which are considered relatively high gain antennas for microwave and MM-Wave applications. The proposed resonant cavity antennas are comprised of a $\frac{\lambda_\circ}{2}$ resonant cavity, constructed between a partially reflective superstrate and a fully reflective ground plane. For both the antennas, the ground plane is realized by the lowest metallic layer of the layer stack, while partially reflective superstrate is constructed with Rogers TMM10i dielectric material. Second, these resonant cavity antennas are fed on-chip by a self-aligned spherical DRA made up of low-cost alumina material. The self-alignment of the DRA is ensured by etching a shallow crate directly on-chip. The results show a gain enhancement of 10 dBi for V-band and 11 dBi for W-band AoC using this approach.

(vii) **The use of high order mode excited DRA:** In [93], the authors have proposed a 270 GHz DRA using 0.1 μm GaAs process which is excited at high order mode instead of its fundamental mode. The use of high order mode excitation makes the DRA easily fabricated, low-cost, and mechanically stable when compared to fundamental mode excitation DRA. To feed the DRA, a cavity based coplanar waveguide patch is designed using GaAs substrate. The cavity, occupied by several back vias, is created at back side of the substrate to force the EM radiations towards upside direction. The high order mode excited DRA enhances the gain by 4 dBi, radiation efficiency by 22 %, and 3-dB bandwidth by 17 %.

(viii) **Exploiting silicon substrate to act as a DRA:** The authors in [94] have proposed an innovative on-chip radiating method for CMOS circuits at MM-Wave and THz. The new radiating method is based on the observation that the silicon dies at higher frequencies (> 200 GHz) can be excited to resonate like a DRA.

The metal patterns such as loop shaped patterns, instead of acting as antenna, can be utilized to excite the silicon die. Once the loop-shaped metallic patterns are fed by the power, it induces an electromagnetic field inside the silicon die. As a result, the silicon die resonates from the front side of the chip. The resonance mode of the silicon die depends on its size. The proposed method offers advantages such as lower chip-area, absence of chip-to-PCB-to-DRA interface and related misalignment issues, low-cost, and less complex design as compared to conventional DRA based AoCs. The authors have demonstrated this method at 280 GHz using 65 nm CMOS process by designing 5×6 array for exciting the silicon die. The excitation array, with an aim of enhancing the radiated power from silicon die, has been realized with the help of injection locked voltage-controlled oscillators. The design radiator achieves a peak EIRP of 24.1 dBm with a chip-area of 2.1 mm^2.

(c) **The use of ADS and ADLs**

(i) **The use of an ADS whose permittivity value is near to Si substrate:** The authors in [52] have utilized an ADS for performance enhancement of a 94 GHz on-chip Yagi antenna using Si-based process (thickness of Si $= 600$ μm, $\rho = 10$ Ω-cm, $\varepsilon_r = 11.9$). Normally, ADS placed above the AoC increases the effective distance between the ground plane and the radiating body, which results in higher radiation efficiency of the AoC. However, the proposed alumina ADS ($\varepsilon_r = 9.8$, thickness $= 2$ μm, conductivity $= 5.8 \times 10^7$ S/m) functions differently because of the close value of its permittivity with the Si substrate permittivity. The use of this ADS results in a balanced EM energy coupling into Si substrate and ADS which recovers the EM radiations directions from backside to the end fire. Consequently, the radiation efficiency of AoC increases and its loss reduces. Results show that a good gain of 0.4 dBi and radiation efficiency of 67 % have been achieved for the proposed AoC.

(ii) **The EM-coupled AoC on quartz ADS wafer to enhance performance:** In [95], the authors have proposed a novel method to enhance 108 GHz – 114 GHz AoC performance using quartz ADS, which has been designed for a wafer-scale phased array transmitter using 180 nm SiGe BiCMOS process. Instead of designing the differential dipole AoC using 180 nm SiGe BiCMOS process and then placing quartz ADS on the top of it as usually is done, the authors have patterned the dipole antenna using 7000 A° sputtered gold on an additional quartz ADS wafer ($\varepsilon_r = 3.8$, thickness $= 100$ μm) and placed it on top of the phased array silicon chip with the help of an epoxy material at the edge of the chip. Ground plane of the antenna is realized using metal 5 and 6 and feeding

network is constructed on top metal layer. The radiating structure is EM-coupled from the feeding network on silicon chip, thus eliminating the need of a metal-via feed and reducing the packaging cost. The proposed AoC shows a good gain of 2.7 dBi and radiation efficiency of about 45 %.

(iii) **The use of ADLs to mitigate antenna back radiation and enable reuse of area below the AoC by digital ICs of SoC based systems:** Besides enhancing the performance of a 60 GHz CMOS based slot AoC, the authors in [96] have proposed a way to reuse the area below AoC with the help of ADLs. The area below the AoC, integrated with the RF and digital ICs, cannot be occupied by other ICs because of the strong EM field of AoC, which can disturb the performance of the other ICs. If the backside EM radiations of the AoC are reduced, the area below the antenna can be reused by other ICs, especially the digital ICs which are less prone to EM coupling as compared to analog and RF ICs. The authors have mitigated the backside EM field of the proposed AoC by placing ADLs on top of the antenna. This boosts the antenna gain by 3.6 dBi, and radiation efficiency by 18.5 %. In addition, it reduces the backside radiations of the AoC significantly, which is evidenced by a 10.8 dB increase in FBR of the antenna. The reduction of backside EM radiations of AoC enables reuse of the area below the AoC for digital ICs of the SoC, thus saving chip-area and cost of the system.

4) METHODS RELATED TO SELECTIVE INCREASE IN SI SUBSTRATE's RESISTIVITY

(a) **The use of proton implantation to enhance the transmission gain of an on-chip DRA for inter-chip wireless communication:** Normally, the proton implantation method is utilized to increase the performance of Si based AoCs which is then confirmed by measuring its gain, radiation efficiency, etc. In [97], however, the authors have applied proton implantation for the performance enhancement of a 180 nm CMOS based cylindrical DRA at 60 GHz by increasing the resistivity of silicon substrate from 10 Ω-cm to 100 Ω-cm and despite measuring AoC's gain and radiation efficiency to see the effect of substrate resistivity increase, they used the designed AoC for an inter-chip wireless communication to verify the efficacy of proton implantation. To perform inter-chip wireless communication, the chips are placed on the same silicon substrate at 4 mm apart. The comparison of the transmission gain of both the wireless inter-chip setups, i.e. the one using low-resistivity substrate based AoC and the other using high-resistivity substrate based AoC shows that the transmission gain is increased by 15 dB in H-plane and 14 dB in E-plane with proton implantation.

5) MEMS FABRICATION PROCESSES

(a) **CMOS-compatible MEMS and silicon micromachined fabrication processes based AoCs:** An inexpensive, novel and CMOS compatible Polymer MEMS fabrication process is proposed in [27] for self-assembled and high efficiency MM-Wave AoCs. The proposed polymer MEMS process mitigates the limiting factors (the high temperature and introduction of gold) of integrating MEMS fabrication technologies with CMOS fabrication technologies since it works on low temperature and prevents the diffusion of gold into the active areas of the CMOS wafers. For the fabrication of MEMS structures in the proposed method, SU-8 photoresist has been utilized because of its low-cost and easy fabrication steps-based advantages. In the proposed MEMS fabrication process, a 40 μm thick SU-8 layer has been utilized as a dielectric substrate for the antenna, while a 500 nm metal layer has been used for the ground and feeding structure. Fabrication steps of the process has been outlined. To verify the effectiveness of the process, a 50 GHz – 67 GHz monopole antenna with transmission line feed and ground plane is fabricated and characterized using this process, which achieves a peak gain of −2.5 dBi. To separate the antenna and the transmission line from lossy Si substrate, a very viscous SU-8 photoresist technique based thick dielectric substrate has been fabricated. The proposed cost-effective and CMOS-compatible process can be used for the design of MM-Wave AoCs on prototype as well as on commercial level.

Another modified Si-micromachined MEMS fabrication process has been introduced in [98], which offers almost zero dielectric loss to the design and fabrication of AoCs, thus enhancing their performance substantially. The proposed process is a modified version of traditional Si-micromachined processes, but facilitates the fabrication of air-filled structures by deep etching of the wafers using etching gas or liquid in contrary to conventional processes. Because of these air-filled structures, the energy can be radiated by the air-media instead of silicon, thus reducing the dielectric loss issue. The fabrication steps of the proposed method have been described. The usefulness of the proposed fabrication process has been validated by the design of two AoCs, one in MM-Wave band and other at THz band. A 60 GHz leaky wave AoC designed in this process provides a peak gain of 12.2 dBi and bandwidth of 8.2 GHz. The second AoC designed using this process operates at 222.3 GHz – 340 GHz, and achieves a peak gain of 10.6 dBi, radiation efficiency of more than 88 %, and bandwidth of 117.7 GHz. The results of both the AoCs substantiate the potential of the proposed process for high performance MM-Wave and THz AoCs.

(b) **Elevation of AoC array from lossy Si-substrate with the help of MEMS fabrication process:** In [99], the authors have proposed a novel method for the

performance enhancement of AoC-based array of 5 × 5 elements at 60 GHz with the help of MEMS fabrication process. In order to reduce the effective dielectric constant of Si substrate, the patch-based AoC arrays have been suspended 60 μm above the ground of Si substrate with the support of several vertical SU-8 photoresist MEMS polymers. The result is the creation of low effective dielectric constant for the AoC-based array, and hence improvement in the performance. The designed array exhibits a radiation efficiency of 80 %, peak realized gain of 19.7 dBi, and −10 dB impedance bandwidth of 2 GHz. Compatibility of this method with the Si processes makes it a good candidate for high performance AoC-based arrays for next generation wireless systems.

6) HYBRID METHODS

The most common trend in recent days is to use the combination of two or more gain enhancement techniques (hybrid methods) to get desired performance. Detail is provided below:

(a) **The use of optimized Si thickness, vertical reflector, and helium 3 ion irradiation:** In [24], the authors have utilized three performance enhancement methods for a 140 GHz dipole AoC using 40 nm CMOS process. First, the dipole antenna chip is placed on a metal plate at an optimized distance, which acts as a reflector for the AoC. The reflector enables AoC to achieve unidirectional radiation characteristics, thus resulting an increase in the gain. Second, the thickness of silicon substrate is chosen to be 250 μm with the help of full wave simulation results, which provides maximum gain of −8.7 dBi for the proposed dipole antenna. To enhance the antenna's gain further, the resistivity of silicon substrate is increased from 10 Ω-cm to 100 Ω-cm with the help of helium 3 ion irradiation process. This results in a 5 dBi rise in the antenna gain.

(b) **The use of asymmetric AMC and off-chip Mu near zero Meta material (MNZ-MM) lens:** In [36], the asymmetric AMC and off-chip Mu near zero Meta material (MNZ-MM) lens have been employed to compensate the limitations of the AMC and the LIA based AoC for the design of a 60 GHz CMOS AoC. Double split ring resonator has been optimized to act as a Mu near zero Meta material using Rogers RT/duriod 5880 material. Asymmetric AMC is placed on metal 6 along with circular AoC, except one cell which is placed in metal 1. This metal 1-layer cell acts as a ground plane for the feeding network. The Asymmetric AMC based circular AoC is placed with a 3 × 3 matrix of double split ring resonator in such an arrangement which ensures maximizing the coupling. The advantages of the proposed approach include 9 % increase in the radiation efficiency, 3.3 dBi enhancement in the gain, 4 GHz increase in |S$_{11}$| (dB) bandwidth, and 3.5 dB rise in FBR.

(c) **The use of reflector and etched corrugations on the antenna edges:** The authors have employed two techniques for the performance improvement of a 60 GHz endfire tapered-slot Vivaldi AoC in [17] using 180 nm CMOS process. First, a planar arc reflector has been used to the back of the antenna, which is constructed using metal vias between metal 6 and metal 1. This reflector mitigates the backside radiations and thus improves antenna gain and radiation efficiency. Second, on the edges of the flaring of the antenna, equal corrugations have been etched. Also, corrugations have been etched at the backed edge of the antenna. The corrugations enlarge the effective aperture area of the antenna and thus improve antenna gain. The excitation of the antenna is done using a double Y-shaped balun which enables transition from coplanar waveguide to slot-line. 1.2 dBi gain enhancement due to first method and 3.2 dBi due to second method have been achieved with an overall radiation efficiency of 32 %.

(d) **The use of optimized Si thickness and process provided loaded dielectric:** In [54], two methods have been used for the performance enhancement of an 140 GHz endfire yagi-udda AoC using 130 nm SiGe BiCMOS. Firstly, an optimized thickness of substrate ($\approx$ 84 μm) is chosen in order to mitigate the effect of high dielectric constant of Si substrate. In addition, antenna is attached to the edge of a metallic supporter to enhance the distance between antenna and its ground plane. The introduction of metallic supporter acts as a reflecting plane. As a result, radiation efficiency is enhanced, and backside radiations are mitigated. Secondly, a rectangular dielectric load was realized using silicon and silicon dioxide layers for gain boost. The dimensions and placement of the dielectric load are optimized to get maximum gain and beamwidth of antenna. The proposed antenna provides the peak gain and radiation efficiency of 4.2 dBi and 83 %, respectively. Using the same design approach, a 1 × 2 array of these antennas is also designed which provides a gain of 7.2 dBi and radiation efficiency of 72 %.

(e) **The use of AMC and ADS as a part of chip package:** Two performance enhancement methods have been applied on a 77 GHz monopole AoC implemented using 180 nm CMOS process in [100] for automotive applications. First, the AMC surface has been designed on metal 1 and a square patch has been selected as an AMC unit cell because of its large bandwidth and reduced reflection loss based advantages. Consequently, 10.25 % enhancement in the radiation efficiency and 8.4 dB in the gain have been achieved. Second, a superstrate has been designed and integrated with the AMC based AoC which not only functions as a part of the chip package, but also enhances the AoC's performance by acting as an impedance transformer between the AoC and air. The use of superstrate for AMC based AoC enhances the gain by 9.1 dB and radiation efficiency by 22.1 %.
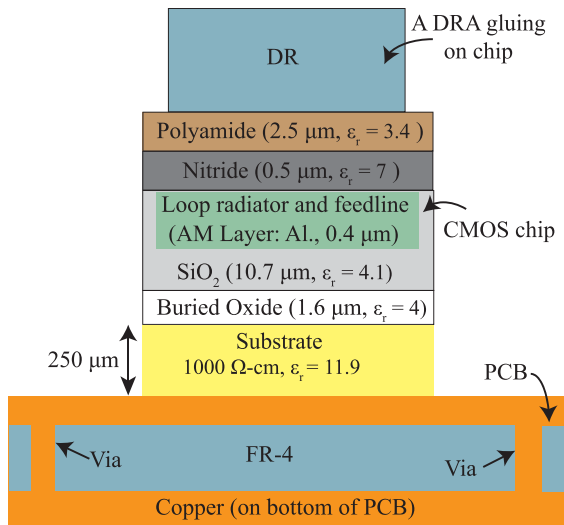
FIGURE 16. The use of three performance enhancement methods for a 65 GHz – 69 GHz loop antenna: A conceptual representation [102].

(f) **The use of backside slots, reflector, and metal-strips in slots:** In [101], three different methods have been utilized for a 60 GHz tapered slot Vivaldi AoC, fed by a double-Y balun, using 180 nm CMOS process. First, the addition of three rectangular slits on the back edge of Vivaldi AoC enhances the gain by 1.23 dBi and radiation efficiency by 1 %. Second, the placement of a backside planner arc reflector, realized using metal vias between metal 1 and metal 6 layers, provides a gain improvement of around 1.19 dBi and radiation efficiency enhancement of about 3 %. Third, the use of circular metal-strips at metal 6 layer to act as an additional director into the antenna slot improves the gain by 0.6 dBi and radiation efficiency by 3.5 %.

(g) **The use of high-resistivity substrate, DRA, and an off-chip ground:** Three methods have been utilized for the performance enhancement of a 65-69 GHz loop antenna using 180 nm CMOS process in [102], which meets the requirements of quad flat no-lead (QFN) package based SoC. First, a high resistivity Si substrate with a resistivity of 1000 Ω-cm is chosen for design of on-chip loop radiator. Second, a dielectric resonator is employed which is fed by the on-chip loop antenna. Third, an off-chip ground is realized with the big die pad of the quad flat no-load (QFN) package. This big die package is always part of a QFN package. During the design of the antenna, a top copper layer of FR-4 PCB is used to model the big die pad of the QFN package Consequently, AoC has achieved a peak gain of 7.8 dBi and radiation efficiency of 96.7 %. The concept is shown in Figure 16.

(h) **The use of metallic reflector and Helium-3 ion irradiation:** The authors have employed two performance enhancement methods in [24] for a 140 GHz folded dipole antenna using 40 nm CMOS process. With selecting an optimized thickness (250 μm) of the substrate,

the antenna is placed on vertical metallic structure which acts as a reflector for the antenna performance enhancement. Helium-3 ion irradiation method is then utilized for further increase in antenna performance by increasing the resistivity of Si substrate in an optimized way. The outcome of the utilization of both the method is a 5 dB gain enhancement of the antenna.

(i) **The use of high-resistivity substrate, ADS, and parasitic substrate:** Three methods have been employed for the DRA AoC [103] at 60 GHz. First, a high-resistivity Si substrate (ρ=2000 Ω-cm) is used. Second, the use of single silicon superstrate enhances the gain of the AoC by 1.4 dBi and radiation efficiency by 0.8 %. Second, the use of a parasitic Rogers RO4535 substrate in between the ADS and DRA AoC enhances the gain and radiation efficiency by 2.5 dBi and 1.3 %, respectively.

(j) **The use of AMC, ADS, and Fresnel lens:** In [104], the use of 3 methods have significantly enhanced the performance of a 71 GHz monopole AoC using 180 nm CMOS process. The use of AMC is the first method which has increased the gain of AoC by 3 dBi. The second method is the use of superstrate which has enhanced the gain by 7 dBi. Third, the use of Fresnel lens has enhanced the gain by 12 dBi. 20 dBi increase in gain has been achieved by a combination of three methods. The novelty of this design is that the combination of superstrate and Fresnel lens has been transformed to act as a package for the AoC, which not only enhances its performance, but also protects it from external effects. To lower the cost of the chip, the package was manufactured additively. The package contributes 18 dBi rise in the gain, which is an extraordinary achievement.

(k) **The use of high-resistivity substrate and ADLs:** In [60], the authors have employed two methods to get high performance AoC. First, a high resistivity (ρ = 3.5 kΩ-cm) in-house CMOS compatible process is utilized for the design of a 300 GHz double slot. Second, ADLs structure is used to increase the equivalent permittivity of the host material from 4 to 32. The ADL structure consists of a stack of 7 layers, each 5 μm far in z-direction (z represents the height). The optimization of antenna and ADLs provide gain and FBR enhancement of 2 dBi and 9 dB, respectively.

(l) **The use of ADS and Silicon superstrate:** In [61], the authors have utilized silicon superstrate and ADS for a 280 GHz dipole AoC to have a comparative potential of both the methods in terms of AoC performance. First, dipole AoC is designed without any performance enhancement method, which exhibits input resistance of 0.16 Ω, bandwidth of 1 %, and radiation efficiency of 36 %. Then a silicon superstrate is used for the dipole antenna, which enables achieving input resistance of 2 Ω (1.84 Ω more than single AoC), bandwidth of 5 % (4 % more than single AoC),, and radiation efficiency of 51 % (15 % more than single AoC). After that, ADLs is placed above the AoC which provides input

resistance of 10 Ω (9 Ω more than single AoC, 5 Ω more than AoC with silicon superstrate), bandwidth of 10 % (9 % more than single AoC, 5 % more than AoC with silicon superstrate), and radiation efficiency of 87 % (51 % more than single AoC, 36 % more than AoC with silicon superstrate). These results clearly validate the effectiveness of ADLs for performance enhancement of AoCs.

(m) **The use of a high-resistivity substrate and hemispherical lens:** In [68], Two methods have been used for the performance enhancement of a 300 GHz 2-elements ring slot array for high temperature-coefficient superconducting receiver front-end. First method is the use of a high resistivity substrate ($\varepsilon_r = 11.68$) for the design of radiator network of the antenna, which is comprised of CPW-fed slot ring array. Second, a hemispherical lens has been employed. The antenna exhibits a good gain of 13.5 dBi and impedance bandwidth of 33 GHz. This antenna also uses a double layered FSS between high-resistivity substrate and lens, which acts as a bandpass filter in contrary to its traditional use in AoC as a performance enhancement source. The FFS based filter rejects the undesired interference from other parts of the superconducting receiver.

(n) **The use of SOI CMOS and off-chip PCB to act as reflector:** Two methods have been utilized for performance boost of a broadband Q-band AoC in [105]. First, the antenna is designed using 180 nm SOI CMOS technology. Second, the authors have mounted the antenna on top of the off-chip PCB, which acts as a reflector for the antenna. The antenna has been made broadband with the use of a couple of on-chip switches which are embedded in the radiator structure. The on and off state of the switch dictates the antenna tuning and extends its bandwidth. A peak gain of 2.2 dBi has been obtained with a broad bandwidth of 29.5 GHz – 51 GHz. The use of reflector has enhanced the peak gain of the antenna by 3.1 dBi.

(o) **The use of NTN layer to enhance the resistivity of Si substrate and metal wall to limit the antenna radiations electric field:** In [106], the authors have presented and utilized two methods to boost the AoC performance. First, they have proposed a novel method to increase the resistivity of silicon substrate. It is well-known that a heavy doping of P-substrate forms a low resistivity P-Well or N-Well in standard CMOS processes, which is unfavorable for AoCs. If somehow the area under the AoC and in its vicinity can be covered by a material which does not permit the decrease in Si substrate resistivity during heavy doping, AoC performance can be increased significantly. High resistivity material NTN is a mask which is utilized for this purpose. The authors have observed that conductivity of the Si substrate can be reduced from 30 S/m to 10 S/m using this method. Second, the authors have used bouncing metal walls, made up of via-connected stacks metal/dielectric layer,

around the AoC in such a manner that these walls are in opposite direction of the antenna edge currents. The walls confine the electric field of the antenna in desired direction and thus enhances its gain. The authors have designed AoC using 4 different methods: first with 180 nm CMOS process, second with 180 nm CMOS with NTN layer, third and fourth with 180 nm CMOS with NTN layer and metal walls. The use of first method only, i.e. NTN layer with 180 nm CMOS for the design of AoC enhances the peak gain by 1.1 dBi. With the use of first and second method, i.e. NTN layer and metal walls, the peak gain of AoC is boosted by 2.60 dBi. In addition, this method protects the AoC from the impacts of residual silicon substrate after fabrication of the antenna. Residual silicon substrate can degrade the AoC gain significantly.

(p) **The use of high-resistivity substrate and substrate thinning:** In [107], The authors have utilized two methods for the performance boost of a 60 GHz AoC, besides presenting a novel integration approach of AoC with the other sections of the SoCs in an area-efficient manner. Before applying the performance enhancement method, the innovative integration strategy of AoC with the SoC is proposed. To reduce the chip-area, the proposed integration approach utilizes on-chip ground supply plane-made up of the top metal of the process- of the SoC to act as antenna electrodes. In other words, the approach makes re-use of the metals of the ground supply plane of the digital circuitry of the SoC. Inductive connections are used to connect the separate parts of the ground planes in this approach. To realize an antenna in this way, a slot is cut in the ground supply plane layer with RF voltage excitation around it. The issue of antenna radiations interference with the digital circuitry has been analyzed thoroughly and concluded that switching currents of digital IC based transistors can disturb the antenna radiation characteristics. A solution is provided which states that a minimum gap between antenna frequency and digital ICs clock frequency should be ensured to avoid interference. To improve AoC efficiency, two methods have been proposed. First, a high-resistivity substrate ($\rho = 7$ kΩ-cm) is utilized. To design the proposed AoC with ground supply interconnects, a high-resistivity substrate test wafer is fabricated which consists of one polysilicon and two metal layers. To contact the antenna with the wafer probe, a balun is used. Second, a ChipFilm technology is utilized to thin the substrate upto 17.5 μm, which offers lesser loss. It is worth mentioning here that this technology is complex compared to CMOS and demands extra steps, equipment and high cost. The designed antenna on thin substrate was glued to a dielectric material RO3003 for mechanical stability. The antenna designed using high-resistivity substrate exhibits a radiation efficiency of 92 %, while the thin substrate-based antenna shows a radiation efficiency value of 61 %.

(q) **The use of DRA and half-mode cavity-based feeding network:** In [108], the use of two methods have enhanced a 135 GHz CMOS process based AoC performance significantly. First, a DRA has been used to increase performance. Second, a half-mode cavity is designed using SIW technology. The cavity is realized using top metal layer, bottom metal layer and stacked vias based rectangular metallic wall. This cavity acts as a feeding network for the DRA, which is placed above the cavity network with an epoxy glue material. The half-mode cavity is also able to resonate at its dominant mode (130 GHz), while DRA dominant mode is at 140 GHz. The use of these two methods resulted in a gain of 4 dBi and radiation efficiency of 62 %.

7) OTHER METHODS

(a) **The use of a shared ground plane for the MIMO AoCs:** In recent days, the significance of MIMO based AoCs has increased significantly because of their widespread use in various emerging applications such as 5G wireless systems, 6G wireless systems, radar systems, etc. However, high performance MIMO based miniaturized AoCs have been scarce till date. In [34], a 60 GHz first on-chip MIMO antenna has been proposed using 65 nm CMOS process for MM-Wave ICs, which utilizes a novel performance enhancement method for the MIMO AoCs along with achieving compactness. The MIMO structure has been realized with two antennas: a folded monopole antenna acts as a main antenna and an Inverted-F antenna IFA) acts as a diversity antenna. The selection of antenna type is dictated by the performance enhancement method, which exploits the use of a common on-chip ground plane for both the antennas to contribute in their radiations and thus enhances their radiation efficiency. The layout has been designed in such a way that on-chip ground plane also acts as the antenna ground plane, which results in gain enhancement. To do so, both the AoCs are placed perpendicular to each other on the chip; the main antenna is placed at the right corner of the RF front-end chip where no pads are located, while diversity antenna is placed at a side of the chip where there are pad rings. To achieve resonance, the fixed length monopole is meandered. To enable the designer to precisely control the resonance frequency of the diversity antenna, a capacitive load is established by reducing the gap between antenna and ground plane. Both the antennas are located on the pad layer of the 65 nm CMOS process. Gain of −3.8 dBi for monopole and −6.1 dBi for IFA has been obtained.

(b) **The use of PCB based cavity and special structures on the package of the chip:** In [109], the authors have proposed solution of the challenges such as ohmic loss introduced by the silicon substrate, higher order substrate modes, and surface waves to the realization of 3 AoCs integrated in 60 GHz FMWC radar chip using

Qubic4X SiGe BiCMOS process. After a detailed study and analysis, the authors have selected cavity-backed on-chip monopole antenna as antenna configuration because of its miniaturization and ability to solve the above-mentioned issues related to AoCs. The cavity is constructed on the low-cost two layers Rogers PCB, with whom is attached the FMCW radar chip. To suppress the higher order modes and surface waves, the two-layer PCB substrate is covered with the plastic mold after attaching it with the silicon die having on-chip antenna. The final solution consists of a silicon substrate with 3 AoCs, PCB substrate with a cavity and interconnects, and a plastic mold. After an optimization, the AoC resulted in 2 dBi gain and 45 % radiation efficiency.

(c) **The use of slots on the ground plane:** The authors have utilized vertical and horizontal slots on the ground plane of a 60 GHz AoC for the radiation efficiency improvement in [110], implemented in 90 nm CMOS. The AoC has been designed on the topmost metal, i.e. metal 9. For the ground plane, first metal 1 and then metal 2 have been selected. Four vertical and horizontal slots have been designed on the ground plane for the efficiency increase of the AoC. It is observed that the location of the slots and their distance from the AoC plays a critical role in determining an optimized efficiency for AoC. A peak efficiency enhancement of about 60 % has been noted for the case when metal 2 is used as a ground plane and a 53 % enhancement in efficiency is obtained when ground plane is on metal 1. The advantage of this method is that it is simple and does not require extra hardware, thus saving the chip-area and cost of the system. In addition, it is flexible with respect to the selection of AoCs ground plane. Metal 1 or metal 2 can be chosen as a ground plane as per the requirements. Moreover, the slots can also be used to achieve desired values of the bandwidth and axial ratio of AoCs besides increasing the efficiency. These advantages make it as an extremely attractive choice as a performance enhancement method for MM-Wave AoCs.

(d) **The use of on-chip metal tiling/dummy metals to act as an AMC:** A cost-effective performance enhancement method for the 60 GHz AoC has been proposed in [111]. It is well-known that the dummy metals are required to be added in the design in order to fulfil the metal density design rules of the CMOS or BiCMOS processes. In this design, the authors have arranged these dummy metal fills to act as an AMC for the lossy Si substrate with the help of innovative design strategies, which can then mitigate the losses offered by the Si substrate. It is observed that a double later metal fill, which has been called as double-layered metal tiles or AMC, are better than single-layer AMC. The proposed method also aids in tuning the impedance of AoC which is often detuned because of the grinded substrate on which AoC is designed. The application of this method for a 60 GHz monopole AoC provides a 3.3 dBi rise

in the gain, 10 % raise in the radiation efficiency, and 5.8 GHz 10-dB bandwidth. Because of its simple fabrication and low-cost based advantages, this method is highly promising for MM-Wave and THz AoC design.

(e) **The use of PCB reflector to enhance AoC Performance:** In [112], a novel method to enhance AoC performance has been proposed where the designed V-shaped patch AoC is glued to an optimized PCB (40 mil thick Rogers 4003), and the ground plane of the AoC is moved from beneath the antenna to the bottom plane of the PCB. This ground plane under the PCB plays a role of a magnetic conductor at the antenna surface, thus increasing its gain and radiation efficiency. Designed in 22 nm digital CMOS technology, the 26.6 GHz – 36 GHz AoC improves its gain by 9.8 dBi and radiation efficiency by 37.3 % with the use of this method.

(f) **The use of low permittivity locally formed porous Si substrate:** In [58], the authors have utilized a low permittivity locally formed porous Si substrate, which is also compatible with the standard low-resistivity Si substrate by an electrochemical etching process. A dipole antenna is designed and manufactured by considering the porous Si as a local substrate on low-resistivity silicon substrate. The porous silicon was fabricated with the help of electrochemistry process on a p^+ – silicon (thickness = 525 μm, $\rho = 1 - 5$ mΩ-cm). The comparison of the antenna with low-resistivity Si substrate-based antenna shows a gain enhancement of 11 dBi.

(g) **The use of inkjet printing process:** In [113], the authors have proposed an inkjet printing process which can be used to design the AoC for standard CMOS based chips after their fabrication. The antenna is designed on top of the manufactured chip with the help of the proposed inkjet printing process by metal patterns. Before printing of the antenna, a polymer SU-8 layer is patterned at the passivation layer in order to distance the antenna from lossy Si substrate. To demonstrate the approach, a monopole AoC is designed at top of a 180 nm CMOS process based 24 GHz oscillator chip. Because of the complex nature of the approach, only H-plane radiation pattern of the antenna could be measured which is consistent with the simulation results. There is no mention of a gain or radiation efficiency of the antenna.

The tabular form representation of the recent advancements in AoC performance-issues-mitigation-methods is provided in Table 2, which reveals several insights. Firstly, the use of AoC performance enhancement methods for MM-Wave band outnumbers their use in RF and THz bands because of the emergence of a variety of innovative wireless applications in MM-Wave band in recent days. Secondly, 51 % is the maximum enhancement in the radiation efficiency in MM-Wave band AoC which resulted by the use of ADS method. Thirdly, 22.10 dBi is the highest rise in the peak gain in this band which is achieved using a combination of 3 different performance enhancement methods,

i.e. AMC, superstrate, and Fresnel lens. This highlights the significance of hybrid methods for the AoC performance issues mitigation for future highly efficient wireless system designs. Consequently, the use of hybrid methods has been accepted widely in MM-Wave band based AoCs to get high performance. Fourthly, there are various innovative performance enhancement methods which have been used for MM-Wave AoCs only. These include inkjet printing post-processing, asymmetric AMC, the exploitation of PCB package of AoC IC, use of dummy metals of the standard Si processes, the use of ground supply plane of the digital circuitry of a CMOS based SoC for AoC design, the use of high resistivity substrate based GIPD technology, the use of a common ground for MIMO AoCs, the use of NTN to increase resistivity of standard CMOS substrate, the Si substrate thinning, and selective LBE. Fifthly, 300 GHz is the maximum and 29.5 GHz is the minimum frequency AoC for which performance enhancement techniques have been employed. Sixthly, the EBG structure (AMC, FSS, PRS, metasurface, metamaterials) is the most widely used method to boost AoC performance in MM-Wave because of their easy fabrication and low-cost based advantages. Seventhly, GaAs and MgO substrates have also been utilized for AoC performance enhancement in MM-Wave band due to high resistivity substrate.

C. RECENT DEVELOPMENTS IN THz BAND (Above 300 GHz)
1) USE OF ELECTROMAGNETIC BAND-GAP REFLECTIVE SURFACES

(a) **The AoC's Performance depends on the location of AMC with respect to the AoC:** According to [132], the AMC based AoC's performance depends on its distance and location from the AMC. In addition, the use of metal vias with AMC can provide better performance for AoC in comparison with AMC only structure. These observations have been made during the design of a 0.65 THz bowtie AoC using 180 nm CMOS process. The AMC is constructed by periodic structure of mushroom like aluminum patches. Through vertical metal vias, these patches are connected to a ground plane, thus working together with the AMC. In first case, the AoC is designed on metal 6 layer and AMC with metal vias is realized on metal 2 layer. This results in a 2 dBi rise in the peak gain. If AMC is used without metal vias on metal 6, this rise in gain is not observed, which confirms the better performance of the use of AMC with metal vias as compared to without metal vias. In second case, antenna is designed on metal 6, but the AMC is realized on various metal layers, i.e. metal 2 to metal 6 one by one and antenna performance is observed with AMC on each metal layer. It is noticed that the best return loss (-26 dB) and peak gain (9.1 dBi) is achieved when AMC and antenna are on the same layer, i.e. metal 6. A maximum gain boost of 4.5 dBi and

maximum decrease in return loss of 15 dB is observed when AoC and AMC are on the same metal layer in comparison with antenna and AMC on different metal layers. In addition, such an antenna, i.e. the antenna and AMC on the same metal layer provides a very good unidirectional properties with an FBR of 19 dB. Based on the results of this study, it can be summarized that the maximum gain, good impedance matching, and unidirectional radiation characteristics are achieved when the proposed AoC and the AMC are on the same metal layer. The antenna designers and researchers can use these observations to optimize the performance of their AMC-based AoC accordingly.

(b) **Metasurface behaving as an AMC:** In [133], the authors have proposed a high gain, 500 μm Polyimide substrate based metasurface structure, which behaves as an AMC for a 0.350 THz – 0.385 THz AoC. The AMC like behaving metasurface structure is implemented by a 2-D composite left/right-handed metamaterial transmission line. To design the metamaterial transmission line, the concentric dielectric rings in the ground-plane of the Polyimide substrate were etched. The radiating element is implemented on the top layer of the substrate and consists of concentric metal rings. An AoC array of 3 × 3 radiating patches was designed using this method which uses two layers of polyamide substrate stacked on each other. The top layer consists of radiating patches; AMC is designed in the middle ground-plane layer, and the underside of the bottom layer consists of feeding network. The proposed metasurface enhances the gain and radiation efficiency of the reported AoC by 5.38 dBi and 20.51 %, respectively.

2) METHODS RELATED TO ENHANCEMENT OF EQUIVALENT DIELECTRIC OF ANTENNA SUBSTRATE

(a) **The use of Lens**

(i) **The use of bullet Si lens to solve narrow bandwidth issue of hemispherical lens:** According to the results obtained in [134], the utilization of a novel bullet Si lens can provide better performance, especially in terms of bandwidth compared to conventionally used hemisphere Si lens for a 0.340 THz bowtie AoC implemented in InP substrate. First, AoC without any lens is designed. Second, a conventional hemispherical lens is utilized to improve AoC performance. The use of this hemispherical lens enhances the gain by 6.1 dBi, but reduces the bandwidth by 50 % in comparison with an AoC without the lens, i.e. the bandwidth is reduced from 40 GHz to 20 GHz. To solve this problem, a novel bullet silicon lens is introduced. The bullet Si lens consists of two structures: a cylinder of 0.2 mm length and a hemisphere with a radius of 1.5 mm. The use of the bullet silicon lens provides a gain of 13.5 dBi (2.2 dBi more than hemispherical

lens based AoC, 6.3 dBi more than single AoC), radiation efficiency of 90 %, and broad bandwidth of 308 GHz – 386 GHz (78 GHz more than hemispherical lens based AoC, 38 GHz more than single AoC).

(ii) **The use of Si hemispherical lens for a dual-band AoC:** The use of performance enhancement methods for multi-band AoCs is highly demanding these days. A dual-band AoC has been designed in [69] using MgO substrate, which operates at MM-Wave and THz bands with operating frequencies of 160 GHz and 0.640 THz. A detailed description of AoC operation has already been discussed in section III.3 (ii) of this article. The AoC provides a peak gain of 19.9 dBi at 0.640 THz

(b) **The use of DRAs**

a) **The use of DRAs which are excited at higher order mode to achieve extra benefits:** In [59], a 0.340 THz, on-chip patch fed novel DRA has been designed using 180 nm CMOS process. Instead of exciting the DRA at its fundamental mode, it is excited at higher order mode of $TE_{\delta 17}$ because of a few advantages. First, a higher order mode excited DRA is easy to fabricate at THz as compared to fundamental mode excited DRA since the thickness of the former (500 μm) is more than the later (100 μm); as a result, not only an additional wafer thinning process is needed for the fundamental mode excited DRA, but it also has higher probability of getting broken during the manufacturing process. The need for an additional wafer thinning process means a higher cost. Second, a higher order mode excited DRA is more reliable than the fundamental mode excited DRA because of its enhanced mechanical stability. The peak gain and radiation efficiency of the proposed antenna are 7.9 dBi and 74 %, respectively with maximum gain enhancement of 6.7 dBi.

b) **The use of stacked DRAs/DRA array:** In [135], the utilization of two DRAs/array of DRAs with slots and vias in standard Si substrate of 50 μm thickness has resulted in a significant performance improvement at 0.450 THz – 0.475 THz. The first DR is glued on the surface of the Si substrate which is fed by a 10 μm wide meandering slot and thus acts as a normal on-chip DRA. The second DR is placed above the first DRA in vertical direction making a series-fed linear array. In between the two DRs, a low dielectric support structure is placed in order to reduce the electromagnetic interactions between DRs. Both the DRs radiate at fundamental frequency of 455 GHz. First DRA radiates efficiently at fundamental mode with an operating frequency of 0.455 THz when excited by the meandering slot and a percentage of the radiations is coupled serially with the second DRA which also radiates at the same mode. To further reduce energy dissipation, the meandering slot is occupied

with a metallic wall of stacked vias. The presence of meandering slot and vias plays a role of series left-handed capacitors and shunt left-handed inductors respectively, mimicking the metamaterial like properties and resulting in a decrease in antenna's footprint and an increase in its performance. The peak gain and radiation efficiency exhibited by the proposed design are 4.5 dBi and 45.7 %, respectively. The smaller chip-area, easy fabrication, and high-performance based advantages make this technique a superb option for THz AoC applications.

3) CMOS-COMPATIBLE MEMS FABRICATION PROCESSES BASED AoCs

(a) **A modified low-loss micromachined Si process:** A modified micromachined Si MEMS fabrication process has been introduced in [98], which mitigates the effect of lossy Si for AoC design. A detailed description of the method is already described in section III.5 (b) of this article since a MM-Wave AoC is also designed using this process. The second AoC designed using this process operates at 0.2223 THz – 0.340 THz, and achieves a peak gain of 10.6 dBi, radiation efficiency of more than 88 %, and bandwidth of 117.7 GHz.

4) HYBRID METHODS

1) **The use of optimized thickness of substrate, metal supporter, and dielectric load:** In [54], three methods have been utilized for the gain enhancement of a 0.320 THz endfire yagi-udda AoC using 130 nm SiGe BiCMOS process. First method is the selection of an optimized thickness (upto $\approx 34~\mu$m) of the silicon substrate. Second method is the introduction of a metal supporter with which the antenna is mounted with upper part ungrounded; this plays a role of a reflecting plane and thus increases the radiation efficiency and reduces the backside radiations. Third method is the design of a dielectric load, using silicon substrate and silicon dioxide layers, with an optimized location and dimensions. The results show gain and radiation efficiency values of 3.9 dBi and 80 %, respectively for the proposed AoC after applying all the methods.

2) **The use of low permittivity DRA and supporter:** In [136], two methods have been utilized for the performance boost of a 0.350 THz SIW-backed on-chip antenna using 130-nm SiGe BiCMOS process, which comes with two low loss thick metal layers (TM1 and TM2) and five thin metal layers (M1 – M5). Before applying the performance enhancement method, the antenna structure is finalized. The on-chip antenna structure is constructed as follows: the driver is comprised of an E-shaped patch antenna realized on TM1, an L-shaped feeding network realized on TM1 and via-stack beneath TM2, and a SIW backed cavity is realized with the help of via-stack from the TM2 metal to the ground plane; antenna ground plane is realized

on bottom most thin layer, i.e. metal 1. To improve the performance, a low permittivity DRA as well as a supporter is glued with the on-chip driver. The use of DRA and supporter has resulted in peak gain improvement by 8 dBi, and radiation efficiency by 50 %. In addition, AoC shows a 3-dB bandwidth of 65 GHz, thus making this antenna suitable for wideband sub-THz applications.

3) **The use of metamaterial and substrate integrated waveguide technologies:** In [137], the authors have used the combination of metamaterial and substrate integrated waveguide concepts for performance enhancement of a 0.28 THz – 0.3 THz patch AoC using Si substrate with a thickness of 50 μm. The square patch has been designed on the top side of the substrate, while the back side is occupied with an Al groundplane. The quarter-mode substrate integrated waveguide cavity under the patch is created by the metal vias in the patch periphery to permit the surface currents to flow towards the ground via short circuited pathway. Two T-shaped slots are then created in such a way to divide the single quarter-mode cavity into equal eight-mode sub-cavities. The resulting sub-cavities have been connected with each other in a manner which ensures radiations emission into the air from the cavities edges as well as T-shaped slots when excited through a coaxial feeding port. The metal vias play a role of shunt left-handed inductance, and T-shaped slots act as series left-handed capacitances. This configuration exhibits the characteristics of metamaterials and enhances the antenna performance, and that too with a small footprint. The AoC obtains a peak gain of 4 dBi and radiation efficiency of 57 %. The proposed approach is attractive for THz applications because of its smaller chip-area based advantages.

4) **The use of novel metasurface slots and coupled feeding:** In [138], the performance of a CMOS AoC with an operating frequency of 0.5 THz – 0.56 THz has been enhanced with the help of two ways: first, by the use of metasurface slots and second, with the use of an innovative coupled feeding mechanism to AoC structure. The design makes use of three layers for the design of AoC in silicon-ground-silicon manner. The ground layer is sandwiched between two silicon layers. A 3 × 3 array of asterisk-shaped radiators have been constructed on the top silicon layer. In order to mitigate the surface waves and substrate losses, three slot lines aligned with the asterisk-shaped radiators have been implemented in the middle ground-plane layer. The metasurface slots of optimized dimensions are then etched on the asterisk-shaped radiators which expand the effective aperture area of the antenna without having any impact on its dimensions. In order to increase the performance of AoC further, the AoC has been excited by a novel feeding structure which consists of an open-circuited microstrip line beneath the bottom silicon layer. The effective coupling of the EM signal,

TABLE 3. Recent developments in AoCs performance-issues-mitigation-techniques at THz bands (above 300 GHz).

Ref.	Performance-Issues-Mitigation-Method	Antenna Type	Freq. (THz)	Technology	Dimensions	Peak Gain (dBi) / Incr. in Gain (dBi)	$\eta_{rad}(\%)$ / Inc. in $\eta_{rad}(\%)$
[132]	High Impedance Surface	Bowtie	0.65	180 nm CMOS	NR	9.1 / 4.6	NR / NR
[134]	bullet Si lens + InP substrate	Bowtie	0.308 – 0.386	InP substrate	InP substrate	−1.53 / 8	90 / 50
[69]	Si hemispherical lens + MgO substrate	Gold thin film with twin slots	0.160, 0.640	MgO substrate	NR	9.7 / NR, 19.9 / NR	NR / NR
[59]	High order mode DRA)	DRA with feeding patch	0.340	180 nm CMOS	0.2 mm^2	7.9 / 7	74 / 54
[136]	Rectangular DRA	SIW-backed DRA	0.325 – 0.390	130-nm SiGe BiCMOS	NR	10 / 8	75 / 50
[135]	Stacked DRAs	Meandering slot with stacked DRA	0.450 – 0.47	standard Si substrate of 50 μm thickness	400 × 400 × 135 μm^3	4.5 / NR	47.5 / NR
[55]	Quartz ADS	Slot-ring antenna array	0.320	180 nm SiGe BiC-MOS	NR	1.7 / NR	32 / NR
[60]	ADS + High resistivity substrate	Double slot	0.3	High resistivity silicon	NR	3.9 / 2	NR / NR
[98]	Modified Si micromachining	Slot like	0.222.3 – 0.340	Si compatible MEMS fabrication process	NR	10.6 / NR	88 / NR
[54]	appropriate Si thickness + process provided loaded dielectric + post-processing substrate thinning	Quasi yagi-udda	320	130 nm SiGe BiC-MOS	0.47 × 0.6 mm^2 (without supported structures)	3.94 / NR	80 / NR
[133]	Metasurface acting as an AMC	EM coupled microstrip feed	0.350 – 0.385	500 μm Polyimide	6 × 6 × 1 mm^3	7.58 / 5.38	60.85 / 20.51
[138]	Metasurface + coupled feeding	Asterisks-shaped based on metasurface slots	0.5 – 0.56	CMOS	200 × 200 × 4 μm^3	5.3 / NR	28.15 / NR
[140]	Si hemispherical lens + InP substrate	Slot	0.110 – 0.400	InP HBT	NR	22 / NR	NR / NR
[141]	Octagonal shorted annular ring	1 × 2 annular ring	0.303 – 0.320	130 nm SiGe BiC-MOS	550 × 1100 μm^2	4.1 / NR	38 / NR
[142]	Si Lens	Folded slot	0.459	65 nm CMOS	NR	NR / NR	32 / NR
[139]	Metasurface slots-based feeding method + novel array configuration	Ring shaped array	0.63	20 μm CMOS	0.16 mm^2	8.1 / NR	38.24 / NR
[54]	optimized Si thickness + process provided loaded dielectric	Yagi-udda	320	130 nm SiGe BiC-MOS	0.47 × 0.6 mm^2	3.9 / NR	80 / NR
[137]	Metamaterial + substrate integrated waveguide	Patch	0.28 – 0.3	Si substrate (thickness = 50 μm)	800 × 800 × 60 μm^3	4 / NR	57 / NR
[143]	Aperture coupled feeding method	Patch	0.29 – 0.316	120 μm Si	20 × 3.5 × 0.126 mm^3	9.6 / NR	55 / NR

applied to the bottom layer input open-circuited line, with the top layer asterisk-shaped radiators is ensured via slot lines on the ground. The simulation results verify the effectiveness of both performance enhancement methods where the AoC obtains a peak gain of 5.3 dBi and radiation efficiency of 28.15 % with miniaturized dimensions of 200 × 200 × 45 μm^3.

A similar method is also utilized in [139] for the design of a 0.63 THz AoC array using three CMOS layers of 20 μm in silicon-ground-silicon pattern. The design

approach is same as in [138] except the configuration of array elements, which is ring-shaped; also, the array elements are interconnected in order to enhance the radiation properties of the array. A gain of 8.1 dBi and radiation efficiency of 38.24 % are reported.

Recent advances in THz based AOCs performance methods that are responsible mitigation of issues are also presented in a tabular form in Table 3. Several important observations can be made from Table 3. First, highest frequency AoC in THz band for which performance enhancement method has

TABLE 4. Summarized relative comparison of some widely used performance enhancement methods.

Performance Enhancement Technique	Ease of Fabrication	Cost	Commercialization Potential	Post Processing Requirements	Chip Area	Supported by Standard Si Processes?	Gain
EBGs	Easy	Moderate to High	High	Very Low	Moderate to Large	Yes	Moderate
LBE	Moderate	Moderate	Moderate to High	Moderate		By few SiGe processes	Moderate
LIA	Difficult	High	Low	High	Large	No	High
DRA	Moderate	Low	Moderate	Moderate	Small	No	High
ADS	Moderate	Moderate to High	Low	Moderate	Large	No	Low
Helium-3 Ion Irradiation		High	Low	Moderate	Small	No	Moderate
Proton Implantation	Moderate	High	Low	Moderate	Small	No	Low
MEMS	Easy	Low	High	Moderate	Moderate	By few processes	Low
High resistivity substrate	Moderate	High	Moderate	Moderate to High	High	No	High

been employed resonates at 0.65 THz. Second, the maximum enhancement in radiation efficiency of an antenna in THz band is 54 % which is obtained by the use of a higher order mode DRA-based performance enhancement method. Third, 8 dBi is the maximum rise in the peak gain of the antenna in this band which is achieved with the help of a combination of novel bullet Si lens and InP substrate-based methods. Fourth, the use of technologies other than CMOS and SiGe BiCMOS to get high performance AoC is more frequent in this band than RF and MM-Wave band. These technologies include InP, MgO, high resistivity Si substrate, MEMS, and Polyimide substrate. In addition, InP substrate has been utilized only in this band for the performance enhancement of AoC because of high values of f_t and f_{max} of its substrate besides high resistivity. Polyamide is another such substrate which has been utilized only in THz band for AoC performance enhancement because of higher thickness of its substrate than standard CMOS and SiGe BiCMOS. However, the Polyamide substrate-based AoC occupies larger chip-area than other technologies-based AoCs. Fifth, the use of hybrid methods, i.e. more than one performance enhancement methods have also been observed in this band. Sixth, the application of performance enhancement methods for AoC arrays has also been reported in this region.

Table 4 depicts a summarized relative comparison of some widely utilized performance enhancement methods so that the relevant researchers and designers can have a quick idea of the fabrication complexities, processing requirements, commercialization potential, and cost of widely used performance enhancement methods. It can be observed from Table 4 that use of EBGs and MEMS as performance enhancement techniques for AoCs has the highest commercialization potential, but at the cost of moderate and low gain, respectively. These methods provide ease of fabrication and are supported by Si processes. Contrarily, use of LIA, Helium-3 irradiation, Proton implantation, and high resistivity substrate require the highest cost amongst other methods which restrict their commercialization potential. Although each

performance-issues-mitigation-method comes with its own advantages and disadvantages as shown by Table 4, it is obvious that the selection of a particular method depends on AoC's targeted application.

IV. AoCs PERFORMANCE-ISSUES-MITIGATION-METHODS: FUTURE DIRECTIONS

This section explores and describes some key future directions with respect to AoC performance-issues-mitigation-methods.

A. INFLUENCE OF IC's PACKAGING ON AoC's PERFORMANCE

It is obvious that the packaging of the AoC also affects its performance. While a widespread research effort has been made on proposing and applying performance enhancement methods for the AoCs, a very little work has been found on exploring and mitigation of the packaging impacts on AoC performance. An effort is made in [100] recently, where the authors have investigated the impact of the package on AMC based AoC's performance. Based on their investigation, the authors proposed an optimized superstrate which is part of the antenna chip package. The special feature of this superstrate-based chip package is that it not only plays a role of a normal package for the chip, but also enhances the AoC's performance. A similar design approach can be seen in [104], where a combination of a Fresnel lens and superstrate was transformed into a additively manufactured package for the AMC based AoC. The package not only protects the AoC from external environmental impacts like a normal chip package, but also enhances its gain by a substantial amount of 18 dBi. These examples highlight the significance of the antenna package for AoC performance enhancement and makes this one of the attractive future directions.

Another promising direction in this regard can be the proposal of novel methods for integrating the AoC with the RF front-end which could ensure performance boost for AoC. One such 3D microfabrication method for a 60 GHz AoC

array has been introduced in [144]. Instead of placing the AoC directly on top of the Si substrate chip as per the normal routine, this approach manages to place the AoC a bit above the lossy Si substrate with the help of a 3D microfabrication method. Because of a more gap between AoC and lossy Si substrate, the loss is reduced and design AoC secured a peak gain of 0.6 dBi and radiation efficiency of 55 %. A similar CMOS compatible 3D self-folding fabrication methodology has been proposed in [145], where 4 elements AoC array at 57.5 GHz achieves a peak gain of 5.8 dBi and radiation efficiency of 45 %. These techniques underline the importance of CMOS-compatible fabrication and integration methods of AoC with RF front-end. In future, an extensive research endeavour is needed in this direction.

B. ANTENNA PERFORMANCE ENHANCEMENT BY OPTIMIZED ANTENNA-RF FRONT-END CO-DESIGN STRATEGIES

AoC, in opposite to off-chip antennas, relaxes the impedance matching network between antenna and RF front-end of wireless system. In fact, the impedance matching network can be eliminated altogether if the antenna and RF front-end are conjugately matched with each other using a co-design method [45]. However, a limited progress has been observed in this regard yet despite a tremendous potential of this technique. Some designs which conjugately match the AoC and RF front-end include [146], [147]. Keeping in view the stupendous advantage of this approach, a profound research activity is the need of the hour.

Another potential direction is to come up with the AoC structures, which can change their impedance without degrading their performance, i.e. gain and radiation efficiency. This will enable an easy integration of these AoC structures with the active CMOS circuits in a highly efficient manner. One such 5.8 GHz AoC has been proposed in [148] using 180 nm CMOS process, where AoC's impedance is changed by modifying only one parameter of its geometry without any degradation in its gain. Another similar example includes a 0.3 THz – 0.31 THz AoC using SIW technology in [149], where antenna's impedance can easily be changed by adjusting the width of substrate integrated waveguide structure in order to match it conjugately with the nearby component of the transceiver. Huge benefit of this design methodology draws intense attention from future directions perspectives.

C. PERFORMANCE ENHANCEMENT METHODS FOR MULTI-BAND, FREQUENCY/POLARIZATION RECONFIGURABLE AoCs AND AoC BASED ARRAYS

The significance of multi-band, frequency and polarization reconfigurable AoCs, and AoC based arrays is proliferating with the emergence of novel applications and various advantages such as smaller footprint, low-cost, and high performance. The multiple-input-multiple-output based antenna arrays are indispensable for several applications, especially next generation wireless technologies such as 5G,

6G, and beyond. However, the scarce number of such AoCs, especially without performance enhancement methods, has thwarted their true potential because of inadequate performance. However, a trend in this direction can be witnessed in recent days. One frequency reconfigurable AoC with 2 performance enhancements methods, i.e. the use of 180 nm SOI CMOS and off-chip reflector has been proposed for Q-band applications in [105]. A 180 nm CMOS based polarization reconfigurable AoC at V-band [82] makes use of the asymmetric AMC as a performance enhancement method and gets a 1 dBi raise in gain and 10 % rise in the radiation efficiency. Two DRA backed antenna arrays, one 2 × 1 and other 4 × 1, have been proposed in [91] with significant gain values. A dual-band AoC [69] utilizes high-resistivity hemispherical lens and obtains significant performance enhancement. AoC of [99] makes use of a MEMS based fabrication process for the performance enhancement. A 1 × 2 array of yagi-udda AoC [54] utilizes two performance enhancement methods. AMC method is utilized in [119] for a 2 × 2 array of AoC. The detail of all these designs can be seen in Table 2 of this article. All these designs operate at MM-Wave. A limited such AoC designs have also been reported in THz band. In [133], a metasurface acting as an AMC based performance enhancement method is utilized for a 3 × 3 THz AoC array. The AoC arrays in [138] and [139] have also employed the performance enhancement methods. Table 3 depicts further detail of these THz AoC designs. One reconfigurable THz AoC has also been designed in [150], but without any performance enhancement method.

Despite a limited development in recent days, a substantial progress is needed with respect to the performance enhancement methods for multi-band, frequency and polarization reconfigurable AoCs, and AoC based arrays to enable a myriad of emerging wireless applications.

D. PERFORMANCE ENHANCEMENT METHODS FOR AoCs FOR RF/MICROWAVE BANDS APPLICATIONS

Although the focus is migrating towards MM-Wave and THz bands for next generation wireless systems because of the availability of large bandwidth, the low-frequency bands, i.e. RF and Microwave bands are popular for a plethora of wireless applications. Sub-6 GHz band, for instance, is one of the potential bands allocated by the Federal Communications Commission for 5G wireless communication [152]–[154]. Internet-of-Things is another prominent emerging application, which makes use of low-frequency bands [155]–[159]. Biomedical implants [160]–[162], wireless sensor networks [163]–[166], unmanned aerial vehicles [167]–[169], and wireless energy transfer [170]–[173] are some other vital applications, which operate in RF and microwave bands. Although a number of AoCs have been designed in RF and microwave bands as listed in [45], the use of performance enhancement methods for these AoCs is scant as evidenced by Table 1 of this article. As a result, the gain and radiation efficiency of these AoCs are at the lower side of performance metric as shown in [45]. One possible reason for this is
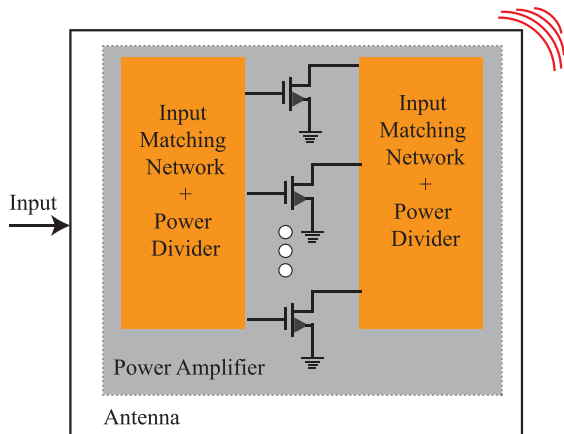
FIGURE 17. Innovative unit cell with an integrated power amplifier and antenna using CMOS technology [151]. This is a potential technique to get AoC at RF and microwave bands because of its high performance and smaller chip-size.

the chip-area tradeoff of performance enhancement methods with the AoC in these bands because of low-frequency, i.e. antenna gain is directly proportional to its aperture size in general. In other words, the use of a majority of performance enhancement methods result in large chip-area of the AoC. As miniaturization is also a key requirement for most of above-mentioned RF and Microwave applications, the trade-off restricted the use of AoCs performance enhancement methods at RF and microwave bands. This pushes the need for the proposal of novel performance enhancement methods for the AoCs in these bands which could also ensure antenna miniaturization. One innovative idea, proposed in [151] for the design of cohabitation based active ICs and antennas at 146 GHz using 65 nm CMOS process, can be a good option to be used for RF and microwave ICs with AoCs. The design approach, shown in Figure 17, unifies the antenna and power amplification function in a single cell which reduces the chip area significantly. Another design which makes use of both, i.e. antenna performance enhancement and miniaturization methods simultaneously has been proposed in [80] at 11 GHz. However, the gain of this AoC is very low, i.e. −29 dBi.

Keeping in view the significance of smaller chip-area, low-cost, and high performance based wireless systems for a variety of RF and microwave applications, it is anticipated that the investigation and proposal of innovative performance enhancement techniques for RF and Microwave AoCs will be one of the key future trends.

E. PERFORMANCE ENHANCEMENT METHODS FOR THE SILICON PHOTONICS AoCs
A recent trend can be witnessed where the passive elements of RF front-end are designed and fabricated in silicon photonics technologies because of various advantages. For example, the silicon photonic technologies are cost-effective than standard silicon technologies. Moreover, these technologies have higher resistivity than silicon technologies which is promising for the AoC design [174]. One such 15 GHz

monopole AoC has been designed in [174] in commercial silicon photonic process. Its functionality is also demonstrated for inter-chip RF data transmission. The peak gain of this AoC is only −0.22 dBi which is low. The reason for low gain is that the primary design objective was to demonstrate the potential of the proposed idea instead of achieving an optimized and high performance. With an expected rapid growth in this trend in the future, it is important for the researchers to come up with innovative performance enhancement methods for the silicon photonic based AoCs too.

V. CONCLUSION
A thorough review of recent developments in performance-issues-mitigation-techniques for AoCs has been presented in this article. It is noted that MM-Wave and THz bands are the most favorable bands for AoCs due to AoCs small form-factor. Moreover, Si technologies (CMOS and SiGe BiCMOS) have emerged as the most suitable candidates for AoCs owing to their low-power, low-cost, high integration and excellent unity-gain frequency based advantages. However, the gain and radiation efficiency degradation, compared to off-chip antennas, is the most serious challenge for Si technologies based AoC design. The main causes of this degradation are low resistivity and high permittivity of Si substrate of Si technologies. To overcome performance issues of AoCs, several mitigation-methods have been proposed and applied. This article presented a critical review of recent advancements in AoCs performance-issues-mitigation-methods for the first time with an aim of providing the researchers a single reference, which can be consulted before adventuring the challenging task of designing high performance AoCs. Some key future directions in this regard are also part of this article.

In the first section of this article, a brief detail of the fundamentals of some widely used AoCs performance-issues-mitigation-methods with their limitations has been provided. These methods include EBG structures, LBE, LIA, ADS, ADLs, DRA, MEMS, selective increase in Si substrate's resistivity, and high resistivity substrate. A comprehensive survey of the recent developments in techniques used to mitigate AoC performance issues has been done in the second section of this article. The recent development in the mitigation-methods has been presented in an organized and structured form and their description is divided into three categories, i.e. RF, MM-Wave, and THz bands. It is noted that the mitigation-methods proposed for MM-Wave AoCs surpassed the methods proposed for RF and THz bands AoCs because of proliferation of novel wireless applications in MM-Wave band. In addition, the use of mitigation-methods in RF band is scarce because of additional challenge of achieving antenna miniaturization. It is observed that the trend of using more than one performance-issues-mitigation-methods for a single AoC is growing rapidly to get very high efficiency AoC based wireless systems. In addition, some performance-issues-mitigation-methods have also been proposed and applied to dual-band AoCs, AoC based arrays, and frequency and polarization reconfigurable AoCs. The use of

high resistivity-based technologies has also been reported for the performance boost of AoC, albeit with their own limitations. It is more likely that AoC will become prevalent in near future driven by the demand from emerging wireless applications. Therefore, highly innovative designs will be desired to meet these challenges. In this regard, a brief description of the future directions with respect to the AoCs performance-issues-mitigation-methods has also been provided in this article. This article is envisioned to act as an excellent single guide for the early stage researchers who want to design high performance AoCs, as well as for the seasoned scholars who wish to contribute by proposing innovative methods for the mitigation of the performance issues associated with the AoCs.

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