

Received November 3, 2020, accepted November 30, 2020, date of publication December 3, 2020,
date of current version December 15, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3042313

Analysis of High-Failure Mechanism Based on Gate-Controlled Device for Electro-Static Discharge Protection

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This work was supported in part by the National Natural Science Foundation of China under Grant 61827812; in part by the Hunan Science and Technology Department Huxiang High-Level Talent Gathering Project under Grant 2019RS1037; in part by the Innovation Project of Science and Technology Department of Hunan Province under Grant 2020GK2018, Grant 2019GK4016, and Grant 2020RC1003; and in part by the Postgraduate Scientific Research Innovation Project of Hunan Province under Grant CX20200478.

ABSTRACT As semiconductor process continues to advance, the miniaturization of feature sizes places higher demands on high-failure electro-static discharge (ESD) applications. This article explores the connection between the physical structure of a device-level silicon controlled rectifier (SCR) and high-failure ESD characteristics. The gate-controlled silicon controlled rectifier (GCSCR) based on the gate control effect is fabricated using the $0.18\mu\text{m}$ standard bipolar complementary-metal-oxide-semiconductor double-diffused-metal-oxide-semiconductor (BCD) process. The ESD characteristics of the device are analyzed by technology computer aided design (TCAD) simulation and equivalent circuits. The transmission line pulse (TLP) is used to test the performance of the device. The results show that when the gate length is $4\mu\text{m}$, the failure current of the device is only 1.56A. When the gate length is $1\mu\text{m}$, the trigger voltage and the holding voltage of the device are 24.4V and 21.1V respectively, and the failure current is 34.94A. According to the test results of the above devices, it can be concluded that the current release mode of GCSCR with different gate sizes significantly affects the ESD characteristics of the device.

INDEX TERMS CMOS process, CMOS technology, electron devices.

I. INTRODUCTION

High-tech chip applications place higher demands on on-chip integrated ESD devices. The SCR can achieve high ESD robustness through structural improvement, layout optimization and other measures [1]–[5]. In a large number of studies on SCR devices, Wang *et al.* proposed a bidirectional SCR device for a high-voltage communication bus. By analyzing the ESD characteristics of laterally-diffused N-type metal-oxide semiconductor (LDNMOS) and laterally-diffused P-type metal-oxide semiconductor (LDPMOS), a method for increasing the holding voltage of the device has been found. The current release capability of the device reaches $87\text{ mA}/\mu\text{m}$, which enables better on-chip integration. The above device structure

provides design ideas for ESD protection of high-voltage communication chips [6]. Xi *et al.* used a 30V complementary diffused metal-oxide semiconductor (CDMOS) process to fabricate a new type of SCR. The results show that the device has good anti-electromagnetic interference capability and ESD release capability. It can be applied to industrial interfaces of $-7\text{V}\sim 12\text{V}$ [7]. Hu *et al.* proposed a novel SCR device with double snapback capability by embedding a grounded-gate N-type metal-oxide semiconductor (GGNMOS) structure on the SCR, and the current release capability of the device reached $33\text{ mA}/\mu\text{m}$. The double snapback capability can further reduce the secondary clamp-voltage, thereby effectively protecting the core chip from ESD interference. The novel device opens up new design ideas for ESD voltage-clamp in 28nm-CMOS process [8]. Huang *et al.* analyzed the latch-up effect of SCR devices and proposed a new latch-up immune SCR device to avoid the

The associate editor coordinating the review of this manuscript and approving it for publication was Yee Sin Ang¹.

latch-up effect of the device by adding an additional bipolar junction transistor (BJT) path [9]. Due to the deep snapback characteristics of the SCR, the holding voltage of the device is low. ESD design in the high-voltage field has higher requirements for holding voltage. Guan *et al.* used a nested structure to significantly improve the SCR holding voltage and achieve high ESD robustness [10]. Many researchers have proposed other methods to improve the ESD characteristics of SCR devices [11]–[19]. And it is commonly accepted that the conduction path of the device directly affects the SCR test indicators. The above research results can solve ESD protection problems in specific fields, but they have not yet studied the potential connection between the physical structure of the device and the high-failure characteristics. The application environment of the industrial-grade communication bus (RS485) is very harsh. The bus requires the on-chip integrated ESD device to have a forward trigger voltage of 14.4V~26.4V, a forward holding voltage of 14.4V~26.4V, and a failure current greater than 20A (HBM>30kV). By analyzing the physical structure and high-failure characteristics of the SCR device, it can provide design ideas for the ESD application of the device in the high-voltage field.

This article presents a GCSCR device structure based on gate-controlled effect. The goal is to study the relationship between the device’s failure level, physical structure and conduction path. The GCSCR device utilizes the electric field effect of the gate to improve the carrier transport of the device. By testing two GCSCRs with different gate sizes, the connection between the physical structure of the device and the high-failure characteristics is verified.

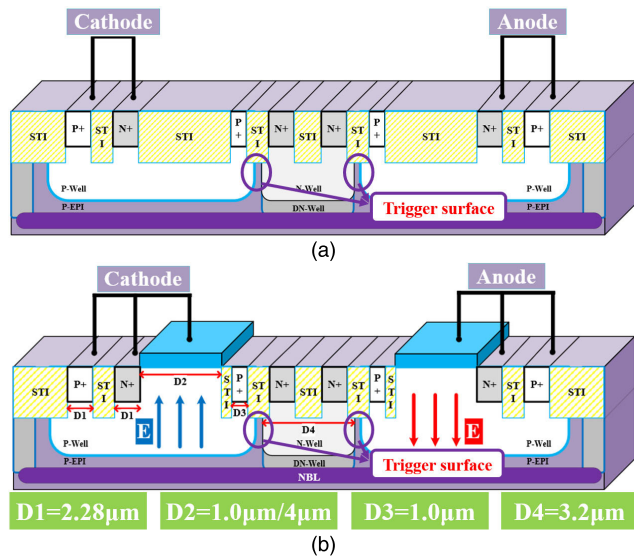


FIGURE 1. (a)Cross section of conventional SCR. (b)Cross section of GCSCR.

II. STRUCTURE AND PRINCIPLE OF GCSCR DEVICES

The cross section of the conventional SCR device is shown in Fig. 1(a), and the cross section of the GCSCR device based on the gate-controlled effect is shown in Fig. 1 (b).

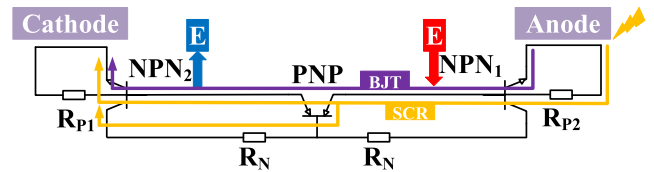


FIGURE 2. The ideal equivalent circuit of GCSCR.

Both types of device use floating P+, P-Well, P-type epitaxy (P-EPI), N+, N-Well and DN-Well to form the trigger surface. The ESD pulse causes avalanche breakdown of the trigger surface of the SCR, and the avalanche voltage and avalanche current gradually increase. When the avalanche current reaches the turn-on current of the internal ESD release path of the device, the low-resistance BJT path or SCR path is turned on. The turn-on voltage at this time is the trigger voltage (V_{t1}). In an ideal environment, the avalanche carrier will generate a voltage drop on the parasitic resistance of the P-Well and N-Well, and rapidly turn on the parasitic negative-positive-negative (NPN) and positive-negative-positive (PNP). During the gradual conduction of the SCR, the device has a negative resistance effect and the voltage drops to the holding voltage (V_h). When the two BJTs work in the saturation zone, the SCR is fully turned on. The main current path consists of anode P+, anode P-Well, P-EPI, N-type buried layer (NBL), P-EPI, cathode P-Well and cathode N+. The working principle of the GCSCR device is different from that of the conventional SCR device. The reason is that the GCSCR device has two polysilicon gates. The polysilicon gate on the left is shorted to the cathode of the device, and the polysilicon gate on the right is shorted to the anode of the device. The device uses electric field effects to significantly improve ESD characteristics [20]. When the device is turned on, the anode of the device is at a high potential relative to the NBL, and the cathode of the device is at a low potential relative to the NBL. Therefore, the gate of the anode generates a vertical downward electric field force, which promotes the transport of carriers between the anode P-Well and the NBL. Based on the same principle, the gate of the cathode generates a vertical upward electric field force to promote the transfer of carriers between the NBL and the cathode P-Well. Thereby the purpose of promoting the release of carriers in the positive feedback loop of the SCR is achieved. The ideal equivalent circuit of the device is shown in Fig. 2. The purple current path represents the BJT path, and the yellow current path represents the SCR path. The electric field effect significantly improves the collection efficiency of the parasitic PNP and the parasitic NPN emitter. Moreover, the initial conduction path of the SCR is a BJT path, and the PNPN path is not completely formed at this time. As the current continues to increase, the SCR path becomes the main release path. The device enters the linearly increasing region from the negative resistance region until the device has a thermal breakdown effect. At this time, the current of the device is called the failure current (I_{t2}).

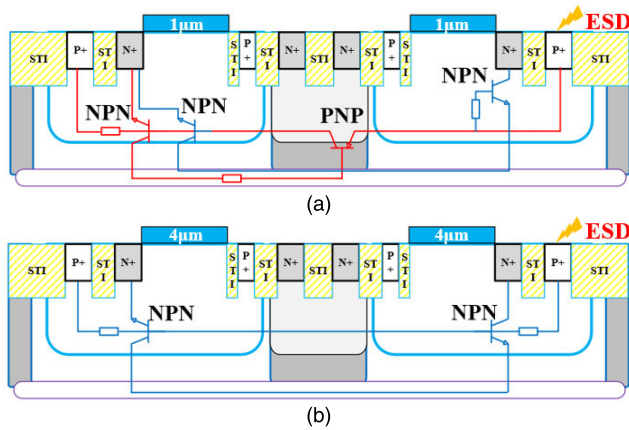


FIGURE 3. (a)GCSCR (Gate=1μm) actual equivalent circuit. (b)GCSCR (Gate=4μm) actual equivalent circuit.

The gate length of the device was designed to be 1μm and 4μm. According to the equivalent circuit, it can be clearly found that when the gate length is increased, the length of the release distance of the ESD stress from the P+ of the anode to the base of the parasitic PNP is increased. Since the formation of the PNP path requires to open two BJT paths, the difficulty of opening the SCR path increases as the length of the conduction path increases. Therefore, in the actual test environment, as the gate length changes, the conduction path of the GCSCR device changes significantly. The actual equivalent circuit for the two types of dimensions is shown in Fig. 3. The blue path is the BJT path and the red path is the SCR path. When the gate length is 1μm, after the device is triggered, the voltage drop generated by the avalanche carrier on the parasitic resistance can turn on the two BJTs, thus forming the BJT path and the SCR path. Also, as the ESD current stress increases, the SCR path will gradually become the main path. When the gate length is 4μm, the anode-to-cathode length of the device increases, which directly leads to an increase in the resistance of the on-resistance of the GCSCR. Therefore, the avalanche carrier cannot quickly turn on the second BJT in a short time, and the GCSCR can only work in a single BJT mode. The GCSCR in BJT mode will have a faster turn-on speed, but the BJT will not be able to withstand large ESD stresses, resulting in a lower failure level of the device.

III. 2D SIMULATION AND ANALYSIS

The GCSCR device uses atlas for device-level 2D simulation to study the physical behavior of the device’s impact ionization distribution, electric field distribution, current path and lattice temperature. In DC simulation, the impact ionization of the device is shown in Fig. 4. The impact ionization is mainly distributed in the P-Well of the cathode. The peak area of the distribution is located at the reverse bias PN junction of P-Well and N-Well, proving that when the ESD stress comes, the first place where avalanche breakdown occurs is the trigger surface of the device. After the device is turned on, the avalanche carriers immediately turn on the

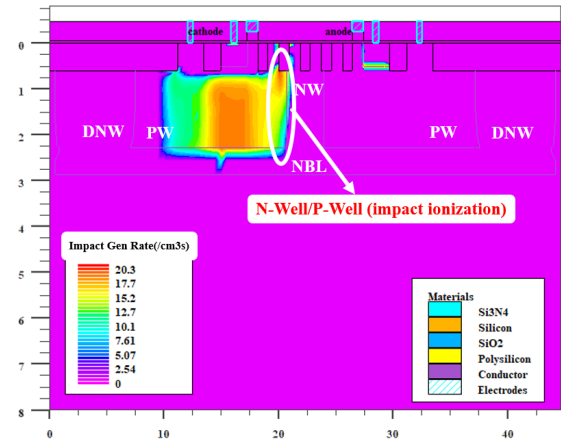


FIGURE 4. The impact ionization(DC) of the GCSCR.

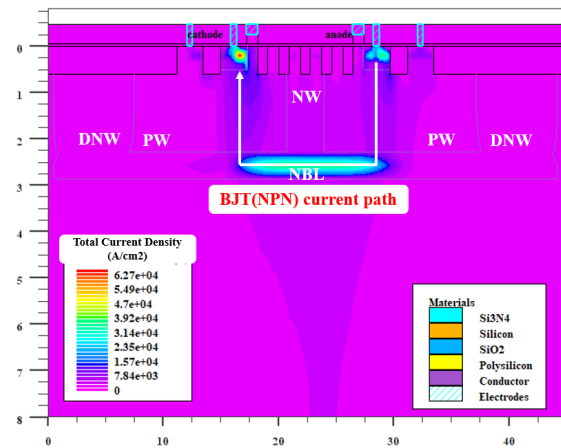


FIGURE 5. The BJT path when the GCSCR is slightly turned on.

BJT path, as shown in Fig. 5. When the device is initially turned on, ESD stress is released from the BJT path (anode N+/NBL/cathode N+), at which point the current density of the device is low and the SCR path is not fully formed. As the current increases, the parasitic NPN and PNP are turned on. An SCR path consisting of anode P+, anode P-Well, P-EPI, NBL, P-EPI, cathode P-Well and cathode N+ is completely formed, as shown in Fig. 6. It can be clearly seen that the ESD current stress at this time is evenly distributed inside the device, and the device has a main SCR path and a secondary BJT path. And the current density has increased by an order of magnitude compared to the current density of Fig. 5. The TCAD simulation cannot quantitatively describe ESD parameters but can predict the operating characteristics of the ESD. When the gate length is 4μm, the device turns on the BJT path in a very short time. Due to the large on-resistance of GCSCR (Gate = 4μm), the device can only work in BJT mode, with faster turn-on speed and lower failure level. When the gate length is 1μm, the on-resistance of the device is smaller than that of GCSCR (Gate = 4μm). Therefore, as the ESD current released by the device gradually increases, the BJT path is replaced by the SCR path to become the main current path.

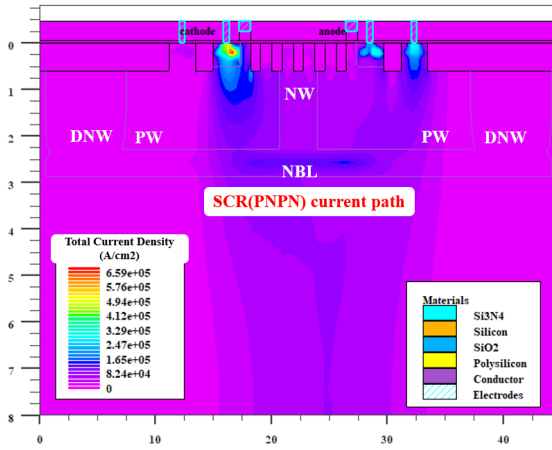


FIGURE 6. The SCR path when the GCSCR is fully turned on.

GCSCR (Gate = 1 μ m) can work well in the positive feedback mode of PNP and release ESD current stably. The failure level of GCSCR (Gate = 1 μ m) is higher, but the turn-on speed of the device is slower.

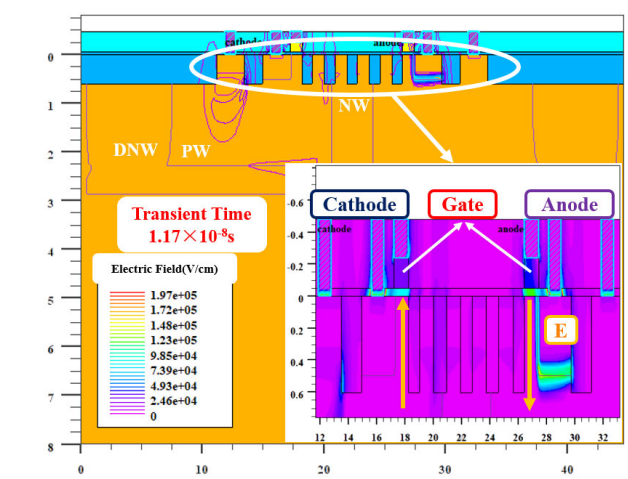


FIGURE 8. The electric field distribution of the GCSCR at clamp-point.

distribution after the GCSCR is slightly turned on is mainly concentrated on the reverse biased PN junction of the trigger surface, and the reverse biased PN junction of the anode N+ and P-Well. The main release path for the initial conduction of the device is the NPN path. At this time, the anode N+ and P-Well constitute the collector of the parasitic NPN and are in a reverse bias state, thus there will be a strong electric field distribution. As the SCR gradually turns on, there is a strong electric field distribution under the polysilicon gates of the anode and cathode. Since the potential of the NBL relative to the anode is lower, the gate of the anode generates a vertical downward electric field force to significantly adjust the carrier transport between the anode P-Well and the NBL. The NBL has a higher potential relative to the cathode, which causes the gate of the cathode to generate a vertical upward electric field force to significantly adjust the carrier transport between the NBL and the cathode P-Well. At the initial stage when the SCR path is fully turned on, due to the existence of the auxiliary BJT path, the reverse biased PN junction of the anode N+ and P-Well still has a strong electric field distribution after the GCSCR is fully turned on. At this time, the device has a local longitudinal electric field. The lateral electric field acts on the inside of the device to promote the transmission of ESD current from the anode to the cathode. GCSCR can achieve the purpose of improving ESD characteristics through the above-mentioned electric field effect.

The two-dimensional simulation results obtained by DC simulation cannot characterize the transient behavior of the device. Therefore, transient simulation is used to further verify the operation of the device. According to the voltage-time of the device, the clamp-time of the device was chosen to be 1.17×10^{-8} s to study the ESD behavior of the device after reaching the clamp-point. Fig. 8 shows the electric field distribution of the device clamp-point. The results show that it is consistent with the DC simulation. When the release path of the device is turned on, the strong electric field force under the gate significantly affects the ESD characteristics of the device.

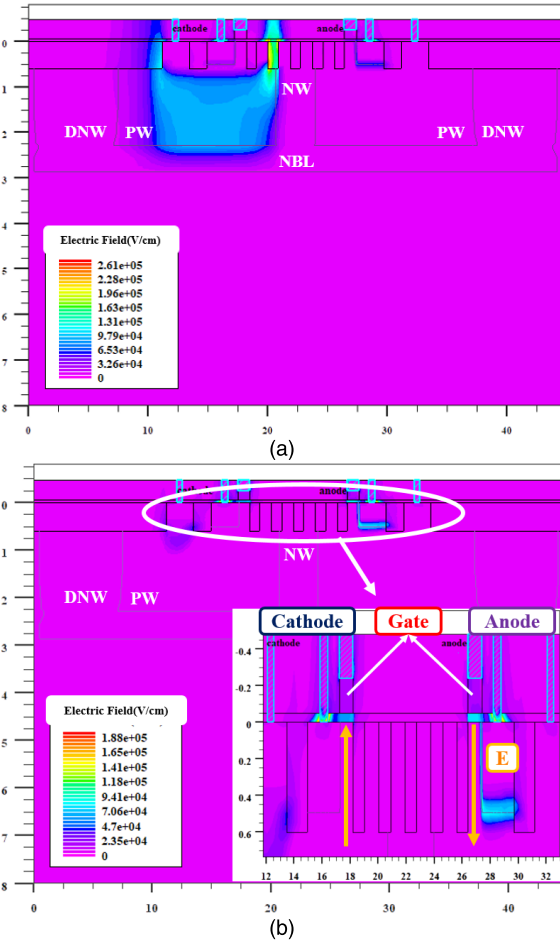


FIGURE 7. (a)The Electric field distribution when the GCSCR is slightly turned on. (b)The Electric field distribution when the GCSCR is fully turned on.

The electric field distribution of GCSCR can be further analyzed according to the different turn-on states of the device, as shown in Fig. 7(a) and Fig. 7(b). The electric field

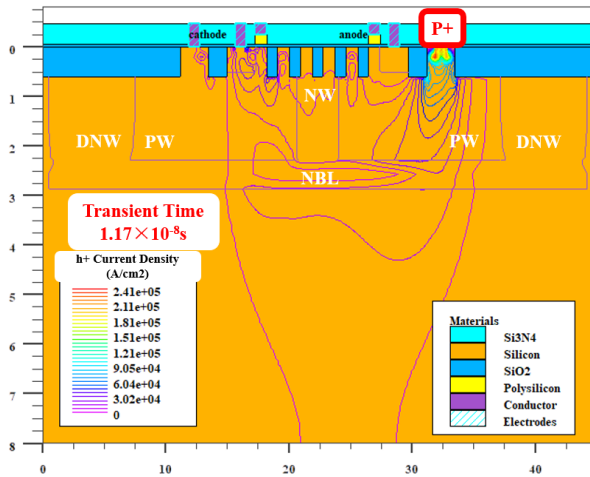


FIGURE 9. The hole current density distribution of the GCSCR at clamp-point.

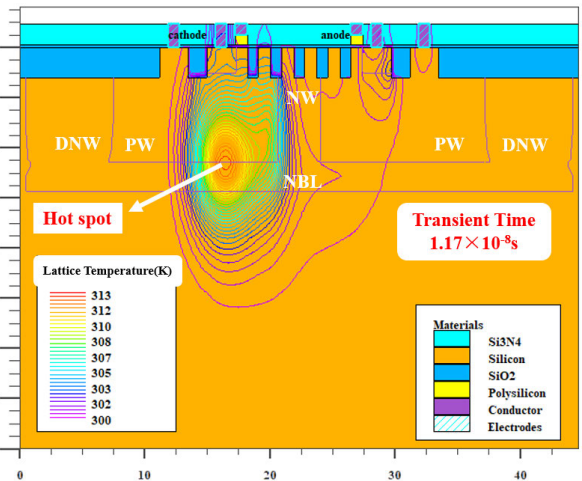


FIGURE 11. The lattice temperature distribution of the GCSCR at clamp-point.

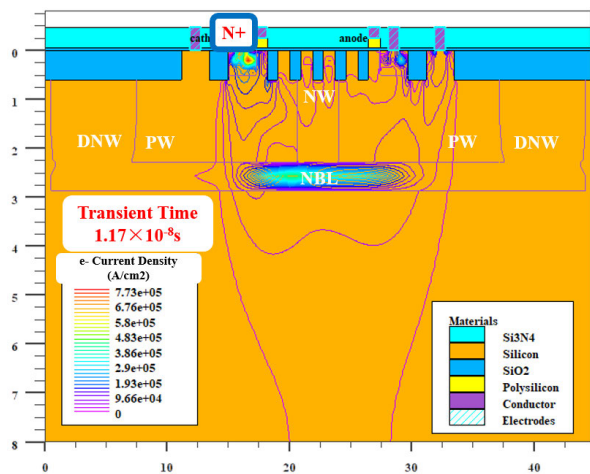


FIGURE 10. The electron current density distribution of the GCSCR at clamp-point.

The electron current distribution and hole current distribution of the GCSCR at clamp-point are demonstrated in Fig. 9 and Fig. 10 respectively. The hole current is mainly released from the anode P+ and is evenly distributed inside the device. The electron current is concentrated in the buried layer NBL, and a high concentration of electron current density exists in the region of the emitter N+ of the parasitic NPN. The distribution of the hole current and the distribution of the electron current show that the PNP path from the anode P+ to the cathode N+ has been completely formed. Fig. 11 reveals the distribution of the lattice temperature of the device at clamp-point. The results show that the hot spot of the device is concentrated on the reverse biased PN junction of the buried layer NBL and P-EPI. At this time, most of the ESD stress is released from the buried layer NBL to the cathode N+, indicating that the parasitic NPN has been turned on and the SCR path of the device has been fully formed.

IV. EXPERIMENTAL VERIFICATION AND DISCUSSION

According to the proposed gate-controlled effect, different sizes of GCSCR are fabricated based on the 0.18μm

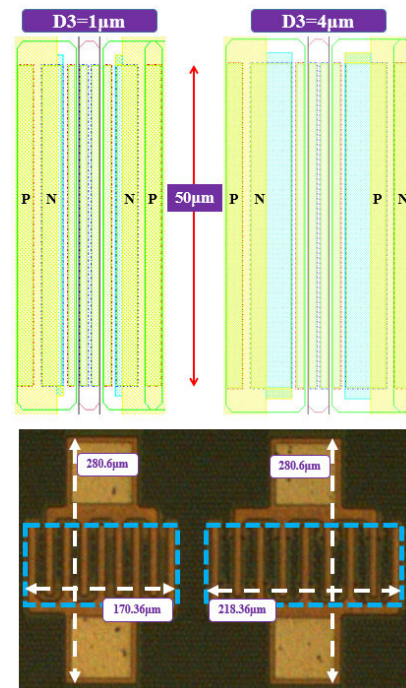


FIGURE 12. Single-finger layout and eight-finger microscope image of the GCSCR devices.

BCD process. The single-finger layout and eight-finger micrographs of the devices are shown in Fig. 12, with a length of 50μm, a number of fingers of 8, and a gate length (D2) of 1μm and 4μm respectively. The remaining dimensions of the two devices are identical (D3=1μm, D4=3.2μm). The device is verified based on the transmission line pulse test system. A current pulse with a rising edge of 10ns, a falling edge of 10ns, a pulse width of 100ns is used to test the ESD characteristics of the two types of devices.

Transparency evaluates whether the ESD device will affect the core circuits when the chip is operating normally. To further verify the transparency of the ESD device, DC test was

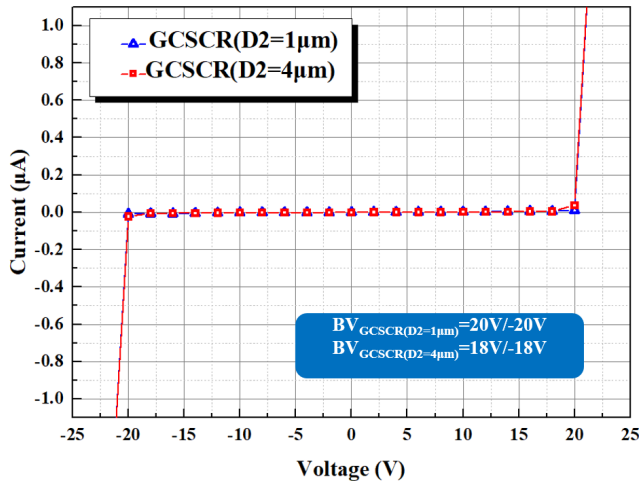


FIGURE 13. DC I-V curves of 8 finger GCSCR (Gate=1 μm), 8 finger GCSCR (Gate=4 μm).

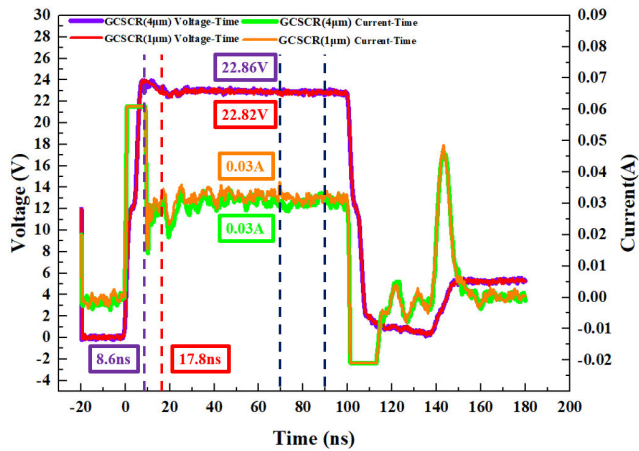


FIGURE 14. Voltage-Time and Current-Time curves of GCSCR (Gate=4 μm/1 μm).

performed on the device structures of the two types of sizes, as shown in Fig.13. The BV of GCSCR (Gate=1 μm) is 20V, and the BV of GCSCR (Gate=4 μm) is 18V. The DC test results show that the two types of device structure will not have leakage drift before the voltage is less than 18V. In order to verify that the two sizes of device structures have different current release modes, the transient voltage-time curve and the transient current-time curve of the trigger point of the GCSCR are obtained through the TLP test, as shown in Fig. 14. Because the structure of GCSCR (Gate=4 μm) and GCSCR (Gate=1 μm) are the same. Therefore, the transient curve only has a slight difference near the open-point. According to the test data of 70ns~90ns, the average clamp-voltage of GCSCR (Gate=4 μm) is 22.86V, and the average clamp-current is 0.03A. The average clamp-voltage of GCSCR (Gate=1 μm) is 22.82V, and the average clamp-current is 0.03A. When an avalanche breakdown occurs on the trigger surface of the device, the point closest to the clamp-voltage value after the voltage pulse is taken as the turn-on point of the device.

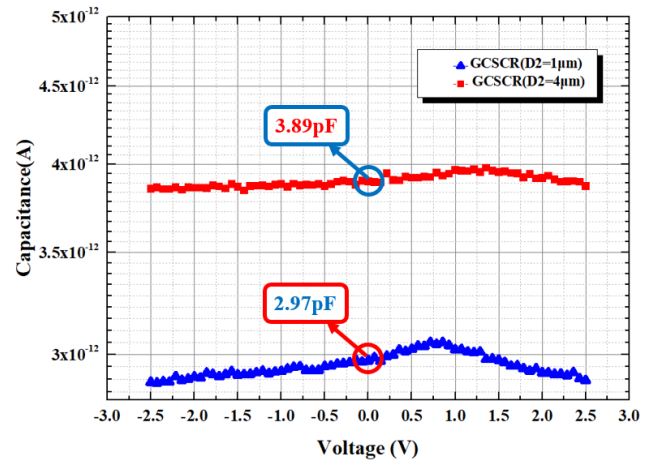


FIGURE 15. Intrinsic capacitance of GCSCR (Gate=4 μm/1 μm).

The turn-on time of GCSCR (Gate=4 μm) is 8.6ns, and the turn-on time (17.8ns) of GCSCR (Gate=1 μm) is twice than that of GCSCR (Gate=4 μm). The SCR path needs to turn on PNP and NPN, and the two BJT's take a long time to form a positive feedback effect. Therefore, the formation of the SCR path takes longer than the BJT path. The intrinsic capacitance test result of the GCSCR device is shown in Fig. 15. When the bias voltage is 0V, the intrinsic capacitance of GCSCR (Gate=1 μm) is 2.97pF, and the intrinsic capacitance of GCSCR (Gate=4 μm) is 3.89pF. The intrinsic capacitance of the device structure of the two sizes is maintained at the pF level.

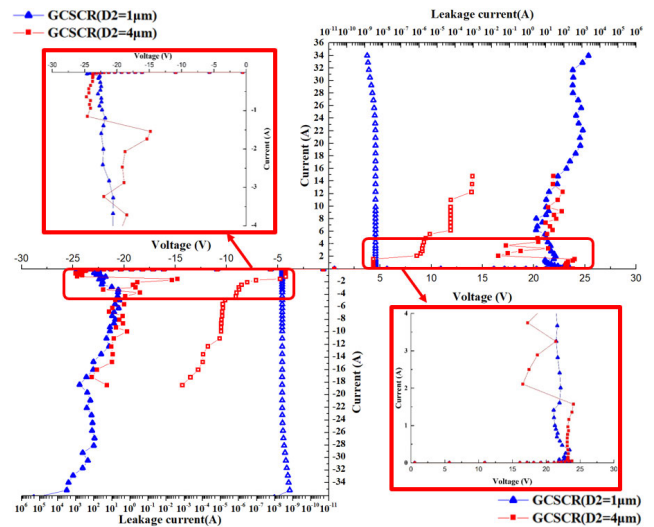


FIGURE 16. TLP I-V curves of 8 finger GCSCR (Gate=1 μm), 8 finger GCSCR (Gate=4 μm).

Fig. 16 indicates the TLP test curve for the devices. Both the forward and reverse test curves have good symmetry. The ESD characteristics of devices with different gate sizes have significant differences. When the gate length is 1 μm, the trigger voltage and the holding voltage of the device are 23.4V and 21.1V respectively. Since the main current path

of GCSCR (Gate= $1\mu\text{m}$) is NBL, the distance between the current path of the anode and the cathode of the device is increased, which effectively increases the holding voltage of the GCSCR device. Therefore, by controlling the current path of the device, the problem of low holding voltage caused by the snapback characteristic of the SCR can be effectively solved. The final failure current of the device is 34.94A. According to the calculation formula of the Human Body Model (HBM), the HBM level of the device is estimated to be 52.41kV, and the test result has already met the integrated ESD window of the RS485 communication protocol. According to the test data, the SCR path of the GCSCR (Gate= $1\mu\text{m}$) is fully turned on, and the on-resistance of the device is small, and the failure voltage is 25.34V. When the gate length is $4\mu\text{m}$ (the structure of the device and the remaining dimensions are consistent), the ESD characteristics of the TLP test curve are significantly different from the ESD characteristics of GCSCR (Gate= $1\mu\text{m}$). Since the trigger surfaces of the two devices are identical, their trigger voltages are approximately the same (23.81V). However, a linearly increasing region is created between the trigger point and the holding point of the GCSCR (Gate= $4\mu\text{m}$). The result shows that when the device is turned on, the BJT path is fully formed. Based on the current release mechanism of BJT, ESD current is transferred from the surface of the device to the cathode. Since the SCR path is not fully opened, the NBL fails to act as the main current path for the device. Therefore, the holding voltage (16.52V) is significantly lower than the holding voltage of GCSCR (Gate= $1\mu\text{m}$). Because the BJT path cannot withstand higher ESD currents, the failure level of the device is lower. The failure current is 1.56A, and the calculated HBM level is 2.34kV.

ESD current can open the PNP path of GCSCR (Gate= $1\mu\text{m}$) while GCSCR (Gate= $4\mu\text{m}$) can only turn on the BJT path, which is the main reason for the large difference in device characteristics. The turn-on of the SCR depends on the conduction of the NPN and the PNP, and the distance between the anode P+ and the cathode N+ is too long, which significantly increases the on-resistance of the device. When the on-resistance is too large to turn on two BJTs in a short time, the device can only turn on one BJT to release ESD current. The failure current of the device is lower, but the turn-on speed is faster. GCSCR (Gate = $1\mu\text{m}$) can open the SCR path, and the device has a higher failure level but slower opening speed. According to the test results of devices of different sizes, it can be concluded that based on the same ESD structure, high-failure characteristics can be achieved by changing the current release mode. For the practical application of the ESD, two different ESD characteristics can be obtained by changing the conductive path and physical structure of the device. The above design method can provide a reference idea for high-failure ESD design. The forward ESD data and reverse ESD data for the two types of devices are shown in Tables 1 and 2 respectively. The comparison between GCSCR (Gate= $1\mu\text{m}$) and references SCR devices are shown in Table 3.

TABLE 1. Positive Test Results of GCSCR Devices.

Device Name	GCSCR (Gate= $1\mu\text{m}$)	GCSCR (Gate= $4\mu\text{m}$)
V_{ci}	23.40V	23.81V
V_h	21.10V	16.52V
I_e	34.94A	1.56A
HBM	52.41kV	2.34kV
Open-time	17.8ns	8.6ns
Finger	8	8

TABLE 2. Reverse Test Results of GCSCR Devices.

Device Name	GCSCR (Gate= $1\mu\text{m}$)	GCSCR (Gate= $4\mu\text{m}$)
V_{ci}	24.60V	23.73V
V_h	21.80V	14.90V
I_e	35.17A	1.54A
HBM	52.75kV	2.31kV
Open-time	18.6ns	8.8ns
Finger	8	8

TABLE 3. Comparison of GCSCR (Gate= $1\mu\text{m}$) and Reference SCR Devices.

Device name	V_{ci}	V_h	I_e	HBM
References [1]	30.2V	17.3V	6.6A	9.9kV
References [3]	21.9V	19.7V	32.2A	48.3kV
References [6]	33.1V	11.7V	4.3A	6.5kV
References [8]	6.0V	4.9V/4.3V	0.5A	0.8kV
GCSCR (Gate= $1\mu\text{m}$)	24.6V	21.8V	35.17A	52.75kV

V. CONCLUSION

In this work, two GCSCR devices with different sizes based on gate-controlled effects verify that the high-failure characteristics can be achieved by changing the current release mode of the device. The working principle of the device is analyzed by two-dimensional device simulation and equivalent circuit. It is proved that the electric field effect of the gate can promote the movement of carriers. According to the results of the transmission line pulse test, the current release mode of the device determines its ESD characteristics. When the gate length is $1\mu\text{m}$, the SCR path can be effectively turned on, and the device has a higher failure level and a slower conduction speed. When the gate length is $4\mu\text{m}$, the device can only operate in BJT mode, resulting in a lower failure level of GCSCR. In summary, analyzing the test data of GCSCR devices shows that different ESD characteristics can be obtained by changing the conductive path and physical structure of the device. This method can provide a reference idea for high-failure ESD design.

ACKNOWLEDGMENT

The authors would like to thank Dr. Yang Wang, Xiangtan University, Miss Yunzhu Ju, Hong Kong University of Science and Technology, for their strong support and kind discuss to this article.

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